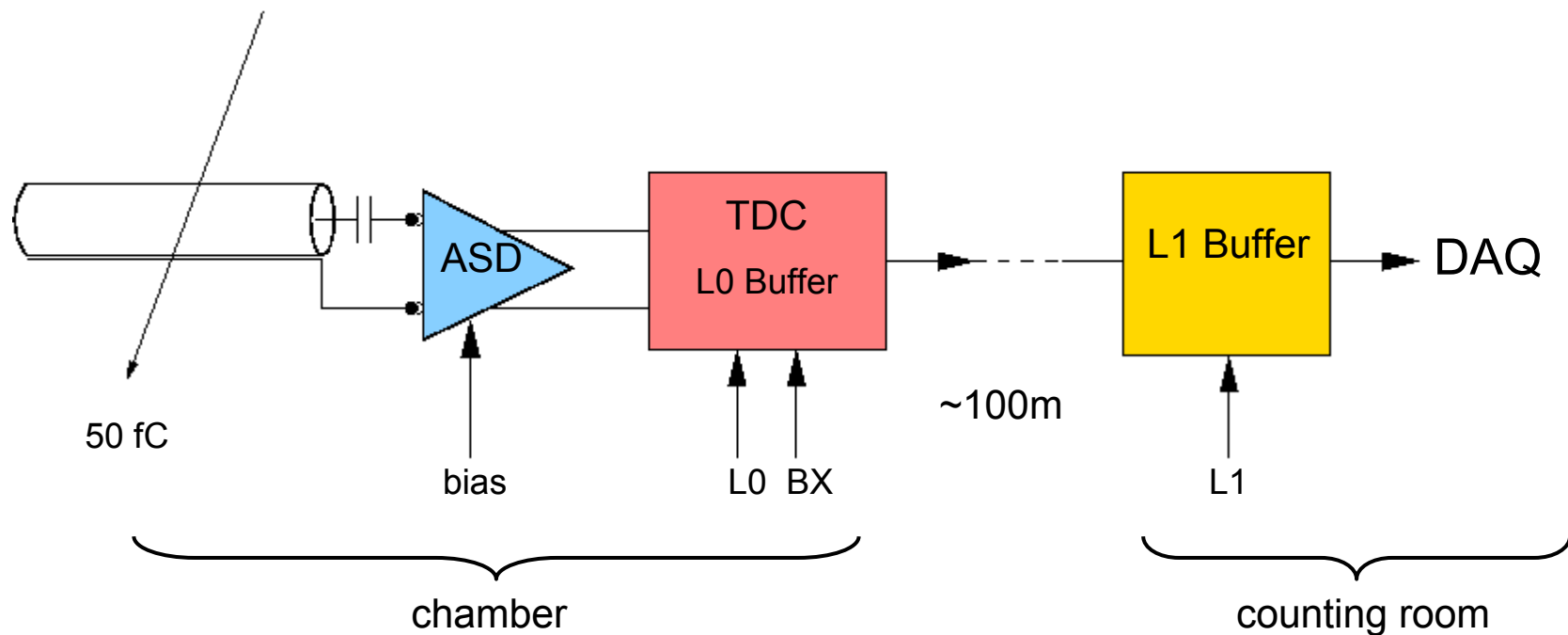
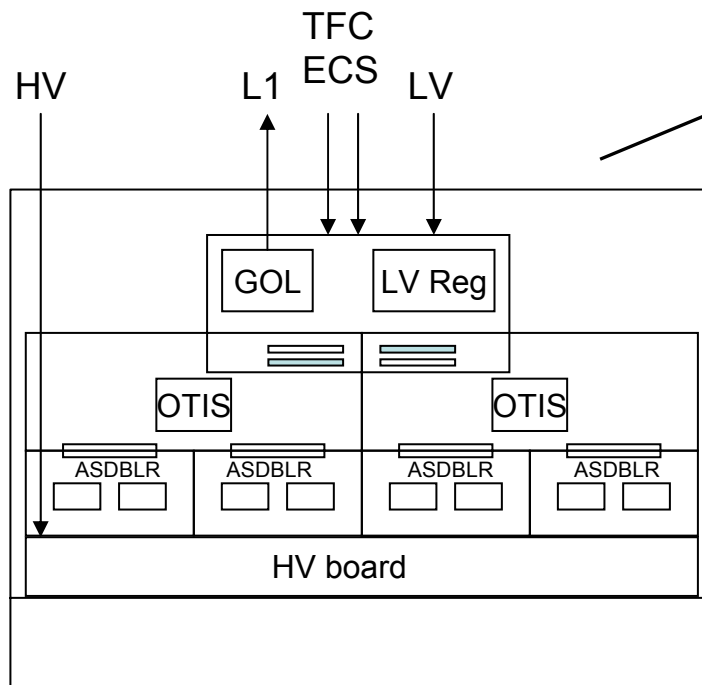


Outer Tracker Electronics





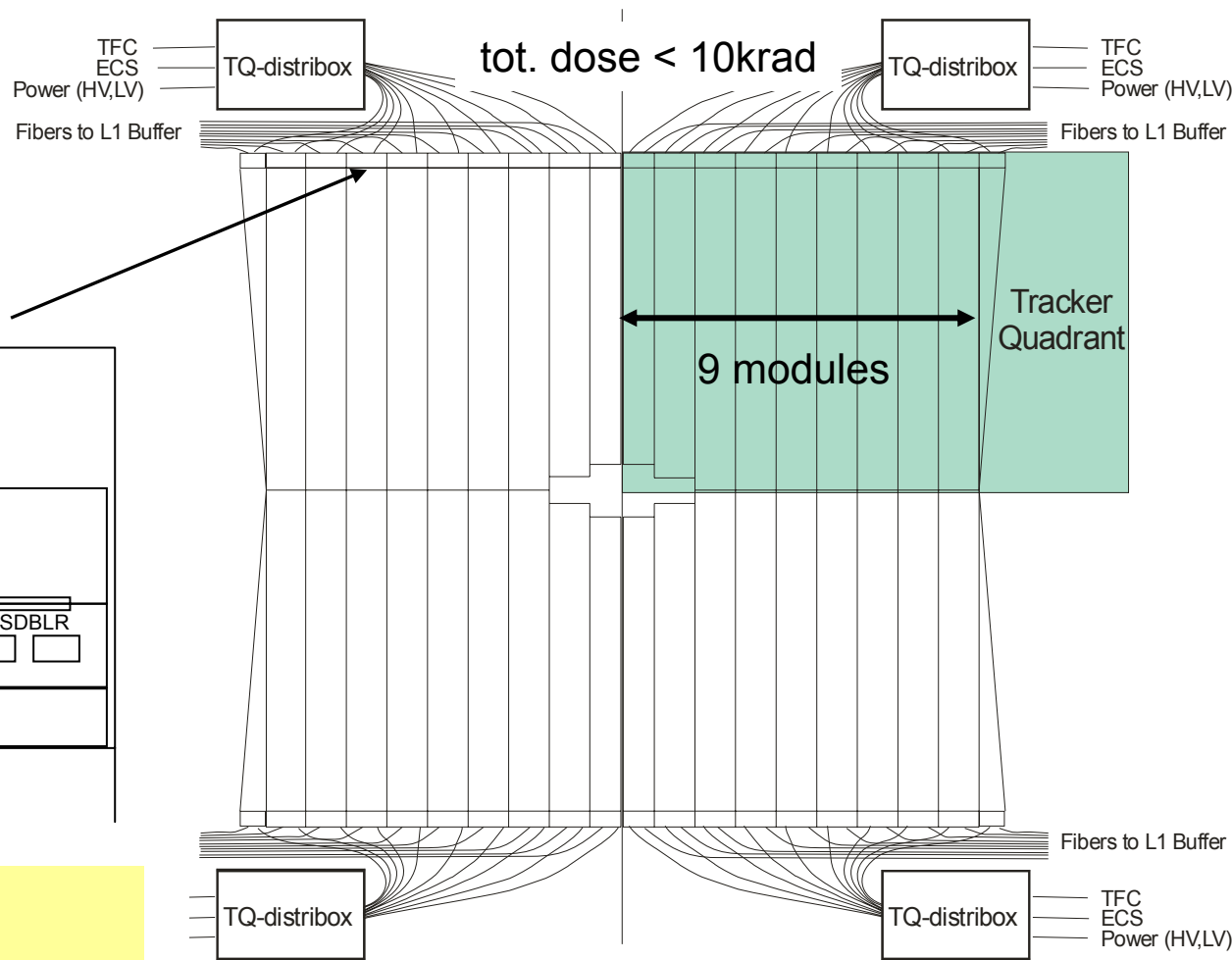
Module End:

128 channels

16 ASDBLR chips

4 OTIS TDC chips

1 optical link: 1.28 Gbit/s

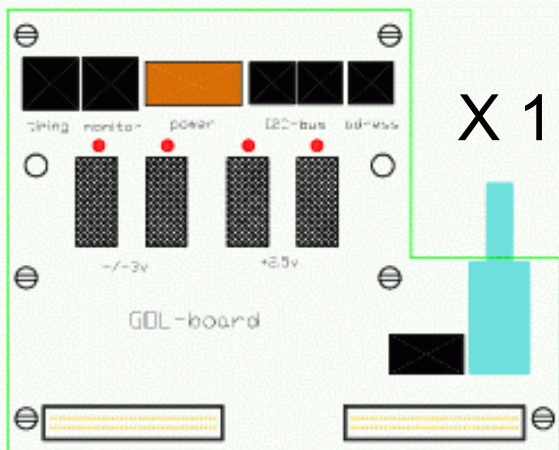


Outer Tracker: T1...3

56000 channels

432 optical links

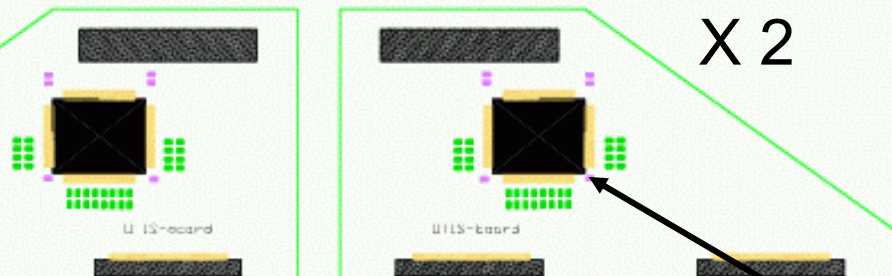
GOL/Aux
Board



Front-end boards:

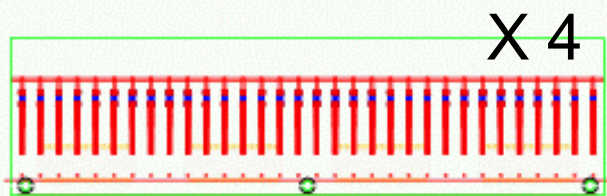
boards	number
GOL/Aux	432
TDC	1732
ASD	3456
HV	1728

TDC
boards



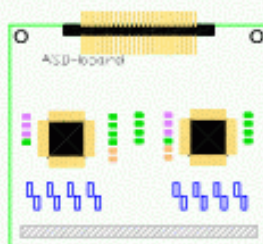
X 2

HV boards



X 4

ASD boards

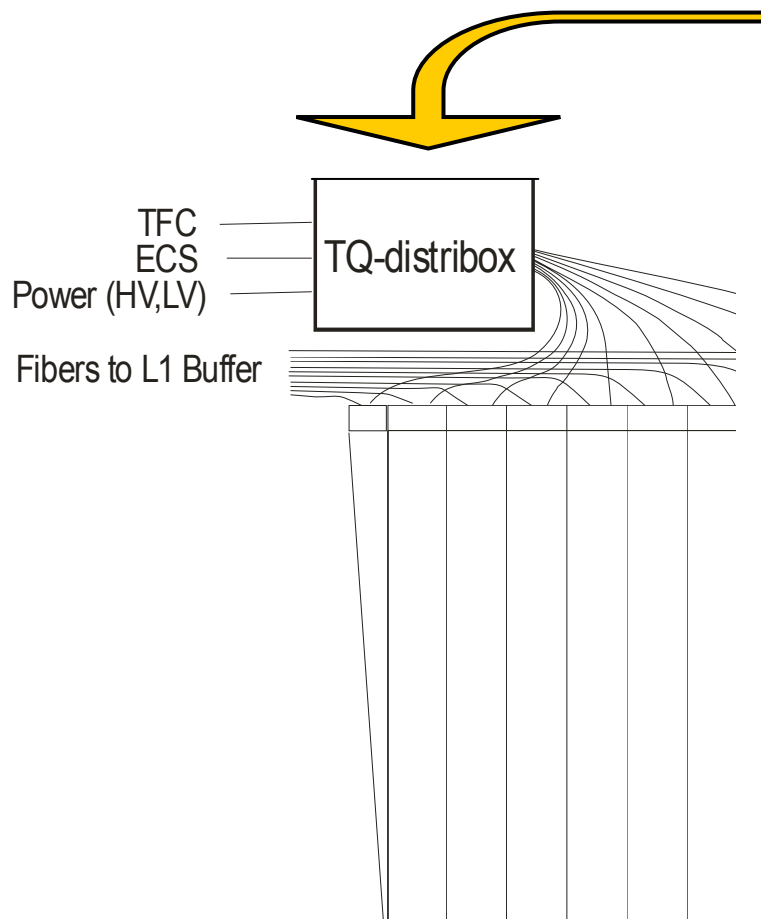


X 8

OTIS TDC chip

H.Deppe
U.Stange

Services:



Service Box

TFC:

TTCrx + Rst Decoder → LVDS Signals → modules

ECS:

SPECS Slave → I2C bus lines → modules
→ JTAG → ADCs → LV sensing

Low Voltage:

passive +/- 5V distribution → modules

High Voltage:

passive distribution → 2 connections/modules

1 service box / 2-stereo-layer quadrant:

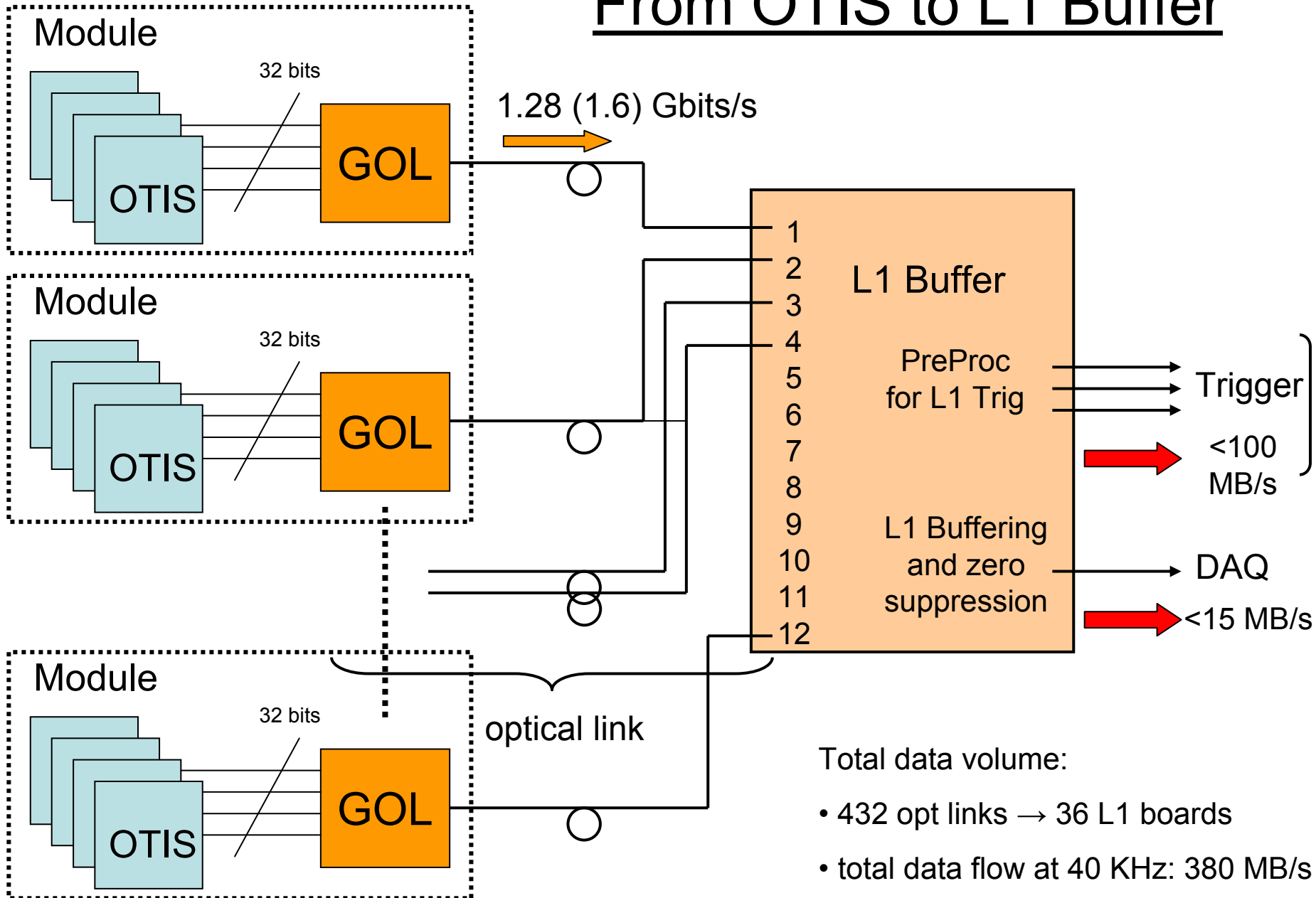
→ $4 \times 2 \times 3 = 24$ Service Boxes

T.Sluijk, A.Zwart

ECS: Expected Data Volume

I2C:	OTIS Initialization	8 Byte/OTIS	at start-up
		32 Byte/module	
		576 Byte/service-box	
	GOL Initialization	4 Byte/GOL	at start-up
		72 Byte/service-box	
JTAG:	LV/Tmp readout	4 (20) Byte/ADC	~1/min (start)
	18 ALICE ADCs	72 (360) Byte/service-box	

From OTIS to L1 Buffer



VCSEL

GOL

EV2-C Layer 1

COL 1,1 TESTBOARD
PHYSIK. INST. UNI HEIDELBERG
RAV/WIE 03-JUN-02

ALTERA
ACEX™
EPW10K10-10-10B128K10

GOL

JTAG

Power

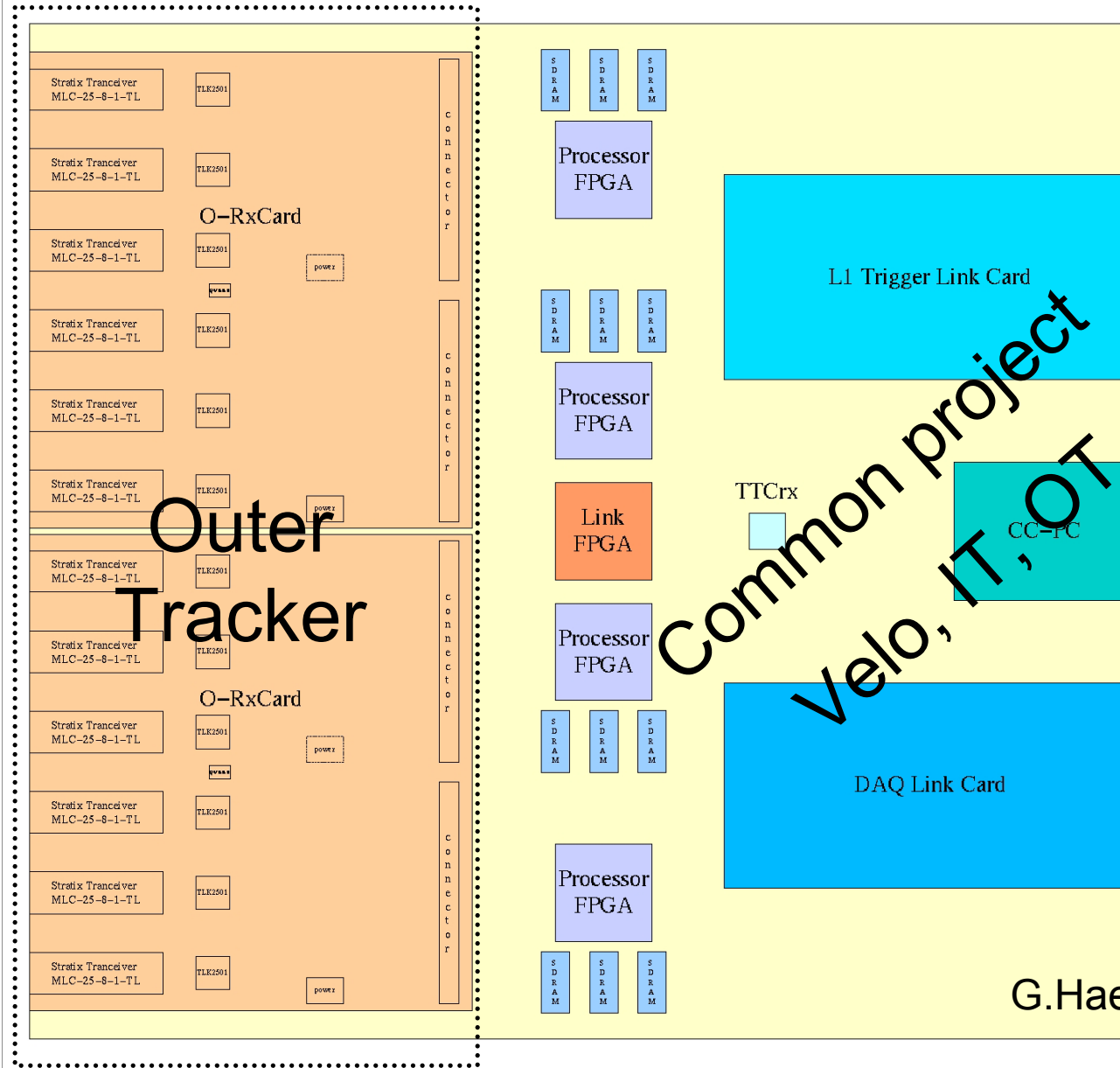
ENTER



⇒ Error rate $< 10^{-13}$

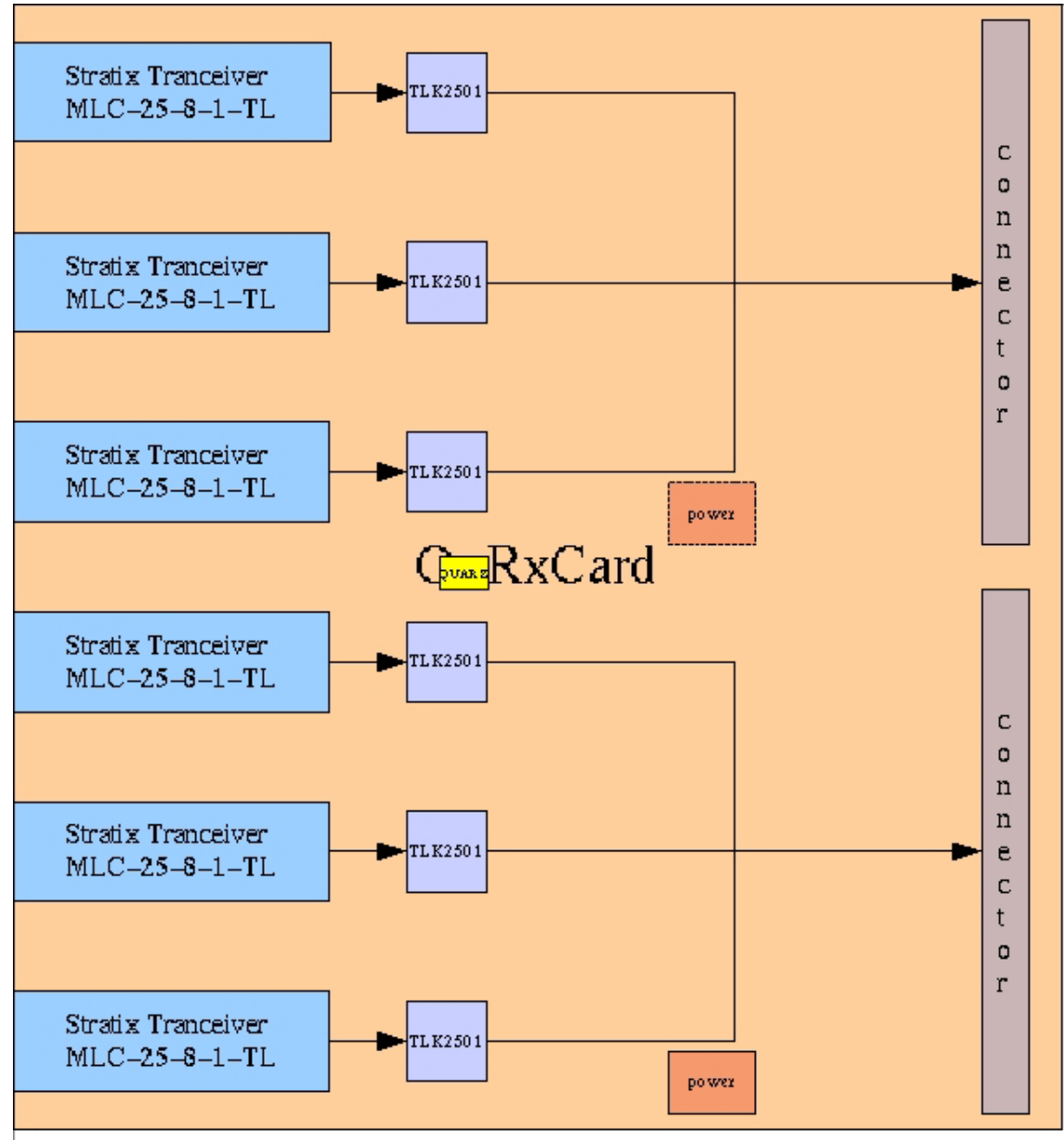
A.Rausch,
D.Wiedner

L1 Buffer Board:



G.Haefeli et al.

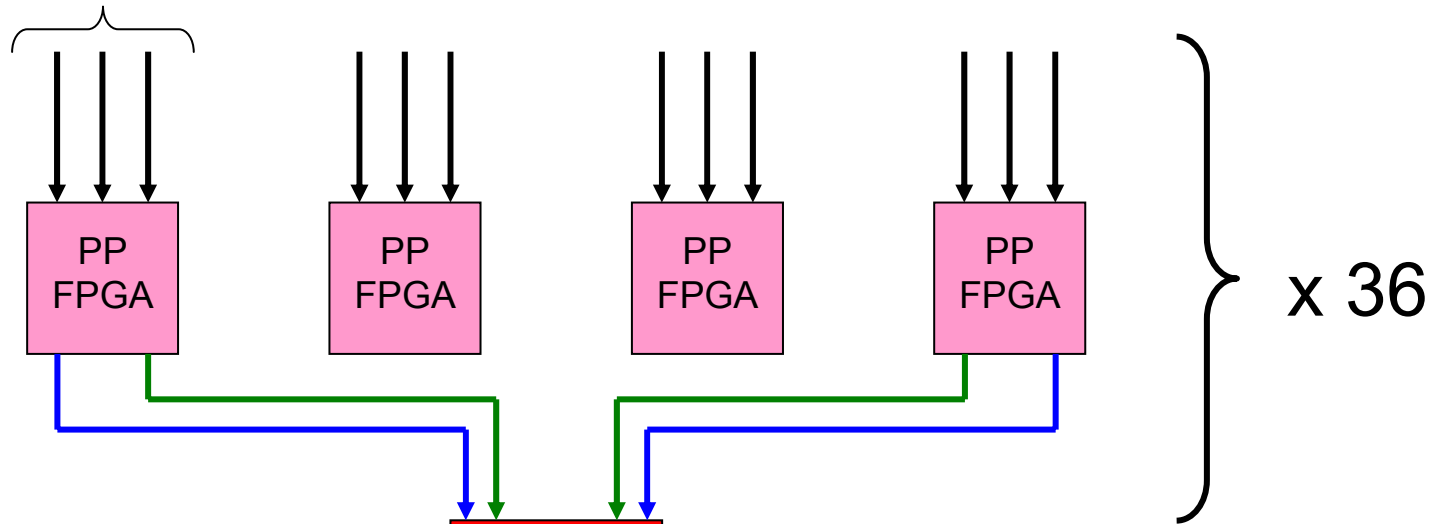
OT Receiver: O-RxCard



A.Rausch,
D.Wiedner

L1T/DAQ Data size:

3 GOL = 12 OTIS = 384 Ch



L1T fragment link:

Occup.	Data/event
2% (av.)	155 bit
4% (max)	278 bit
Hit mask	416 bit

@1.1MHz

L1T Link: 680 Mbit/s

@ 1.1MHz (2%)

Occup.	Data/link	tot evnt
0%	204 Byte	7.3 kByte
2% (av.)	266 Byte	9.6 kByte
4 % (max)	328 Byte	11.8 kByte

DAQ Link: 10.6 MByte/s @ 40kHz (2%)

Outer Tracker Electronics: Time Schedule

