The OTIS TDC for LHC*b* Status and Prospects

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Outline

- LHC*b*-Outer Tracker Front End Electronics & OTIS Architecture

- The OTIS Chip:
- TDC Architecture
- Read-Out Modes

- OTIS 1.1 Prototype
- Measurements & Test Results

- OTIS 1.2
- Changes and Improvements

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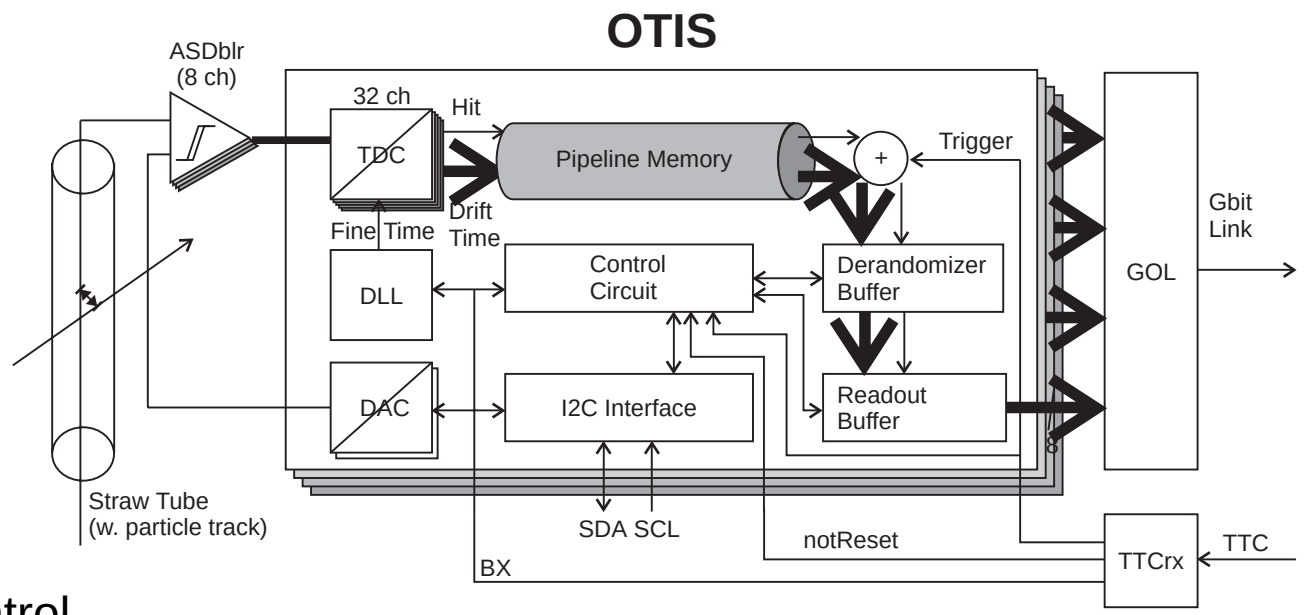
Outer Tracker Front End Electronics

Outer Tracker

- Straw Tubes with 5mm ⌀
- About 50 000 channels
- 128 Channels per module
- On-detector F/E electronics

FRONT END Electronics

- ASDblr discriminator
- OTIS TDC
- GOL readout
- TTCrx and SPECSslave control



OTIS Requirements

- ≤ 1ns resolution
- up to 55ns drift time
- 40MHz clock driven design
- Dead Time free operation
- 1.1MHz L0 trigger rate

- 4µs L0 trigger latency
- (160 samples pipeline depth)
- up to 10% occupancy
- radiation tolerant design

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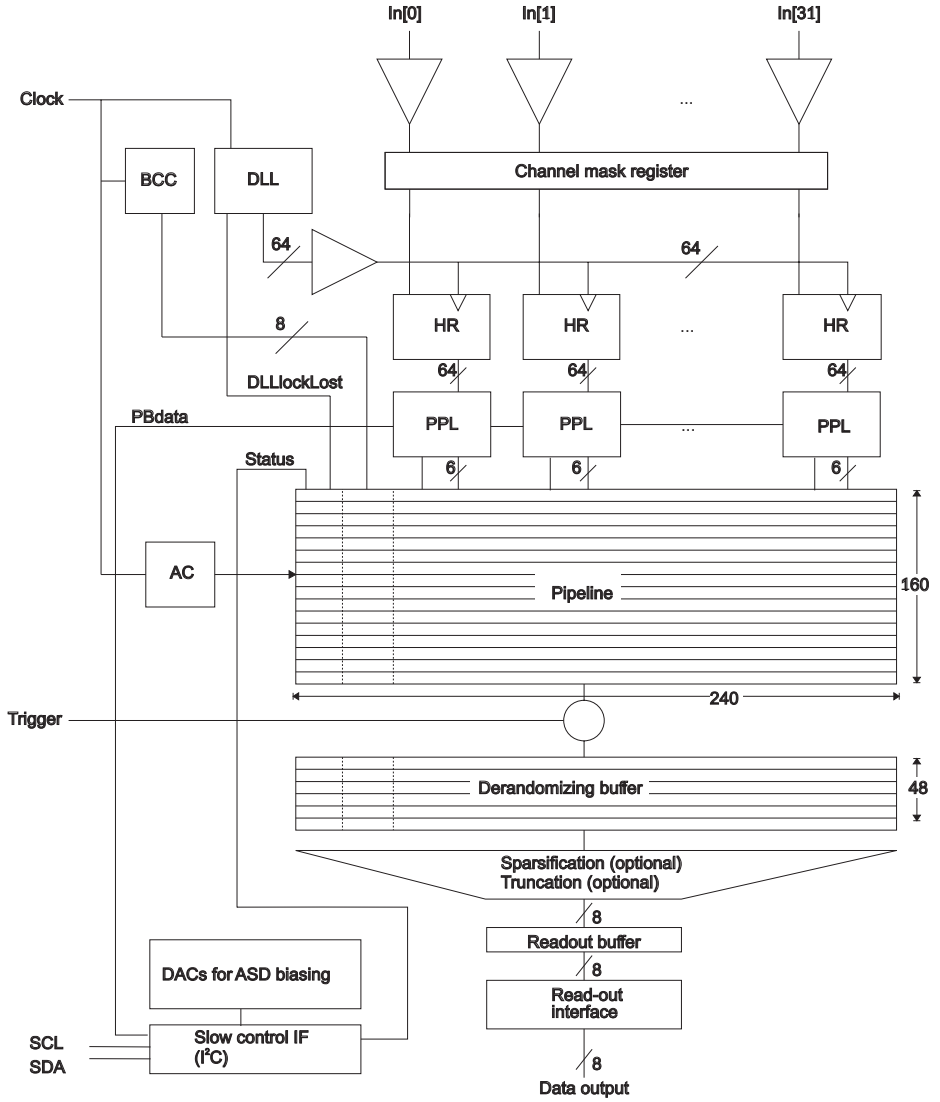
OTIS Schematics

Components:

- 32 maskable channels
- TDC core, consisting of
- DLL, hit register & pre-pipeline logic
  6-bit driftime measurement
- Pre-Pipeline register
  insertion of playback data
- Pipeline memory & derandomiser buffer:
  intermediate storage to compensate L0
  trigger latency and rate fluctuations
- Control circuit
  memory & trigger management
  output data formatting
- Slow control interface
  programming of operational parameters
  status monitoring
- DACs
  ASD threshold adjustment



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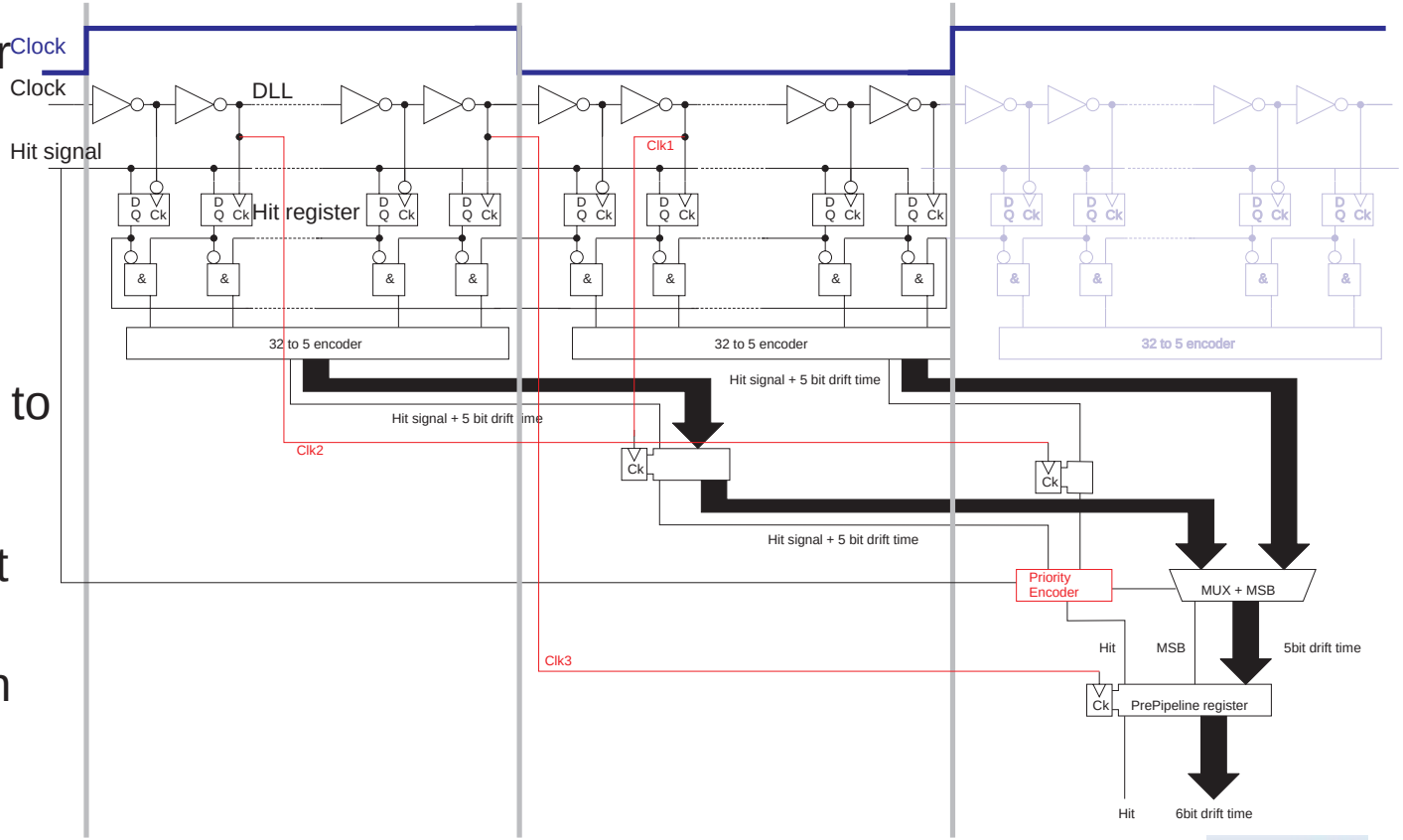
OTIS 1.1 TDC

TDC Modifications

- Revised clocking schema:
- ALL TDC clocks derived from DLL (i.e. controlled delays vs. uncontrolled delays of OTIS 1.0 timer block)
- TDC consists of only 1 clock domain (boundry between PrePipeline register and memory)
- Modified hit bit handling to supress more than 1 hit/BX and prevent propagation of the hit bit into the next BX
- Balanced drive & load in DLL to fix last bin mismatch



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Readout

- 1, 2 or 3BX per trigger can be searched for hits, i.e. the maximum drift time is 75ns
- 2 different readout modes (data formats)
- 8bit parallel output port
- 40MHz clock synchronous
- 320Mbit/s data rate
- Differential CMOS signals (LVDS on OTIS 1.0)
- ”DataValid” signal indicates data transmission
- Four OTIS chips can directly interface to 1 GOL chip

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Readout Mode I

Encoded Hitmask

- only first hit per channel and trigger is read out
- 25ns (1BX) 50ns (2BX) or 75ns (3BX) max. Drifttime
- 900ns readout time
- no truncation or sparsification
- unrestricted occupancy
- 8bit drift time encoding (byte aligned data)
- Optional "Comma" in front of non-consecutive readouts

Bit	0...31	32...39	....	280...287
Data	Header	Drift Time (ch 1)	....	Drift Time (ch32)

8 Bit drift Time encoding

First Hit Position	Data
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	11XXXXXX

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Readout Mode II

Plain Hitmask

- up to 1 hit/BX (i.e. up to 3 per channel) and trigger
- 25ns (1BX) 50ns (2BX) or 75ns (3BX) max. Drifttime
- fixed 900ns readout time by truncating or adding “0”s to the data stream (selectable)
- max. 87.5% occupancy for 1BX
- max. 37.5% occupancy for 2BX
- max. 20.8% occupancy for 3BX
- **8bit drift times = byte alignment of the data**
- Not implemented on OTIS 1.0
- Removed from OTIS 1.1 due to circuit size
- Modified to fit on OTIS 1.2

Modified !

Bit	0...31	32...63	64...71	....	58+(8n)..71+(8n)
Data	Header	1 Hitmask	Drift Time [1]	....	Drift Time [n]

Bit	0...31	32...95	96...103	....	90+(8n)..97+(8n)
Data	Header	2 Hitmasks	Drift Time [1]	....	Drift Time [n]

Bit	0...31	32...127	128...135	....	122+(8n)..129+(8n)
Data	Header	3 Hitmasks	Drift Time [1]	....	Drift Time [n]

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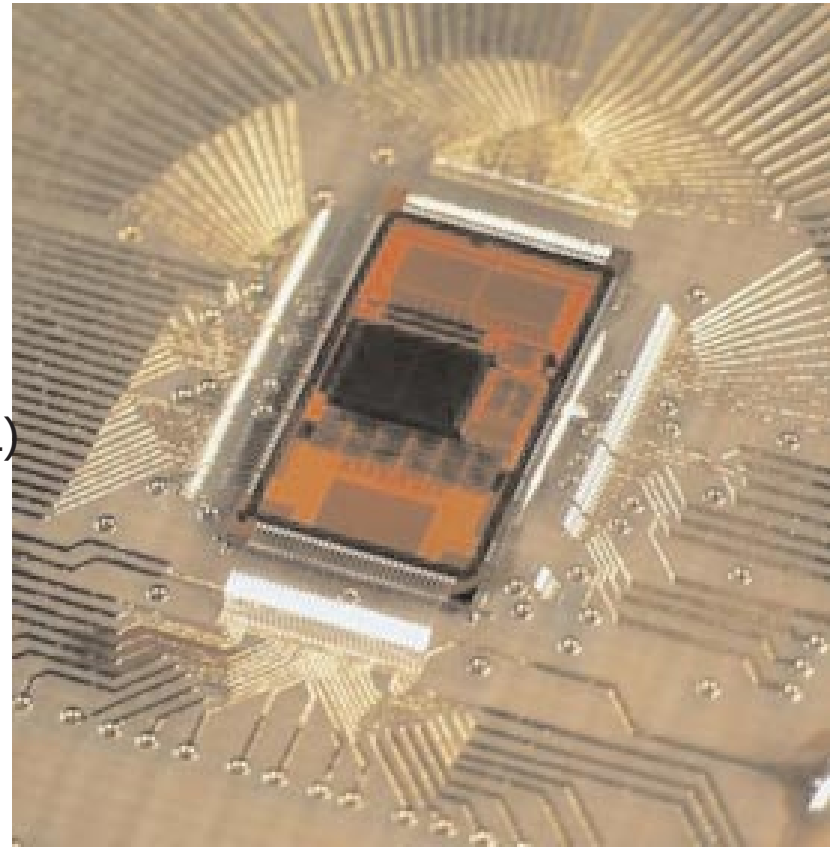
OTIS 1.1

2nd full-scale prototype

- Manufactured in commercial 0.25µm CMOS technology
- Die Size 5.1mm x 7.7mm
- Submitted November '03
- Back February '04



Improvements

- Fixed TDC missing-code problem
- Matched load of last DLL element (improved DNL)
- “DataValid” signal for GOL control
- Slow data readout via I^2C interface
- Buffered outputs for ASD threshold adjustment
- Differential CMOS outputs

Restrictions

- Still only implements the “Encoded Hitmask” readout mode

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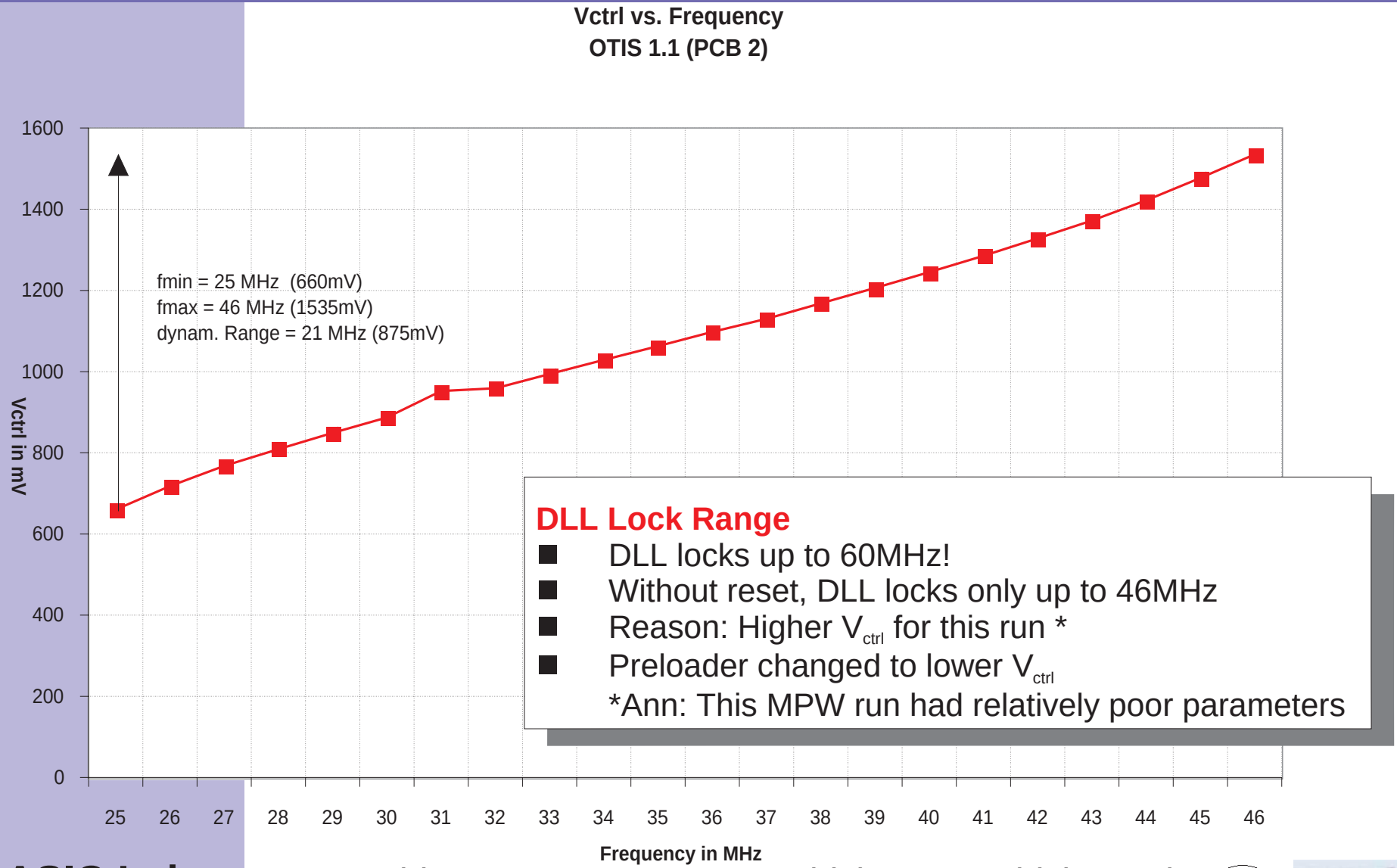
OTIS 1.1 Results I



DLL Lock Range

- DLL locks up to 60MHz!
- Without reset, DLL locks only up to 46MHz
- Reason: Higher V_{ctrl} for this run *
- Preloader changed to lower V_{ctrl}

*Ann: This MPW run had relatively poor parameters

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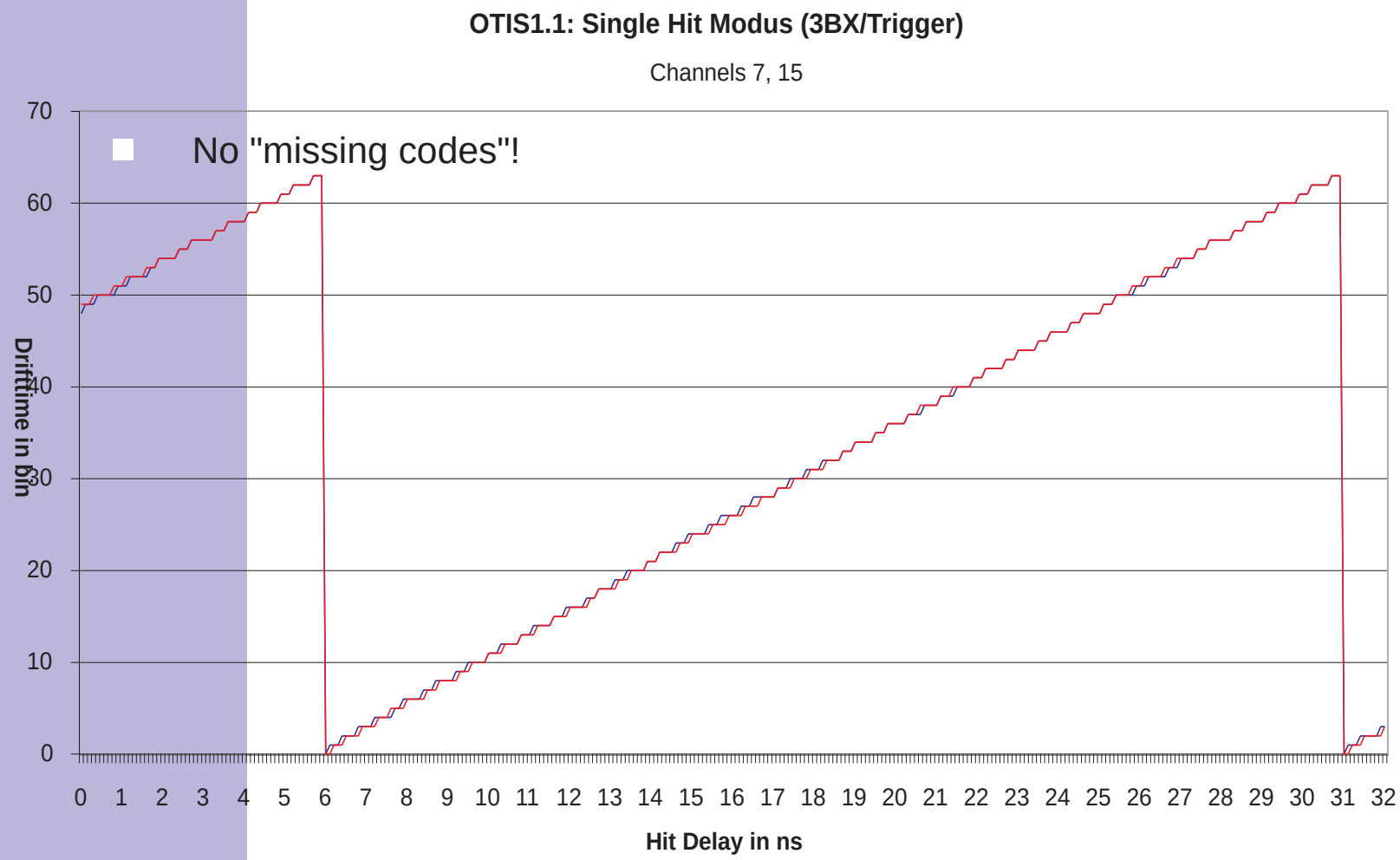
OTIS 1.1 Results II



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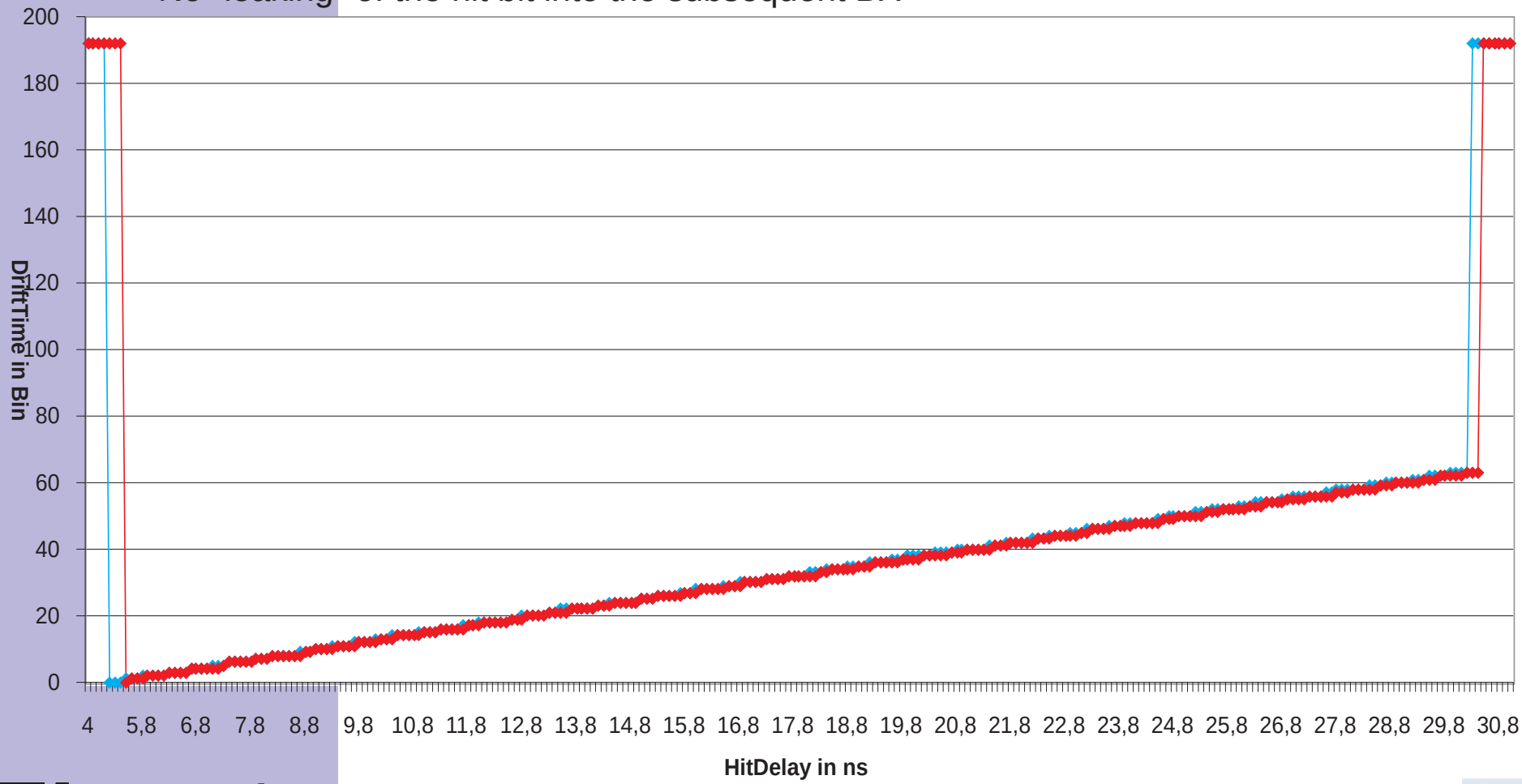
OTIS 1.1 Results III

OTIS 1.1 Single Hit Modus (1BX/Trigger)
Channel 15&16 (PowerSupply only VDDd)

- No "leaking" of the hit bit into the subsequent BX



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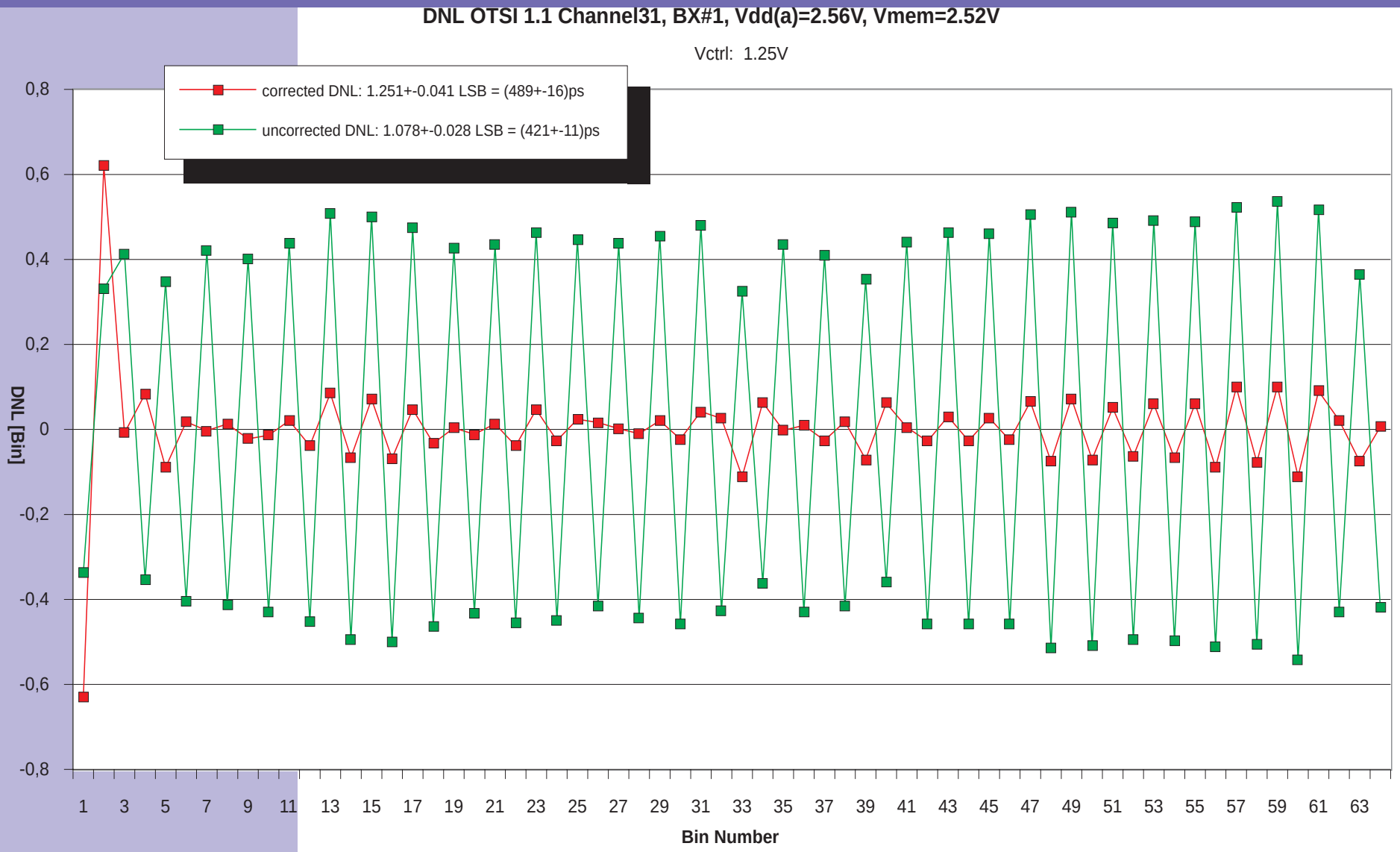
OTIS 1.1 Results IV



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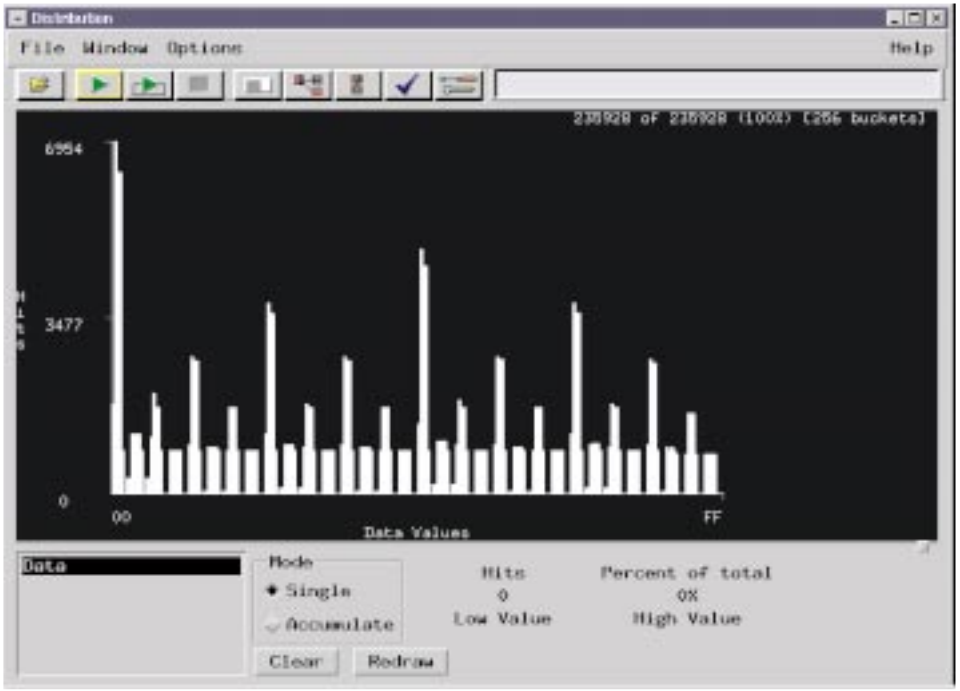
OTIS 1.1 Results V

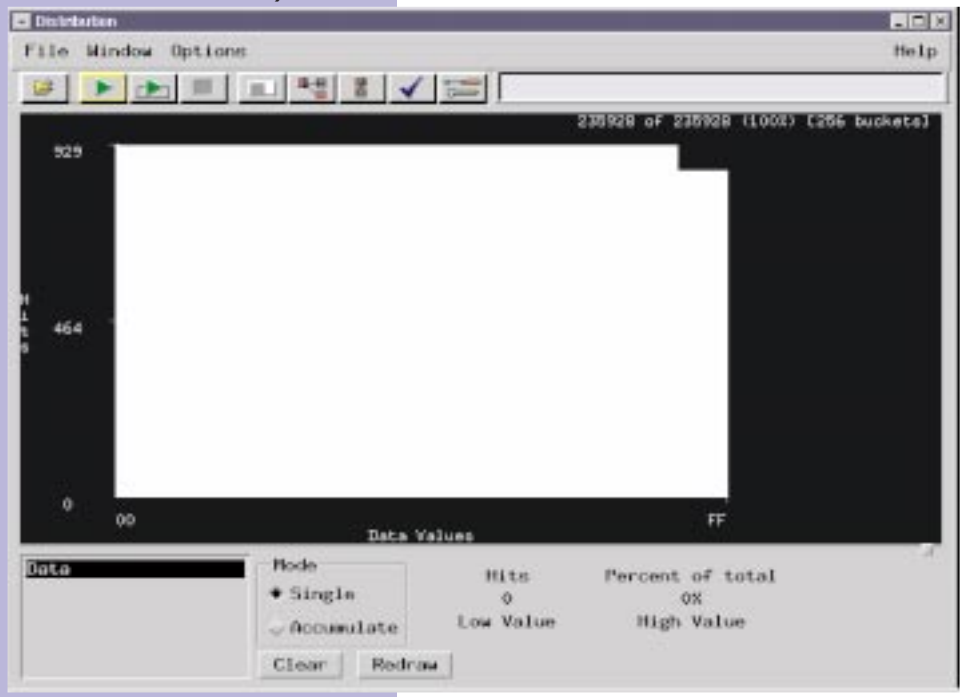
BX-Counter

- Histogram of the BX-number shows a weird distribution
- Increasing the memory's power supply from 2.5V to 3.5V solves the problem
- Histogram with V_{mem}=3.5V shows expected shape (dent on top left due to LHC cycle)



Cause:

- Evaluation of the shematic shows a gate load of 50 cells + 1.6mm wire load for the BX-bits (compared to 2 for drift-time bits)



- Memory outputs can only drive ~100fF (2 cells and some 10µm of interconnect)
- Increasing V_{mem} increases memory speed and output level (wrt. to the unchanged threshold of subsequent gates)
- Driving capability of memory was not (and can not) considered during synthesis of of the Fast-Control circuit

Fix:

- Insertion of buffers

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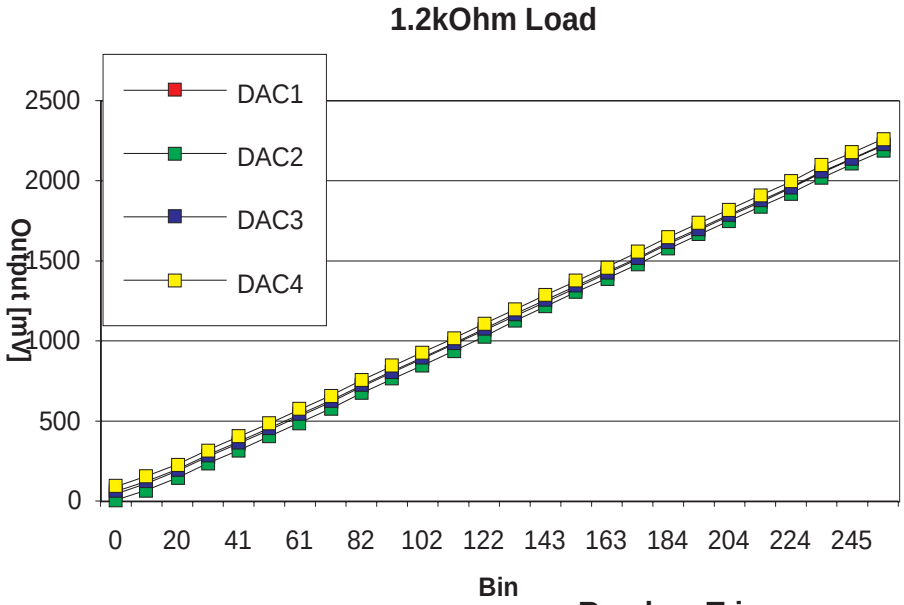
OTIS 1.1 Results VI

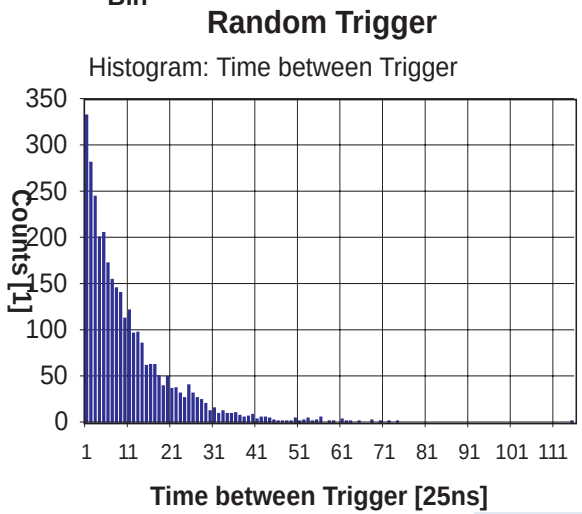
DAC's

- Good linearity
- Offset spread of 80mV$_{pp}$ assumed to originate from source followers



Random Trigger Test:

- 15:35 h @ 1.1MHz
- 6.14*10^{9} Triggers
- Chips still in sync
- no missing triggers
- BX and EV counters in sync



Memory Self-Test:

- works OK despite the BX counter problems

Resets:

- work as designed
- Caveat:
- Discharge PWR-Up cap is very slow even if clocks and power are cut

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OTIS 1.2 Changes

Summary of changes:

- Implementation of 2nd (multi-hit) readout mode
- Drive matching of DLL to improve DNL
- Fix of BX counter data by buffers driving the fast-control inputs
- Drive matching of memory-fast control interface by decoupling buffers (fine-time and hit bits) for yield reasons
- DAC buffers with dummy structures to improve matching (offset spread)
- Add missing inverter to fix V_{ctrl}-monitoring
- Added pull-up pad for DLL-reset
- Minor changes and cosmetics: pad ring, power bars etc.

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Summary & Outlook

OTIS 1.1:

- Fulfills all LHC*b* requirements (timing, control signals etc.)
- Will seamlesly fit into the OTR readout chain
- Has a perfectly working TDC
- Still misses the 2nd readout mode
- Gives erratic BX counter values
- But: EV-counter works (usability for test beams)

OTIS 1.2:

- Incorporates an further improved TDC (DNL in first bin)
- Features all readout modes
- Also includes minor improvements mentioned before

- Will be submitted in the CERN MPW13 run for production at the 24. May
- Chips from an engineering run (i.e. higher quantities) can not be expected before Q2 2005

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