ASIC Labor Heidelberg

OTIS

TDC for LHCb Outer Tracker Readout

Electronics Meeting OT

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OTIS GROUP, Heidelberg University

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OTIS TDC

Changes OTIS 1.0 => OTIS 1.1

- TDC-Core
- Digital Part
- Pad Layout & Misc

Chip Geometry OTIS1.X

- Package size
- Testboards (COB)

New OTIS Reference Manual

http:/wwwasic.kip.uni-heidelberg.de/lhcbot/secure/Specifications/OTIS11-UserManual.pdf

Usr: Otis

Passwd: DriftTime

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OTIS TDC Core

	OTIS 1.0 Submitted Apr 02 / Back Jul 02	OTIS 1.1 Submitted Nov 03 / Back Feb04
DLL DNL	1.39 ± 0,06 LSB (540ps)	0.64 ± 0,05 LSB (250ps) (expected)
DLL Lock Lost		Check of DLL Lock Lost (merged to Error bit)
Drift Time Encoding	Timing Problems	Seperate Time Domains‘ (TDC-Core and Mem&FC) Clock domain boundry between PrePipeReg and Memory Improved routing All TDC clock‘s derived from DLL
Hit bit handling	Problems with propagation of HitBit to next BX	Driver added and improved routing

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OTIS Digital Part

	OTIS 1.0 Submitted Apr 02 / Back Jul 02	OTIS 1.1 Submitted Nov 03 / Back Feb04
Read Out Mode	Mode I (Encoded Hitmask)	Mode I (Encoded Hitmask) Mode II not implemented
Derandomizer Buffer Output	Registerblock's are used for intermediate storage	Latching functionality of SRAM used
Revised Reset schema	L0- and PWRUp Reset	BX- and Event Counter Reset added DLL-Reset via Pad + I2C added
BX-Counter		BX counter 12bit int / 8bit ext L0 Reset sets BX-C to 0 BX Reset sets BX-C to Latency+Offset(*) BX-C rollover after 1 machine-cycle(*)

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OTIS Digital Part

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Address schema	7 bit I2C 5 OTIS ID	7 bit I2C 12 OTIS ID
DAC		Voltage Buffer added to serve ASD-X threshold levels
Slow Control (I^2C)	Input pads 2.5V	Input pads 5V compatible Triple redundant 1 Event readout via I2C (*)
Fast Control: Data Output	LVDS Output	Data Output differ.CMOS DataValid Signal added „Komma“ for nonconseq. readout (*)
Debug and Service Features	D-Buffer Fill Level Monitoring of R/W Pointer Start/Stop Read Out Sequence MemorySelf-Test	SEU for SlowControl Event-ID Register via I2C Revision Register DLL Lock Information

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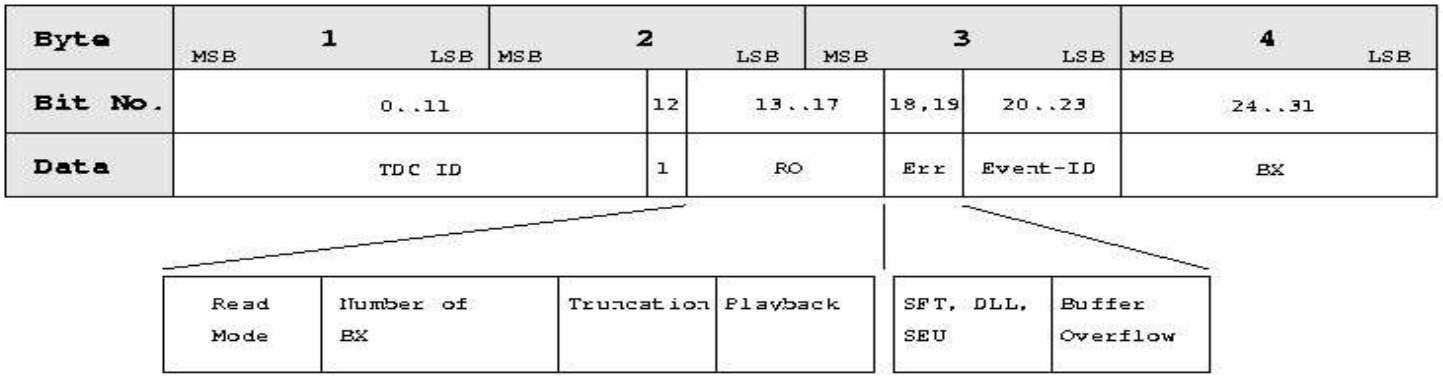
Header Data format OTIS 1.1

Header Data Format (OTIS1.1)



Annotations:

Event-ID added (represents number of actual data output sequence since Event-ID reset)

Error bit (Self Test Failed, DLL Lock Lost, SEU Detected) are merged to one Error bit for OTIS 1.1

Truncation: no use on OTIS 1.1

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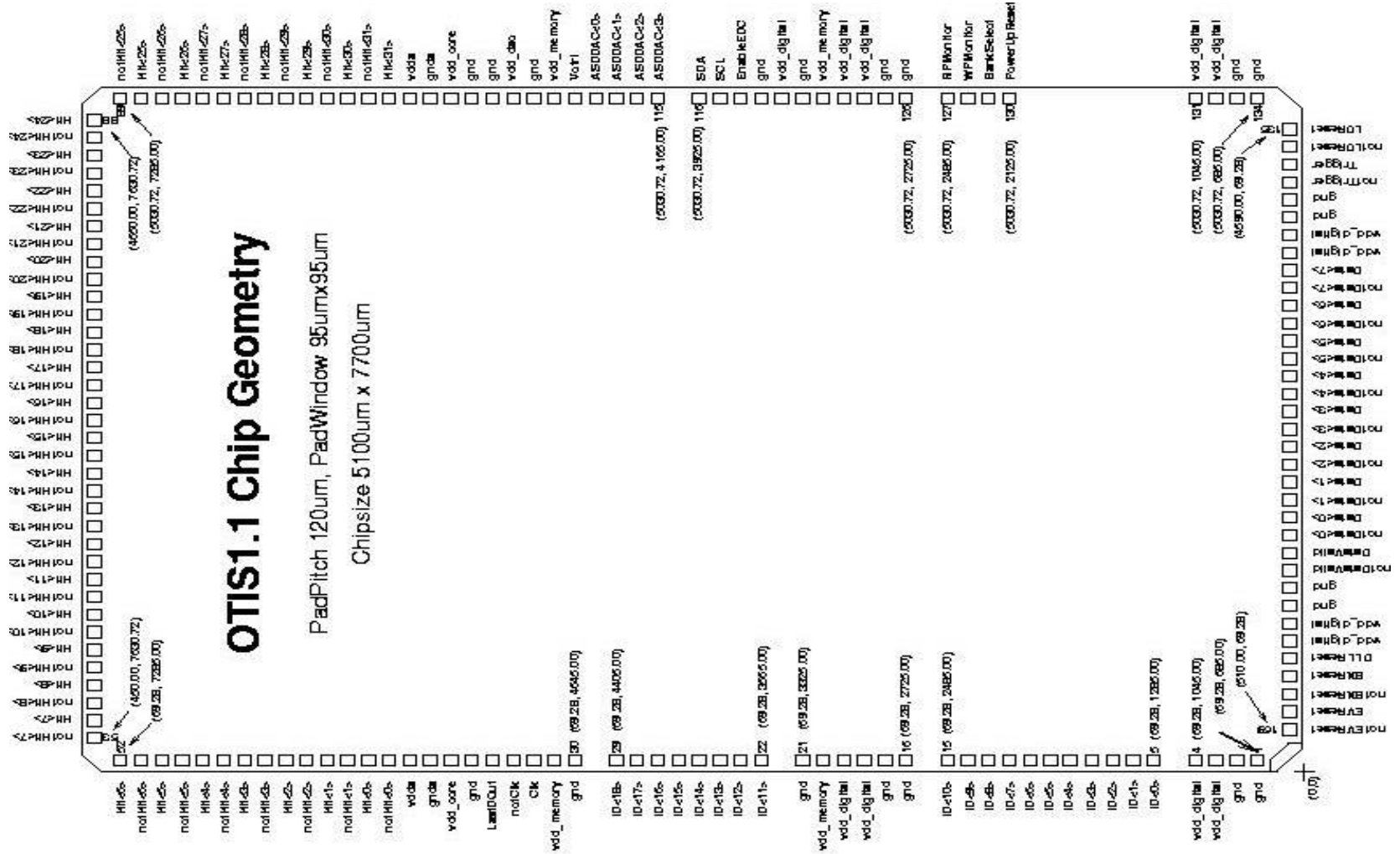
Pad Layout OTIS 1.1



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Chip Geometry OTIS 1.1

Chip & Package Geometry :

Size:	5100µm x 7700µm
Number of Pads:	169 = min. pins required
Pad Pitch:	120µm

LQFP :	176 pins	208 pins
Body size:	24mm x 24mm x 1.4mm	28mm x 28mm x 1.4 mm
Die pad size:	8mm x 8mm	11mm x 11mm
Problems:	Die pad size to small	Die pad size OK
	Bonding to close	Bonding OK

For test purposes COB technology possible
Bondwire length about 10mm to 12mm possible
For COB Gold surface for PCB essential

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