L1 Buffer Emulation

Stratix Evaluation Board

- same FPGA-Chip as TELL1-Board
- same memory interface as TELL1-Board

L1 Buffer Emulation (I)

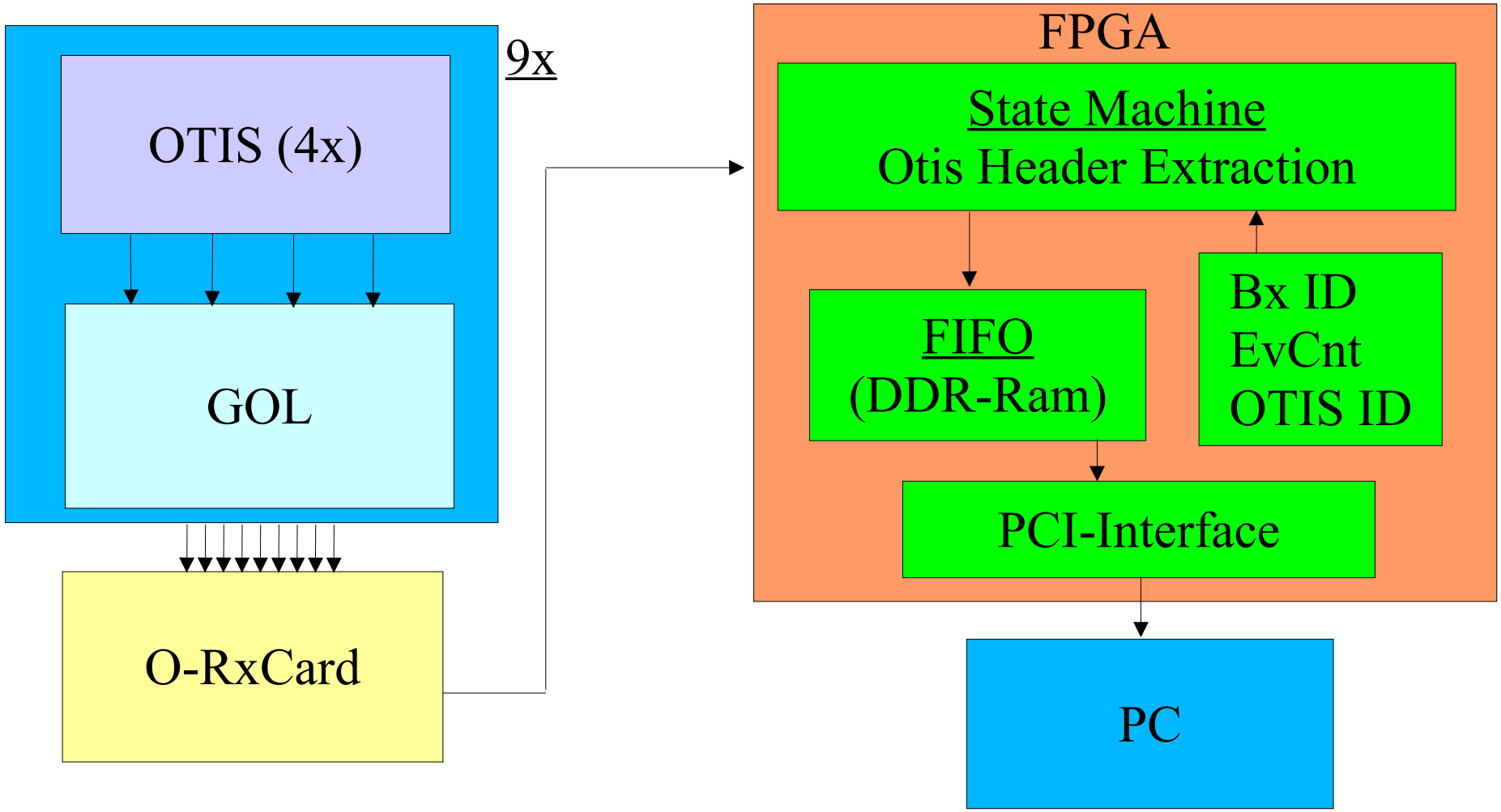
Input : 16 Bit @ 80 MHz Data from O-RxCard + Status Bits.

Actions :

(1) Synchronize on bit stream using OtisID's.
(2) Data processing (e.g. zero suppression).
(3) Store data in memory (up to 256 MB).
(4) Read data via PCI Bus.

Output : 32 Bit @ 33 MHz to PC via PCI Bus.

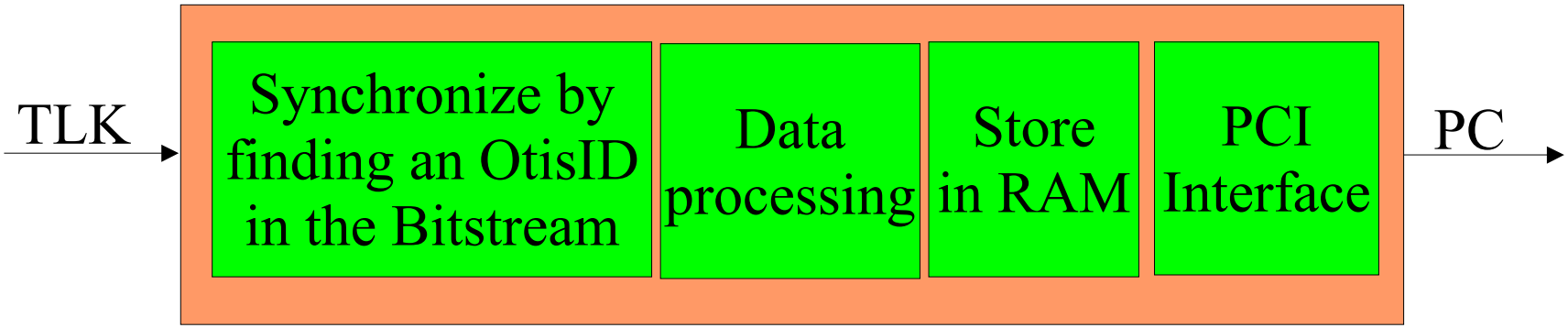
PCI-DAQ


9x
OTIS (4x)
GOL
O-RxCard
FPGA
State Machine
Otis Header Extraction
FIFO
(DDR-Ram)
Bx ID
EvCnt
OTIS ID
PCI-Interface
PC

Design flow

- Design → FPGA Advantage (HDLdesigner)
- Simulation → Modelsim (HDLdesigner)
- Synthesis → Leonardo Spectrum (HDLdesigner)
- Place & route → Quartus II

L1 Buffer Emulation (II)



Designed	done	--	--	in progress
Simulated	done	--	--	--
Synthesized	in progress	--	--	--
Place & route	--	--	--	--

First working setup : ~ end of february.