

Test results of the Prototype Outer Tracker Front-End Box

Ad Berkien
Tom Sluijk
Albert Zwart

GOL-AUX Board

- Four OTIS boards connected to the GOL-AUX board (R190-R192 removed). Oscillations observed on the supply voltages:
 - Tantal Elco's 100uF added on the power inputs and on the output of the negative regulator.
- Clock distribution is bad, BX- counter in OTIS are not equal
 - LVDS repeater (SN65LVDS108) mounted and connected to the OTIS connectors
- Settings:
 - Module location address switch = 1
 - I2C addresses 0x8 - 0xC
 - I2C pull-up 1K to 2.5V
 - Seldiv (J101) must be 1 >> GOL ready

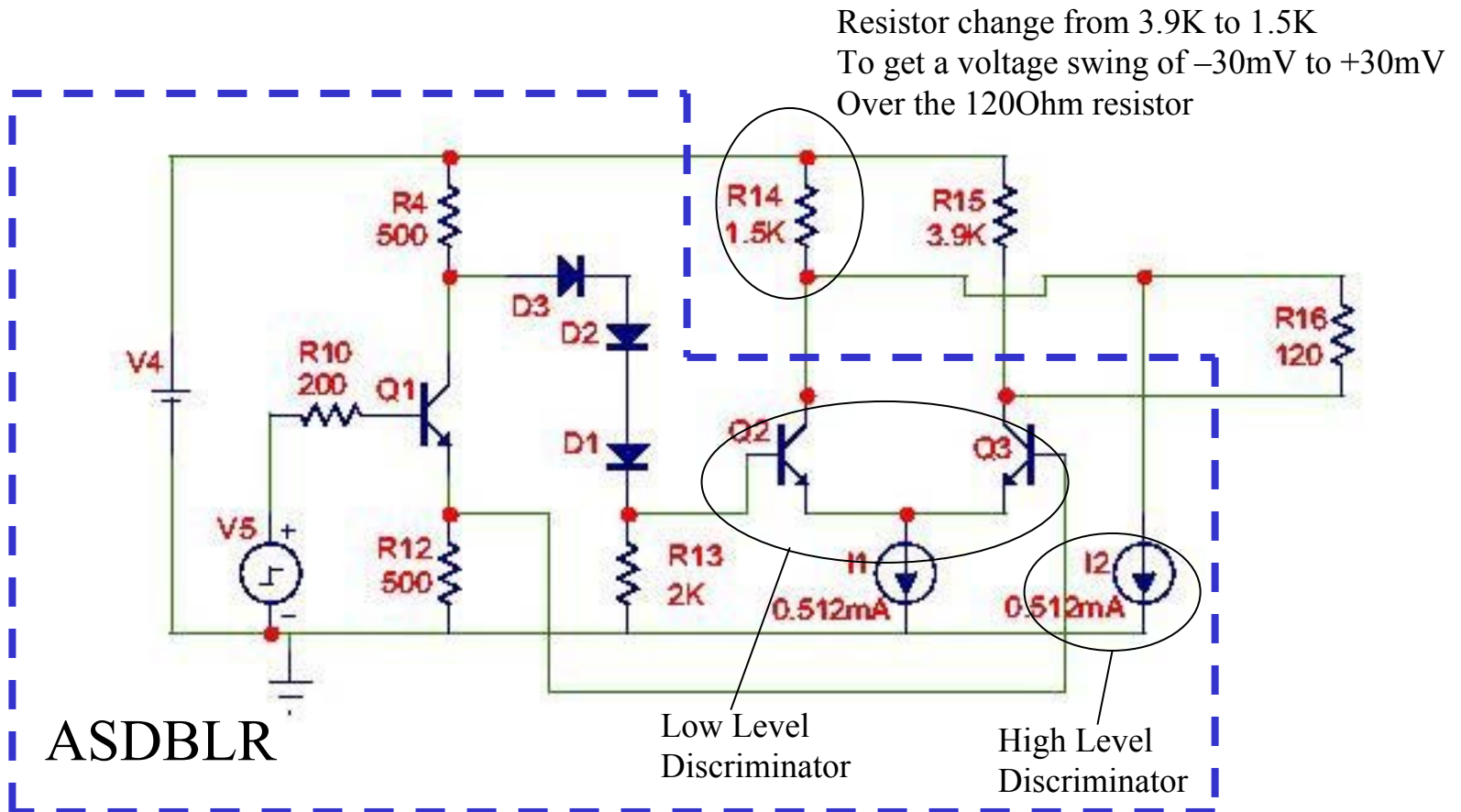
OTIS Boards

- Terminators (120 ohm) installed on clock vias and covered with epoxy
- Board manufacturer error; the inner layers are not 100u as requested
 - Too much voltage drop over the integrated coil for the digital VDD of the OTIS, new coil mounted.
 - Less heat spreading and conduction in the board.
- I2C clamp diodes removed, did not work as on the testboards(not understood)
- -3V power connection to the ASDBLR board has too much coupling to the digital VDD of the OTIS, noisy ASDBLR -3V power.
- +3V for the ASDBLR is also used for the LVDS receivers for the data to the GOL this makes a noisy ASDBLR +3V power.
- Cut in the ground plane under the coils gives an 10% increase of the inductance.

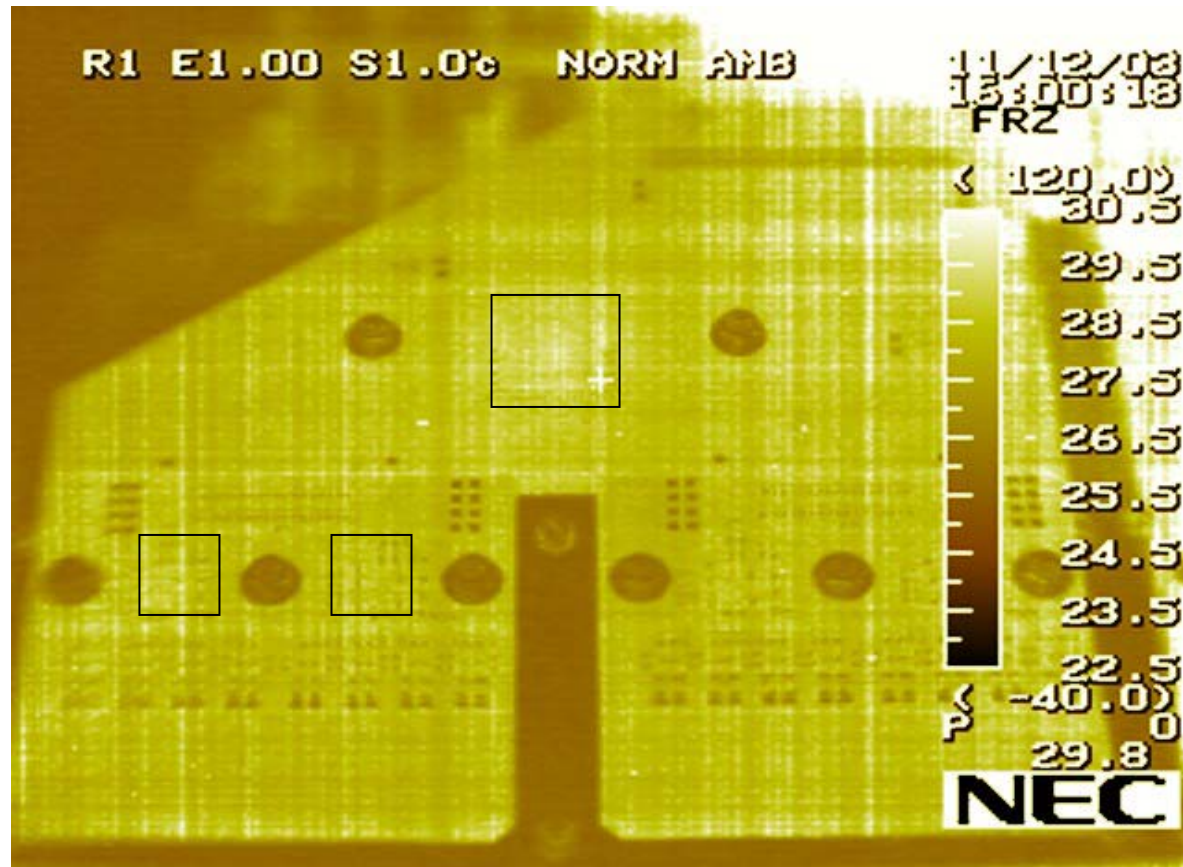
ASDBLR Boards

- ASDBLR changed; the high level discriminator cannot be disabled anymore
 - Change in the output resistors.
- Half of the channels are connected to the inverted input of the ASDBLR instead of the non-inverted input.
- Noise performance of the ASDBLR is better when the inverted input is left unconnected.

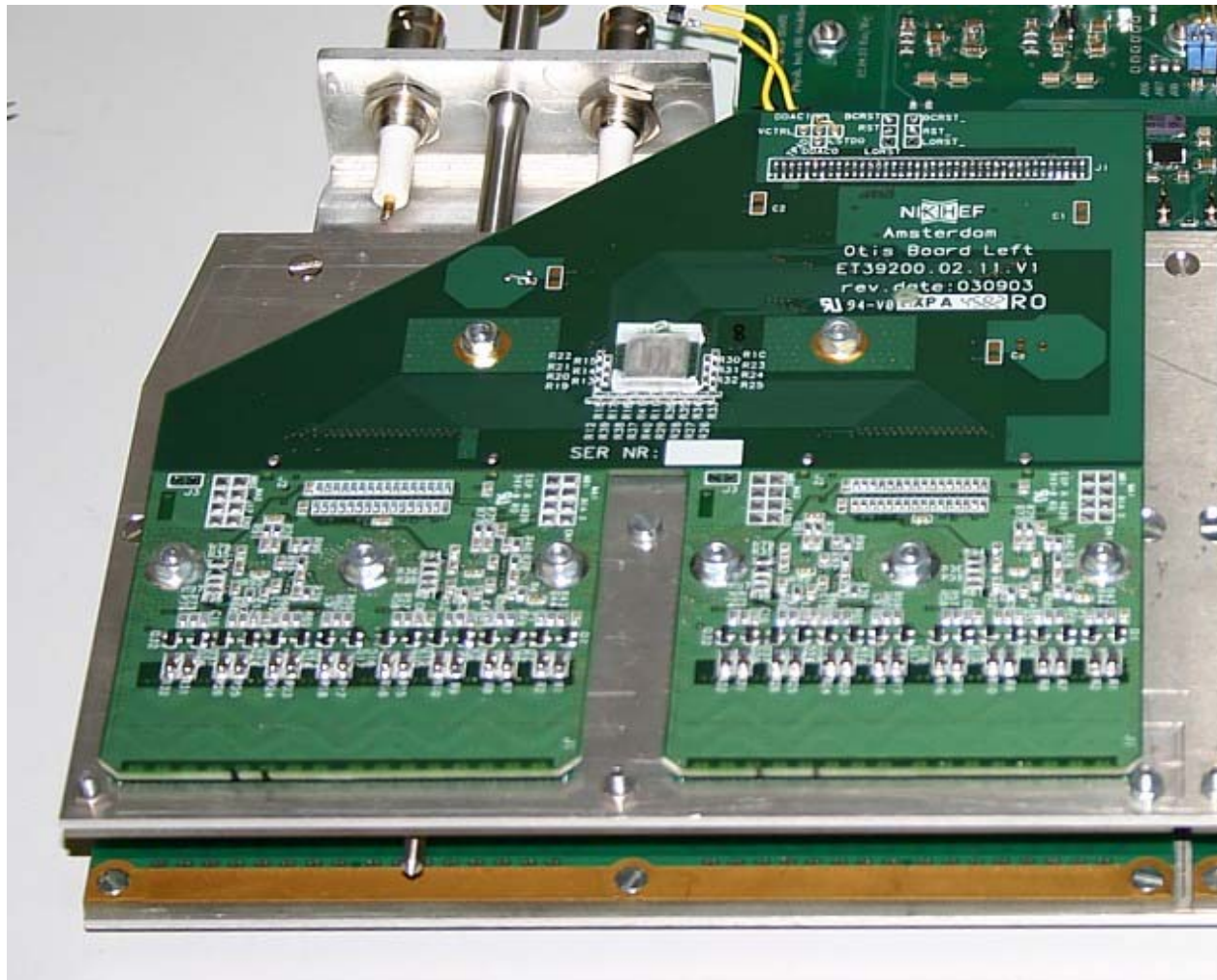
Output Circuit of the ASDBLR



Temperatures of the Otis and ASDBLR Boards



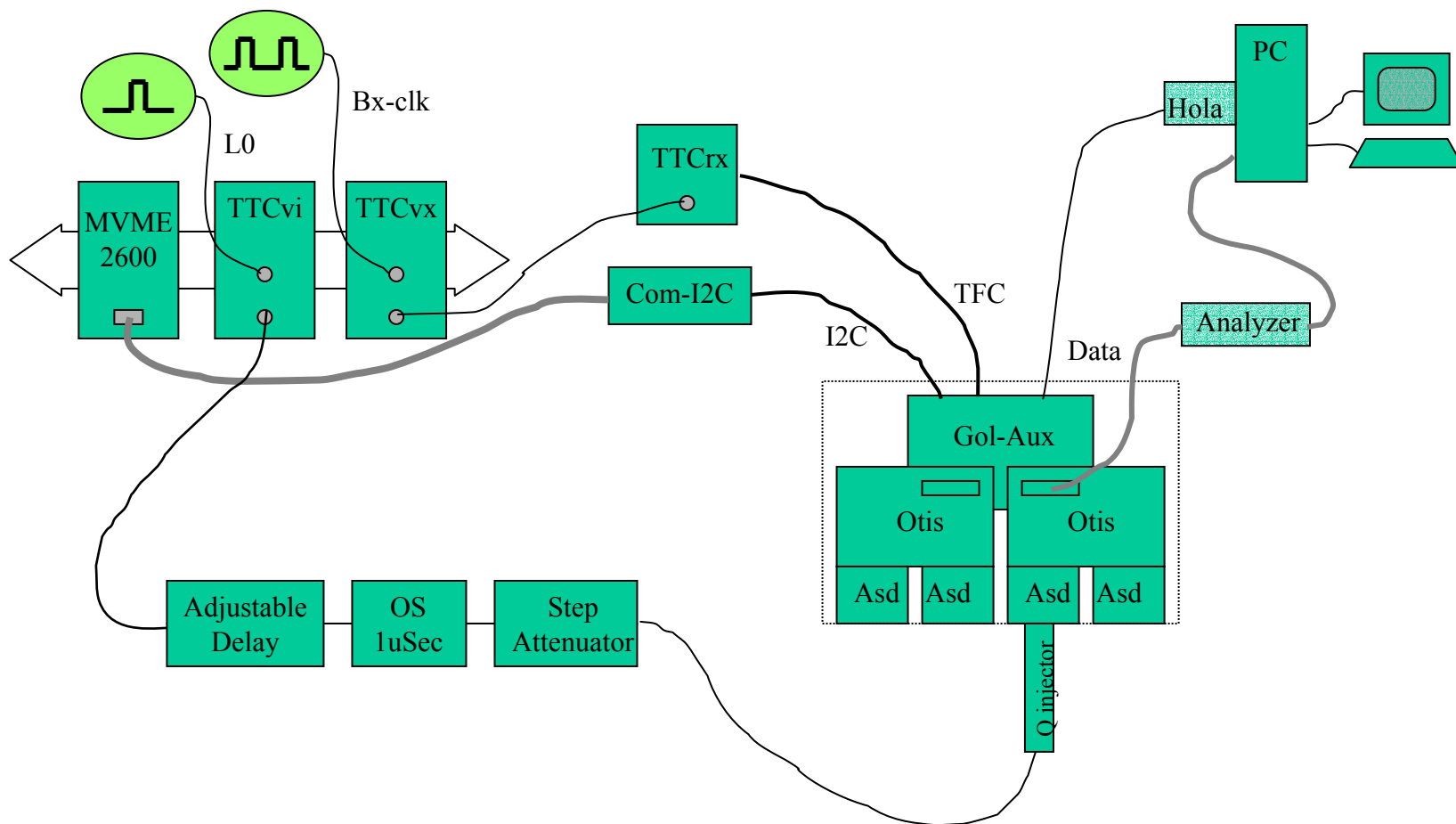
Area of the Temperature Picture



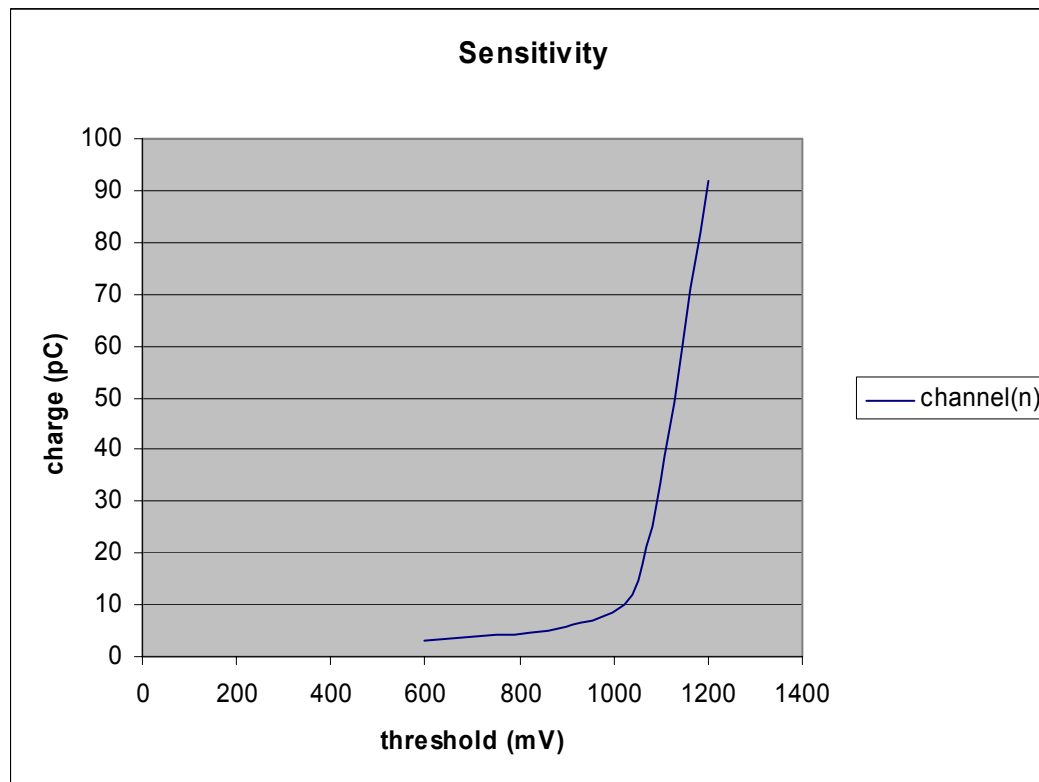
Power

- ASDBLR Board
 - Draws 150mA from the positive supply and 110mA from the negative supply
- OTIS Board
 - Draws 320 mA from the positive supply only
- Complete Front-end Box
 - Draws 2.6 A from the positive supply (+5.3V) and 0.9 A from the negative supply (-5.3V) if the the supplies are switch on simultaneously, if the supplies are switched on sequentially, the current of the positive supply is 180 mA higher (regulator in a different mode??)
- The currents mentioned are typical values!

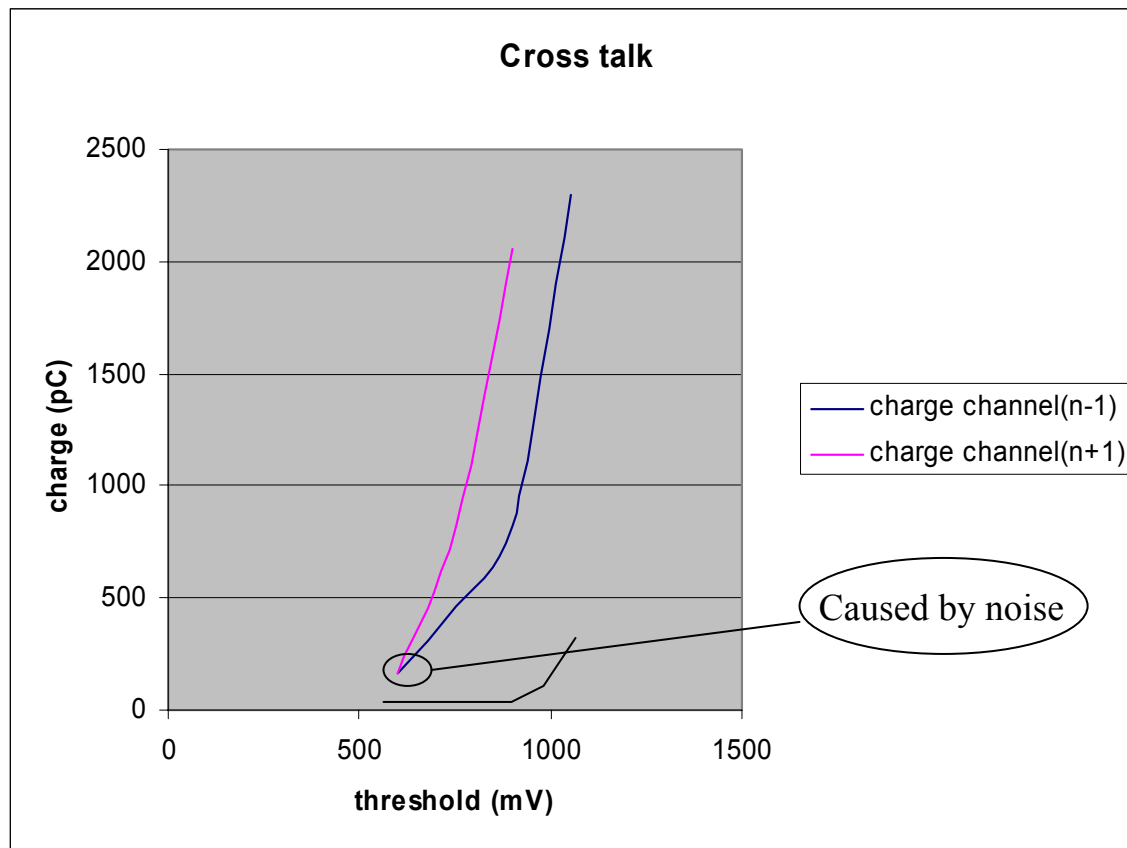
Test setup



Input Sensitivity



Cross talk



Noise Sources

- Via Power on the Otis board:
 - Otis read-out; the LVDS receiver is powered by the +3V that is also used for the ASDBLR. This causes noise hits at thresholds < 750 mV. In the next version this LVDS receiver is not needed anymore.
 - Bx-Clock; there is a capacitive coupling between the power to the ASDBLR boards (-3V) and the digital power plane of the OTIS. This causes noise hits at thresholds < 600 mV. Care must be taken in the next Otis board to keep the digital power plane from the power routing to the ASDBLR boards. Also keep outs in the GND plane are needed to keep the coupling to the ASDBLR power as low as possible. The tests are done with an 'open' Front End box, the coupling will be lower when the outer plates are mounted.
- At the Input of the ASDBLR:
 - The inputs of the ASDBLR are symmetrical, so the circuit at the negative input is the same as the positive input, this causes noise to be injected in the negative input. If the negative input is left open the noise hits at a threshold of 550 mV goes from 35% to 1,8%. The cross talk figures do not change when the negative input is left open.

Noise

The noise figure is determined by applying test pulses at a specific threshold level and measure the hits at output of the ASDBLR. At a threshold of 750 mV and a testsignal < 3 pC, no hits at the output. If the test pulse is 5,8 pC every testpulse gives a hit at the output.

This gives a noise figure of 2,8 pC.