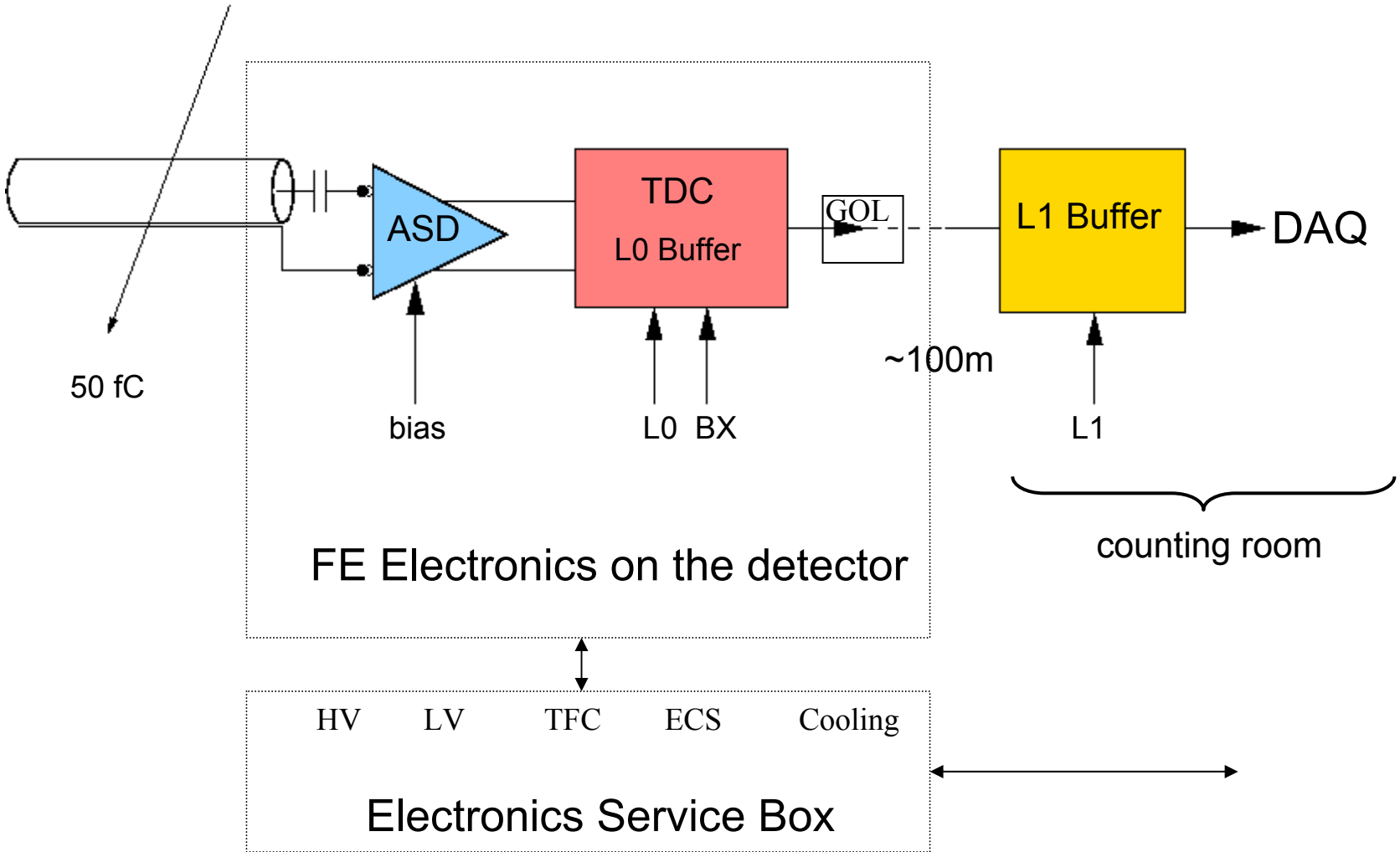
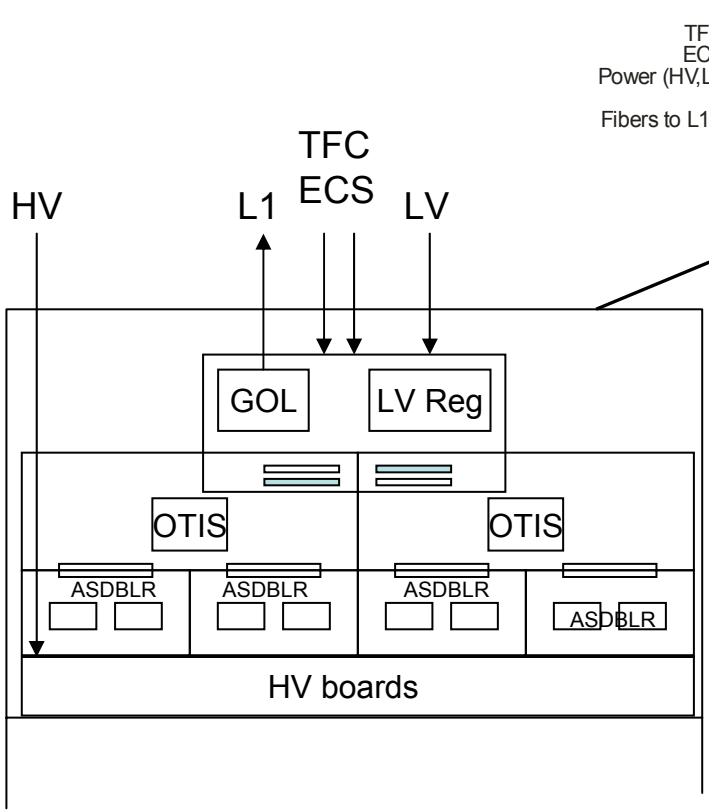
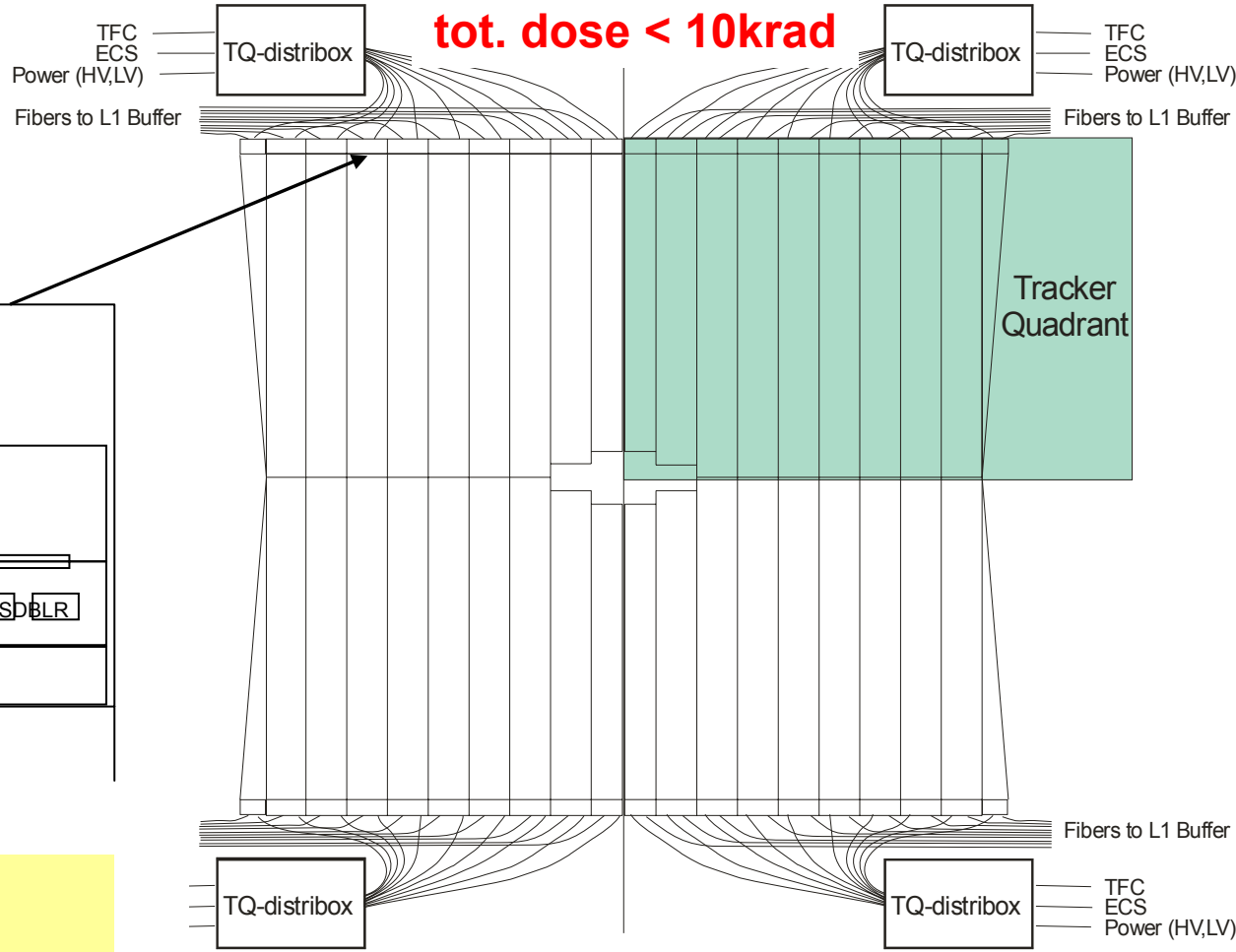
FE Electronics - Overview







Module End:

128 channels

16 ASDBLR chips

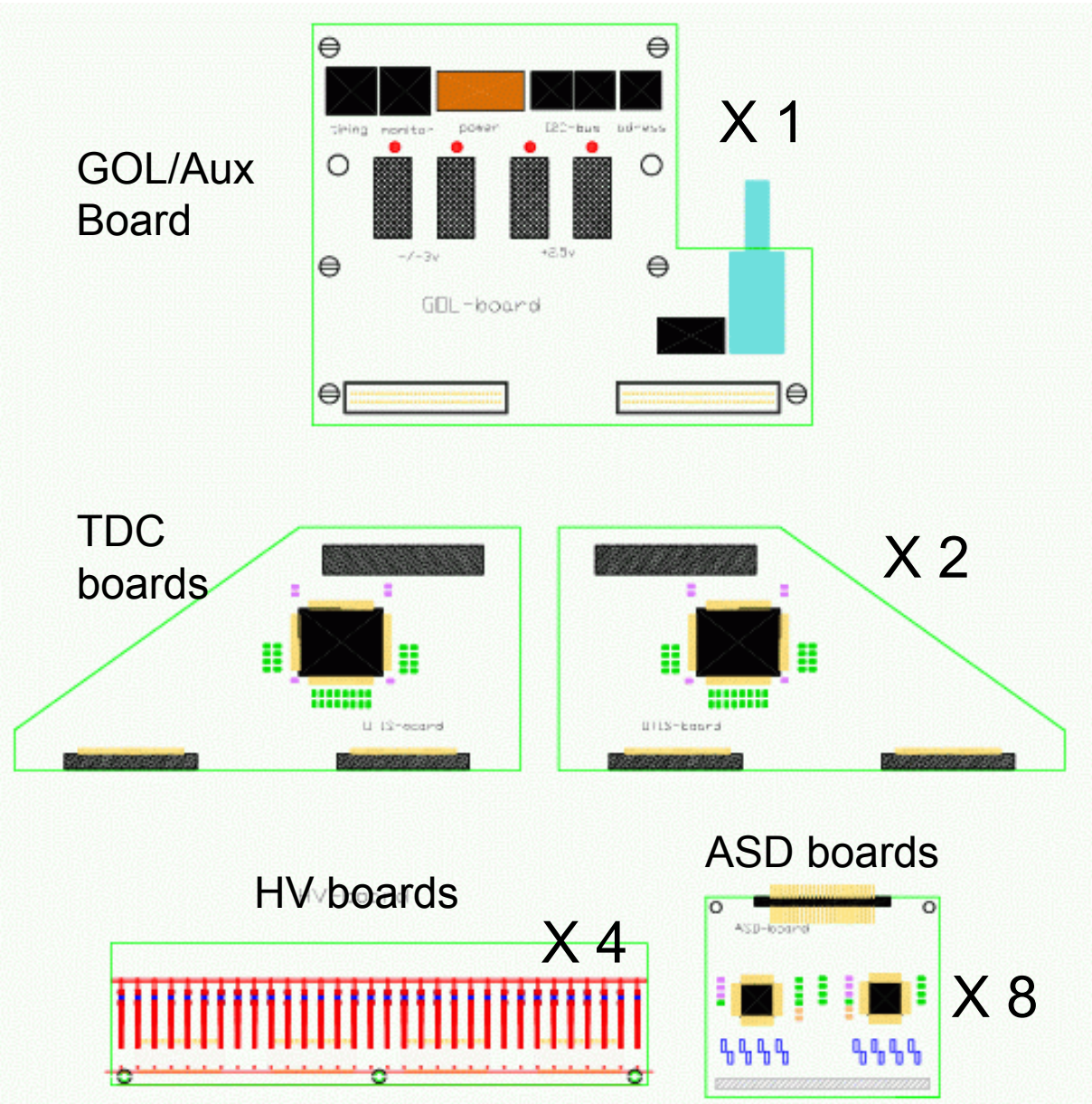
4 OTIS TDC chips

1 optical link: 1.28 Gbit/s

Outer Tracker: **ST1…3**

56000 channels

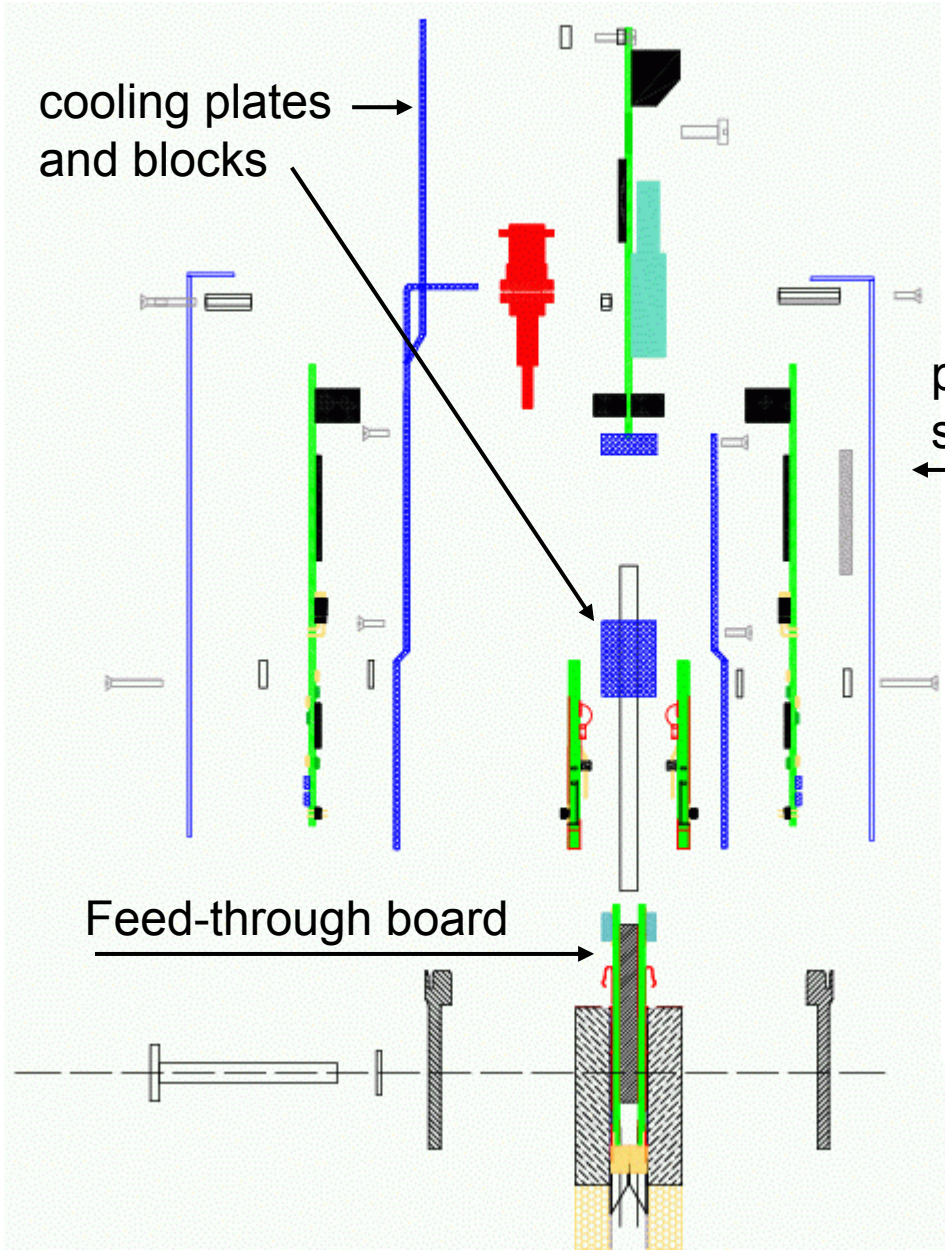
432 optical links

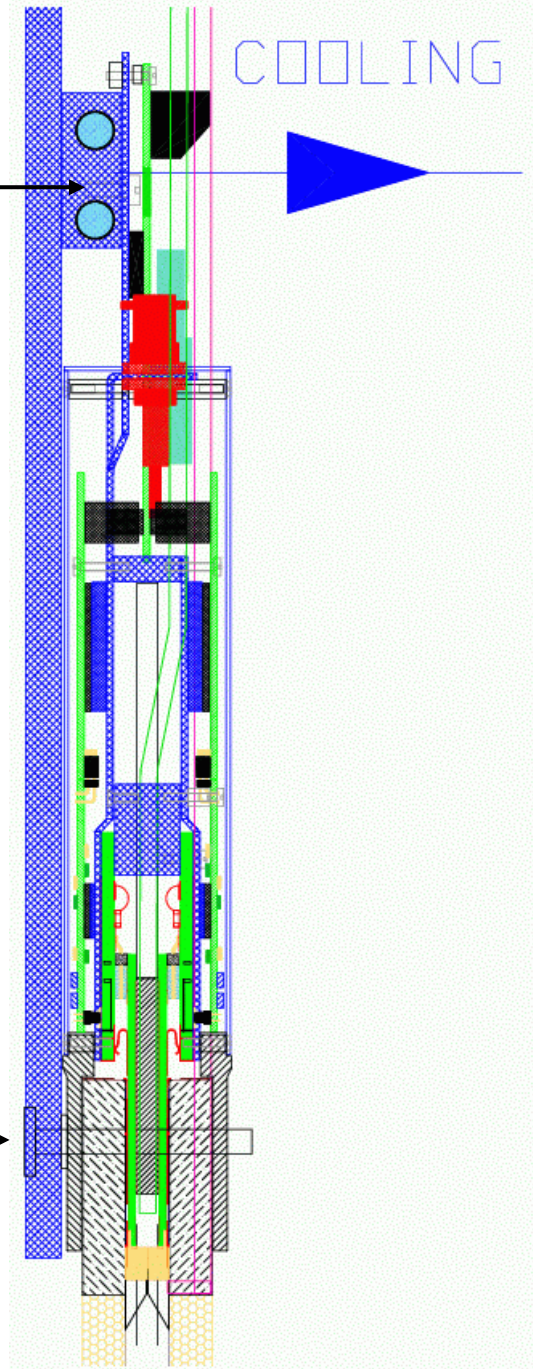


Front-end cards:

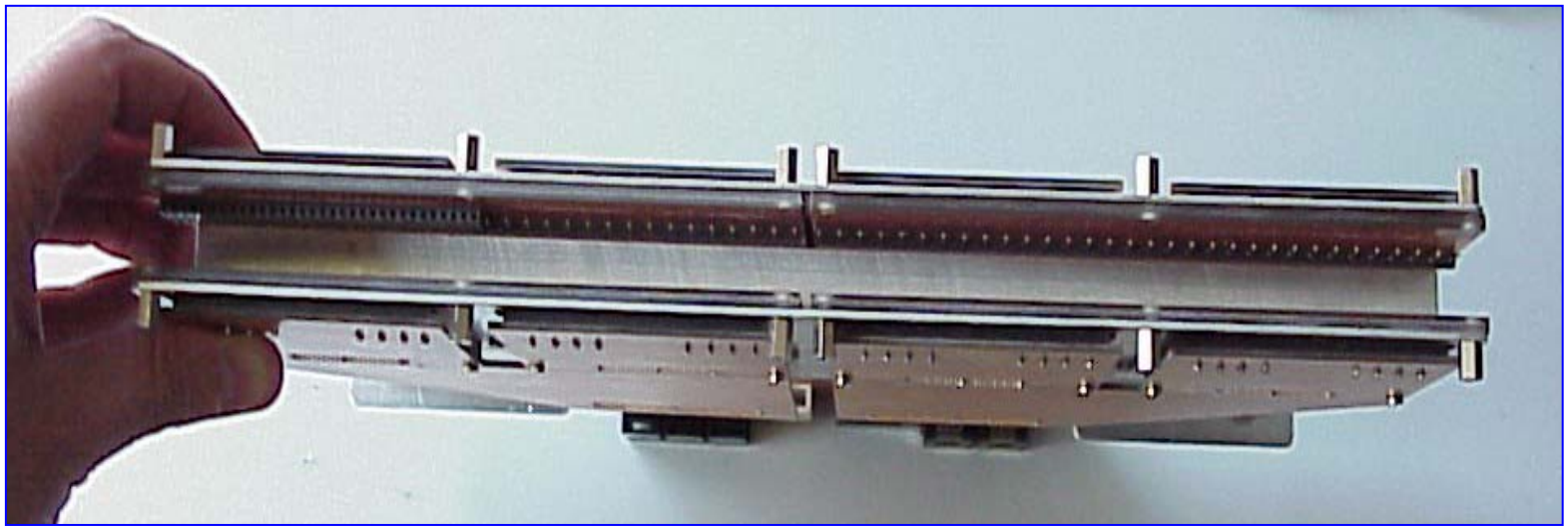
- have to fit inside a closed metal shielding box: **25 x 30 x 4 cm**
- excellent ground connection to straw-tubes and module reference ground
- power dissipation of cards is about **22 W / box** → water cooling
- easy access should be maintained

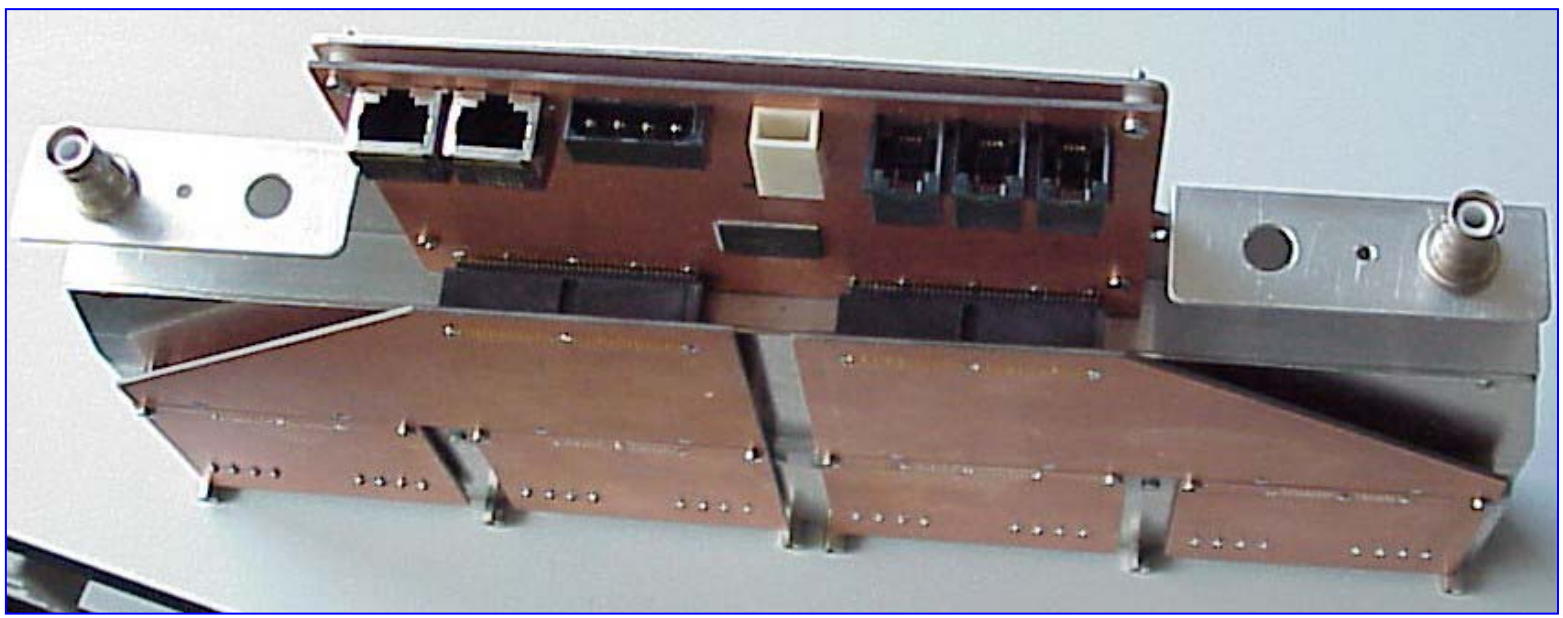
Front-end electronics box: How it fits together



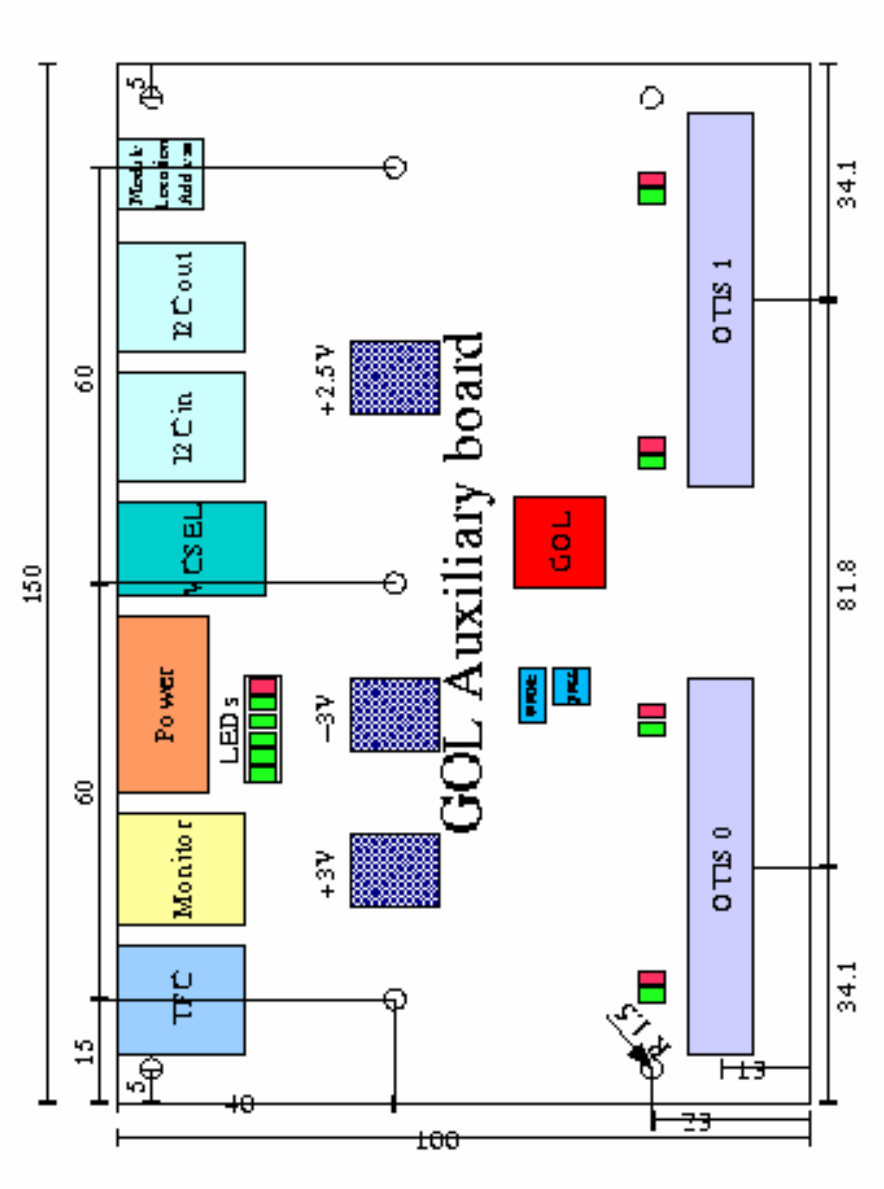


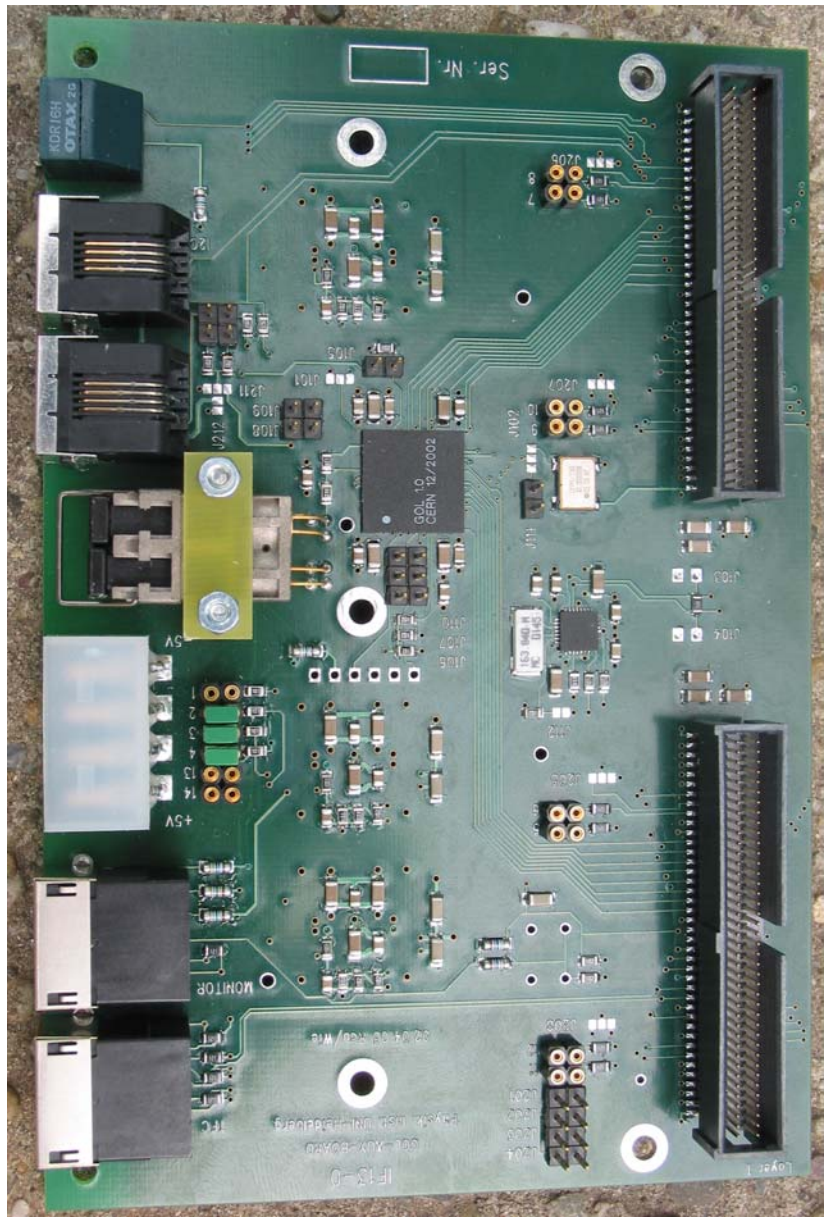
Mock-up of Electronics Box



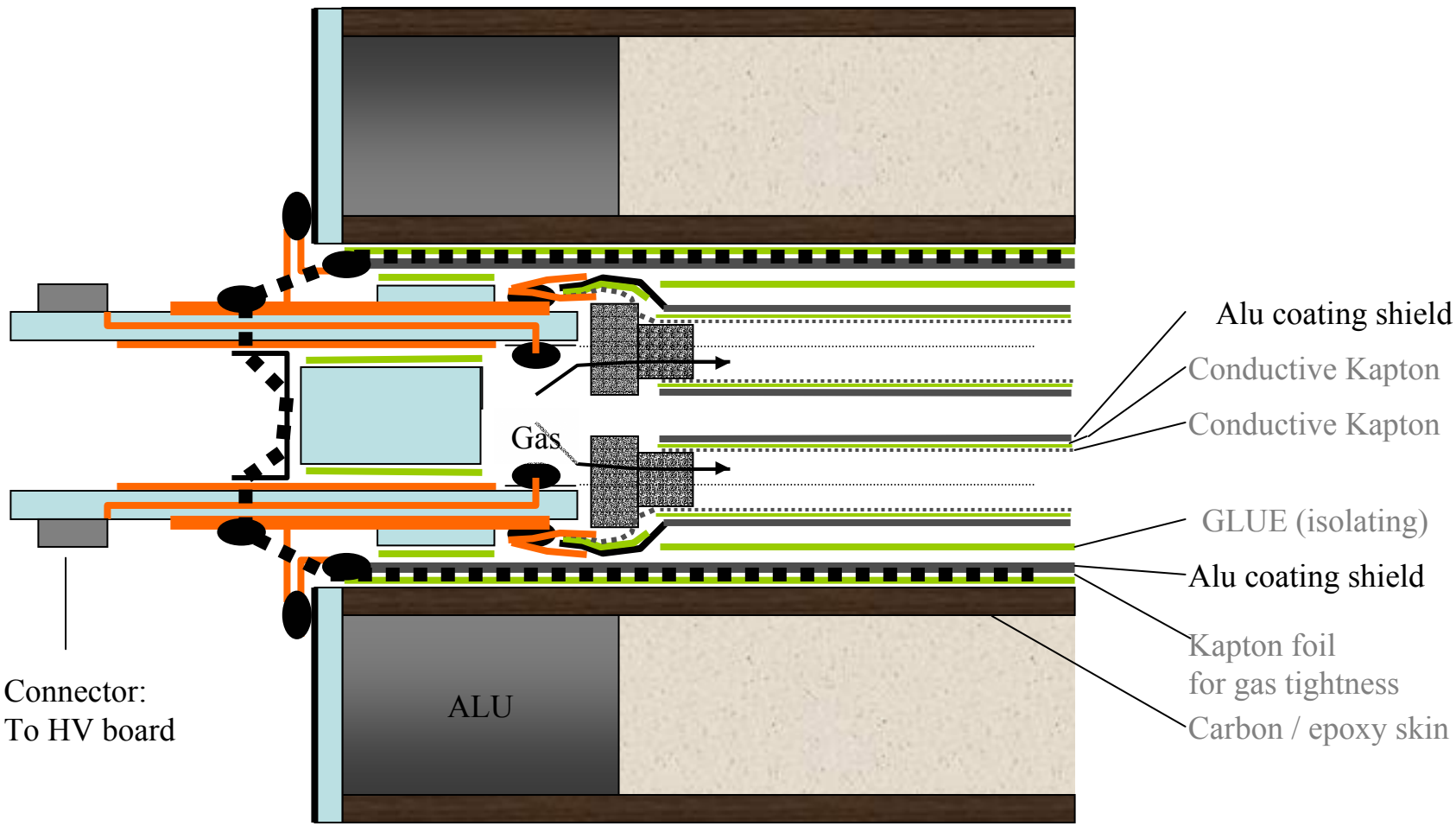


GOL Auxiliary Board

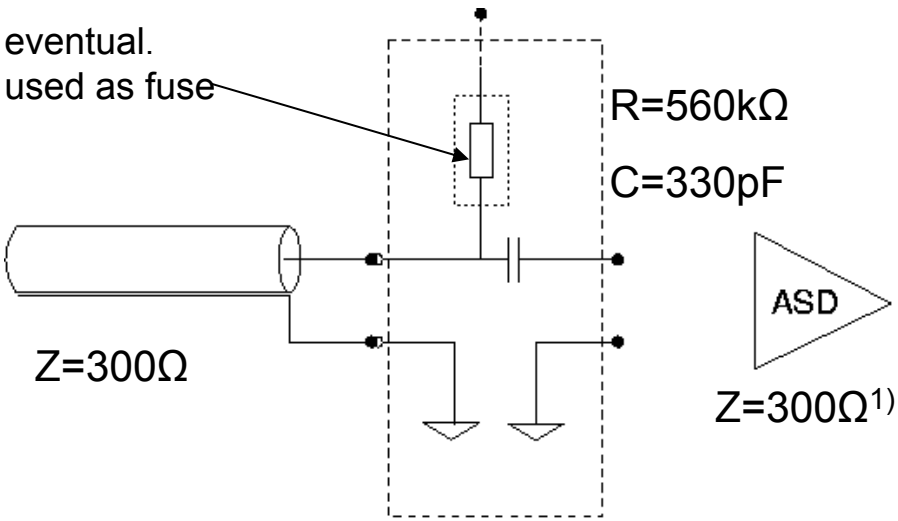


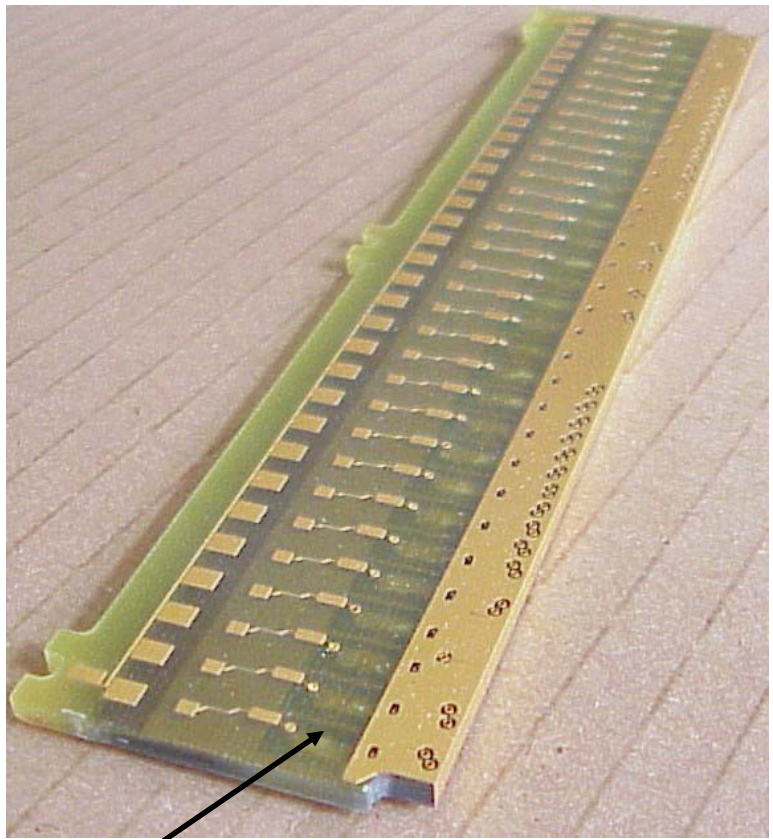


Module Interface: Feed-Through Board



HV Boards



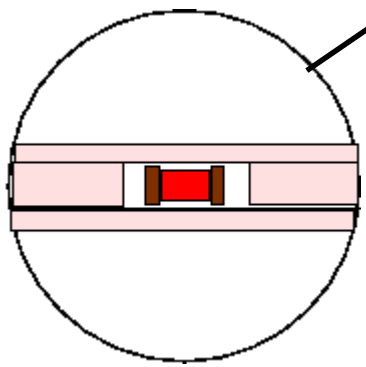


Capacitors:

JOHANSON 302R29W331KV4E

Max. Volt.: 4kV

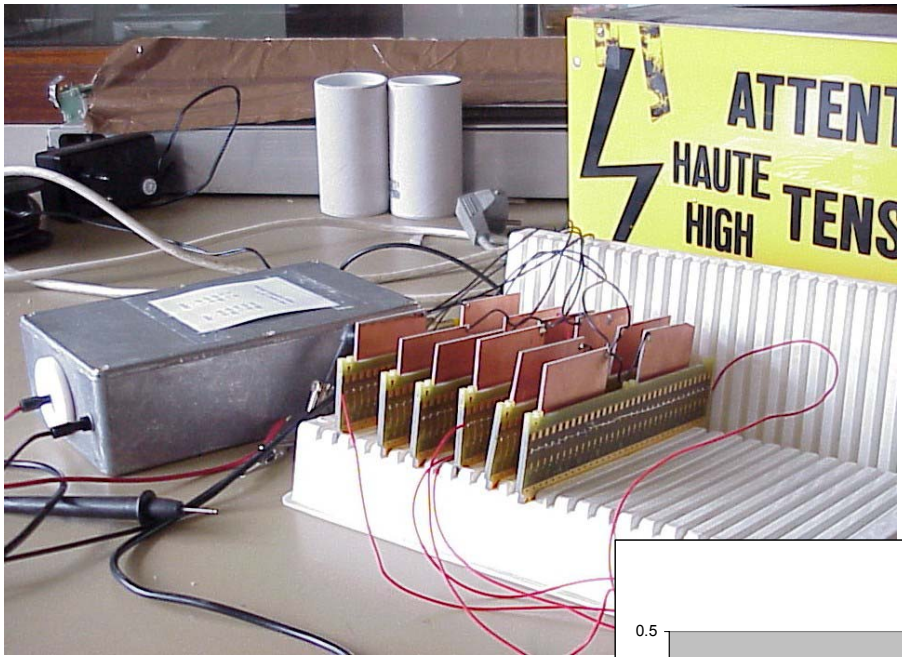
Size: 4.6 x 2 x 1.5 mm^3



32 channels per board

Capacitors embedded in PCB:

1) Z=150Ω at high frequencies + 150Ω in series



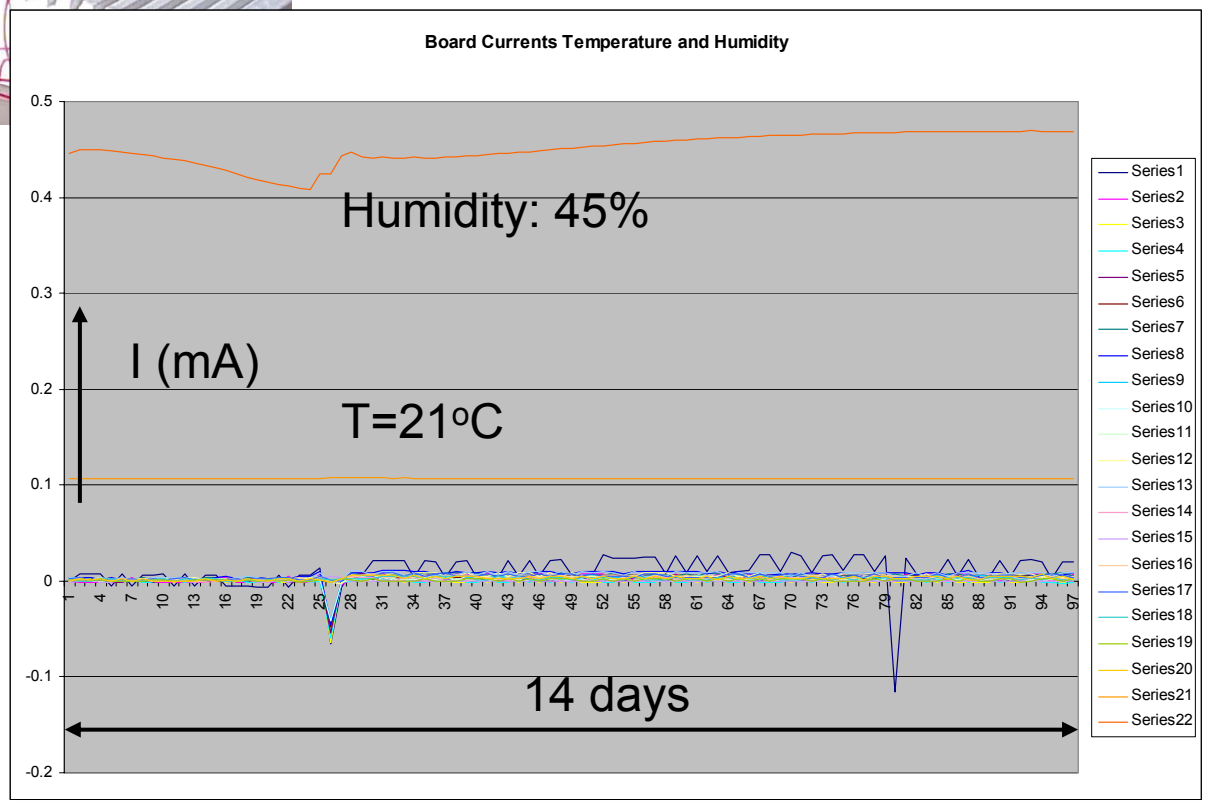
Long term tests:

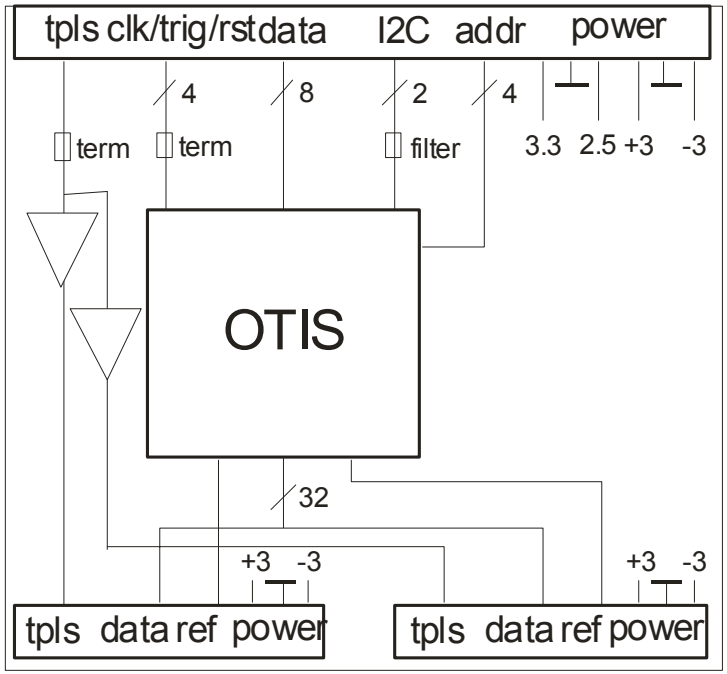
19 boards = 608 channels

1. HV = +2.5 KV, t = 14 days
   → I (32 cha) < 50 nA
   → 1 failing cap

2. Temperature cycling:
   every hour 25-65°C
   HV = +2.5 KV, t = 14 days
   → 1 failing cap

⇨ More studies needed

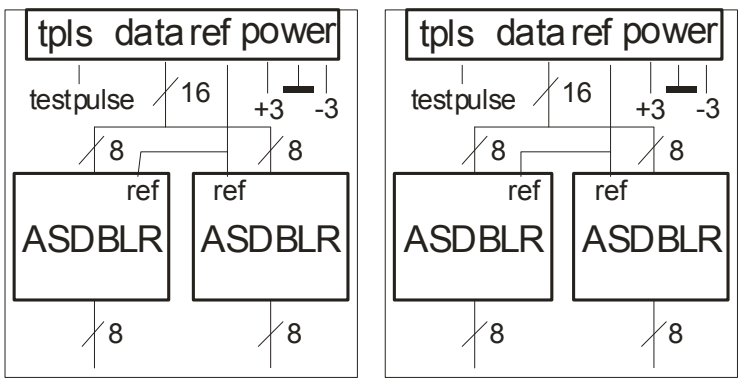




min.
42 pins
connector

TDC board:

- radiation hard OTIS TDC chip
- provides bias voltage for ASD
- power rooting for ASDBLR card
- test pulses for ASDBLR



min.
38 pins
connector

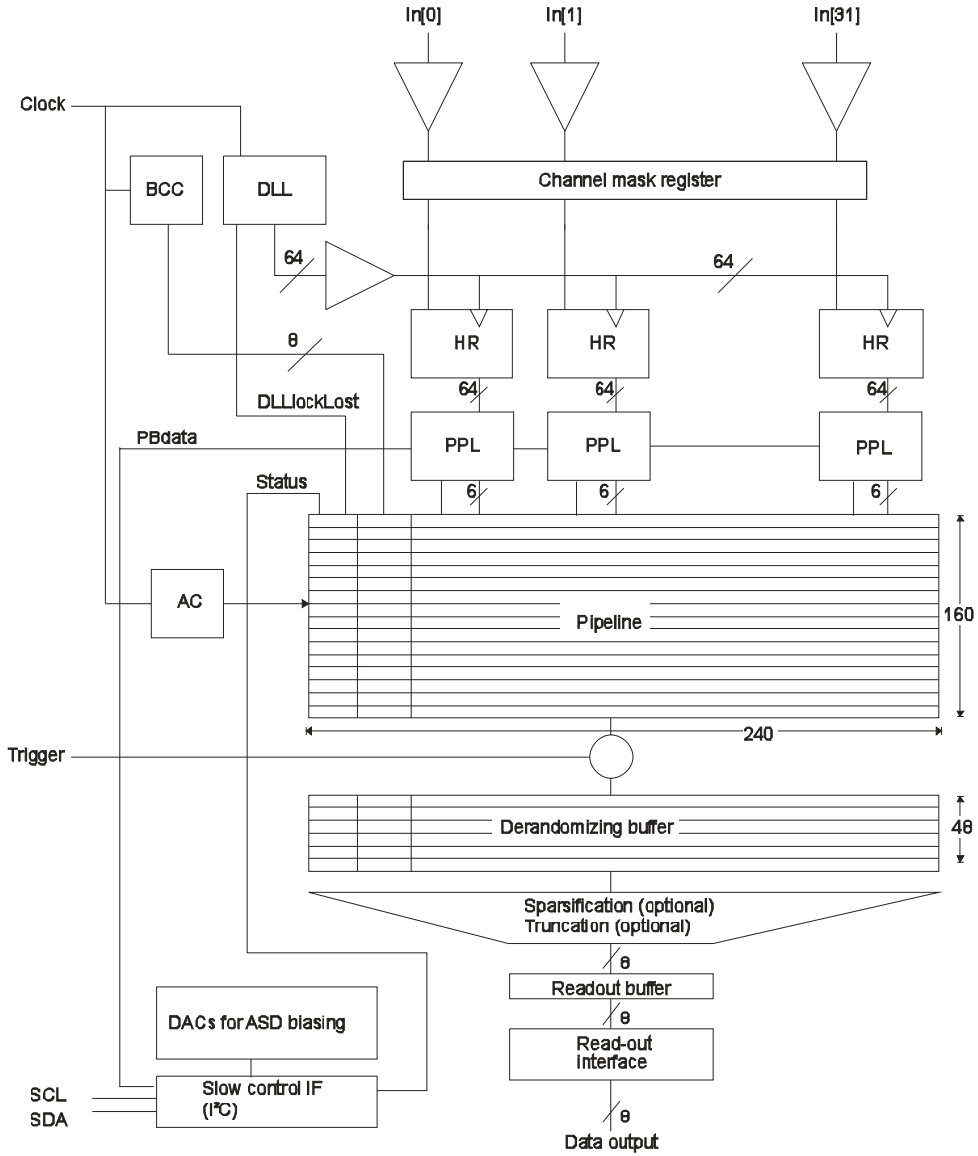
ASD board:

ASDBLR Chip

ATLAS DMILL version 02

⇨ joining ATLAS chip order

⇨ **building first BGA prototype**



OTIS TDC Chip

Components:

- **32 maskable channels**
- **DLL, HitRegister, PrePipeline:**
  6 bit drift time encoding:
  1 bit ↔ 0.39 ns (req. resolut. < 1ns)
  playback data feed-in (testing)
- **Pipeline, Derandomizing Buffer:**
  buffer length: 160 evts ↔ 4.0 μs
- **Control Algorithm:**
  Memory and trigger management,
  2 read-out modes: 1, 2, 3 BX/evt
- **I2C Slow Control Interface:**
  Programming, ASD bias setting
- **DAC:** ASD-Chip bias

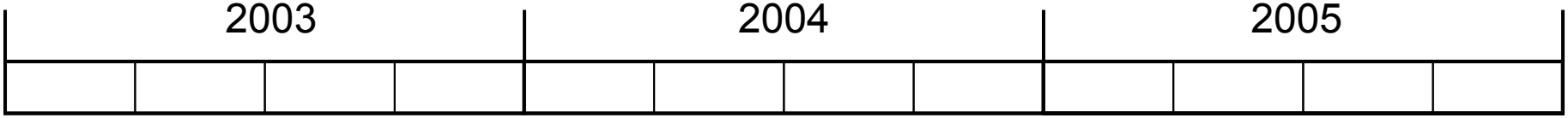
⇨ **0.25 μm CMOS technology**

OTIS1.0 Status ⇨ Chip Review 05/06/03

DLL Lock Range	25-60 MHz @ 300K 10-90°C @ 40 MHz
DLL Lock Time	≤ 1µs
DLL DNL	0,54 ns
PowerUp Reset	as expected
Power Consumption	550mW
DLL: Lock Time	≤ 1µs
Lock Lost	not observed
DAC	as expected
Slow Control	as expected
Fast Control: Memory, Data Output, Debug Features	no errors found
Memory Selftest	timing problems
Drift Time Encoding	timing problems

understood

Outer Tracker Electronics: Time Schedule



07/03 Validation of OTIS baseline

01/04 Delivery of OTIS1.1

03/04 Start pre-series production

06/04 Pre-series finished: start mounting

01/05 Delivery of OTIS1.2

03/05 Start Mass Prod