Compulsory Master seminar

Ruprecht-Karls University, Heidelberg

Monolithic Active Pixel Sensors

Part of the series of lectures:

Particle tracking and identification at high rates

Winter term 2017/18

Christof Sauer

Supervised by: Prof. Dr. André Schöning

December 8, 2017

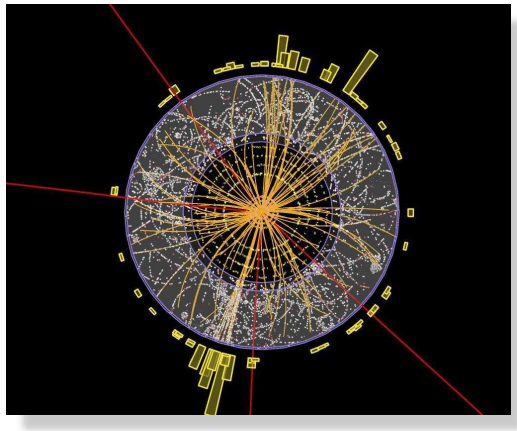
Today's agenda

1. **Motivation** - pixel detectors in experimental particle physics
2. **State of the art** - hybrid pixel detectors (recap)
3. **Monolithic Active Pixel Sensors (MAPS)**
   - brief historical outline & basic concepts
   - standard MAPS & readout
   - High Voltage(HV)-MAPS & readout
4. **Summary**

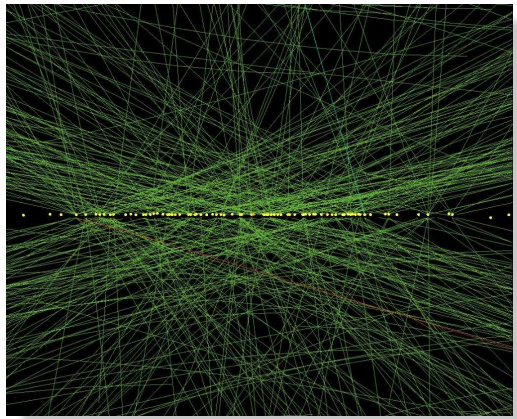
(Silicon) Detectors

Semiconductor detectors are...

- sensitive to ionizing radiation:
  - charged particles
  - (photons)
- pixel- and strip detectors
- most close to the interaction point
- a key for **track**- (a) and **vertex** (b) reconstruction
  - momentum measurement
  - pile-up suppression
  - *b*-tagging



(a)



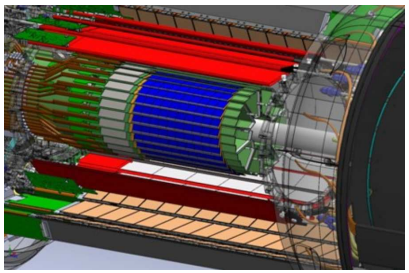
(b)

(a) 3μ event at ATLAS;
(b) 78 rec. vertices at CMS

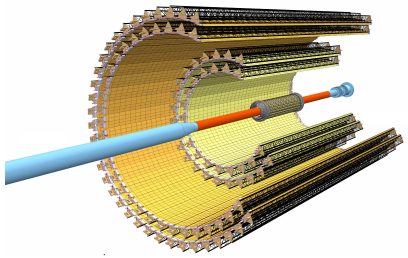
(**source:** ATLAS/CMS CERN)

Collider experiments - a harsh environment for pixel detectors

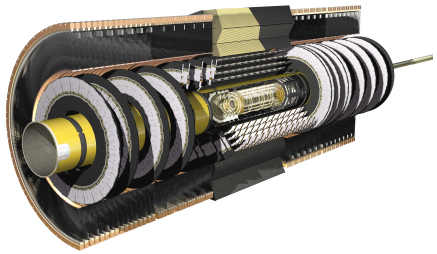
STAR ☆[1]



ALICE



ATLAS EXPERIMENT



	STAR	ALICE (Pb)	ALICE-HL	ATLAS
Bunch crossing (ns)	200000	20000		25
Particle Rate (kHz/mm^2)	100	15		1000
Particle Fluence (n_{eq}/cm^2)	10^{12}	10^{13}		10^{15}
Pixel Technology	MAPS	Hybrid	MAPS[2]	Hybrid[3]
Material Budget (x/X_0)	0.4 %	1 %	0.3 %	1.9 %
Thickness (sensor+ASIC) (μm)	$\sim$ 50	200 + 150	$\sim$ 50	200 + 250
Pixel Size (μm^2)	21×21	50×425	29×27	50×250

[1] Experiment at Relativistic Heavy Ion Collider (RHIC) Brookhaven National Laboratory, United States (studies QGP)
[2] Upgrade of the Inner Tracking System to MAPS in 2019/2020
[3] Refers to innermost pixel detector - Insertable B-Layer (IBL)

Hybrid pixel detectors (recap)

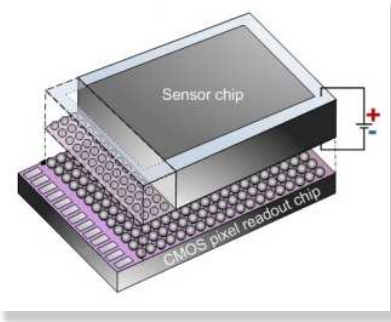
Sensor and readout electronics **separated**

Advantages

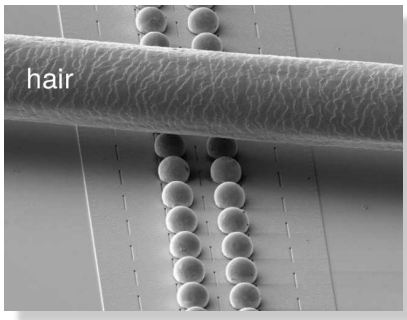
- optimization of sensor and readout electronics
- large signal (d $\sim$ 200 μm)
- usable in High Voltage (HV) applications

Disadvantages

- complex, non-standard technology (error-prone)
- increased multiple scattering (sensor + ASIC)
- large power consumption



(a)



(b)

(a) hybrid pixel detector;
(b) solder bumps

(**source:** http://x-ray.camera)

Hybrid pixel detectors (recap)

Sensor and readout electronics **separated**

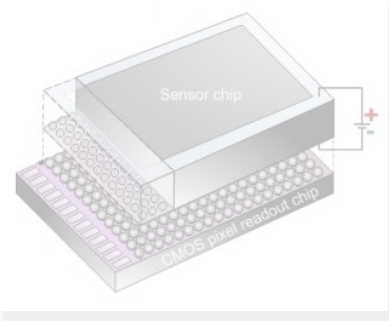
Advantages

- optimization of sensor and readout electronics
- large signal (d $\sim$ 200 μm)
- usable in High Voltage (HV) applications

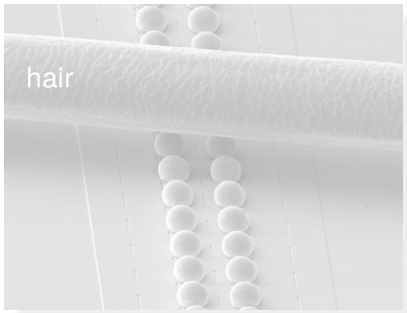
Disadvantages

- complex, non-standard technology (error-prone)
- increased multiple scattering (sensor + ASIC)
- large power consumption

State of the art for all LHC-collider-detectors



(a)



(b)

(a) hybrid pixel detector;
(b) solder bumps

(**source:** http://x-ray.camera)

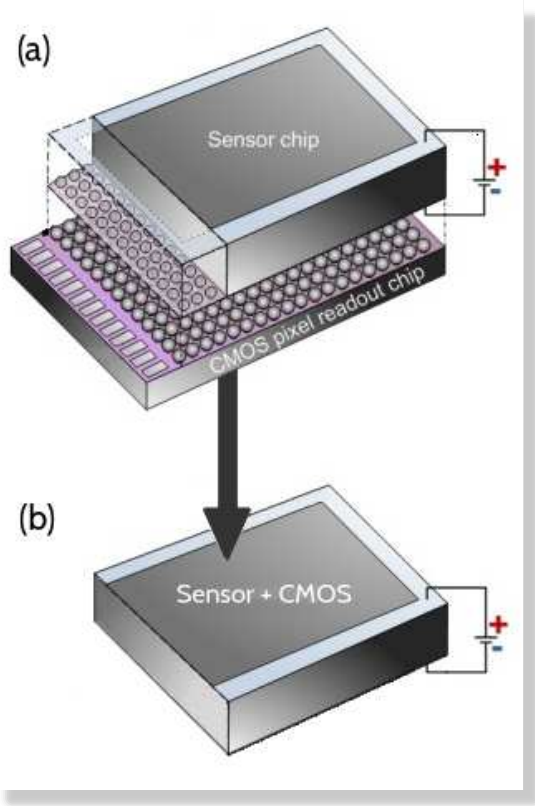
Monolithic active pixel sensor

Monolithic **A**ctive **P**ixel **S**ensor (MAPS)

...ASIC & sensor on same substrate

...includes at least one amplifier

(**source:** http://x-ray.camera)



(a) hybrid pixel detector

↓

(b) MAPS

Basic idea

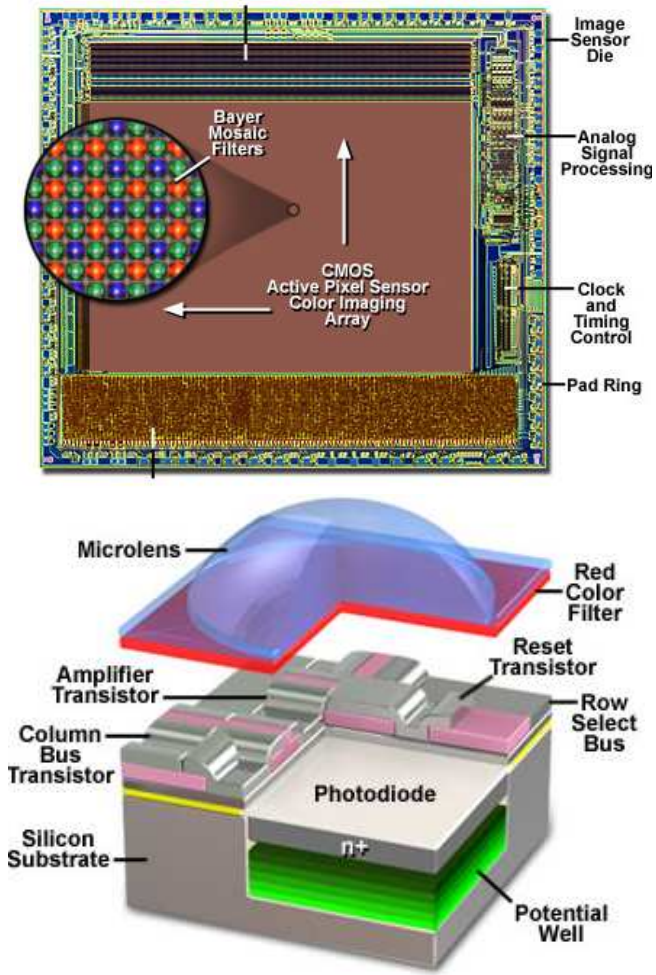
- readout circuit & sensor on same substrate
- standard CMOS for ASIC[1]
- thin sensors (d $\sim$ 50 μm)

[1] Application-specific integrated circuit

Monolithic active pixel sensor

MAPS - "old" technology with a new livery

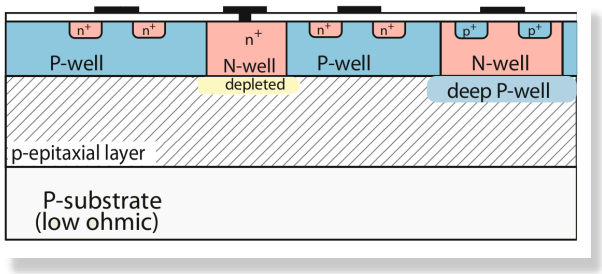
- developed in the 1970s
- renaissance in the early 1990s
- used in visible light applications (today standard)
- **Scientific use for HEP**
  - **first MAPS system used in STAR (2014)**



source: https://micro.magnet.fsu.edu/primer/digitalimaging/

Implementation concepts

electronics **outside** charge collection diode



charge collection by *diffusion*

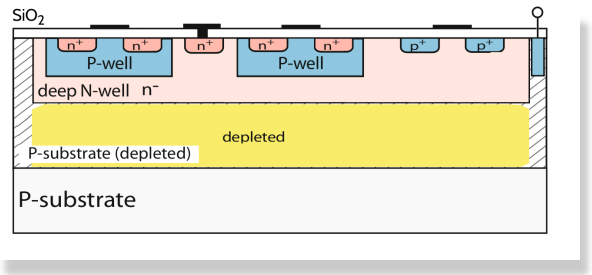
Standard-MAPS

Application: ALICE (2019/20)

STAR

---

electronics **inside** charge collection diode



charge collection by *drift*

HV-MAPS

design proposed by Ivan Perić[1]

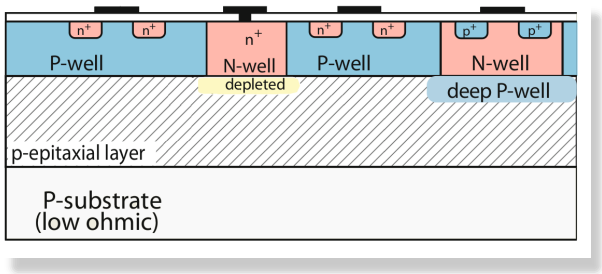
Application: $\mu 3e$(**Mu3e**)-experiment

ATLAS HL-LHC(?)

[1] A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology (Institut für Technische Informatik, Mannheim-Heidelberg, Germany 2007)

Implementation concepts

electronics **outside** charge collection diode



charge collection by *diffusion*

Standard-MAPS

Application: ALICE (2019/20)

STAR

---

electronics **inside** charge collection diode

charge collection by *drift*

HV-MAPS

design proposed by Ivan Perić[1]

Application: $\mu 3e$(**Mu3e**)-experiment

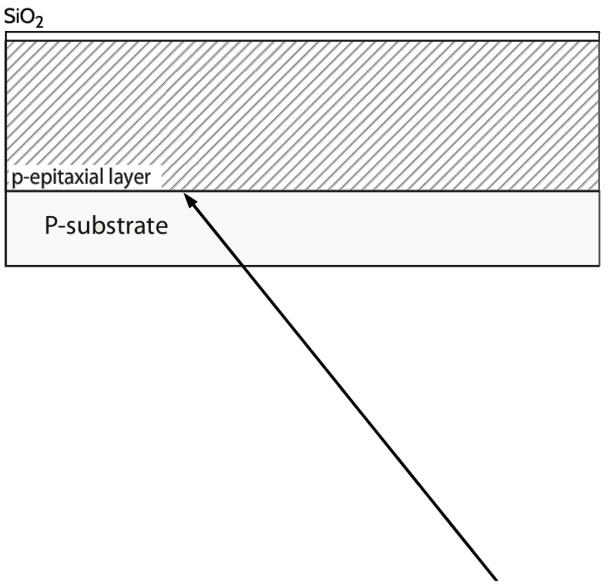
ATLAS HL-LHC(?)

[1] A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology (Institut für Technische Informatik, Mannheim-Heidelberg, Germany 2007)

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



reflective potential barrier $\Delta V \propto \ln \frac{N_{p++}}{N_{p-}}$

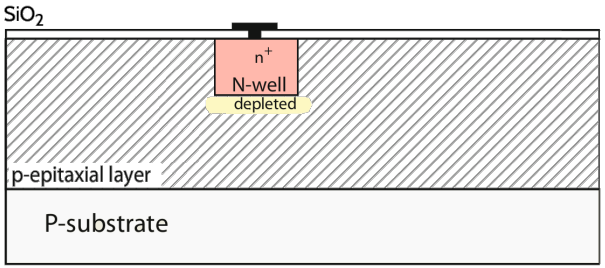
- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



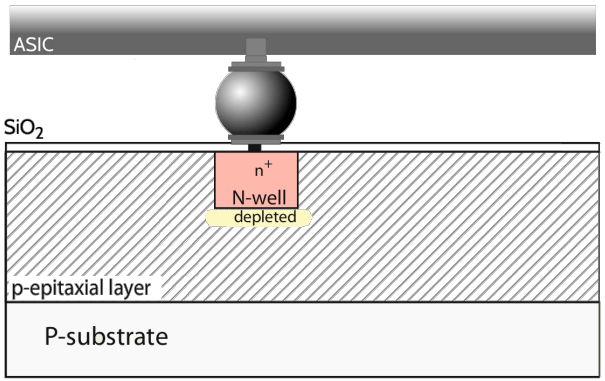
- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

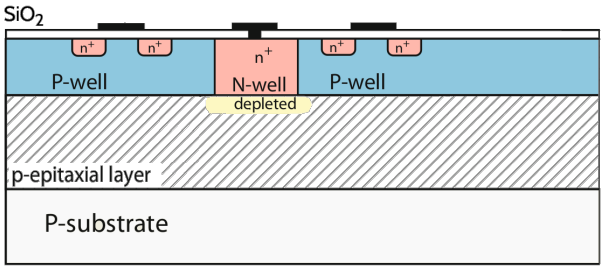
$\rightarrow$ **hybrid solution**

passive sensor & ASIC **separated**

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

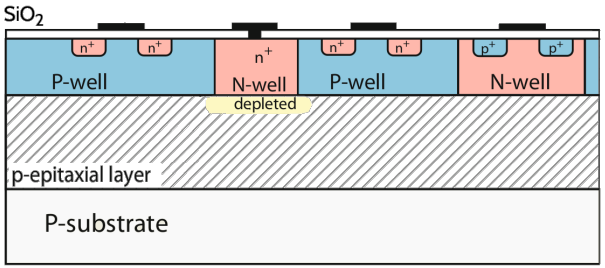
→ **monolithic solution**

sensor & ASIC on **same** substrate

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



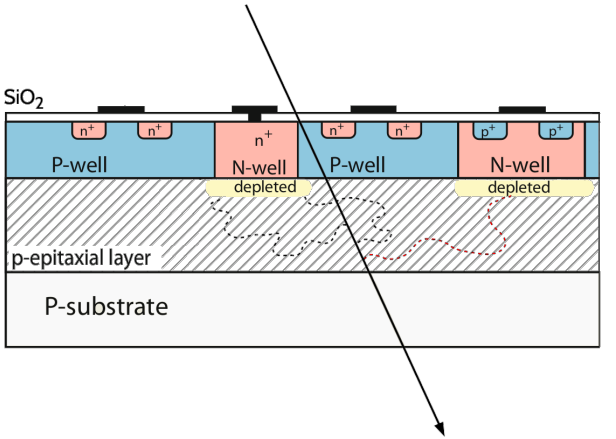
- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



→ reduced detection efficiency!

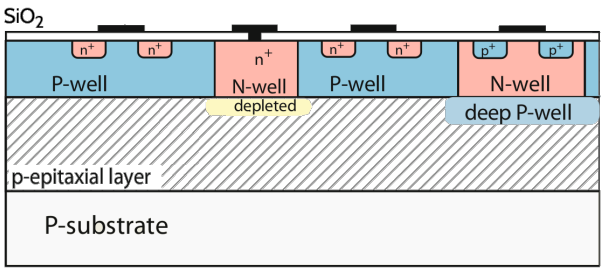
- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

} full CMOS

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



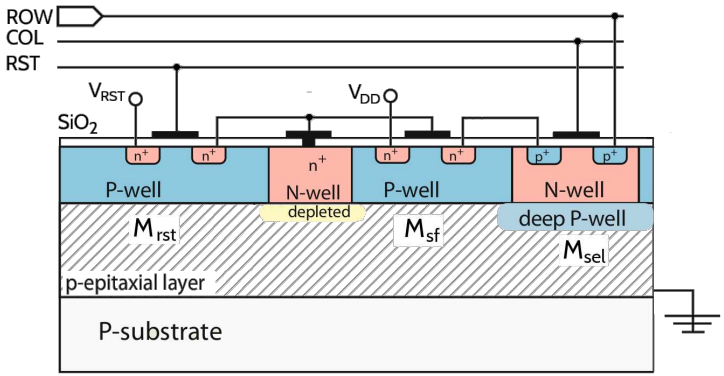
- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

Standard-MAPS

Standard-MAPS for a simple 3-transistor architecture

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



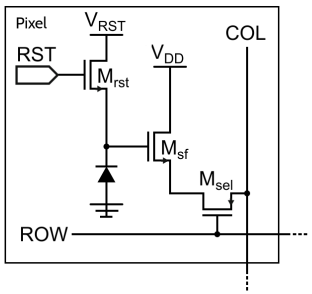
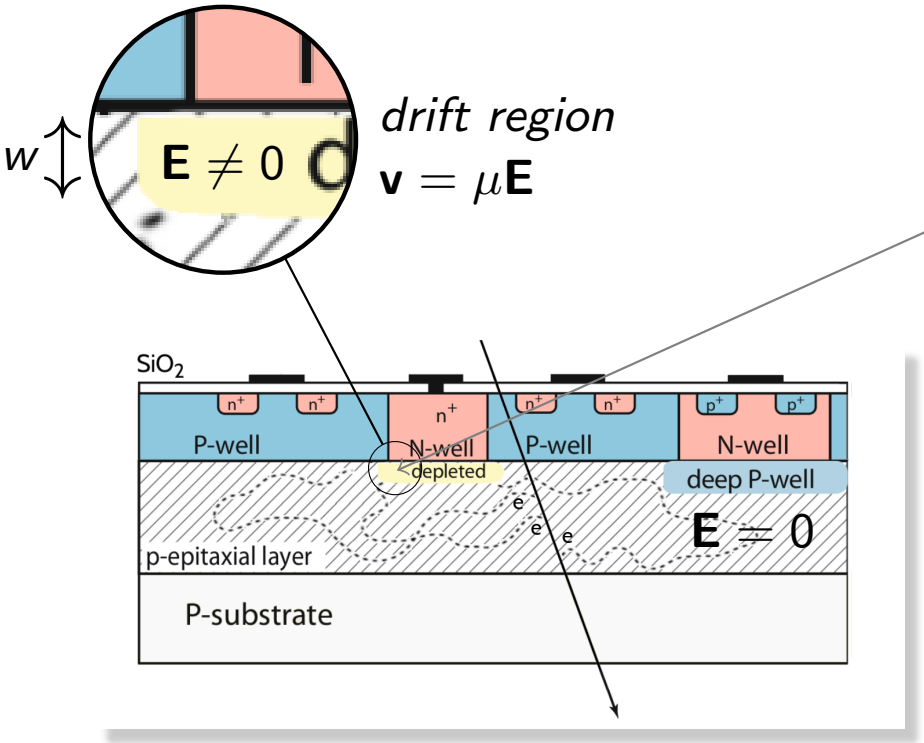


Fig. one pixel cell

- high doped P-substrate
  (support, potential barrier, seed crystal)
- low doped, high resistivity P-epitaxial layer
- gate isolation SiO_2 layer
- N-well (charge collecting diode)
- integrate ASIC (only NMOS transistors)
- implant deep P-well for PMOS transistors
  - NMOS-transistor(s)
  - PMOS-transistor

  } full CMOS

Depletion width & potential barrier



(intrinsic) depletion width

- build-in voltage pn-junction (diode)

$$V_{\text{bi}} = \frac{K_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right) \sim 100\,\text{mV}$$

- depletion width

$$w \propto \sqrt{\frac{N_D + N_A}{N_D N_A}(V_{\text{bi}} + V_{\text{bias}})}$$

$$\approx \sqrt{\frac{1}{N_A}(V_{\text{bi}} + V_{\text{bias}})}$$

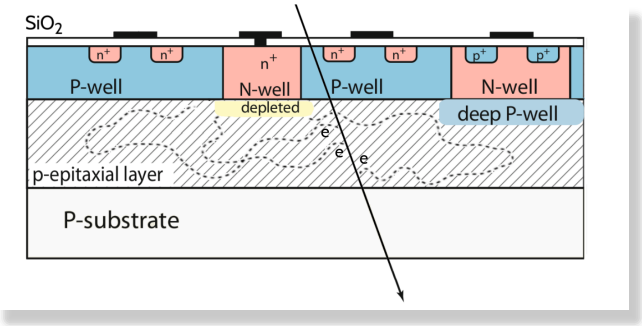
$$\frac{w}{d} \approx \frac{60\,\text{nm}}{50\,\mu\text{m}} = 0.1\,\% \; (V_{\text{bias}} = 0\,\text{V})$$

$$\frac{w}{d} \approx \frac{0.2\,\mu\text{m}}{50\,\mu\text{m}} = 0.4\,\% \; (V_{\text{bias}} = 1\,\text{V})$$

$\rightarrow$ **charge collection NOT dominated by drift!**

Charge collection

Charge collection by **diffusion** (**drift** near electrode)



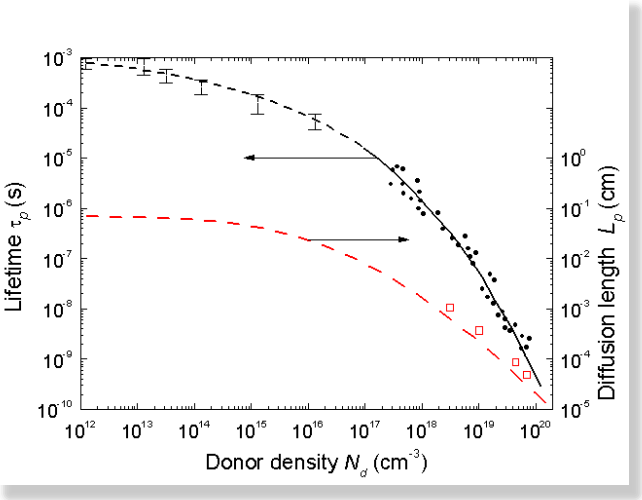


Fig. lifetime τ_e and diffusion length L_e of electrons in p-type Si vs. donor density

Source http://www.ioffe.ru/SVA/NSM/Semicond/Si/electric.html

low recombination probability required

$L_{\text{free}} \gg d$ (**free** diffusion length L_{free})
$L_{\text{free}} \sim 1000\,\mu\text{m}$ with $N_D < 10^{14}\,\text{cm}^{-3}$

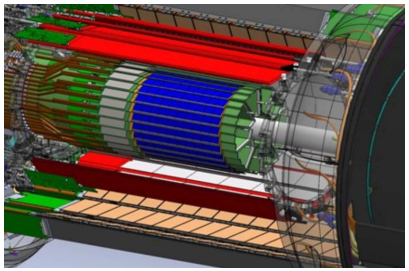
$\rightarrow$ applicable ($d \sim 50\,\mu\text{m}$)

diffusion

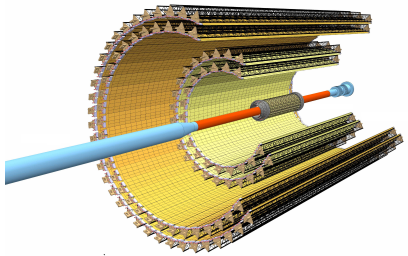
- fick's 2nd law $\frac{\partial c(\mathbf{x},t)}{\partial t} = \mathrm{D}\Delta c(\mathbf{x},t)$
  diffusion constant $\mathrm{D}_{e,h} = \frac{k_B T}{q}\mu_{e,h}$ (Einstein relation)
- diffusion length $\sigma = \sqrt{2\mathrm{D}t} \propto \sqrt{\mu t T}$
  $\mu_{e,h} = 1400,\ 470\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$
- in the order of $t \sim 100\,\text{ns}$ (electrons)

Collider experiments - a harsh environment for pixel detectors

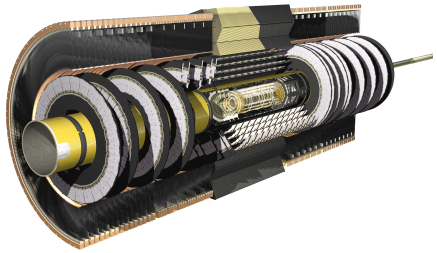
STAR ☆[1]



ALICE



ATLAS EXPERIMENT



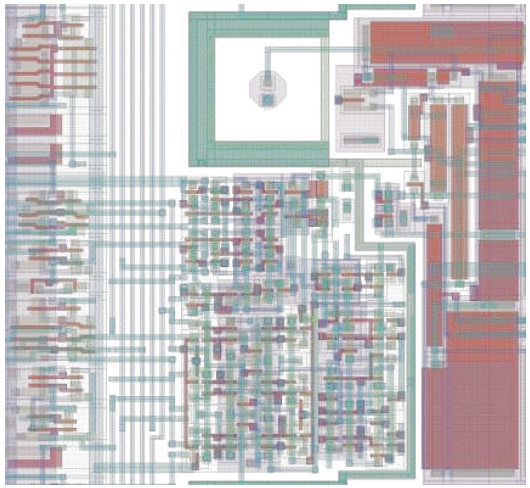
	STAR	ALICE (Pb)	ALICE-HL	ATLAS
Bunch crossing (ns)	200000	20000		25
Particle Rate (kHz/mm^2)	100	15		1000
Particle Fluence (n_{eq}/cm^2)	10^{12}	10^{13}		10^{15}
Pixel Technology	MAPS	Hybrid	MAPS[2]	Hybrid[3]
Material Budget (x/X_0)	0.4 %	1 %	0.3 %	1.9 %
Thickness (sensor+ASIC) (μm)	~ 50	$200 + 150$	~ 50	$200 + 250$
Pixel Size (μm^2)	21×21	50×425	29×27	50×250

[1] Experiment at Relativistic Heavy Ion Collider (RHIC) Brookhaven National Laboratory, United States (studies QGP)
[2] Upgrade of the Inner Tracking System to MAPS in 2019/2020
[3] Refers to innermost pixel detector - Insertable B-Layer (IBL)

Implementation example

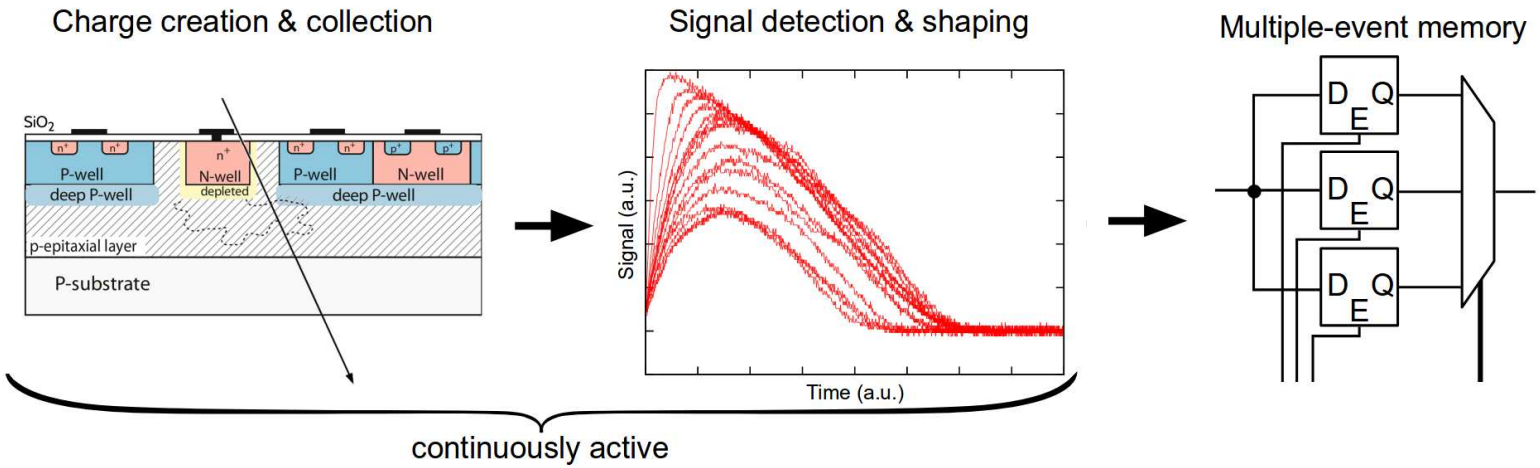
Layout: **ALPIDE pixel** (ALICE)

Source: Overview of the ALPIDE Pixel Sensor Chip with focus on Readout Features



in pixel functionalities

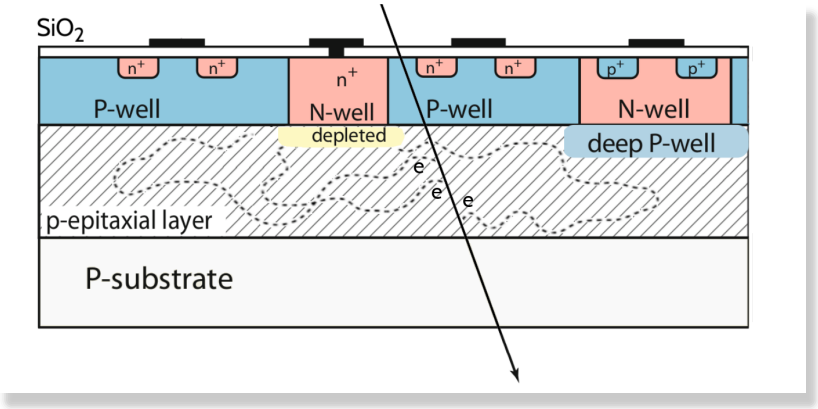
- amplifier
- comperator
- hit storage register



Standard-MAPS summary

Design concept: electronics **outside** charge collection diode

Application: **ALICE** (2019/20), **STAR**



advantages

- low material budget
- only CMOS
- low noise $\delta V = \frac{\delta Q}{C_{\text{Diode}}}$
- low power consumption $P_{\text{Diode}} \propto C_{\text{Diode}}^{m}$, $m \geq 1$

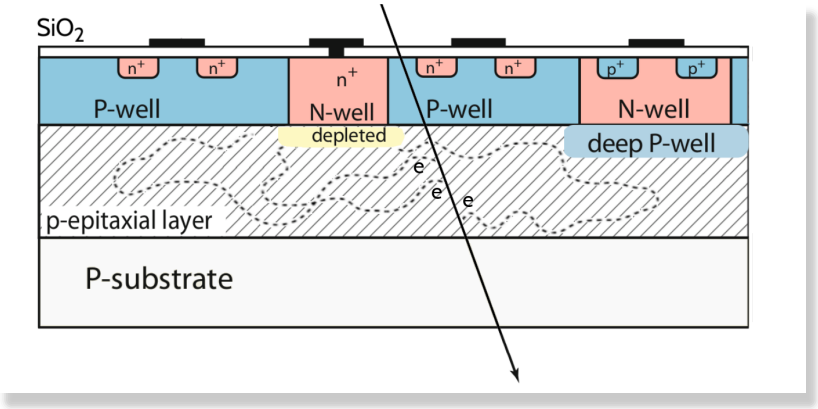
disadvantages

- small Signal ($S_{\text{MIP}} \sim 80\,\text{eh-pairs}/\mu\text{m}$)
- limited radiation tolerant
- slow (charge collection by diffusion)

Standard-MAPS summary

Design concept: electronics **outside** charge collection diode

Application: **ALICE** (2019/20), **STAR**



advantages

- low material budget
- only CMOS
- low noise $\delta V = \frac{\delta Q}{C_{\text{Diode}}}$
- low power consumption $P_{\text{Diode}} \propto C_{\text{Diode}}^{m}$, $m \geq 1$

disadvantages

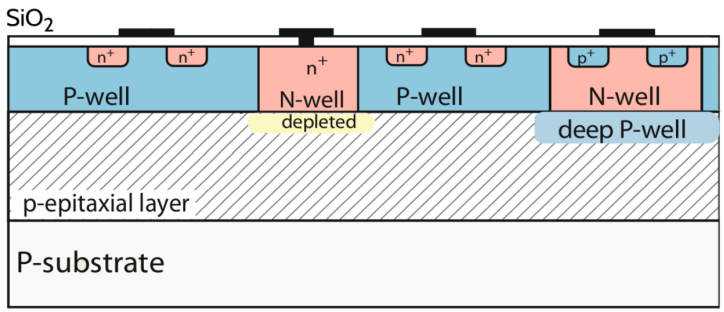
- small Signal ($S_{\text{MIP}} \sim 80\,\text{eh-pairs}/\mu\text{m}$)
- limited radiation tolerant
- slow (charge collection by diffusion)

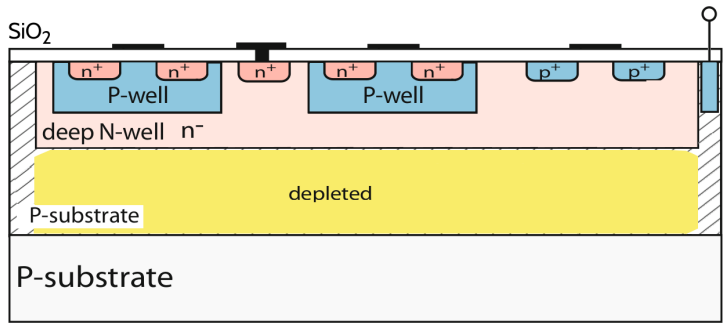
not suitable for ATLAS nor CMS!
(time resolution $\sim 25\,\text{ns}$)

$\rightarrow$

Deep N-Well HV-MAPS

Standard-MAPS





HV-MAPS

- integrate transistors into diode ("smart diode", full fill factor)
- deep N-well shields low voltage devices
- HV required (based on HV-CMOS)
- fully or partially depleted sensor
- full CMOS (no P-shield)

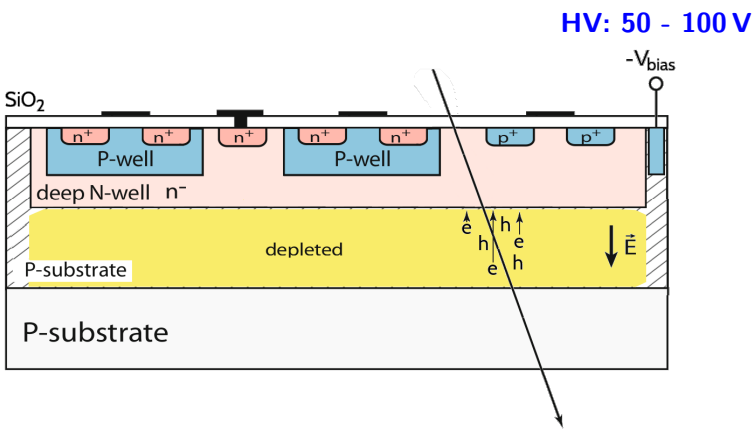
HV-MAPS

HV-MAPS for a simple 3-transistor architecture

design according to Ivan Perić[1]

based on AMS[2] *180 nm HV-CMOS process*

integrated functionality: reset (M_{rst}),
readout (M_{sel}),
source-Follower (M_{sf})



- **fast** charge collection by drift ($\mathbf{v} = \mu\mathbf{E}$, $E \approx \frac{V_{bias}}{d}$)
- time resolution ~ 1 ns

  suitable for ATLAS, CMS & Mu3e (~ 25 ns)
- depletion width $d \approx \sqrt{\rho V_{bias}}$
- improved radiation hardness

[1] former privatdozent at university of Heidelberg (ZITI), now professor at Karlsruher Institut für Technologie (KIT)

[2] Austria Mikro Systeme AG

Example: **MuPix**-chip (Mu3e)

HV-MAPS for Mu3e

Mu3e in a Nutshell

- planed experiment at PSI, Switzerland
- searches for LFV process $\mu^- \rightarrow e^- e^+ e^-$ with BR $\sim 10^{-16}$ ($BR_{SM} \sim 10^{-54}$)
- high rates ($2 \cdot 10^7 - 2 \cdot 10^9$ muons/s, Phase IA,B-II)
- pixel tracker based on HV-MAPS

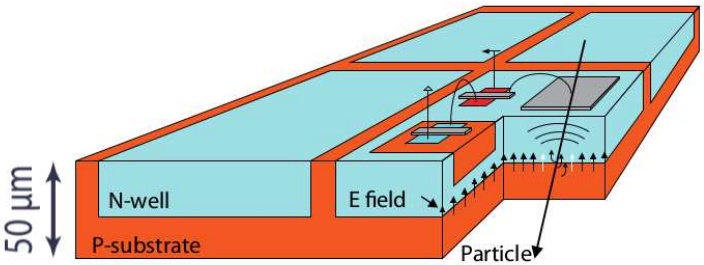


Fig. deep N-well MuPix7 pixel

pixel Size	material Budget	time Resolution
80 × 80 μm	≤ 1 ‰/Layer	≤ 20 ns

Tab. pixel Requirements

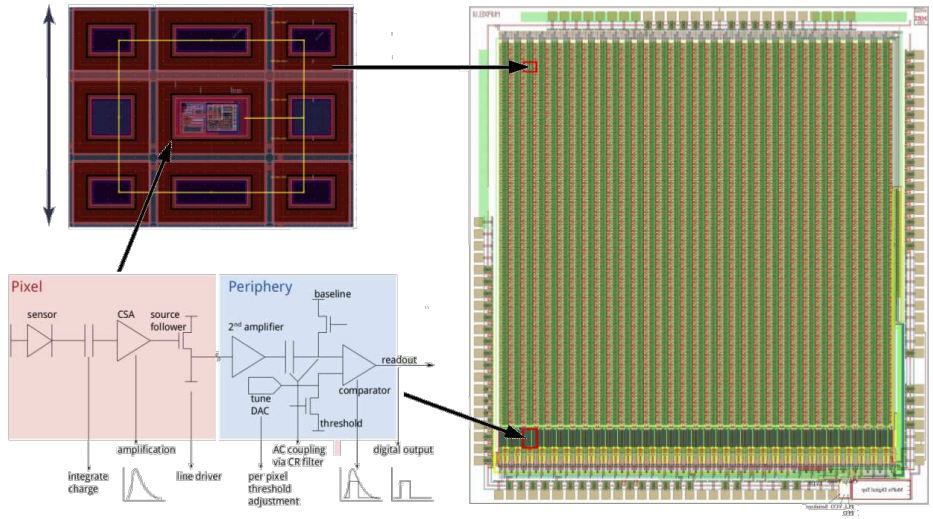


Fig. MuPix7 chip & pixel

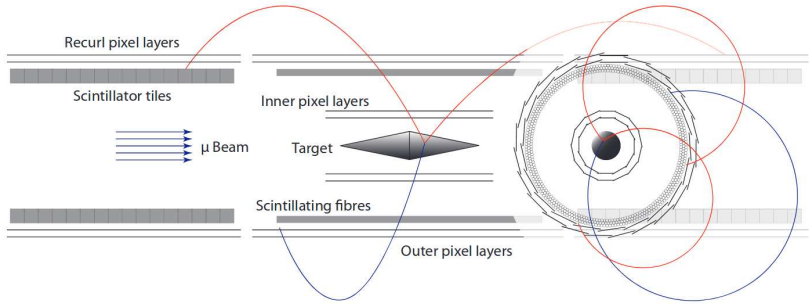
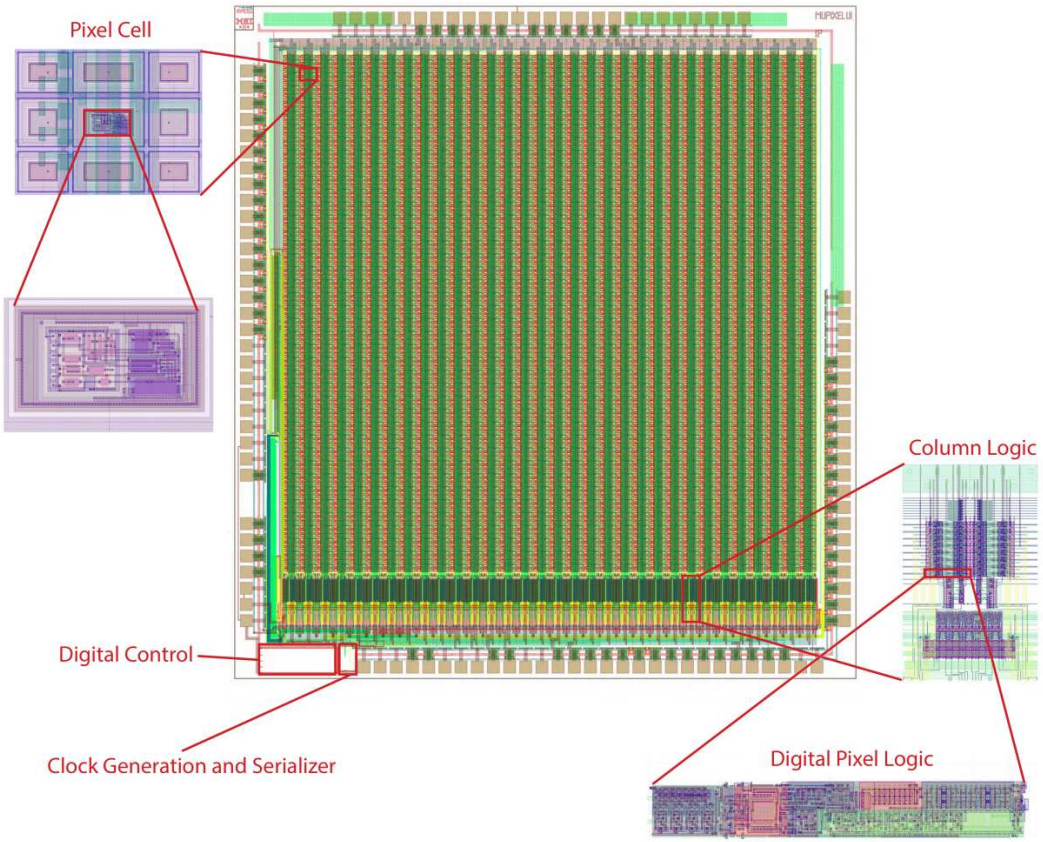


Fig. detector concept

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



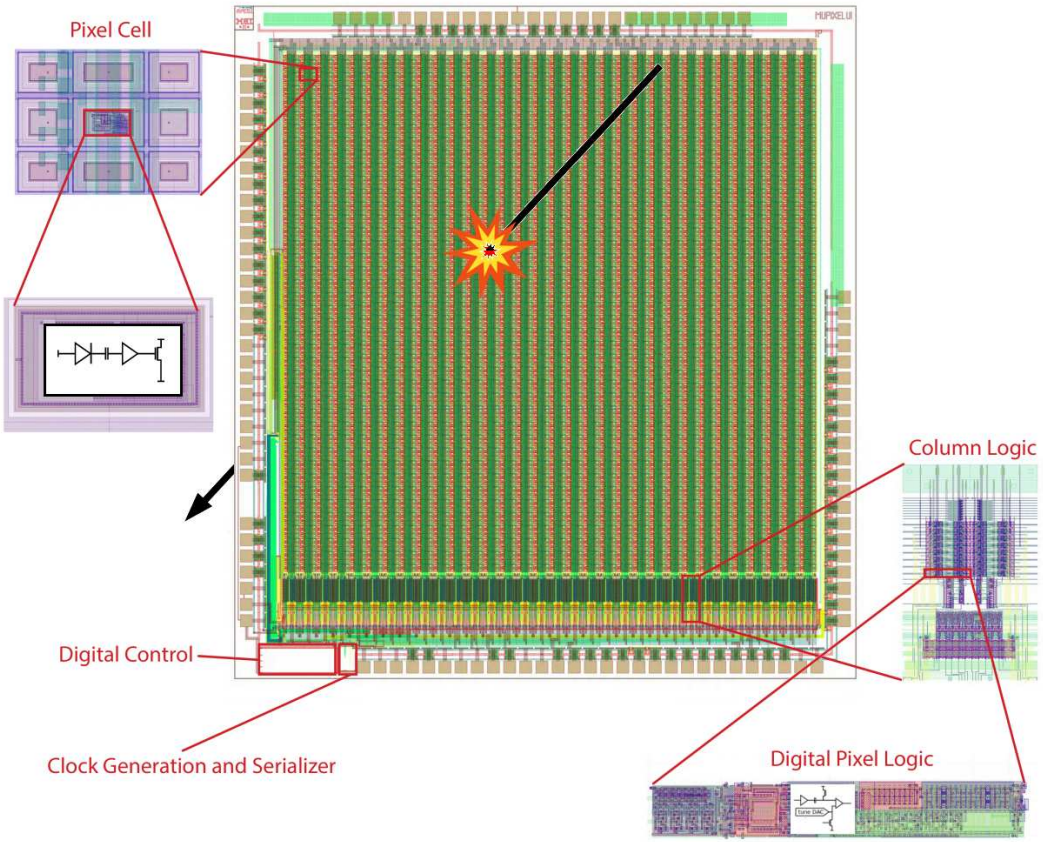
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



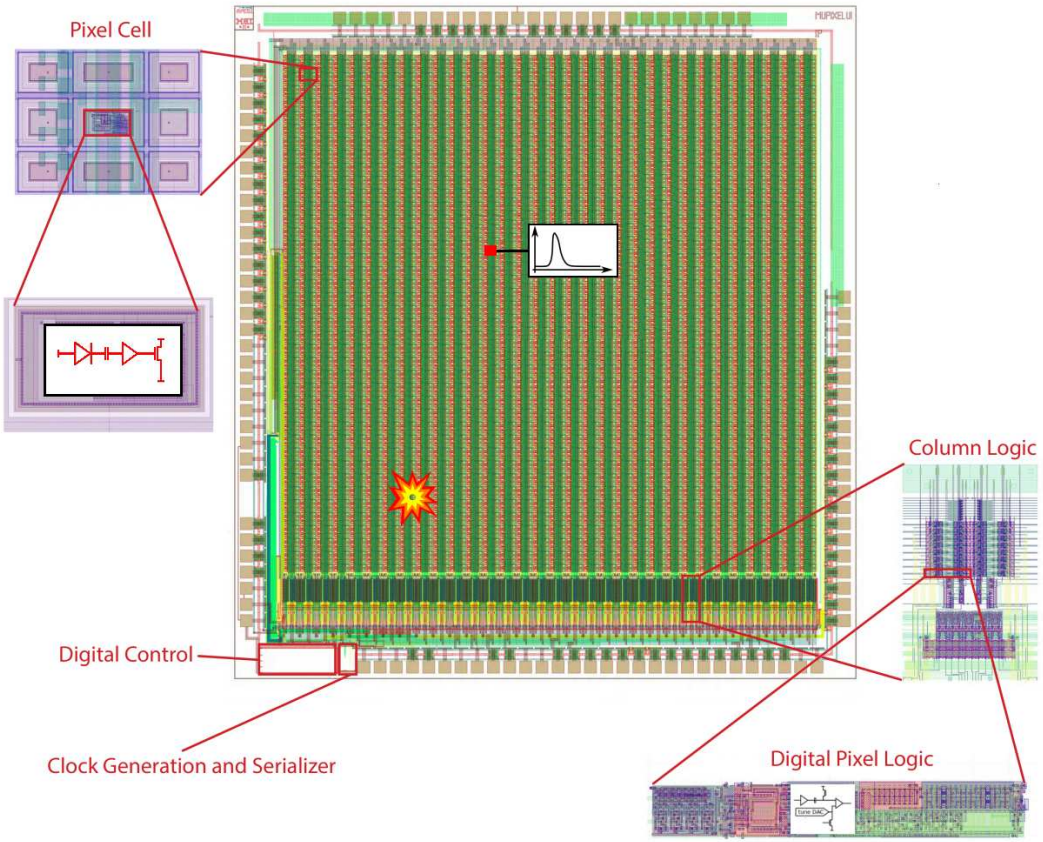
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



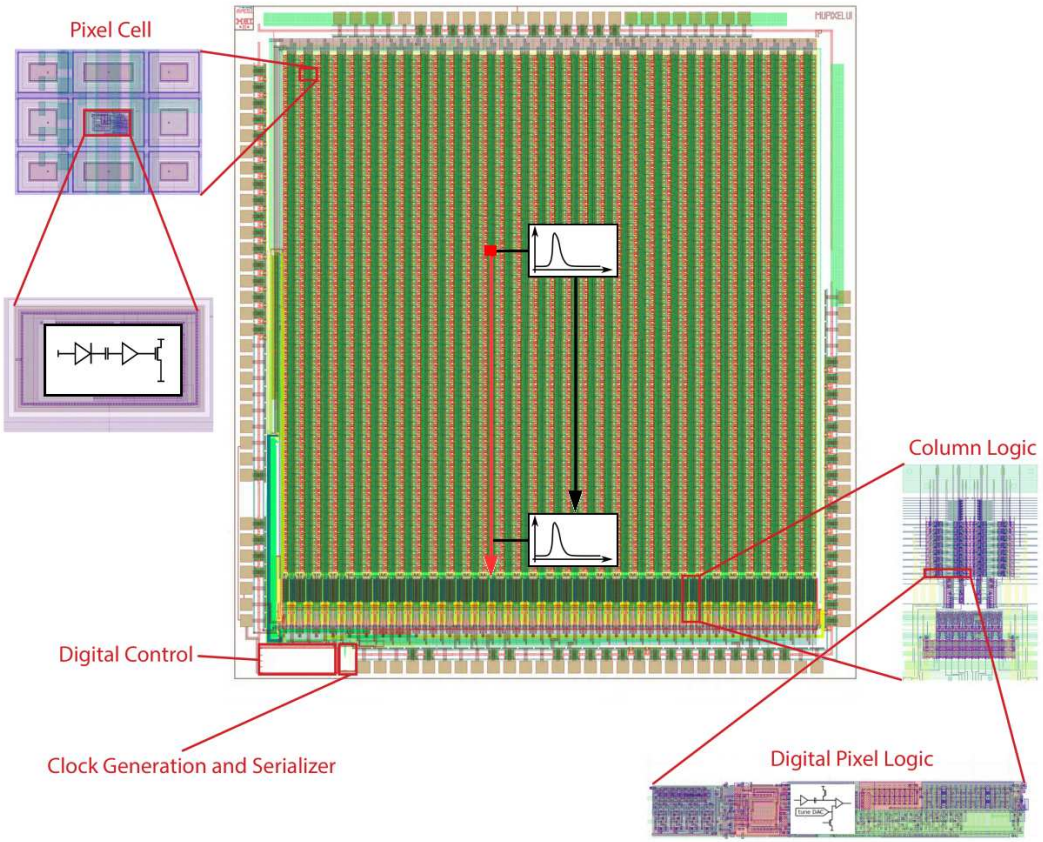
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



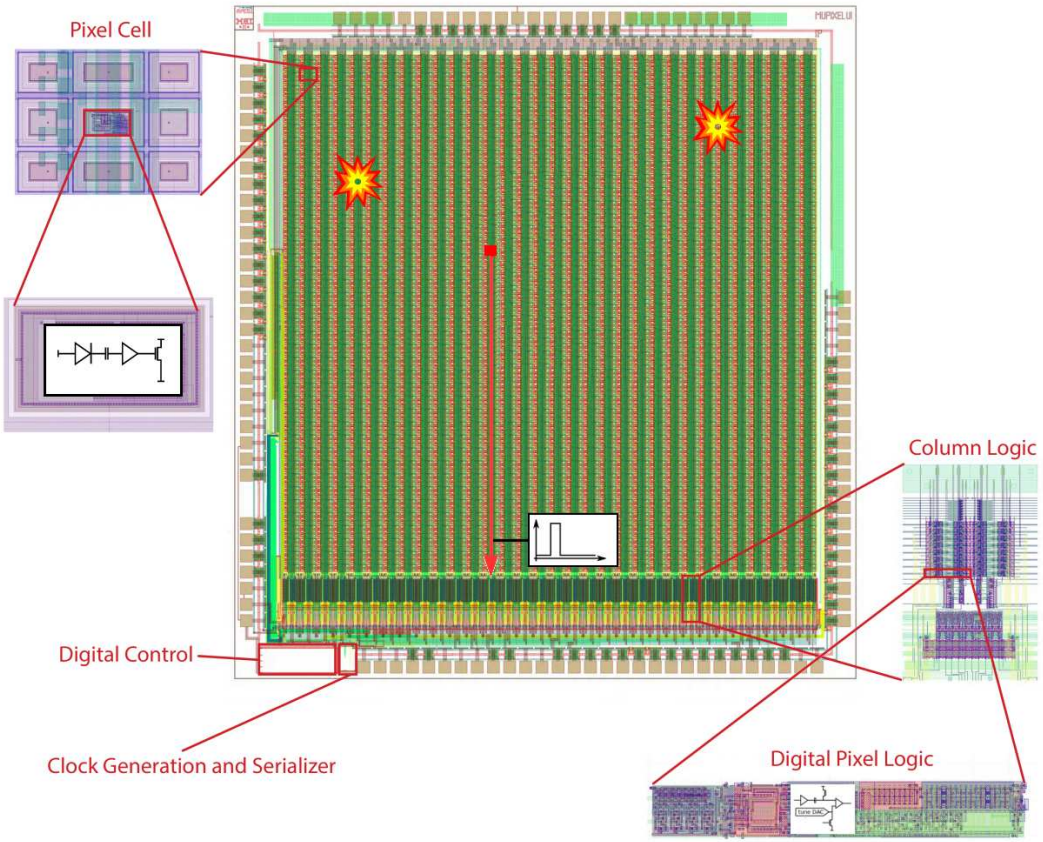
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



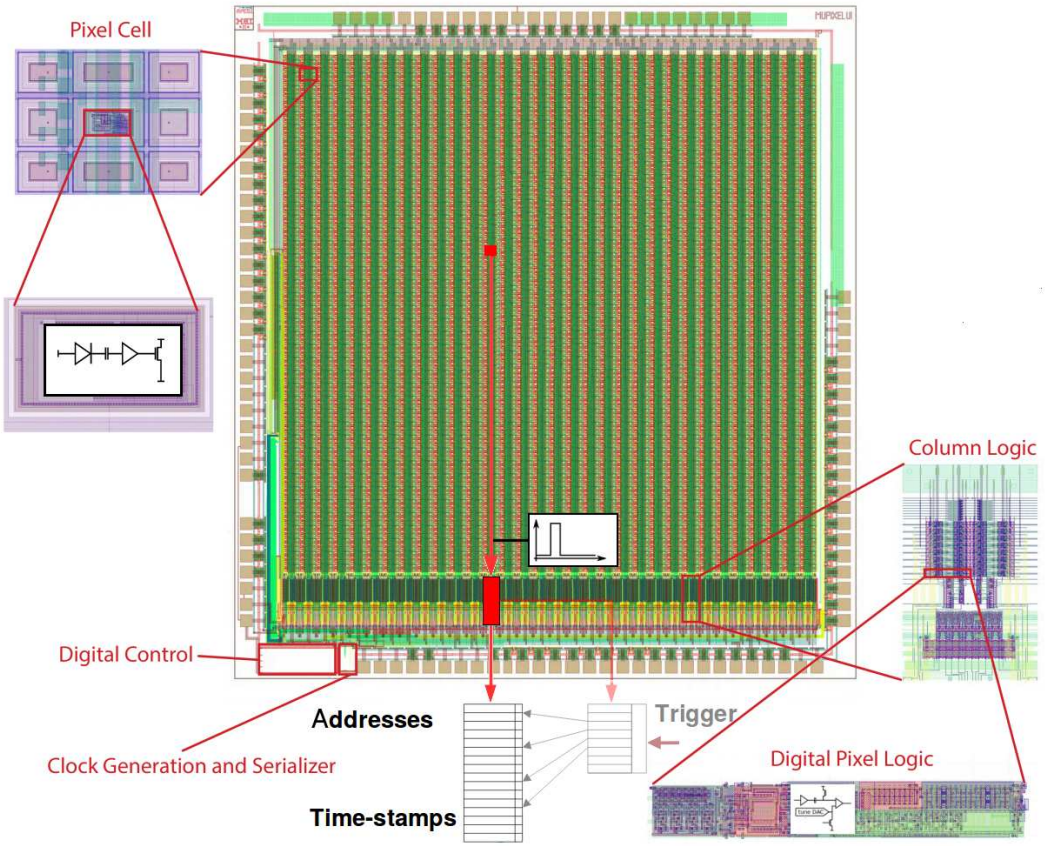
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



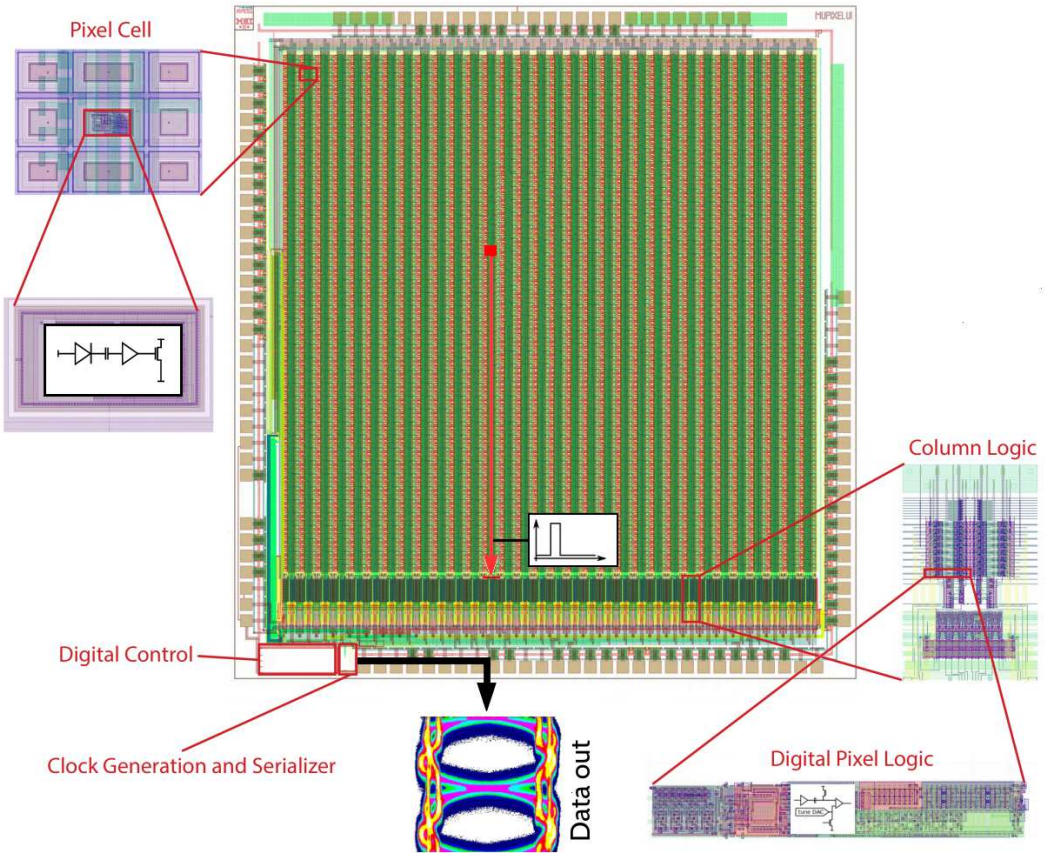
- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

R/O architecture: self-triggered

Self-triggered readout

used in the **MuPix7**-chip



- particle hits pixel, charge is collected by diode
- voltage at **C**harge **S**ensitive **A**mplifier (**CSA**) proportional to charge
- CSA signal send to chip periphery via transmission bus
- comparator compares signal to threshold voltage and digitize signal
- time-stamp and pixel address stored in **E**nd **O**f **C**olumn (**EOC**) buffer
- valid hit information sent out serially

source: https://www.psi.ch/mu3e/poster-gallery

Summary

MAPS starting to make their way into HEP

- ASIC in sensor substrate
- only standard CMOS technology
- small pixel size (spatial resolution)
  - improved vertex resolution
- low material budget
  - reduced multiple scattering
- standard MAPS (diffusion) or HV-MAPS (drift)
- sufficient radiation tolerant
  - standard-MAPS $\leq 10^{13}\ n_{eq}/cm^3$
  - HV-MAPS $\geq 10^{15}\ n_{eq}/cm^3$

the growing MAPS family

That's it

Thanks for your attention!

References

1 Kolanoski, H.; Norbert, W. *Teilchendetektoren: Grundlagen Und Anwendungen.* (2016) Springer.

2 *A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology* - Perić, Ivan Nucl.Instrum.Meth. A582 (2007) 876-885

3 I. Perić, *High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments*, Nucl. Instrum. Meth. A 731 (2013) 131, 2013.

4 *Studies of irradiated AMS H35 CMOS detectors for the ATLAS tracker upgrade* - Cavallaro, Emanuele et al. JINST 12 (2017) no.01, C01074 arXiv:1611.04970 [physics.ins-det]

5 *CMOS monolithic active pixel sensors for high energy physics* - W. Snoeys, Volume 765, 2014, Pages 167-171, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2014.07.017

6 *ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade* - M. Mager, Volume 824, 11 July 2016, Pages 434-438, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2015.09.057.

7 *MuPix7-A fast monolithic HV-CMOS pixel chip for Mu3e* - Augustin, H. et al. JINST 11 (2016) no.11, C11029 `arXiv:1610.02210` [physics.ins-det]

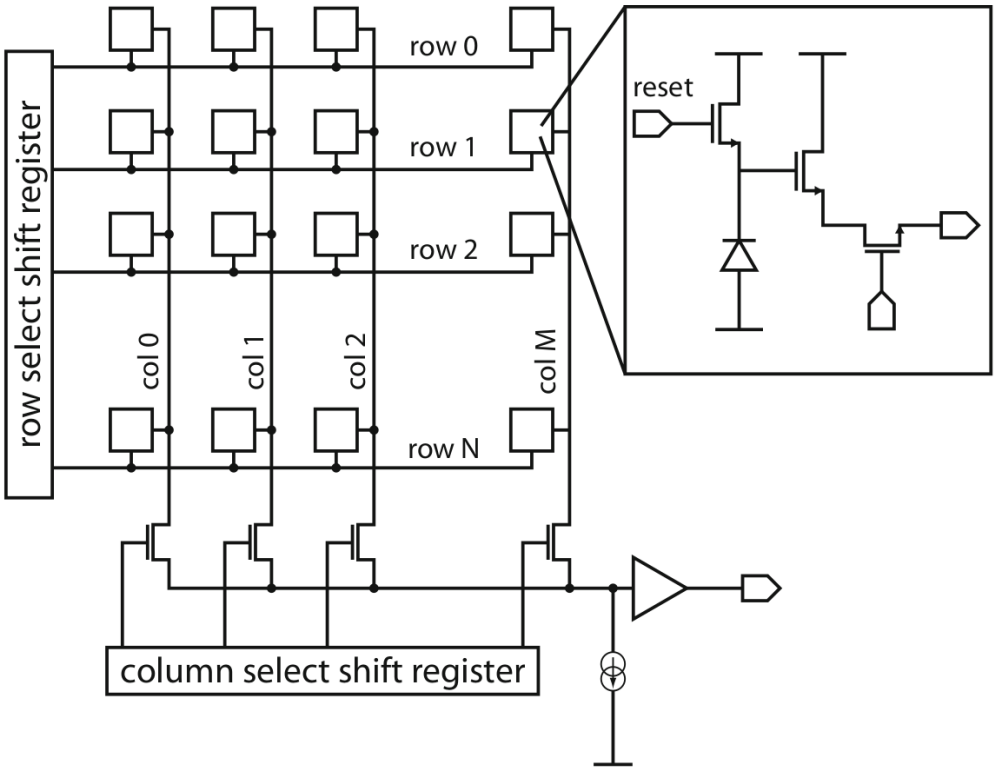
8 *The MuPix high voltage monolithic active pixel sensor for the Mu3e experiment* - H. Augustin, et al. JINST 10 (2015)

9 *CMOS Monolithic Active Pixel Sensors (MAPS) for future vertex detectors* - R. Turchetta, CCLRC, Rutherford Appleton Laboratory, Chilton, Didcot, Oxfordshire, OX11 0QX, UK

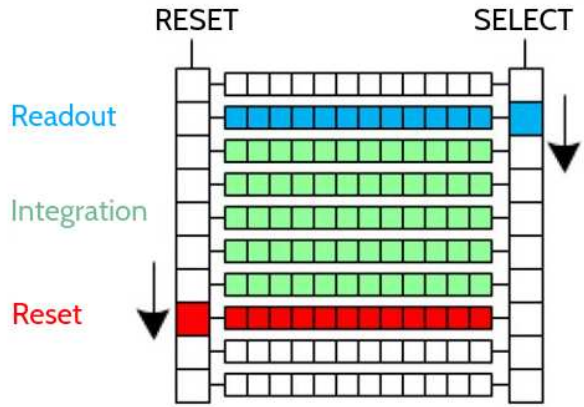
R/O architecture: rolling shutter

Rolling shutter

concept used by **STAR**



- hit causes voltage drop $\delta V_{\text{out}} = \delta Q / C_{\text{Diode}}$
- sequential readout (row by row)
- pixel is connected to its column
- discriminator marks hit as valid
- low digital noise
- intrinsically slow ($\sim 100\,\mu$s)

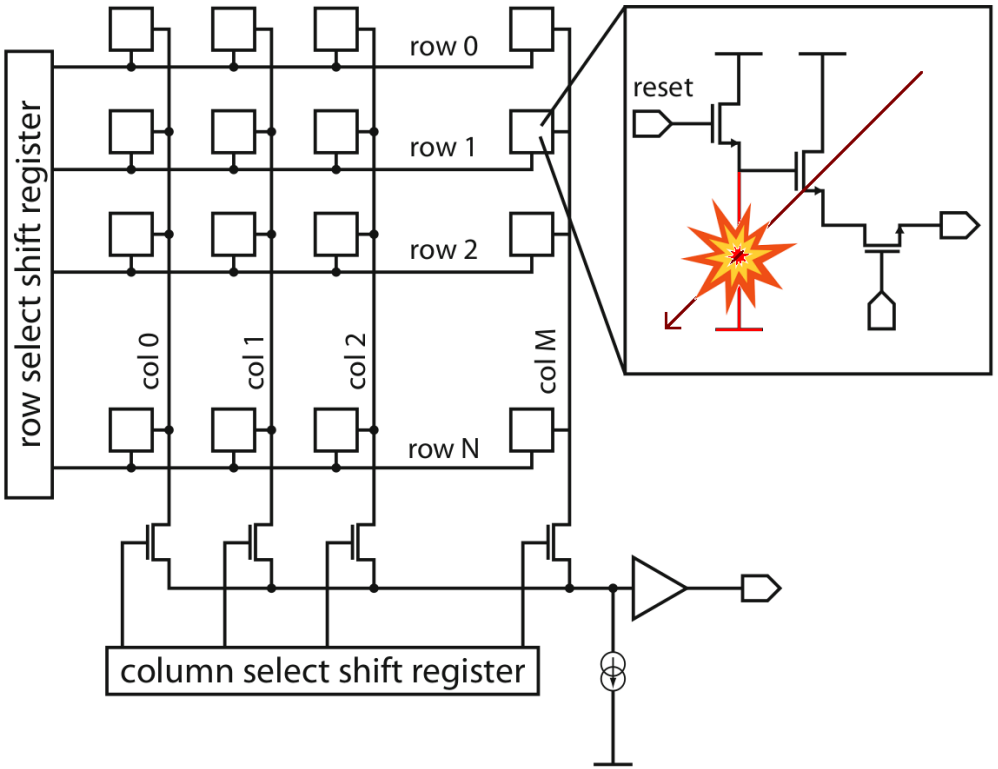


http://unaligned.org/bigcam/sensor.php

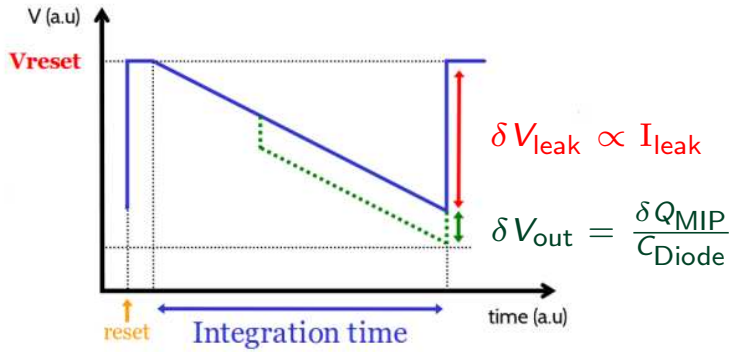
R/O architecture: rolling shutter

Rolling shutter

concept used by **STAR**



- hit causes voltage drop $\delta V_{\text{out}} = \delta Q / C_{\text{Diode}}$
- sequential readout (row by row)
- pixel is connected to its column
- discriminator marks hit as valid
- low digital noise
- intrinsically slow ($\sim 100\,\mu$s)

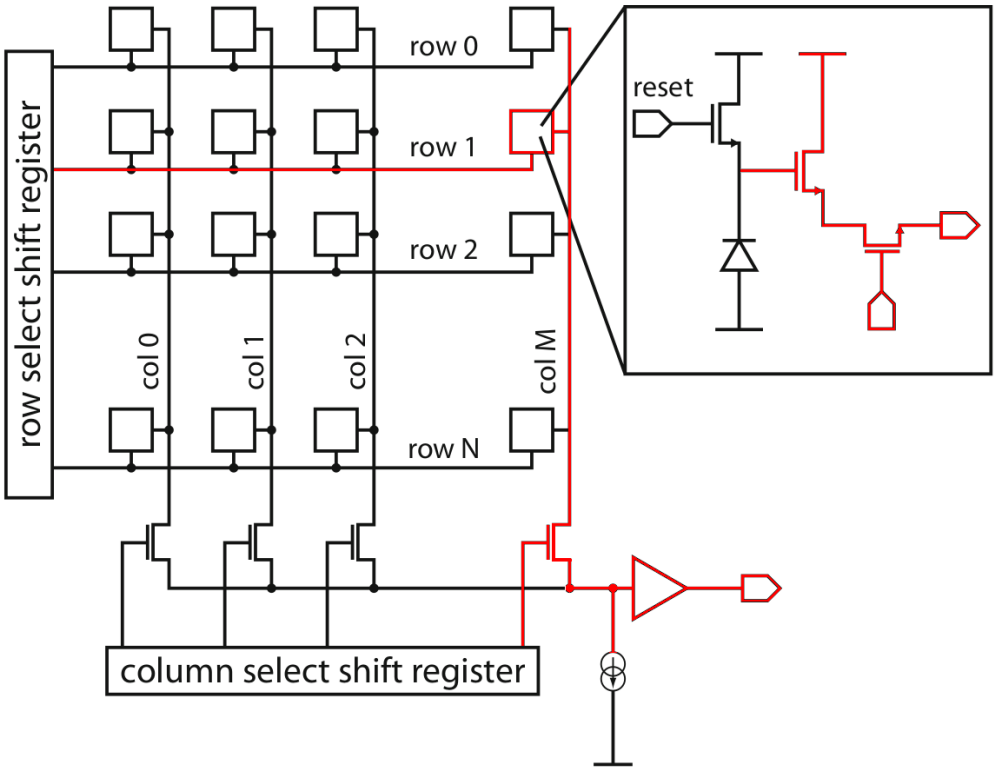


http://unaligned.org/bigcam/sensor.php

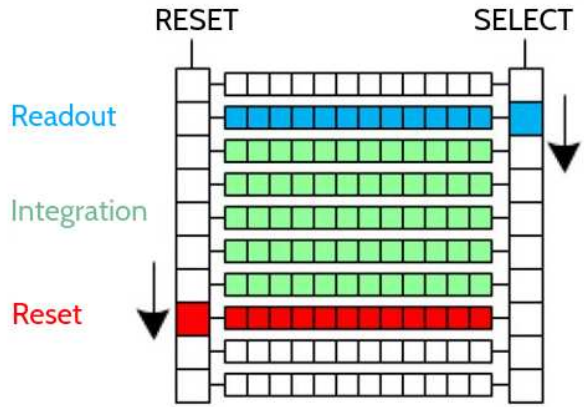
R/O architecture: rolling shutter

Rolling shutter

concept used by **STAR**



- hit causes voltage drop $\delta V_{\text{out}} = \delta Q / C_{\text{Diode}}$
- sequential readout (row by row)
- pixel is connected to its column
- discriminator marks hit as valid
- low digital noise
- intrinsically slow ($\sim 100\,\mu$s)



http://unaligned.org/bigcam/sensor.php

Make the Depletion Zone Visible

Edge Transient-Current Technique (eTCT)

eTCT

- Laser beam directed at sensor
- Laser imitates ionizing radiation
- Signal proportional to charge
- Scan for different positions

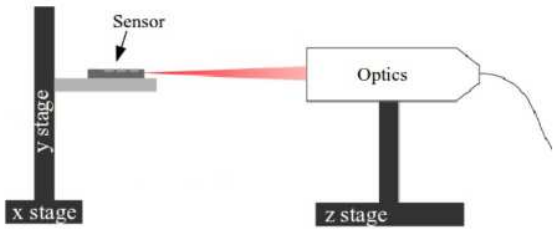
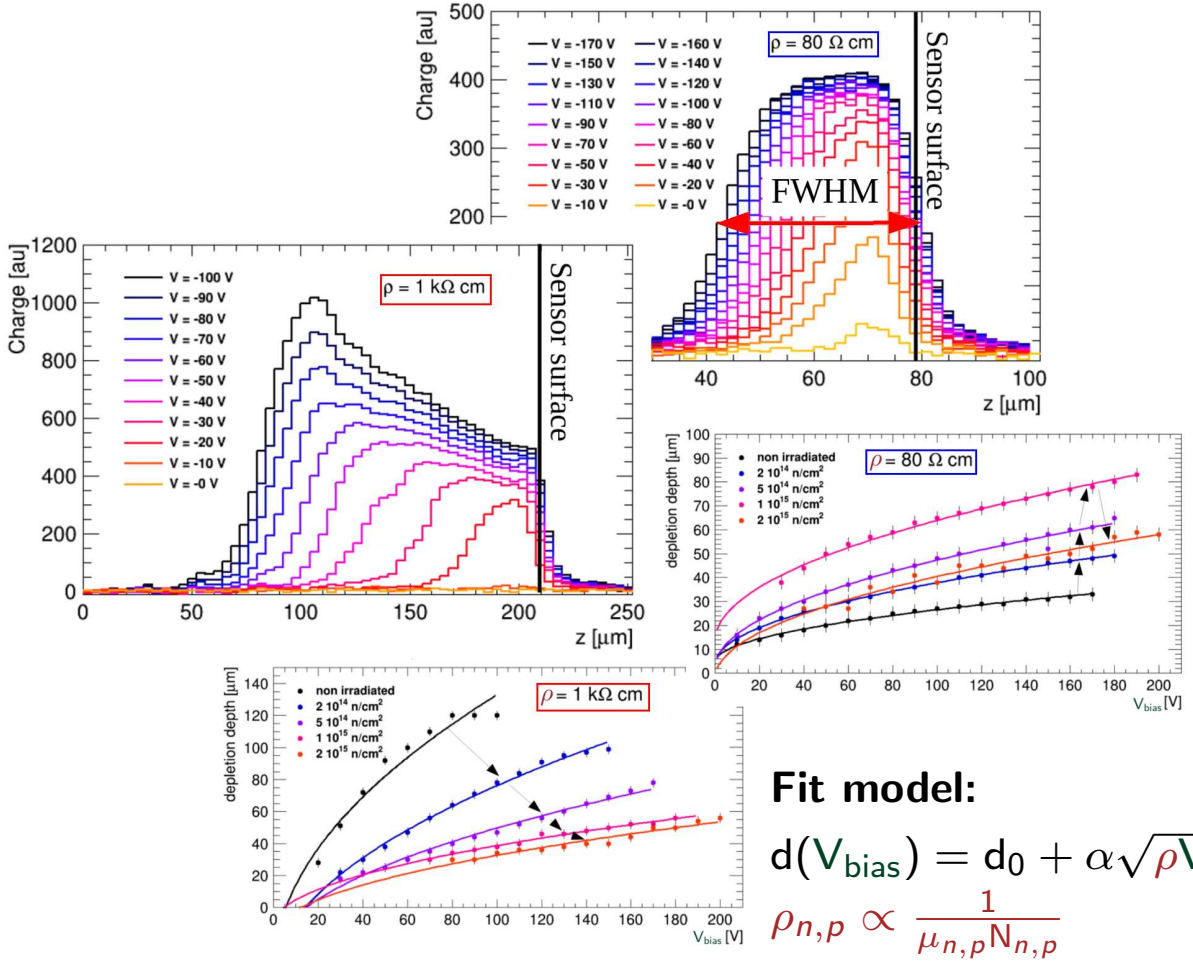


Fig. Experimental setup



Fit model:

$$d(V_{bias}) = d_0 + \alpha\sqrt{\rho V_{bias}}$$

$$\rho_{n,p} \propto \frac{1}{\mu_{n,p} N_{n,p}}$$

Plots based on H35Demo chip by KIT
(Investigate the possibility for installation in the ATLAS HL-LHC)
source: Edge TCT study on irradiated AMS H35 CMOS devices for the ATLAS IT