White Paper

Excalibur Embedded Processor PLD Stripe Power Consumption

Introduction

Two components comprise the total power consumption of an ARM®-based Excalibur device:

- PLD power consumption—calculated by using the APEX power calculator located at http://www.altera.com/products/devices/apex/apx-power_calc.html
- Embedded stripe power consumption

This document discusses how to calculate the power consumption of the embedded stripe for the family of ARM-based embedded processor devices.

Test Environment

The test referenced in this document exercises the embedded stripe logic and its interfaces. The test is conducted at low temperature and high V_{CC}, but with varying clock frequencies for both the embedded stripe and the embedded stripe interfaces. In this test, the embedded processor makes continual memory accesses; and the timer, UART, and EBI are enabled. The PLLs are locked and are used to drive the embedded stripe logic. Small portions of logic reside in the PLD and exercise the embedded stripe interfaces with the PLD as follows:

- The DPRAM interface makes a memory access on every clock edge
- A master in the PLD writes to a slave in the PLD via the PLD-to-Stripe bridge, over AHB2, and finally out of the stripe-to-PLD bridge.
- Transactions from the PLD master to the PLD slave travel across AHB2 continuously.

The following graphs represent the power consumption for the embedded stripe and the contributions due to the respective interfaces.

Power Consumption Graphs

Figures 1 to 3 show the current consumed by the embedded stripe.

Figure 1 on page 2 plots the current consumed by the embedded stripe with the PLD interfaces disabled.

Figure 1. Current Consumed by the Embedded Stripe versus AHB1 Clock Frequency

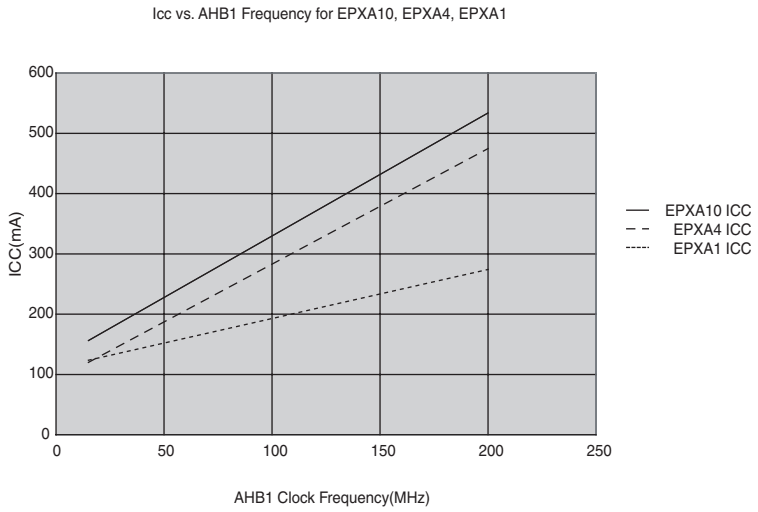


Figure 2 and 3 show the current consumed due to the embedded stripe PLD interfaces.

Figure 2 plots the current consumed due to the embedded stripe bridge interface.

Figure 2. Current Consumed Versus Clock Frequency Due to the Embedded Stripe Bridge Interface

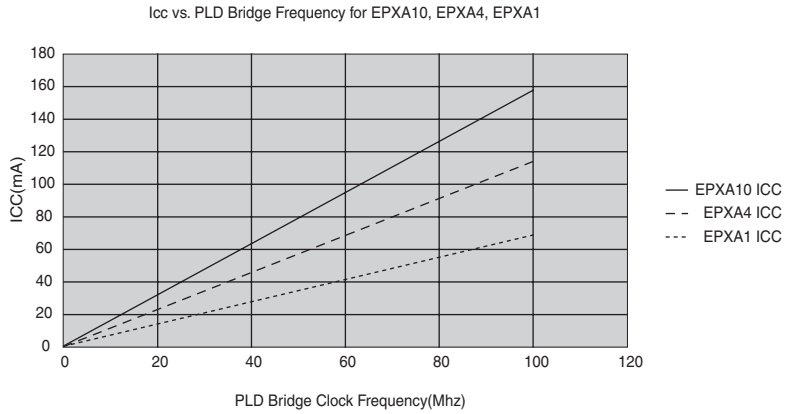
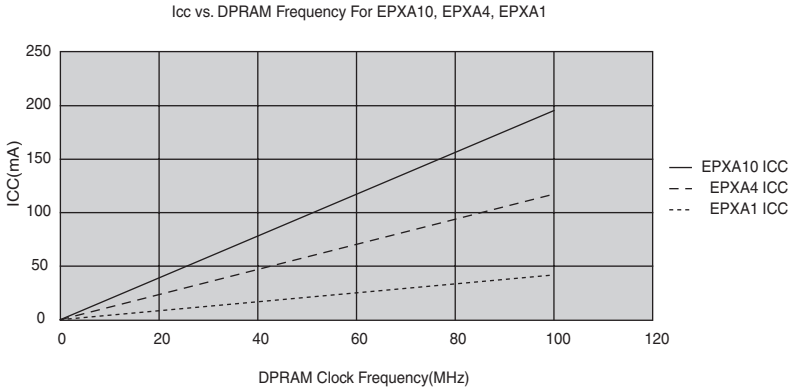


Figure 3 on page 3 shows the current consumed due to the embedded stripe DPRAM interface.

Figure 3. Current Consumed Versus Clock Frequency Due to the DPRAM Interface



Calculation Procedure

The total current consumption of the embedded stripe is the sum of the relevant values exemplified for the device. For example, the algorithm for the EPXA10 is:

Total I_{cc} = *EPXA10* I_{cc} *Figure 1* + *EPXA10* I_{cc} *Figure 2* + *EPXA10* I_{cc} *Figure 3*.

If either of the two PLD interfaces is not used, it can be omitted from the calculation.

EPXA10 Example Calculation

The following example calculation for the EPXA10 presupposes frequencies for AHB1 of 125 MHz, for the PLD bridge interface of 35 MHz, and for the DPRAM of 75 MHz:

EPXA10 I_{cc} *Figure 1* = 390 mA
EPXA10 I_{cc} *Figure 2* = 65 mA
EPXA10 I_{cc} *Figure 3* = 120 mA

Total embedded stripe I_{CC} for the EPXA10 is 575 mA

Conclusion

The power consumed by the embedded stripe is a function of the clock frequencies of the stripe and the respective PLD interfaces. The total power consumed by the ARM-based Excalibur device is the sum of the embedded stripe and the PLD. The PLD power consumption is calculated using the APEX power calculator.

EXCALIBUR™

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com