

Introduction

Density increases in programmable logic devices (PLDs) have led users to integrate more functions into today's PLDs. This increase in functionality has allowed PLDs to play a major role in transmitting data between boards or nearby systems, making accessibility to a variety of I/O buffers with different capabilities an important feature.

LVDS is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications. LVDS has become popular with system designers throughout the industry for a variety of applications. From high-speed backplane applications to a high-end switch box, LVDS has proven to be the technology of choice. LVDS is a differential signaling standard, so it has a high noise immunity and its low voltage swing allows for data transfers at high speeds.

APEX Devices

Altera® APEX™ devices offer a wide range of I/O buffers. Designers can use various types of I/O buffers such as LVTTTL, LVCMOS, SSTL-2, SSTL-3, CTT, and GTL+. However, the highest performance standard available in APEX 20KE and APEX 20KC devices is the LVDS I/O standard.

Altera's APEX 20KE and APEX 20KC devices have 16 input and 16 output dedicated True-LVDS™ channels equipped with embedded serializer/deserializer and phase-locked loop (PLL) technology capable of transferring data at 840 megabits per second (Mbps) per channel. The multiplexing of parallel data allows system designers to reduce bus width between two points while transmitting data at the same bandwidth.

When an application requires more than 16 LVDS channels, APEX 20KE and APEX 20KC devices can enable their general-purpose I/O pins to communicate with other LVDS devices at speeds of up to 156 MHz. This technique can be used for any APEX 20KE or APEX 20KC device in any package.

This application note describes how to utilize APEX 20KE and APEX 20KC general purpose I/O pins for LVDS signaling. This application note covers the following topics:

- Overview of LVDS characteristics
- Overview of APEX I/O standards
- Board implementation and SPICE simulation report
- Quartus™ II software implementation

LVDS Characteristics

Figures 1 and 2 show a typical LVDS application and its signal levels. Input signals are converted to LVDS signals by the transmitter. Typically the signals are transmitted over a pair of PCB traces, but a combination of a PCB trace, connectors, and cables are common. The media is then terminated by a $100\ \Omega$ resistor, and because LVDS buffers are current, driven the combination of the termination resistor and the transmitter's current, creates a signal swing of approximately 350 mV at the receiver's inputs. The receiver's threshold region is $\pm 100\text{ mV}$, and the common mode is $\pm 1\text{ V}$ above and below the 1.2-V offset voltage.

Figure 1. LVDS Application

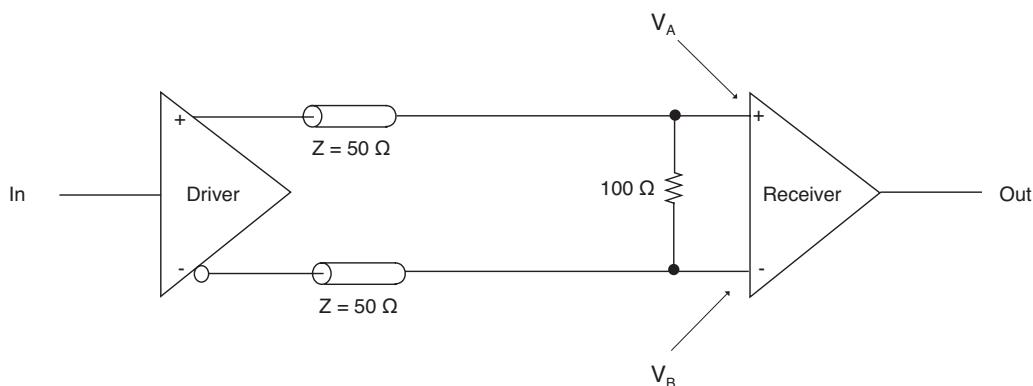


Figure 2. Typical LVDS Signal Levels

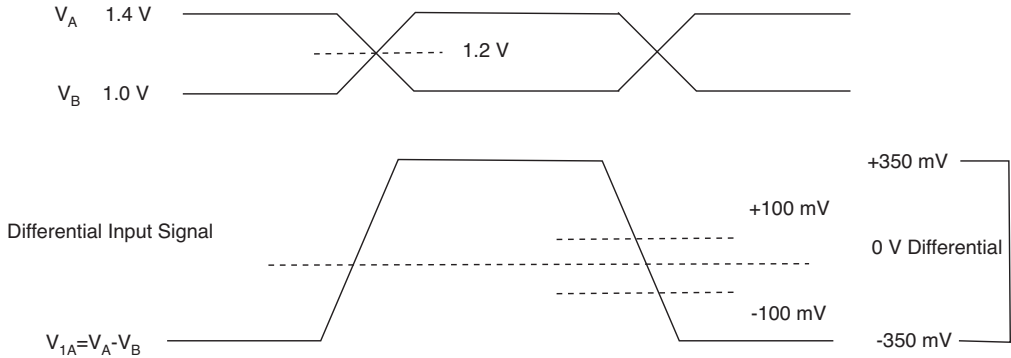


Table 1 displays LVDS parameters commonly used by chip vendors.



For more information on LVDS signaling, go to the International Engineering Consortium web site (<http://www.iec.org>).

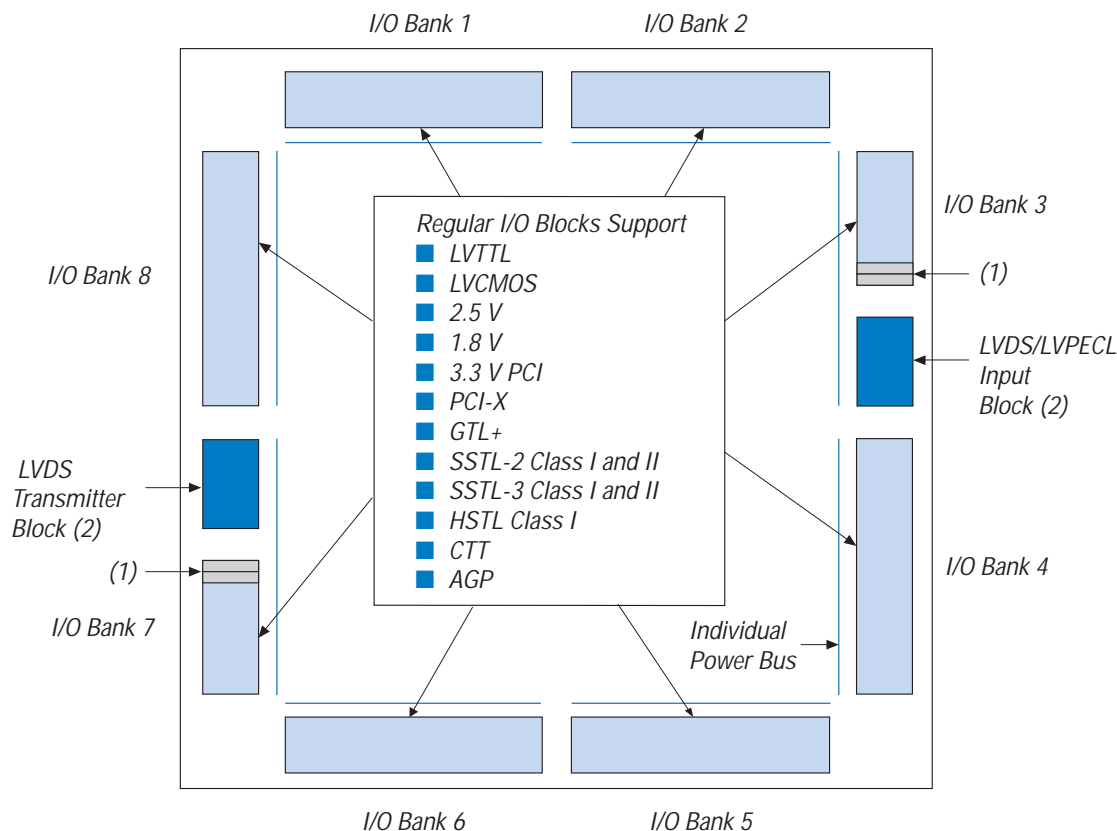
Table 1. APEX 20KE and APEX 20KC LVDS Levels for 3.3-V I/O Specifications

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_{CCINT}	Core supply voltage		1.71	1.8	1.89	V
V_{CCIO}	I/O supply voltage		3.0	3.3	3.6	V
V_{OD}	Differential output voltage	$R_L = 100 \Omega$	250		450	mV
V_{OD}	Change in V_{OD} between H and L	$R_L = 100 \Omega$			50	mV
V_{OS}	Output offset voltage	$R_L = 100 \Omega$	1.125	1.125	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	$R_L = 100 \Omega$			50	mV
V_{TH}	Differential input threshold	$V_{CM} = 1.2 \text{ V}$	-100		100	mV
R_L	Receiver differential input resistor		90	100	110	Ω

APEX 20KE and APEX 20KC I/O Block Standards

Altera's APEX 20KE and APEX 20KC devices have eight programmable I/O banks that support many I/O standards. Two of the eight I/O banks include the True LVDS input or output buffers. The LVDS I/O buffers are strategically placed at the edge of the die to help reduce possible reflection or skew. Figure 3 shows the APEX 20KE and APEX 20KC device I/O banks.

Figure 3. APEX 20KE and APEX 20KC Device I/O Blocks

**Notes:**

- (1) The first two I/O pins that border the LVDS blocks can only be used for input to maintain an acceptable noise level on the V_{CCIO} signal.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Voltage-Referenced I/O Standards

Many of the new I/O standards use an externally-supplied reference voltage V_{REF} to determine the incoming logic level. For example, when an input level is above the V_{REF} voltage, it is a logical high, and when an input level is below the V_{REF} voltage, it is a logical low. APEX 20KE and APEX 20KC devices support one V_{REF} per I/O bank.



For more information on voltage-referenced I/O standards, refer to *Application Note 117: Using Selectable I/O Standards in Altera Devices*.

Receiving LVDS Signals Using General-Purpose APEX I/O pins

Receiving LVDS signals at 156 MHz on general-purpose I/O pins is accomplished by selecting the SSTL-2 Class II, terminating the incoming LVDS signals using two 50 Ω resistors where their junction is connecting the V_{REF} of the I/O bank used. This scheme is shown in Figure 4.

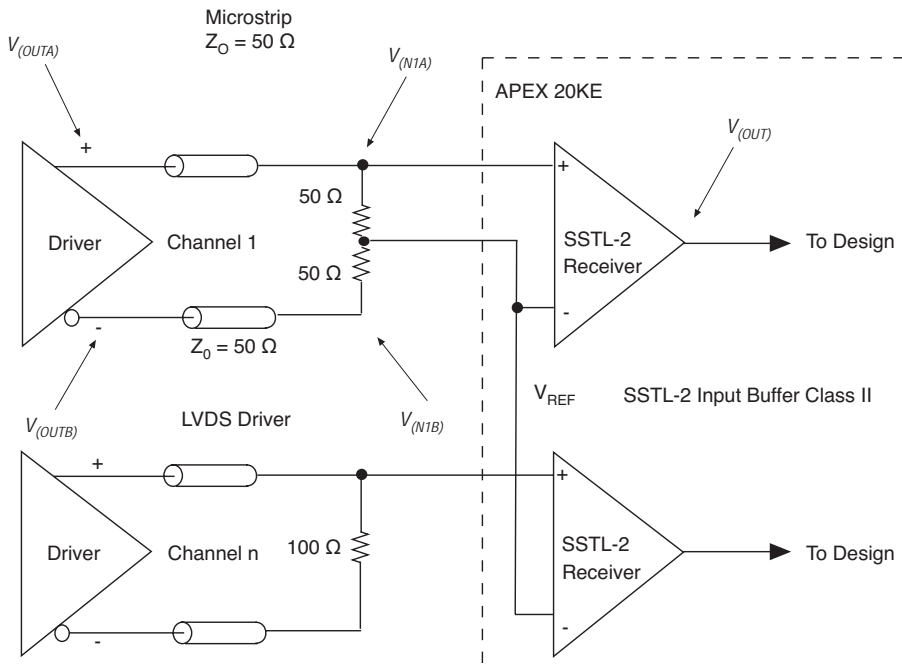
The SSTL-2 Class II buffers have a V_{REF} value similar to the LVDS common mode voltage; therefore, it is well suitable for receiving LVDS signals.



For more information on receiving LVDS signals using general-purpose APEX I/O pins, refer to *Application Note 117: Using Selectable I/O Standards in Altera Devices*.

When more than one LVDS channel is connected to the same I/O bank, the V_{REF} pin is supplied by the first channel. The other channels may be terminated by utilizing a standard 100 Ω resistor.

Figure 4. Receiving LVDS Signals

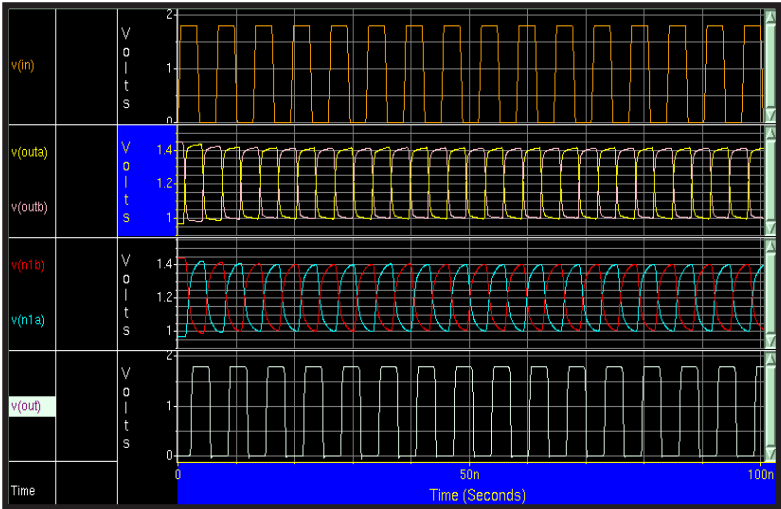


LVDS to SSTL-2 SPICE Simulation

SPICE simulations may be utilized to validate a design technique. The simulation was set up using Altera’s LVDS and SSTL-2 SPICE models. This method was simulated using the APEX 20KE or APEX 20KC device driver and receiver SPICE models. Signals were monitored at driver output V_{OUTB} , V_{OUTA} , receiver input V_{N1A} , V_{N1B} , and receiver’s output V_{OUT} . The model for the media was a pair of 6-in. differential microstrip PCB traces. **Figure 4** is a schematic representation of the simulation setup. A typical signal at 156 MHz was applied to the LVDS driver and the signals were monitored at driver output, receiver input, and receiver output.

Figure 5 demonstrates the result of this simulation using nominal models. The results across industrial temperature (fast and slow models) were similar. The simulation shows that the scheme would work well in a point-to-point topology. The simulated circuit was also validated in the laboratory environment using a test board.

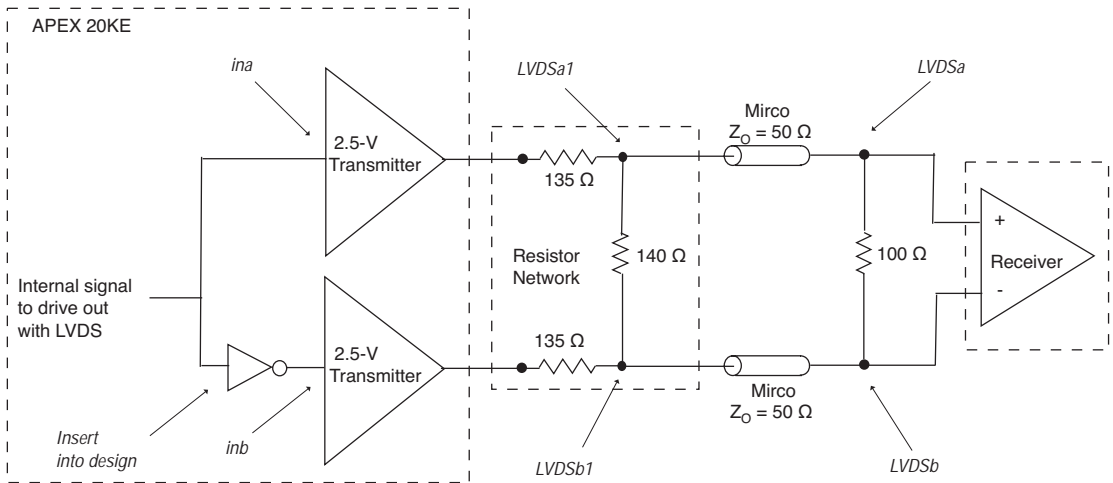
Figure 5. LVDS Transmitter to SSTL-2 Receiver SPICE Simulation



APEX 2.5-V I/O Buffers to LVDS

The interface from a non-LVDS I/O buffer to an LVDS receiver buffer is implemented by using a resistor network. The resistors attenuate the driver outputs to levels similar to LVDS signaling for recognition by an LVDS receiver. This method was also simulated using APEX 2.5-V drivers and LVDS receiver SPICE models. Driver inputs (*ina* and *inb*), the resistor network (*LVDSa1* and *LVDSb1*), and receiver inputs (*LVDSa* and *LVDSb*) were monitored. Figure 6 shows a schematic representation of the setup.

Figure 6. General Purpose I/O to LVDS Receiver

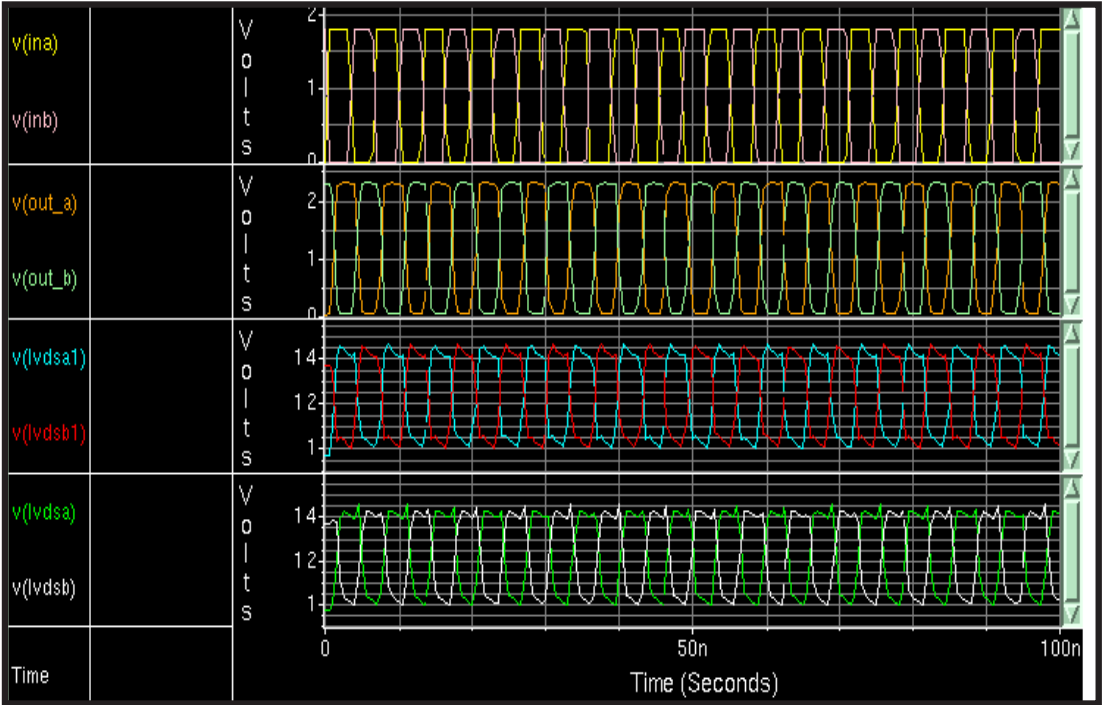


LVDS to 2.5-V SPICE Simulation

The simulation was set up with models used in the previous experiment. The media was also kept constant: a pair of 6-in. differential microstrip PCB traces. Signals at 156 MHz were applied to the drivers with opposite polarity and were monitored at various locations of the circuit.

Figure 7 demonstrates the result of this evaluation at room temperature using nominal models. The results across industrial temperature (fast and slow models) were similar. The SPICE simulation shows the data was correctly transferred to the destination.

Figure 7. General Purpose I/O to LVDS Receiver SPICE Simulation



Implementing LVDS with Quartus II Software

This section describes how to implement LVDS using general-purpose I/O pins in the Quartus II software. An effective way to transmit or receive data is to use the source synchronous clocking system. This method utilizes the clock to transmit or capture the data. Designers can also use the synchronous clocking method, which does not require any special design technique.

LVDS Receiver Interface

Implementing a LVDS using APEX 20KE or APEX 20KC general purpose I/O pins require that the differential signal first be converted to a single-ended signal. The LVDS receiver interface utilizes the SSTL-2 Class II I/O standard for implementation. Because conversion is done external to the device, the functional design would be entered using single-ended I/O buffers. The LVDS signal is converted to SSTL-2 Class II using external resistors on the board (see Figure 8).

In a Quartus II software reference design for capturing serial stream data, both clock and data are driven into the circuit. The CLK signal is inverted to sample the LVDS data in the middle of the data eye. The output of the register will drive a shift register which converts incoming serial data to parallel data (four bits at the time). The data is then driven to the LPM_FIFO_DC dual-clock first-in first-out (FIFO) controlled by a two bit counter. The two bit counter enables the FIFO to read data four bits at a time while the circuit writes into the FIFO on every clock cycle.



Pin and I/O standard assignments can be assigned to the procedure outlined in the LVDS Pin Assignment Procedures section.

Figure 8. Receiver Implementation

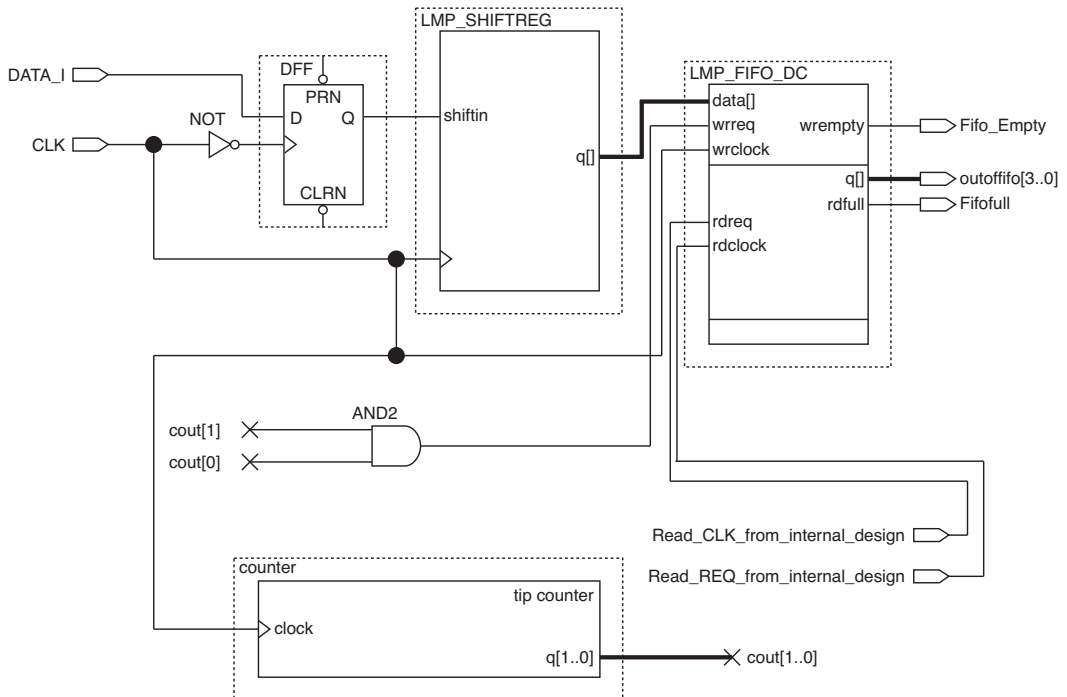
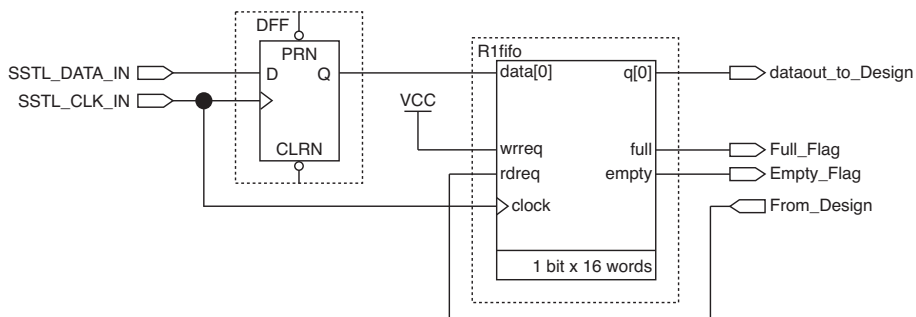


Figure 9 shows a Quartus II software reference design for capturing data that is presented to the device as a bus. Both clock and data are driven into the device. The data is captured by a FIFO and read into the design. The designer controls the data read into the design through the rdreq internal input pin.

Figure 9. Alternate Receiver Implementation



LVDS Transmitter Design

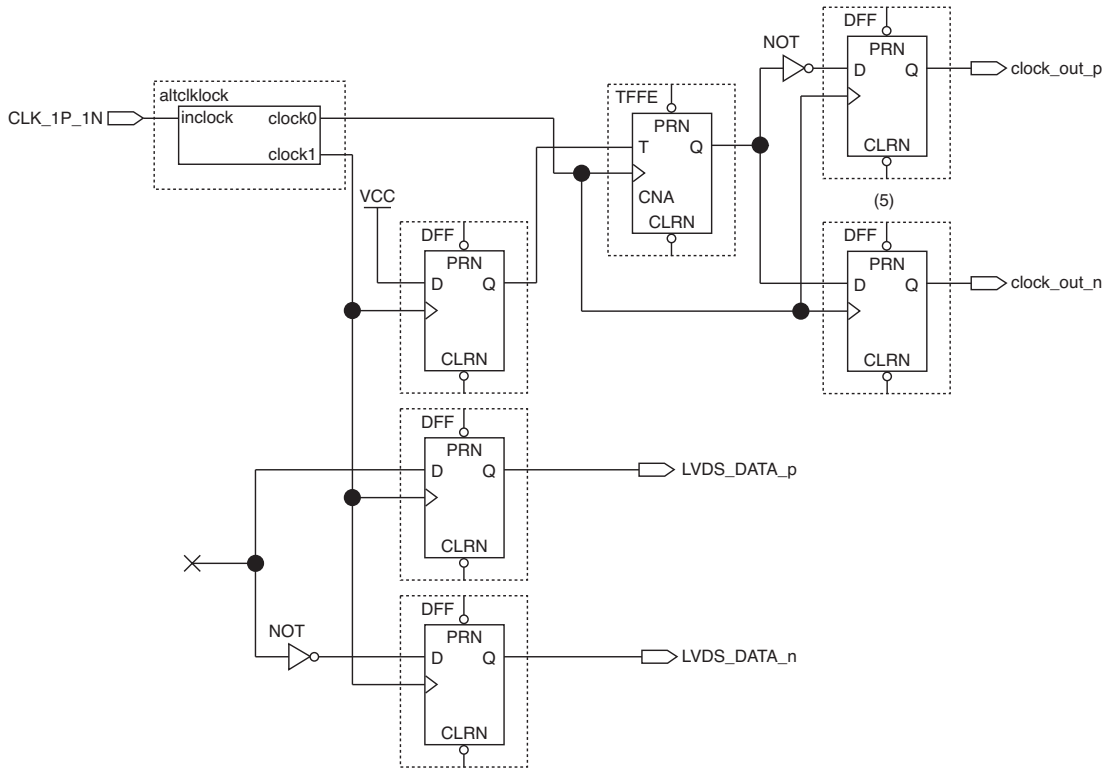
In order to transmit data, 2.5-V drivers convert the signal-ended signals to differential outputs. The sample design is shown in [Figure 10](#).

The transmitter design uses one of four PLLs within the APEX 20KE or APEX 20KC device to provide $\times 1$ and $\times 2$ multiples of the clock input. The $\times 1$ and $\times 2$ clocks synchronize outgoing clock and data signals.

The data is connected to two flip flops with one connected to an inverter. The LVDS_DATA_p and LVDS_DATA_n signals are clocked by the $\times 1$ multiple of the input clock to the PLL. The differential clock is created using the same technique is connected to a TFF.

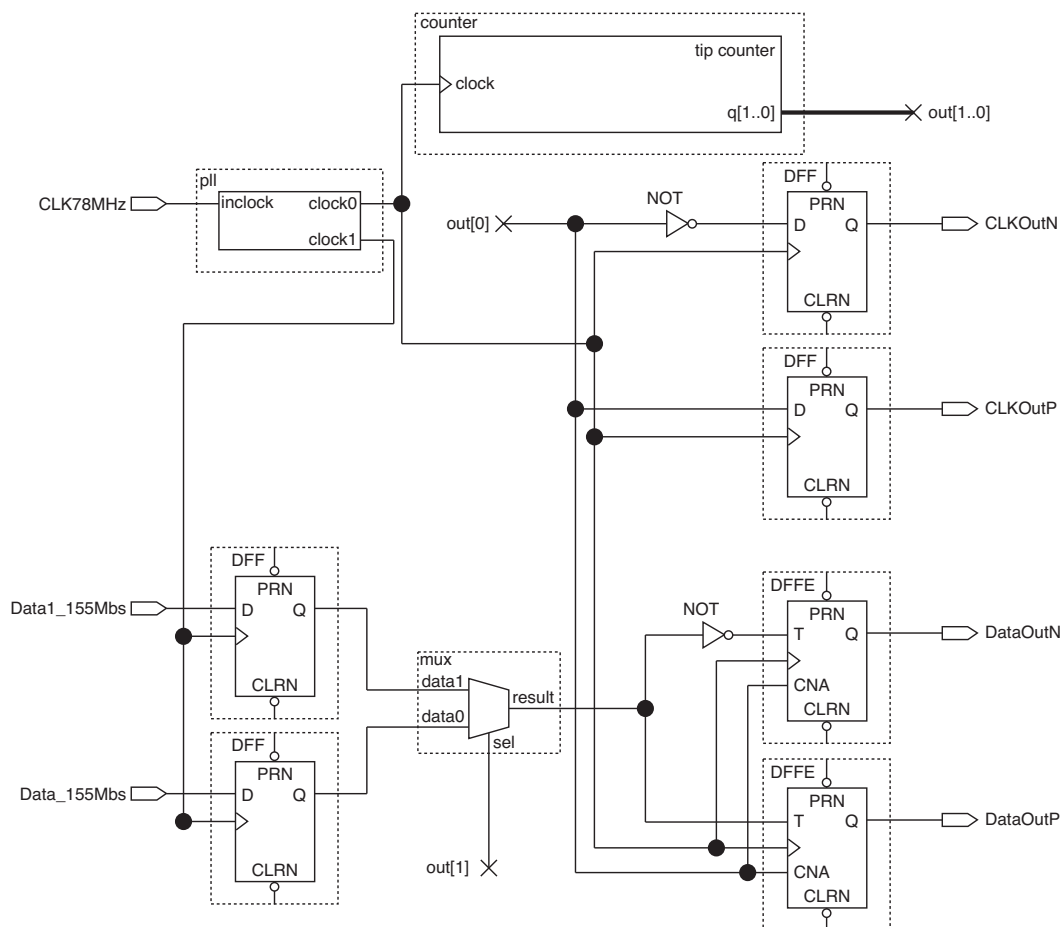
Place LVDS output pin pairs so that the skew between the positive and negative signals of the differential pair are minimized. If necessary, use the APEX 20KE or APEX 20KC device IOE registers and select adjacent pins on the package.

Figure 10. LVDS Transmitter Design Implementation



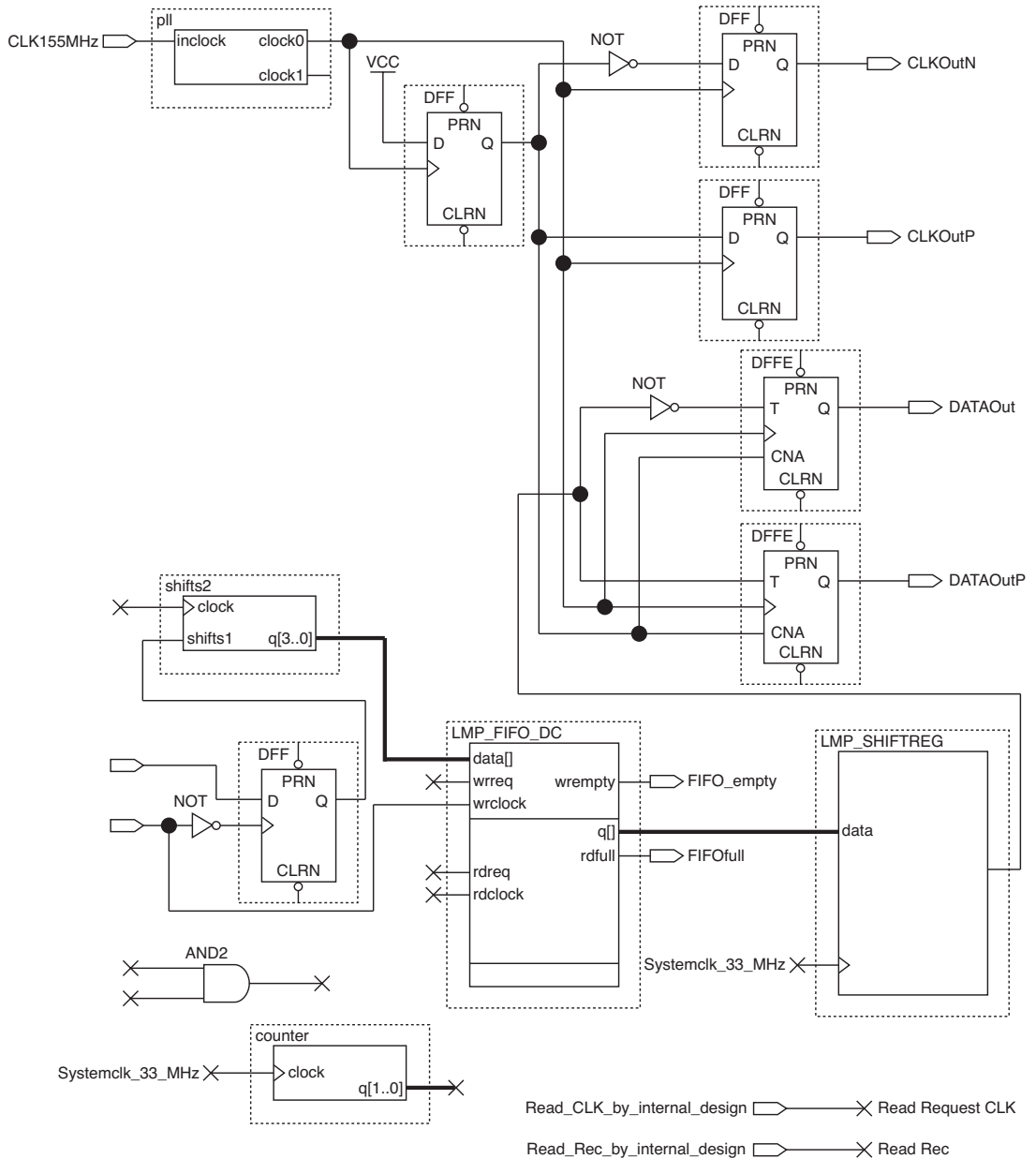
Some logic array designs run at a 78-MHz clock speed. Therefore, use the `altlock` PLL megafunction to multiply the logic array frequency by four, and use the PLL's output to transmit data. The design shown in [Figure 11](#) shows this system implementation in the Quartus II software.

Figure 11. Transmitter Implementation in Quartus II Software



In systems where the LVDS data rate is not a multiple of the systems clock, use a combination of a counter and a FIFO to cross domain boundaries (see [Figure 12](#)).

Figure 12. Transmitter Implementation in Quartus II Software



LVDS Pin Assignment Procedures

APEX 20KE or APEX 20KC device I/O pins are assigned to specific I/O banks. When you assign a signal to a pin and select SSTL-2 Class II as the I/O standard, all pins within that I/O bank operate at 2.5 V. Therefore, assign all SSTL-2 Class II pins to the same bank to avoid consuming I/O pins unnecessarily.

Pin and I/O Standard Assignment

Use the following steps to assign pin and I/O standards.

1. With the project open in the Quartus II development software, choose **Compiler Settings** (Processing menu).
2. Select the **Chips & Devices** Tab.
3. In the **Family:** field select **APEX 20KE**.
4. In the **Target device** field, select the radio button titled **Specific device** selected in the 'Available devices' list.
5. In the **Available devices:** field, select the appropriate device.
6. Click on the **Assign Pins** button in the **Target device** field. The **Pin Assignments** window will open.
7. In the **Available Pins and Existing Assignments:** field select an I/O pin for assignment.
8. Type in the name of the clock signal or data in the **Pin Name:** field of the Assignment category.
9. In the **I/O Standard** field, select **SSTL-2 -II** from the drop-down list of available selections.
10. Click the **Add** button to create the pin and I/O standard assignment.
11. Click **OK** to exit the **Pin Assignments** window.
12. Click the **Apply** button in the **Compiler Settings** window for the changes to take effect.
13. Click **OK** to exit the **Compiler Settings** window.

Assign the V_{REF} pin within the same I/O bank as the SSTL-2 Class II pins. Use the previous procedure to assign the V_{REF} pin. The SSTL-2 Class II I/O standard must be selected for the V_{REF} pin. To enable the pin to be used as a V_{REF} pin, check the box that enables the feature Reserve Pin (even if it does not exist in the design file) and select **As V_{REF}** from the drop down list associated with the reserve pin field.



The reference designs discussed in this application note are available on the Altera web site at <http://www.altera.com>.

Conclusion

Altera's 16 transmitter and 16 True-LVDS solution are the preferred choice for today's high-speed, high-performance systems. In applications requiring more than 32 LVDS I/O pins or where True LVDS I/O pins are not available, an external resistor network can be used to interface LVDS signals to APEX 20KE or APEX 20KC devices and its general-purpose I/O pins.



For more information on I/O standards supported by APEX 20KE and APEX 20KC devices, see *Application Note 117: Using Selectable I/O Standard in Altera Devices*.



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