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**Development and Characterisation
of a Radiation Hard Readout Chip
for the LHCb Outer Tracker Detector**

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Zusammenfassung

Entwicklung und Test eines strahlenharten Auslesechips für das äußere Spurkammersystem des LHCb-Detektors.

Die Rekonstruktion von Teilchenspuren im äußeren Spurkammersystem des LHCb-Detektors erfordert die Messung der Driftzeiten in den Straw-Proportionalzählern. Hierzu wurde ein TDC (Time to Digital Converter) Chip entwickelt, der sich in das Datenerfassungsschema des LHCb-Experiments integriert und die Anforderungen des Detektors erfüllt.

Der OTIS Chip ist in einem kommerziellen $0,25\ \mu\text{m}$ CMOS Prozess gefertigt. Die totzeitfreie Driftzeitmessung mit einer nominellen Auflösung von $390\ \text{ps}$ und einem Messbereich von $25\ \text{ns}$ übernimmt der 32-Kanal TDC-Kern. Die gemessenen Driftzeiten werden bis zum Eintreffen einer Triggerentscheidung nach $4\ \mu\text{s}$ zwischengespeichert. Im Fall einer positiven Triggerentscheidung werden die entsprechenden Daten von der digitalen Steuereinheit des OTIS Chips aufbereitet und in einem LHCb konformen Datenformat an die weiterverarbeitende Elektronik gesendet. Den Spezifikationen entsprechend akzeptiert der OTIS Chip Triggerraten von bis zu $1.1\ \text{MHz}$. Die Driftzeitmessung sowie die Datenverarbeitung im OTIS Chip sind unabhängig von der Kanalbelegung des Detektors.

Im Rahmen dieser Arbeit wurde die digitale Steuereinheit des TDC Chips entwickelt und neben anderen Komponenten mit dem TDC-Kern in den OTIS Chip integriert. Verschiedene Testchips und Prototypen des TDCs wurden im Labor getestet. Die aktuelle Chipversion OTIS1.2 erfüllt sämtliche Anforderungen und ist bereit für die Serienfertigung.

Abstract

Development and Characterisation of a Radiation Hard Readout Chip for the LHCb Outer Tracker Detector.

The reconstruction of charged particle tracks in the Outer Tracker detector of the LHCb experiment requires to measure the drift times of the straw tubes. A Time to Digital Converter (TDC) chip has been developed for this task. The chip integrates into the LHCb data acquisition schema and fulfils the requirements of the detector.

The OTIS chip is manufactured in a commercial $0.25\ \mu\text{m}$ CMOS process. A 32-channel TDC core drives the drift time measurement ($25\ \text{ns}$ measurement range, $390\ \text{ps}$ nominal resolution) without introducing dead times. The resulting drift times are buffered until a trigger decision arrives after the fixed latency of $4\ \mu\text{s}$. In case of a trigger accept signal, the digital control core processes and transmits the corresponding data to the following data acquisition stage. Drift time measurement and data processing are independent from the detector occupancy.

The digital control core of the OTIS chip has been developed within this doctoral thesis. It has been integrated into the TDC chip together with other constituents of the chip. Several test chips and prototype versions of the TDC chip have been characterised. The present version of the chip OTIS1.2 fulfils all requirements and is ready for mass production.

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Introduction

Since in the middle of the year 2000 the Physics Institute of the University of Heidelberg is participating in the development of detector modules and the corresponding readout electronics for the LHCb Outer Tracker detector.

This thesis describes the evolution of the OTIS TDC chip for the readout of the Outer Tracker detector. This VLSI chip has been developed and characterised in collaboration with the ASIC-laboratory Heidelberg.

The specification phase of the readout chip started in summer 2000, in parallel with the development of prototype components of the chip. The first submission of a test chip, containing a first version of the time digitisation unit took place in October 2000. The successful tests of this prototype chip and of the pipeline memory test chip triggered the assembly of the complete readout chip, which has been submitted in May 2002. The table in appendix C summarises the different chip submissions until the current chip version `OTIS1.2` which is described in this thesis.

Chapter 1 describes the LHCb experiment and the different parts of the LHCb detector. The demands for the OTIS chip are derived from the Outer Tracker sub-detector and from the data acquisition system. Chapter 2 briefly introduces radiation hard design techniques together with the major steps of the digital design flow. Chapter 3 describes the design of the OTIS chip and chapter 4 details its digital control core. Measurement results from chip version `OTIS1.2` are presented in chapter 5.

1 The LHCb Experiment

The LHCb experiment is one of the five high-energy physics experiments that are currently under construction at the CERN¹ particle collider LHC². In contrast to the two general purpose experiments ATLAS and CMS, the LHCb experiment concentrates on CP violation and other rare phenomena in B meson decays: its detector is designed to exploit the large number of $b\bar{b}$ -pairs that are produced in the proton-proton interactions at the LHC. The other experiments Alice and TOTEM -the latter is installed in the CMS forward region- concentrate on heavy-ion physics respectively the measurement of the total pp cross section at the LHC.

From the start of operation in 2007, the LHC will collide beams of protons at a centre of mass energy of $\sqrt{s} = 14 \text{ TeV}$ with a design luminosity of $\mathcal{L} = 1.0 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. The beams of lead nuclei collide at $\sqrt{s} = 1150 \text{ TeV}$ with $\mathcal{L} = 1.0 \cdot 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$. Other general LHC parameters are listed in table 1.1 [LHC05].

LHC Parameters for Nominal Proton Performance	
Machine Circumference	26658.883 m
Revolution Frequency	11.2455 kHz
Bunch Crossing Angle	285 μrad
Total Number of Particles	$3.23 \cdot 10^{14}$
DC Beam Current	0.582 A
Stored Energy per Beam	362 MJ
Total Radiated Power per Beam	3.8 kW

Table 1.1: General LHC parameters [LHC05].

Because of the high $b\bar{b}$ production cross section of $500 \mu\text{b}$ and the high luminosity, the LHC will be a copious source of B mesons. A variety of b-hadrons, such as B_u , B_d , B_s , B_c and b-baryons will be produced at high rate. The LHCb experiment will be able to trigger and reconstruct many different final states of b-hadron decays with high statistics. The experiment offers the following capabilities:

- trigger sensitivity to both leptonic and hadronic final states,
- particle identification and good mass resolution to suppress background signals from b-hadron decays with the same topology as the $b\bar{b}$ signal,
- precise reconstruction of primary and B vertices and
- a tracking system with good momentum resolution.

Physics Perspective

In proton-proton collisions at 14 TeV , the $b\bar{b}$ production cross section is expected to be of the order of $500 \mu\text{b}$ which leads, even for the modest luminosity of $2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$, to about

¹European Organization for Nuclear Research

²Large Hadron Collider

10^{12} $b\bar{b}$ -pairs in a standard year of operation (10^7 s). From all inelastic interactions, the fraction of events with $b\bar{b}$ pair will be approximately $5 \cdot 10^{-3}$. This large b-quark production rate outperforms any existing machine and allows to study decay channels with branching ratios down to 10^{-7} with high statistics. An overview of the expected event numbers for some relevant decay channels is given in table 1.2.

Decay Modes	Visible Br. fraction	Offline Reconstr.
$B_{d}^0 \rightarrow \pi^+ \pi^- + \text{tag}$	$0.7 \cdot 10^{-5}$	6.9 k
$B_{d}^0 \rightarrow K^+ \pi^-$	$1.5 \cdot 10^{-5}$	33 k
$B_{d}^0 \rightarrow \rho^+ \pi^- + \text{tag}$	$1.8 \cdot 10^{-5}$	551
$B_{d}^0 \rightarrow J/\psi K_S + \text{tag}$	$3.6 \cdot 10^{-5}$	56 k
$B_{d}^0 \rightarrow \bar{D}^0 K^{*0}$	$3.3 \cdot 10^{-7}$	337
$B_{d}^0 \rightarrow K^{*0} \gamma$	$3.2 \cdot 10^{-5}$	26 k
$B_s^0 \rightarrow D_s^- \pi^+ + \text{tag}$	$1.2 \cdot 10^{-4}$	35 k
$B_s^0 \rightarrow D_s^- K^+ + \text{tag}$	$8.1 \cdot 10^{-6}$	2.1 k
$B_s^0 \rightarrow J/\psi \phi + \text{tag}$	$5.4 \cdot 10^{-5}$	44 k

Table 1.2: Expected number of events after reconstruction from one year (10^7 s) of data taking with an average luminosity of $2 \cdot 10^{32} \text{cm}^{-2} \text{s}^{-1}$ [TP98].

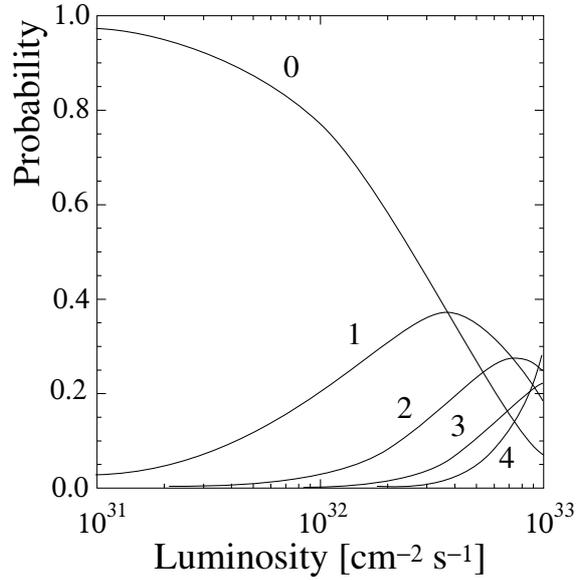


Figure 1.1: Probabilities for having 0, 1, 2, 3 and 4 pp interactions per bunch crossing as a function of the machine luminosity at LHCb. The number of bunch crossings with one pp interaction is maximum at approximately $4 \cdot 10^{32} \text{cm}^{-2} \text{s}^{-1}$ [TP98].

Optimal Luminosity

The LHCb experiment operates at an average luminosity of $\mathcal{L} = 2.0 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$, which should be possible to obtain from the beginning of LHC operation. The luminosity at the LHCb interaction point can be kept at its nominal value while the luminosities at the interaction points of the other LHC experiments are being progressively increased until their design values. Apart from being available right from the start, the modest luminosity at the LHCb interaction region keeps the detector occupancy low and reduces the radiation damage. When operating at $2 \cdot 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$, the number of events with two or more pp interactions per bunch crossing is suppressed. The reduced particle density per event facilitates event reconstruction. On the other hand, at the nominal LHCb luminosity, the number of events with single pp interaction is reasonable large compared to the number of empty events. Figure 1.1 shows the probabilities for having zero, one, two, three and four pp interactions per bunch crossing as a function of the machine luminosity (assuming an inelastic pp cross section of 80 mb [TP98]).

The LHCb detector houses the Outer Tracker detector subsystem which is used for the reconstruction of tracks from charged particles. The track reconstruction requires drift time measurement for all 55,000 Outer Tracker detector channels. The following sections shortly describe the Outer Tracker sub-detector and the other constituents of the LHCb detector. The necessity to develop a new TDC chip for the readout of the Outer Tracker is derived from the foreseen place of installation and from the underlying data processing concept. The key design parameters are presented.

1.1 The LHCb Detector

The LHCb detector is installed in the experimental area of LHC Interaction Point 8 that was formerly occupied by the DELPHI³ experiment. The detector is aligned with respect to a right-handed coordinate system which is centred on the interaction point with x horizontally pointing away from the LHC centre, y vertically pointing upwards and z pointing along the beam pipe towards the LHCb muon chamber. At the LHC proton-proton collisions, the production of $b\bar{b}$ -pairs strongly peaks towards small polar angles with respect to the beam axis. This drives the layout of the LHCb detector (see fig. 1.2) which is that of a typical fixed target spectrometer. Its acceptance, except for the 10 mrad cone of the beam pipe, is 300 mrad in the horizontal bending plane of the 4 Tm dipole magnet and 250 mrad in the non-bending plane.

Technological constraints and performance issues changed the detector design compared to the initial Technical Proposal [TP98] from 1998. For example, two major changes are the reduced number of tracking stations and the new mirror material of the RICH1 detector. Both changes significantly reduce the material budget and they therefore reduce multiple scattering of charged particles. A summary of the detector design changes is available in the corresponding technical design report [TDR9].

Though evolving, the basic layout of the LHCb spectrometer remains unchanged from that of the technical proposal. It consists of beam pipe, Vertex Locator, a tracking system (Trigger Tracker, Inner and Outer Tracker), dipole magnet and a particle identification system (Ring Imaging Cherenkov detectors, calorimeters and muon system).

³DEtector with Lepton, Photon and Hadron Identification

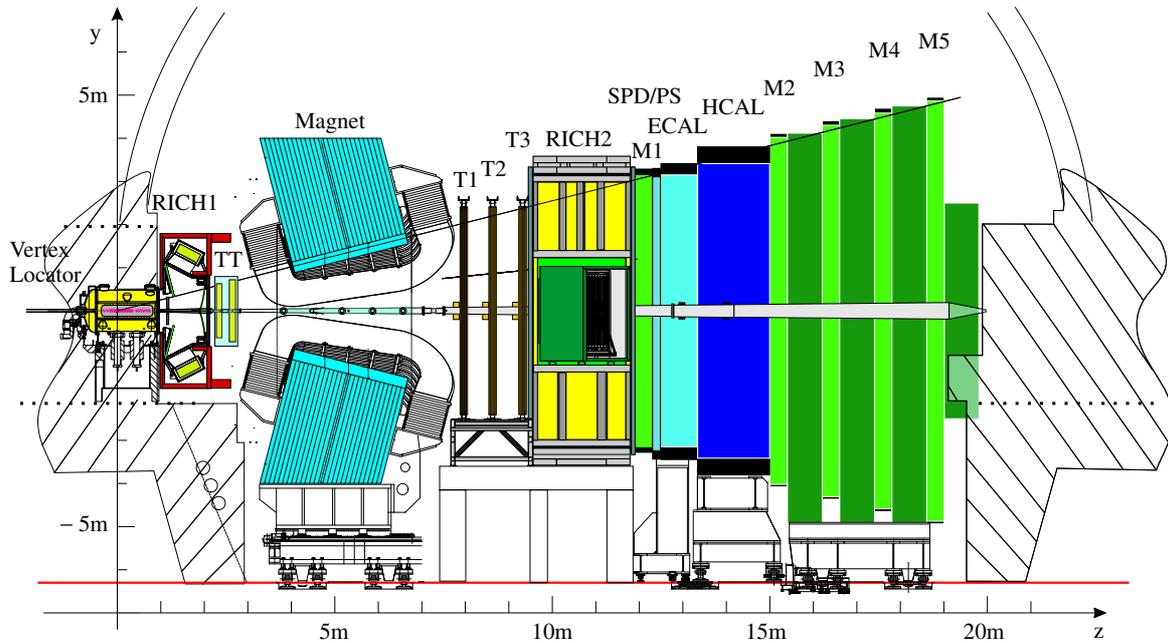


Figure 1.2: View of the LHCb detector in the y - z -plane. The drawing shows the Vertex Locator, the dipole magnet, the two RICH detectors, the tracking stations (TT and T1-T3), the electromagnetic and hadronic calorimeters (ECAL, HCAL) and the muon stations (M1-M5). Scintillating pad detector (SPD) and preshower (PS) are part of the electromagnetic calorimeter.

Beam Pipe The LHCb beam vacuum chamber has to withstand an average pressure of 10^{-9} mbar whilst introducing as few material as possible to the region of high particle density. The beam pipe consists of 1.0-2.4 mm thick cones, bellows and flanges made of beryllium, aluminium, an AlBe-alloy and stainless steel. The 20.8 kg design transects the whole detector and provides a 54 mm beam aperture at its narrowest end.

Magnet The spectrometer dipole is placed near the pp-interaction point in order to keep its size small. The iron shielding house of the RICH1 detector attenuates the stray field for the upstream sub-detector and allows operation of its photon detectors. The water-cooled magnet provides a maximum vertical field of 1.1 T and a field integral of 4 Tm. To be able to control systematic errors that might arise due to left-right asymmetries of the LHCb detector, it is possible to change the orientation of the magnetic field. The magnet weighs 1500 t and dissipates 3.5 MW of electric power.

Vertex Detector The main task of the vertex locator subsystem (VELO) is the precise measurement of track coordinates of charged particles close to the pp-interaction region. Each of the 21 VELO stations consists of two r - and ϕ -measuring silicon strip detectors mounted perpendicular to the beam axis. The stations are split in two slightly overlapping halves allowing the retraction of the sensors during beam injection. A corrugated aluminium box separates the primary beam vacuum from the secondary vacuum of the VELO vessel, at the same time serving as RF shield. The 175,000 VELO channels allow for primary vertex reconstruction with $42 \mu\text{m}$ resolution in the z -direction. Depending on the decay channel, the B-mesons decay length can be determined with an average resolution between $220 \mu\text{m}$ and $370 \mu\text{m}$ [TDR5]. Two additional upstream placed stations of r -measuring sensors form the VETO detector. This pile-up veto counter allows to suppress bunch crossings with multiple pp-interactions by counting the number of primary vertices.

Tracking System The tracking system of the LHCb detector, split into Trigger Tracker (TT), Inner Tracker (IT) and Outer Tracker (OT), provides track reconstruction and momentum measurement of charged particle tracks. It also links the measurements in the vertex detector with that of the calorimeters and the muon detector. Three IT/OT stations are placed between magnet and RICH2 detector; the TT station sits between RICH1 and magnet. The TT and IT stations are built of always four stereo layers of silicon microstrip detectors (200 μm pitch) with a total surface of 12.5 m^2 and 310,000 channels. The boundary between the inner tracking system and the coarser grained Outer Tracker is chosen such that the particle fluxes in the outer tracker stay below $1.4 \times 10^5 \text{ cm}^{-2}\text{s}^{-1}$. This allows to deploy the straw tube technology to cover the 300 m^2 surface of the Outer Tracker. This sub-detector will be composed of 55,000 straw tubes of 2.5 m length and 5 mm diameter each.

RICH Detectors Two Ring Imaging Cherenkov (RICH) detectors are foreseen for the LHCb detector. Both provide hadron identification for particle momenta up to 60 GeV/c (RICH1) and 100 GeV/c (RICH2) respectively. The RICH1 detector is placed between vertex detector and dipole magnet. It uses silica aerogel and fluorocarbon (C_4F_{10}) gas radiators and provides an angular acceptance of up to 300 mrad. The RICH2 detector is placed behind the tracker stations. It uses gaseous CF_4 and its angular acceptance (120 mrad horizontal \times 100 mrad vertical) fits the high momentum tracks that pass the magnet. The 440,000 RICH detector channels are read out with a combination of Hybrid Photon Detectors (HPD) and silicon pixel chips.

Calorimeters The LHCb detector includes an electromagnetic and a hadronic calorimeter (ECAL and HCAL) for photon, electron and hadron identification plus energy and position measurement. The ECAL uses *shashlik* technology, that is, wavelength-shifting (WLS) read-out fibres penetrate stacks of lead (2 mm) and scintillating material (4 mm). In contrast to the vertically orientated ECAL stacks, the HCAL uses iron/scintillating (4 mm/16 mm) tiles parallel to the beam. For better electron identification and π^0 suppression, a combination of single plane preshower (PS) and Scintillating Pad Detector (SPD) is placed in front of the ECAL. In total, all four calorimeter parts combine 20,000 channels.

Muon Detector The muon detector subsystem provides muon track and p_t -information for the LHCb L0 trigger plus off-line muon identification. The muon detector consists of one Cathode Pad Chamber (CPD) station that is placed before the calorimeters and four Multi-gap Resistive Plate Chamber (MRPC) stations that are installed behind an iron shield after the calorimeters. The total number of physical channels of all five multiple wire proportional chambers is 120,000 - these are combined to 26,000 readout channels. Relying on the high penetrative power of muons, the off-line muon identification counts detector hits within a field of interest around the extrapolation of tracks through vertex and tracking system.

1.2 The LHCb Trigger and Data Acquisition System

Starting from the 40 MHz bunch crossing rate at the LHC and assuming an average event size of 100 kB, the primary data rate of the LHCb detector calculates to 40 TB/s. A manageable data rate for event storage is achieved by deploying a three-level trigger and data acquisition system that selects interesting events and results in a data recording rate of about 200 Hz.

About 100,000 $b\bar{b}$ -pairs per second will be produced in the LHCb experiment at the foreseen luminosity and the $b\bar{b}$ -production cross-section of about 500 μb . However, events with fully reconstructed interesting $b\bar{b}$ final states represent only a small fraction of the total

$b\bar{b}$ sample: the small branching ratios (10^{-3} to 10^{-7}) and the limited detector acceptance lead to a total rate of interesting events of a few Hertz. On the other hand, the cross-section of events that produce at least two tracks in the LHCb acceptance is about 70 mb. That is, the trigger system must be able to efficiently select one interesting event out of 10^7 .

Additional to the selection of a large number of final states, the trigger system must provide unbiased control channels as well as channels for detector alignment and calibration studies.

The three LHCb trigger levels are:

- **Level-0 Trigger** The L0 trigger stage reduces the event rate to 1 MHz. This is a rate at which in principle all LHCb sub-detectors (except for RICH) can contribute to the next trigger level. L0 triggers are generated by the Level-0 Decision Unit (L0DU) based on transverse momentum information from the calorimeters and the muon detector. An event may be rejected when it consists of too many charged tracks or when it originates from multiple pp-interactions.

The L0DU is implemented in full custom hardware. It operates fully clock synchronous and it provides trigger decisions with a fixed latency of 4 μ s. The trigger algorithm does not depend on occupancy or history, and -of course- a L0 trigger decision does not stop further data recording. The L0 decision unit passes the trigger decisions to the Readout Supervisor which transmits the trigger to the all front-end devices.

- **Level-1 Trigger** The L1 trigger decision is based on a software analysis on part of the detector data. The information used is from Level-0, the vertex locator and the trigger tracker. The algorithm reconstructs tracks in the VELO and links these tracks to Level-0 muons or calorimeter clusters. Events are selected based on tracks with large transverse momentum and significant impact parameter to the primary vertex.

The L1 algorithm is implemented on a commodity processor farm, which is shared between Level-1 and High-Level Trigger (HLT). It reduces the 1 MHz L0 rate to 40 kHz and generates trigger decisions with a variable latency of about 1 ms. All LHCb sub-systems which provide data for the Level-1 trigger do interface to the same TELL1-board [Hae03] to store the data in the L1 buffer, to perform zero-suppression and data formatting.

- **High-Level Trigger** The High-Level Trigger is a software implementation running concurrently to the L1 algorithm on the same processor farm. The HLT algorithm analyses the complete detector data and performs track reconstruction with almost final accuracy. The definite event selection is a combination of confirming the previous L1 decision and selecting cuts dedicated to specific final states. An output rate of 200 Hz is expected requiring a data storage rate of 20 MB/s.

In the LHCb environment, the *front-end* system is defined as the processing and buffering of all detector signals until they are delivered to the *data acquisition* system. The DAQ system in contrast is defined as the physical implementation of the L1 trigger and the High Level trigger made as a shared CPU farm. The timing control of the complete front-end system and the delivery of the two trigger decisions are performed by the global Readout Supervisor (RS) over the TTC system using optical fibres. Control and monitoring of all parameters in the front-end system is performed via the Experiment Control System (ECS). Figure 1.3 shows the block diagram of the LHCb front-end electronics and its interface to trigger, DAQ and experiment (or detector) control system.

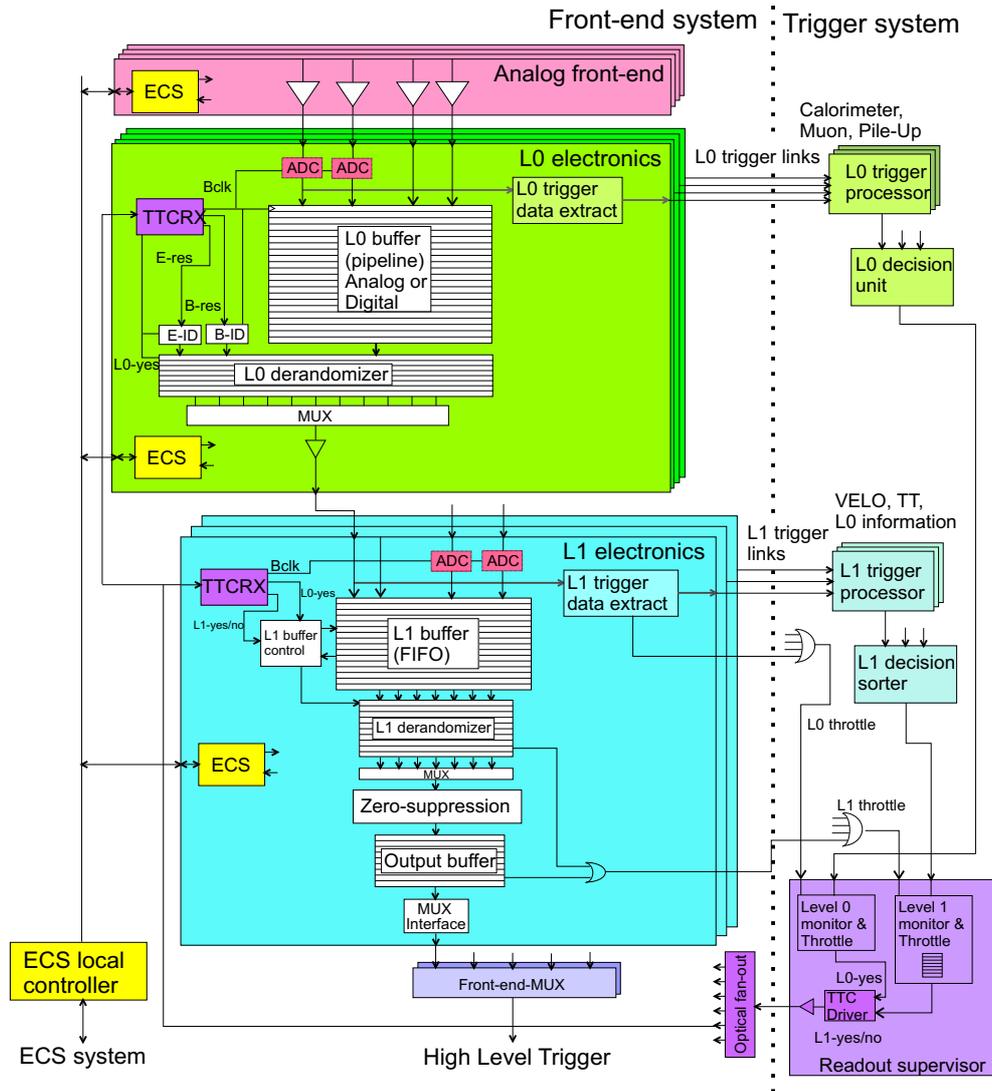


Figure 1.3: Block diagram of front-end electronics and its interface to Trigger, DAQ and Detector Control System. [Chr03a]

1.3 The Outer Tracker Subsystem

The Outer Tracker detector is part of the LHCb tracking system. Its 55,000 channels cover the LHCb acceptance up to 300 mrad in the bending plane and 250 mrad in the non-bending plane except for the cross-shaped area around the beam pipe that is covered by the inner tracker. The Outer Tracker modules consist of straw tube drift cells with a drift coordinate resolution of 200 μm . The following sections describe the layout of the Outer Tracker modules and give a survey of the components of the Outer Tracker readout electronics.

1.3.1 Outer Tracker Detector

The Outer Tracker detector is placed between the LHCb magnet and the RICH2 detector. The three Outer Tracker stations approximately measure 5 m \times 6 m (height \times width). They are modularly composed of drift chamber modules with maximum dimensions of 500 cm \times 34 cm \times 3.1 cm. The varying module dimensions originate from the geometry of the Inner

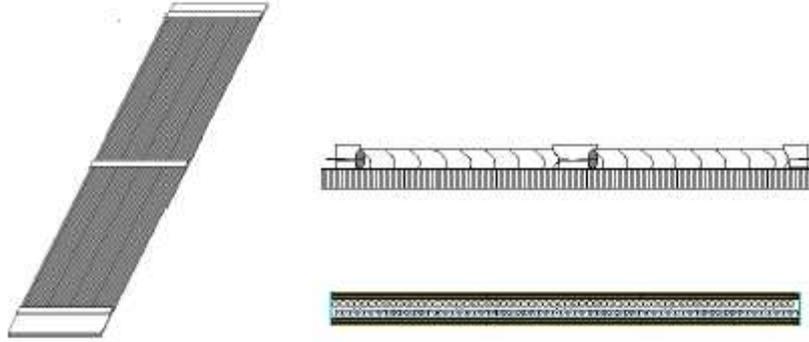


Figure 1.4: Schematic view of a straw tube module (not to scale). *Left:* 2×64 straw tubes (mono-layer) of one detector module. *Top right:* Side view of a detector module mono-layer. Two 2.4 m tubes cover the module height. *Down right:* Transverse section of a detector module. Two mono-layers form the 34 cm wide module.

Tracker and the fact that the Outer Tracker is vertically split in two halves that can be retracted from the beam pipe respectively from the Inner Tracker.

Each drift chamber module houses two layers of straw tubes that are glued to the support material. The straws (64 tubes per layer, see figure 1.4) are 5 mm in diameter and 2.4 m long. That is, the module length is covered with always two straw tubes that connect to the readout at the far end with respect to the beam pipe. The anode wire of the straw tube is a gold covered tungsten conductor of $25 \mu\text{m}$ cross section dimension. The resulting anode wire pitch within one straw tube layer is 5.25 mm. The cathode of the drift chamber consists of three materials: conductive Kapton (resistivity: $60 \text{ k}\Omega/\text{m}$) as inner layer followed by a layer of non-conductive Kapton to ensure gas tightness and an outside shielding layer of aluminium. Ar/CO₂ (70:30 percent by volume) will be used as counting gas. At an operating voltage of 1500 V, the gas gain is approximately 35,000 and the maximum drift time is about 44 ns [Ber05].

The three Outer Tracker stations each consist of four layers of drift chamber modules (see figure 1.5). The outer two module layers per stations are installed vertically, whereas the inner two layers are tilted by $+5^\circ$ and -5° with respect to the y-axis. The stereo layers allow the extraction of two particle coordinates per tracking station.

1.3.2 Outer Tracker Readout Electronics

An ionizing particle that passes through one gas-filled Outer Tracker straw tube generates primary electron-ion pairs that drift apart to the anode and cathode of the chamber due to its radial electric field. Multiplication processes increase the amount of free charge in the gas and while the electrons are collected on the anode, the remaining ions slowly move towards the cathode. The motion of all charges in the electric field causes a capacitively induced voltage signal that is digitised with the ASDblr discriminator chip that additionally cancels the slow ion signal tail. The drift time of the ionisation clusters is measured with the OTIS TDC. That is, the TDC chip measures the time alignment of the digitised straw tube pulse with respect to the bunch crossing clock. The digitised drift times are temporarily stored in the L0 buffer that is also included in the OTIS chip. On a positive L0 trigger decision, the digitised data is transmitted to the Level-1 buffer boards, which are the front-end of the common readout system. Figure 1.6 shows the different components the Outer Tracker

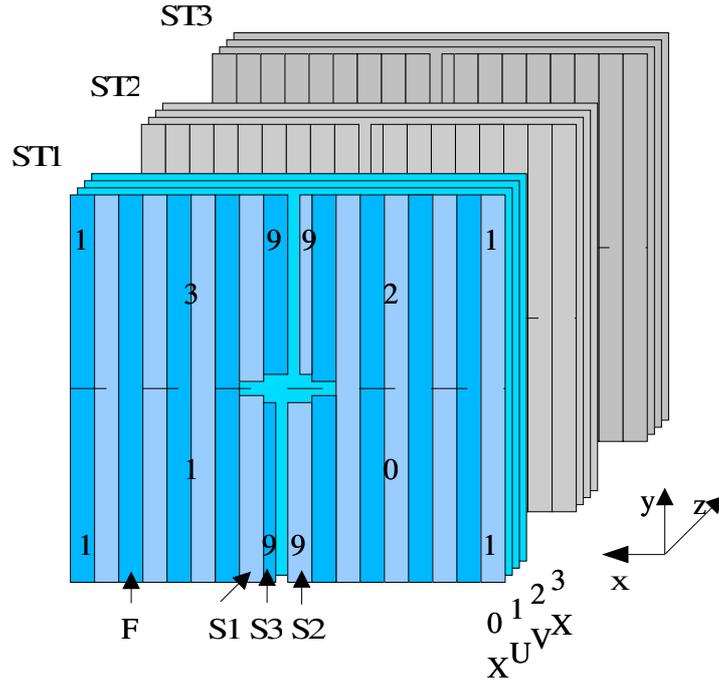


Figure 1.5: Schematic view of the three stations of the outer tracker detector. The modules within one station are vertically aligned (X) or tilted by $+5^\circ$ (U) or -5° (V) with respect to the y-axis.

front-end electronics consists of (excluding the power regulators that supply the low voltage). The on-detector components are:

ASDblr Chip The ASDblr ASIC [Bev94, Bev96] is an eight-channel amplifier-shaper-discriminator chip with baseline restoration designed for the readout of the ATLAS Transition Radiation Tracker (TRT). It is implemented in a radiation tolerant $0.8\mu\text{m}$ BiCMOS technology (DMILL) and typically consumes 40mW per channel ($\pm 3\text{V}$ power supply). The ASD chip generates a differential output signal for any input signal above the externally set threshold. Two $3.9\text{k}\Omega$ pull-up resistors and one $120\text{k}\Omega$ termination resistor interface the open-collector outputs of one ASD channel to the LVDS input of the OTIS chip [Slu03]. Always 32 channels from four ASDblr chips connect to one OTIS TDC.

OTIS Chip The OTIS chip provides the drift time measurement for the Outer Tracker detector. The 32 channel TDC operates synchronous to the 40MHz bunch crossing clock. It provides intermediate data storage in the L0 pipeline until a positive L0 trigger decision arrives. The chip then transfers the corresponding event data to the following GOL serialiser chip. The OTIS chip is able to cope with the 1.1MHz LHCb L0 trigger rate and the output interfaces from always four OTIS TDCs (8 bit differential CMOS outputs each) connect to one GOL chip. The OTIS TDC receives its clock and other control signals from the ECS and the RS. Each OTIS chip provides the threshold voltages for the four ASD chips that connect to the TDC.

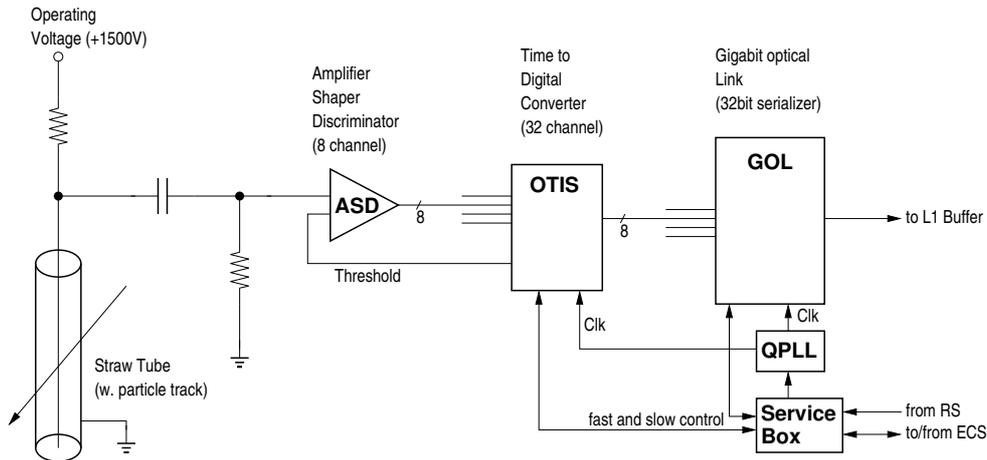


Figure 1.6: Schematic of the Outer Tracker front-end electronics. The passage of an ionizing particle results in a straw tube pulse that is digitised with the ASDblr chip. The drift time measuring OTIS chip stores the data in the L0 pipeline until a positive L0 trigger decision arrives. The drift time data is then passed to the GOL chip that optically transmits the triggered data to the L1 buffer board.

GOL Chip The GOL chip [Mor05] serializes the TDC data and outputs the data to an optical link. Its input interface is 32 bit wide what allows to connect always four TDC chips to one GOL chip. The serializer chip uses the 8 bit/10 bit line-coding scheme such that either Gbit Ethernet or Fibre Channel receivers can be used at the off-detector L1 buffer boards. The resulting data rate is 1.6 Gbit/s. The GOL chip receives its clock and other control signals from the ECS and the RS. The QPLL chip is used to stabilize the received clock signal from the TTCrx chip.

Service Box The Service Box is the interface between the Outer Tracker front-end electronics and the LHCb TFC and ECS systems. It receives, decodes (TTCrx chip) and distributes the optically transmitted timing and fast control signals from the readout supervisor. These signals include the LHC system clock, L0 and L1 trigger decisions and reset signals. The data transfer to and from the ECS is controlled by the SPECS slave chip [Bre03]. It provides the slow control signals for chip setup or temperature control.

1.4 Requirements to the Outer Tracker Readout Chip

The readout systems of the different LHCb sub-detectors have to cope with the demands of the detector environment and they have to be compatible with the general LHCb trigger and data acquisition system.

The readout of the Outer Tracker detector for example requires time digitization. But only the general purpose TDC chip *HPTDC* [Chr04a] was available for this task. However the HPTDC chip does not optimal fit for the readout of the Outer Tracker. This is because of its data driven architecture: the state of the chip depends on the detector occupancy and hence there is always the risk of buffer overflows in the HPTDC. Furthermore the HPTDC is not radiation hard so it cannot be placed directly on-detector. Therefore it has been decided to develop a dedicated TDC chip (OTIS) that fulfils the demands of the Outer Tracker and the LHCb DAQ scheme. Parallel to its development, the *B-Timizer* [Zwa01], a fall-back solution that is based on the HPTDC ASIC, has been developed and tested. The B-Timizer

decreases the risk of buffer overflow errors by only using half of the TDC channels for high occupancy detector areas. This doubles the buffer space for the connected channels at the cost of an increasing readout link count. The differential output signals from the ASDblr chip would have been transported to the off detector placed B-Timizer by means of twisted pair cables.

The following sections summarize the key features of the Outer Tracker detector and the LHCb data acquisition system that the OTIS based readout architecture at large or the OTIS TDC chip in particular has to cope with. Important figures are summarized in table 1.3.

Outer Tracker Features and Requirements	
Counting Gas	Ar/CO ₂ (70:30)
Operating Voltage	1550 V
Max. Drift Time	50 ns
Temperature Range	10 ... 70°C
Max. Occupancy	10%
Radiation Dose (10 y)	≤ 10 krad (≤ 1 Mrad) ⁴
ASDblr Dead Time	> 25 ns
TDC Resolution	< 1 ns
Data Acquisition Requirements	
Clock driven design	—
Bunch Crossing Clock	40.08 MHz
L0 Trigger Latency	160 Clock Cycles
Max. L0 Trigger Rate	1.1 MHz
Consecutive L0 Trigger	Max. 16
L0 Gap	None
Samples per L0 Trigger	1, more if required
L0 Derandomizer Buffer Depth	16 Events
Derandomizer Readout Time	Max. 900 ns

Table 1.3: Features and key parameters of the Outer Tracker detector and the data acquisition system.

1.4.1 Demands given by the Detector Environment

The geometry of the Outer Tracker straw tubes (5 mm diameter, 2.5 m length) and the Ar/CO₂ counting gas result in drift times of around 50 ns. This requires that the OTIS chip is able to record drift times that exceed its basic measurement range (25 ns as defined by the 40 MHz interaction rate) by the factor two or three. The data recording should be independent from the detector channel occupancy which is expected to be approximately 7% [Ber05].

At the foreseen place of installation at the upper and lower edges of the Outer Tracker modules, the expected radiation dose for an operation of LHCb of ten years is about 10 krad. Initially, the LHCb Technical Proposal [TP98] and the Outer Tracker Technical Design Report [TDR6] both foresaw two Outer Tracker stations within the LHCb magnet. The radiation levels at these stations would have been about 1 Mrad. In the meantime, the optimised

⁴This figure represents the initial design specification including the high radiation levels for the meanwhile skipped Outer Tracker stations within the magnet (see section 1.4.1).

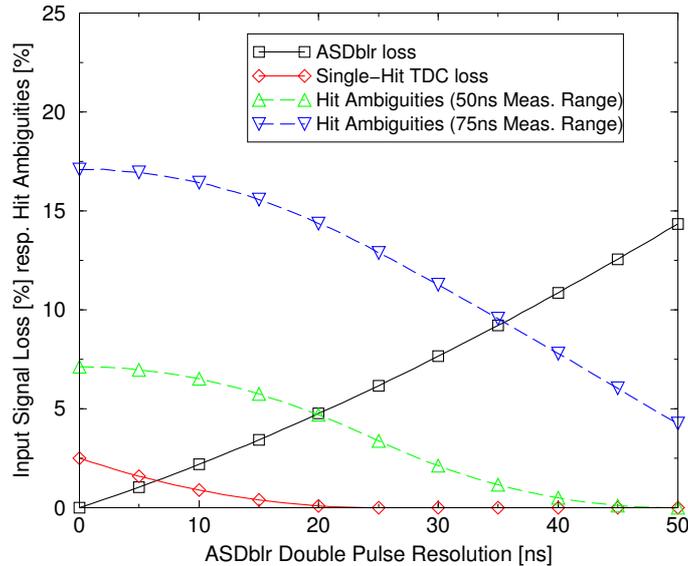


Figure 1.7: Simulation of the detector signal loss for varying ASDblr double pulse resolution (detector occupancy: 10%; max. drift times: 50 ns). The contributions of ASDblr and TDC (solid lines) to the dead time are independent from the measurement range. The number of hit ambiguities (dashed lines) rises with the measurement range (combination of two or three basic measurement ranges).

detector design [TDR9] skipped the magnet stations in order to reduce the material budget of the detector. The remaining three stations (see chapter 1.1) only have to withstand radiation levels of about 10 krad. Apart from total dose effects, Single Event Upset (SEU) may be of concern.

The input and output interfaces of the OTIS chip are defined by ASDblr and GOL chips. The minimum double pulse resolution of 25 ns of the discriminator chip [Dre01] allows to use a single-hit respectively a first-hit TDC implementation. That is the TDC only measures the arrival time of the first input signal per channel and measurement period. Both, the ASDblr double pulse resolution and the single-hit TDC scheme contribute to the combined dead time of the front-end electronics because of pile-up (additional hits from one or more pp interactions occurring in the same bunch collision as the $b\bar{b}$ event) and spill-over (additional hits from neighbouring bunch crossings). The spill-over of detector signals from neighbouring bunch crossings introduces hit ambiguities that possibly complicate the track reconstruction.

Figure 1.7 shows the simulations of all three effects for varying ASDblr double pulse resolution and two measurement ranges (50 and 75 ns). The simulation assumes equally distributed drift times of up to 50 ns, a detector channel occupancy of 10% and ASDblr double pulse resolutions between 0 and 50 ns. The diagram shows the percentage of lost detector signals (solid lines) due to the ASDblr double pulse resolution and the single-hit TDC scheme. The total dead time is completely determined by the ASDblr dead time. The contribution of the single-hit TDC scheme is only visible for ASDblr double pulse resolutions that are below the limit of the discriminator chip. The diagram additionally shows the percentage of hit ambiguities (dashed lines) that must be solved during track reconstruction. The maximum allowed drift time in this simulation is set to 50 ns and so the number of hit ambiguities rises when selecting a 75 ns measurement range instead of a 50 ns range.

Other general conditions are given from the installation of the OTIS chip in the Outer Tracker front-end electronics box. For example, the modular design of the front-end box foresees a dedicated PCB for the OTIS TDC. This facilitates replacement if service becomes necessary and allows to use chip-on-board technology. The power dissipation per front-end box will be about 25 W [Slu02]. As it is not possible to release the heat into the experiment hall, it is foreseen to mount the main cooling plate of the electronics box against a water-cooled frame. The expected temperature at the OTIS chip will be approximately 50°C.

1.4.2 Demands given by the LHCb DAQ & Trigger Scheme

The integration of the OTIS chip into the LHCb Outer Tracker front-end electronics requires occupancy independent operation synchronous to the 40 MHz bunch crossing clock. The digitised drift times must be stored in the level-0 trigger pipeline buffer until the level-0 trigger decision accepts or rejects the data from a given bunch crossing. The time until a trigger decision arrives is fixed to 4 μ s or 160 bunch crossing cycles. Accepted data must be extracted from the pipeline buffer and temporarily stored in the L0 derandomizer buffer, waiting to be transferred to the subsequent L1 front-end electronics.

The expected level-0 trigger rate is 1.1 MHz. This relatively high trigger rate determines the readout speed of the derandomizer buffer which is 900 ns. The front-end chips must be able to cope with sequences of up to 16 positive L0 trigger decisions. This leads to a derandomizer buffer size of 16 events.

The L0 front-end chips must add sufficient status and identification tags to the recorded data samples to facilitate system monitoring and event reconstruction. The identification tags not only display the geometrical origin of the event fragment (chip identification number) but also allow to set up and maintain correct system synchronisation (bunch crossing and event identification numbers).

2 Chipdesign

The OTIS chip is fabricated in a commercial 0.25 μm CMOS process which has been proven by the RD49 collaboration [Ada00, RD49] to be radiation hard for up to 30 Mrad total dose. The expected radiation levels and particle fluxes (see table 2.1) within the LHCb environment require the use of such a technology and the application of radiation tolerant layout techniques.

	Total Ionising Dose (10 years)	Max. Particle Flux (Hadrons > 20 MeV, 10 years)
LHCb Detector	$5.8 \cdot 10^6$ rad(Si)	$1.4 \cdot 10^{14}$ cm^{-2}
Outer Tracker	$6.6 \cdot 10^3$ rad(Si)	$8.7 \cdot 10^{10}$ cm^{-2}

Table 2.1: Maximum expected total ionising dose and particle flux (hadrons > 20 MeV) for ten years of operation in the LHCb detector respectively in the Outer Tracker sub-detector. [BG04, Tal00]

The following sections summarise the relevant radiation effects in MOS devices and introduce radiation hard design techniques. The radiation tolerant digital library and the corresponding (digital) design flow is presented.

2.1 Radiation Effects

Radiation effects on electronics can be divided into three different categories according to their effect on the electronic components [Dre89, Fac99]:

- **Total Ionising Dose Effects** Total ionising dose (TID) effects are gradual effects that will accumulate during the whole lifetime of LHC. Charged particles (electrons and hadrons) and neutral particles (neutrons and photons) can directly and indirectly deposit energy along their track and create electron-hole pairs in the silicon dioxide¹.

The probability of the recombination of the electron-hole pairs is lowered by the presence of an electric field in the oxide, as both start to drift in the field. Because of their high mobility, the electrons can easily leave the oxide, the holes instead can be trapped and build up charge in the oxide. This will lead to threshold voltage shift (charge build-up in the gate oxide), to the formation of leakage current paths (charge build-up in the lateral oxide) or to the creation of defects at the interface between silicon and silicon dioxide that also influence the threshold voltage.

- **Displacement Damage** Hadrons can cause the displacement of atoms in the silicon lattice of active devices. The displacement damage reduces the minority carrier lifetime in the silicon substrate and thereby affects the function of the bulk device. MOS transistors in contrast are *surface devices*. Their active structures only penetrate the silicon bulk to a typical depth of 300 nm. CMOS integrated circuits are therefore not

¹The pair creation energy in SiO_2 is 17 ± 1 eV

considered to suffer degradation by displacement damage. Optical devices (e.g. lasers and LEDs) may be very sensitive to this effect.

- **Single Event Effects** Single event effects (SEE) are localised single-particle induced radiation effects that can either cause transient or static signal changes (e.g. in combinational logic respectively in memory devices) or they can permanently destroy the affected circuits.

Electron-hole pairs that are generated along the track of an ionising particle near a pn-junction (such as drain/bulk) will be separated by its electric field. The passage of an ionising particle induces a current spike that may locally disturb the function of electronic circuits. For the deep-submicron technology used for the OTIS chip only two effects are of importance: Single Event Upset (SEU) and Single Event Latch-up (SEL).

An SEU normally refers to the bit flip in memory circuits such as RAMs, latches and flip-flops. The deposited charge is sufficient to flip the value of the storage element.

SEL: the parasitic bipolar transistors within CMOS circuits can be triggered by the local deposition of charge to generate a kind of short circuit between the power supply and ground. The large currents caused by this short-circuit effect can permanently damage the components of the circuit.

2.2 Radiation Hard VLSI Circuit Design

2.2.1 Process Technology

The hole trapping that is responsible for the threshold voltage shift (charge build-up) depends on the thickness of the oxide. A decrease in the thickness of the gate oxide increases the probability for electrons to tunnel into the oxide and recombine with the trapped holes, thus removing the threshold voltage shift ΔV_{th} . This effect results in an increased radiation hardness of processes with a gate oxide thickness below 10 nm, as shown in figure 2.1. The gate oxide of the process that has been chosen for the OTIS chip is $d_{ox} = 6.2$ nm. This process is therefore intrinsically radiation hard.

2.2.2 Layout Techniques

Enclosed Gate Structures

The charge build-up in the gate oxide can be decreased by scaling down the device dimensions, but trapped charges in the lateral oxide can still lead to leakage currents between source and drain. MOS field effect transistors with an enclosed gate structure (also called *edgeless* transistors) avoid parasitic paths between source and drain. Figure 2.2 shows the principle drawing of a rectangular and an enclosed gate structure.

The width W of such an enclosed gate can be calculated from the effective aspect ratio $(W/L)_{eff}$ of the transistor [Fac98] which is given by

$$\left(\frac{W}{L}\right)_{eff} = 4 \cdot \underbrace{\frac{2\alpha}{\ln \frac{d'}{d'-2\alpha L}}}_1 + 2K \cdot \underbrace{\frac{1-\alpha}{1.13 \cdot \ln \frac{1}{\alpha}}}_2 + 3 \cdot \underbrace{\frac{d-d'}{L}}_3, \quad (2.1)$$

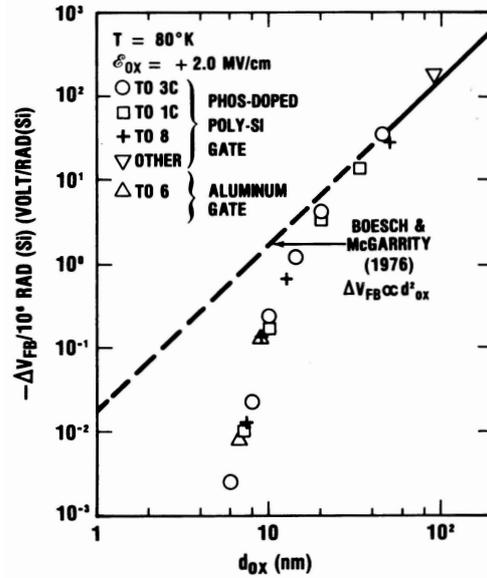


Figure 2.1: ΔV_{FB} (i.e. ΔV_{TH}) per unit dose for different thicknesses of the gate oxide d_{ox} . The dashed line represents the d_{ox}^2 dependency valid for thick oxides [Dre89].

where L is the (drawn) length of the transistor, d and d' are the sections as depicted in fig. 2.2 and α and K are fitting parameters:

$$\alpha = 0.05 \quad K = \begin{cases} 3.5 & \text{for } L \leq 0.5 \mu\text{m} \\ 4.0 & \text{for } L > 0.5 \mu\text{m}. \end{cases}$$

The three terms represent the linear part between two corners (1), the triangular corner segment (2) and the rectangular region of the corner (3).

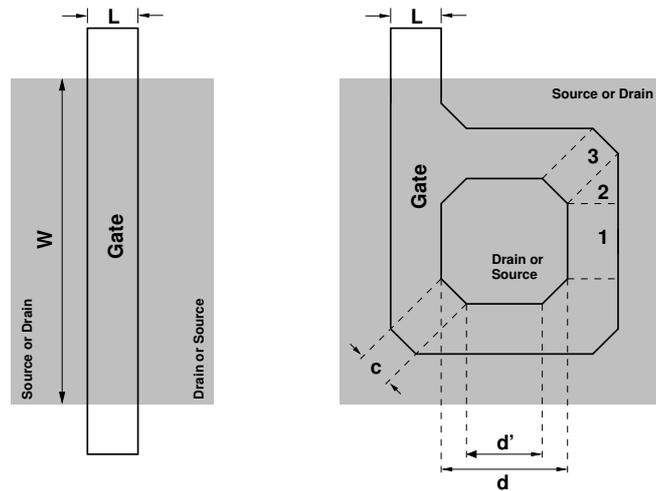


Figure 2.2: Principle Drawing of the geometry of a linear (left) and an enclosed (right) transistor.

The drawbacks of an enclosed transistor layout are the increase in area consumption and parasitic capacitances, the need for a special device modelling and the broken device symmetry (the outer region shows a larger gate-diffusion overlap capacitance).

Guard Rings

The possibility of single event latch-up in a radiation environment requires the consequent use of guard rings (low-impedance connection to the local substrate) around the MOS devices. The increased distance to other active devices and the reduced resistance from the substrate to the power supplies prevent the creation and the triggering of the parasitic bipolar transistors what would otherwise short-circuit power and ground.

2.2.3 Redundancy

Single event upsets cannot be avoided on the device level. But the effects of this localised phenomenon can be reduced by using three storage devices to represent one digital bit. The state of the represented bit is defined by majority voting of the states of the corresponding devices.

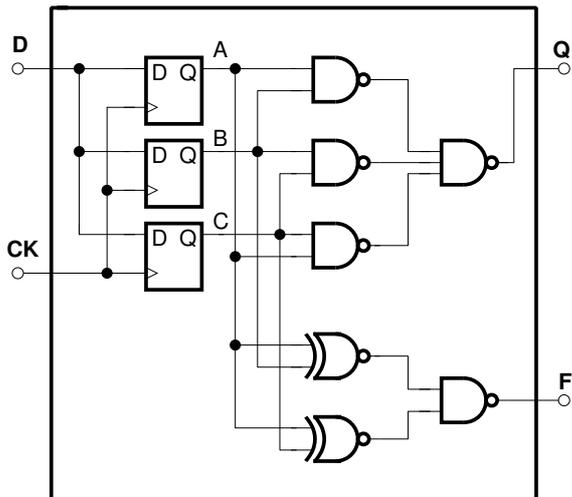


Figure 2.3: Triple redundant flip-flop with majority voting for the output (Q) and state-change indicator (F). [Bau02]

A	B	C	Q	F
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Table 2.2: Truth table of the triple redundant flip-flop. A, B, C represent the output nodes of the internally used standard flip-flops.

Figure 2.3 shows the schematic view of the triple redundant flip-flop. It consists of three single flip-flops and a combinational circuit that builds the majority vote of all three bits and flags their inequality. Table 2.2 shows the corresponding truth table.

The expected SEU rate calculates from the SEU cross section of the storage device and from the flux of particles that dominate the single event effects (hadrons > 20 MeV in case of LHC [Fac99]). The SEU cross section of a standard flip flop is $\sigma_{FF} < 1.7 \cdot 10^{-15} \text{ cm}^2$ [Chr03b]. Taking into account 1100 flip-flops in the control core of the OTIS chip and 10^7 seconds of data taking per year, then the maximum SEU rate in the digital control of the OTIS chip

calculates to

$$\begin{aligned}
 f_{\text{SEU}} &= 1100 \cdot \sigma_{FF} \cdot \phi_h \\
 &= 1100 \cdot 1.7 \cdot 10^{-15} \text{ cm}^2 \cdot \frac{8.7 \cdot 10^{10}}{10 \cdot 10^7} \cdot \frac{1}{\text{cm}^2 \text{ s}} \\
 &= 1.6 \cdot 10^{-9} \text{ Hz.}
 \end{aligned}$$

This is 0.3 single event upsets per day and all 2000 OTIS chips of the LHCb Outer Tracker. Because of the large area overhead of the triple redundant flip-flops, it has been decided not to use the threefold registers in the fast control core of the OTIS chip. Only the quasi-static flip-flops of the slow control core (I²C-interface, setup and configuration registers) are triple redundant.

2.2.4 Radiation Hard Digital Library & Design Flow

Standard Cell Library

A library of digital standard cells exists for the selected 0.25 μm process [Ada00, DST02]. This facilitates the design of digital circuits of significant size and complexity. The library consists of 30 core cells, 16 I/O pads and 6 power pads. The core cells include simple inverter, NAND and NOR gates but also multiplexers, latches and flip-flops. Radiation tolerant layout techniques have been employed on the cell layouts to achieve total dose hardness levels that are consistent with the LHC environment.

The standard cell library additionally contains the verilog simulation library files and the timing information library file (TLF). These are needed for the digital simulation and the logic synthesis.

Digital Design Flow

The main steps of the digital top-down design flow are:

- **Verilog RTL Model Creation** The register transfer level (RTL) models are an abstract description of the hardware. The behavioural models do not imply any particular gate-level implementations.
- **RTL Simulation** The RTL models are validated through simulation by means of a number of testbenches that are also written in Verilog. The timing information that is needed for simulation is included in the standard library and is based on an average gate load.
- **RTL Synthesis** The synthesis process generates a possible gate-level realisation (netlist) of the input RTL description that meets the user-defined constraints such as area or timing. The targeted logic gates belong to the standard cell library and the timing information is extracted from lookup tables that provide cell propagation delay and output signal slope based on the input signal slope and the output load (CMOS Non-linear Delay Model). The considered delays are at this step correct for the gates but only estimated for the interconnections.

The design compiler managed to create gate-level realisations of the OTIS control core for clock frequencies up to 55 MHz (the intended operation frequency will be 40 MHz). The longest reported timing path belongs to the output of the trigger FIFO-full flag.

- **Post-Synthesis Gate-Level Simulation** The testbenches used for the RTL model simulation can be reused for the gate-level simulator. The timing information from the synthesis step is back-annotated through a standard delay format (SDF) file that was created by the design compiler.
- **Standard Cell Place & Route** The place & route (P&R) step infers a geometric realisation (layout) of the gate-level design. Like the design compiler, the P&R tool extracts the gate delays and, in addition, it calculates the single net RC-delays based on the Wire-Load-Model (WLM) from the standard cell library. The SDF description now includes cell delay and interconnect delay. During signal routing or clock tree generation, the P&R step changes the input netlist because of buffer insertions.
- **Post-Layout Gate-Level Simulation** The Verilog gate-level netlist and the more accurate SDF data from the P&R step can be simulated with the existing testbenches. Scaling factors can be applied to the SDF description to account for possible process variations.
- **System-Level Integration** The layout description is integrated as block in the top level of the designed system and the extracted timing information is used in system-level simulations. Geometrical (design rules) and logical (matching of netlist and layout description) verification finalise the design flow.

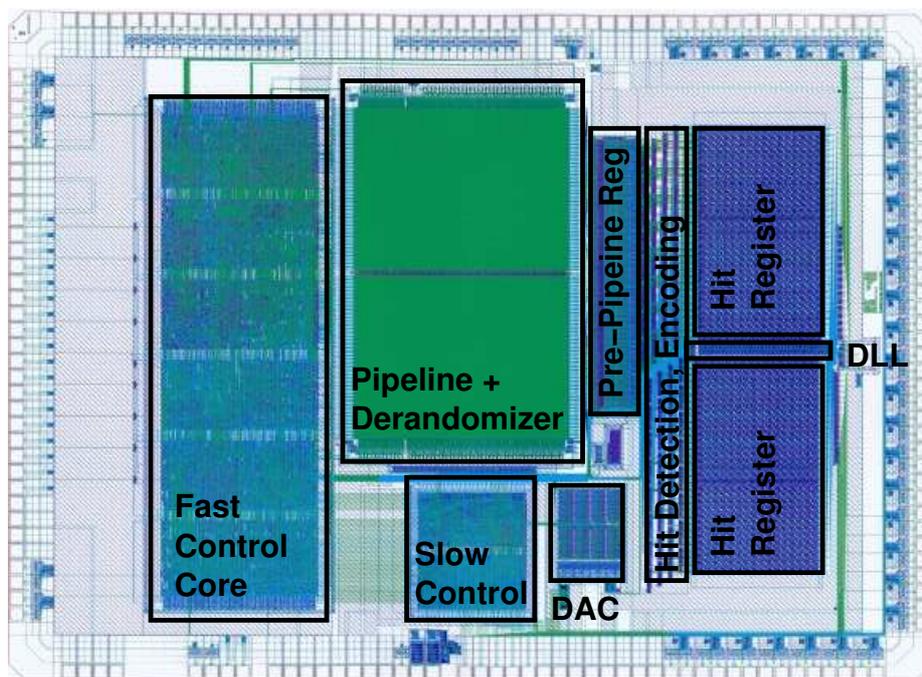


Figure 2.4: Layout view of the OTIS1.2 chip (7 mm × 5.1 mm). The major building blocks of the chip are labelled.

Figure 2.4 shows the layout view of the OTIS1.2 chip. Major building blocks such as the pipeline memory, the TDC core or the fast control unit are marked (see chapter 3 and 4). After system-level integration, the system-level simulation could demonstrate the correct interworking of all major chip constituents.

3 Chip Architecture

This chapter describes the OTIS¹ chip in its existing version OTIS1.2. The OTIS chip is an integrated 32 channel Time to Digital Converter (TDC) designed for the Large Hadron Collider beauty experiment (LHCb). More precisely, the chip is designed for the readout of the LHCb Outer Tracker (OT). The chip meets all specifications given by the experiment and is in its present state ready for mass production.

Section 3.1 introduces the basic functionality of the chip by means of the data flow through the TDC chip. At this level of abstraction *data* represents detector signals at the input interface as well as single drift time data derived from the input signals or the fully formatted data sets at the output interface. Sections 3.2 to 3.5 give in detail descriptions of the single components the OTIS chip is composed of. These are TDC core, pre-pipeline register, L0 pipeline plus derandomizer and digital control core.

3.1 Block Schematic

Figure 3.1 depicts the block diagram of the OTIS chip. The diagram shows all major components of the TDC chip plus their main interconnections. The following paragraphs describe these components and their basic functionality on the basis of the block diagram following the data path through the chip. More detailed descriptions of Delay Locked Loop (DLL), pipeline memory and control core follow after this introductory section.

Input Interface and Channel Mask Register At the input side, the OTIS chip receives 32 digitised detector channels from four ASDblr [Bev94, Bev96] discriminator chips. On the OTIS chip itself, every single channel can be disabled by setting the corresponding bit of the channel mask register. The possibility to disable channels will be used in case of unconnected inputs due to module geometry or in case of noisy detector channels. Apart from disabling single channels by means of the channel mask register, the threshold voltages of the ASDblr discriminator chips can be set to switch off groups of always eight detector channels at once.

Other input signal categories range from infrastructure (power supply, chip identification and programming interface) to timing and fast control signals (LHC bunch crossing clock, L0 reset and trigger signals).

TDC Core The TDC core combines those parts of the chip which are directly linked to the drift time measurement. These are the delay locked loop, the Hit Register (HR) and the drift time encoder.

The DLL is a chain of 32 voltage controlled delay elements consisting of two delay stages each. As the LHC clock signal propagates through the DLL, every delay stage retards the clock signal by the 390 ps nominal propagation time. The full length of the DLL results in a signal delay of 25 ns or one LHC clock cycle. A dynamic phase detector compares original clock and delayed clock signal. Upon their phase alignment, the DLL is speeded up or slowed down until both clock signals are in phase. This situation, called *lock state*, is mandatory for exact drift time measurement as it allows to derive 64 time reference signals from the

¹Outer Tracker Time Information System

taps that follow every delay stage. In the lock state, a drift time measurement can either be accomplished by storing the state of the DLL (i.e. the state of all time reference signals) at the time of an incoming detector signal or by using the DLL outputs to scan and latch the detector pulses. In both cases each detector channel requires 64 bits of storage capacity to hold the data that represents the drift time information. As it has been decided to scan and latch the incoming hit signals, this register is called Hit Register, and the drift times are extracted by encoding the position of the (first) 0-1 transition that is found in the sampled data. Additional to the drift time encoding, each channel encoder provides a 1-bit flag that indicates valid drift time data.

Pre-Pipeline Register Data from the drift time measurements of all 32 channels and status information is arranged in the pre-pipeline register. The pre-pipeline register acts as an input buffer for the L0 pipeline memory. Additionally, data gets linked to a bunch crossing identification number which provides an experiment-wide identification tag in order to ease event reconstruction.

The dimension of the pre-pipeline register is 3×240 bits. Thus it is able to store three independent sets of data. One of those is exclusively used for the data that is produced by the TDC core. The other two register banks serve as programmable and selectable data sources which are used in case of memory self-test or playback operation mode.

L0 Pipeline and Derandomizer Buffer While the L0 pipeline is used for intermediate data storage until a L0 trigger decision arrives, the derandomizer buffer is used to compensate fluctuations in the trigger rate.

Every clock cycle, a new data set must be stored to the L0 pipeline. Each data set, treated as a single data word, is 240 bits wide and consists of drift times, hit mask, status information and a bunch crossing identification number. In the LHCb experiment it takes exactly $4 \mu\text{s}$ or 160 clock cycles until a trigger decision arrives. Therefore the minimum length of the L0 pipeline is 160 words. During design phase it has been decided to add an additional safety margin of 4 words resulting in 164×240 bits of storage capacity in the L0 pipeline. A new data set overwrites old pipeline content if the L0 trigger latency (plus four extra clock cycles) expires without a trigger decision.

Upon an incoming trigger signal, the corresponding pipeline content gets transferred to the derandomizer buffer. In principle, each trigger signal causes one data set to be copied to the derandomizer. But as the TDC chip allows to extend the basic measurement range of 25 ns by combining two or three data sets, an arriving trigger signal can cause up to three copy operations. Thus the resulting number of data sets to be transferred to the derandomizer buffer depends on the programmable hit search depth (1, 2 or 3 BX) and the actual trigger sequence. The derandomizer buffer of the OTIS chip must account for events that consist of up to three data sets. The derandomizer buffer depth therefore exceeds the recommended size of 16 words [Chr01] by a factor of three. Its resulting dimension is 48×240 bits. Both, pipeline and derandomizer buffer are composed of dual ported SRAM cells. A precise description of their implementation follows in chapter 3.4.

Digital Control Core The digital control core of the OTIS chip provides the circuitry for memory and trigger management, data formatting and basic debugging features. It additionally includes the I²C programming interface for operation parameter setup and chip monitoring. The control circuit is subdivided into two parts as a consequence of the two clock domains they operate at: the fast control part which is run by the 40 MHz LHC clock signal and the slow control part which is driven by the 400 kHz I²C clock [Phi00] asyn-

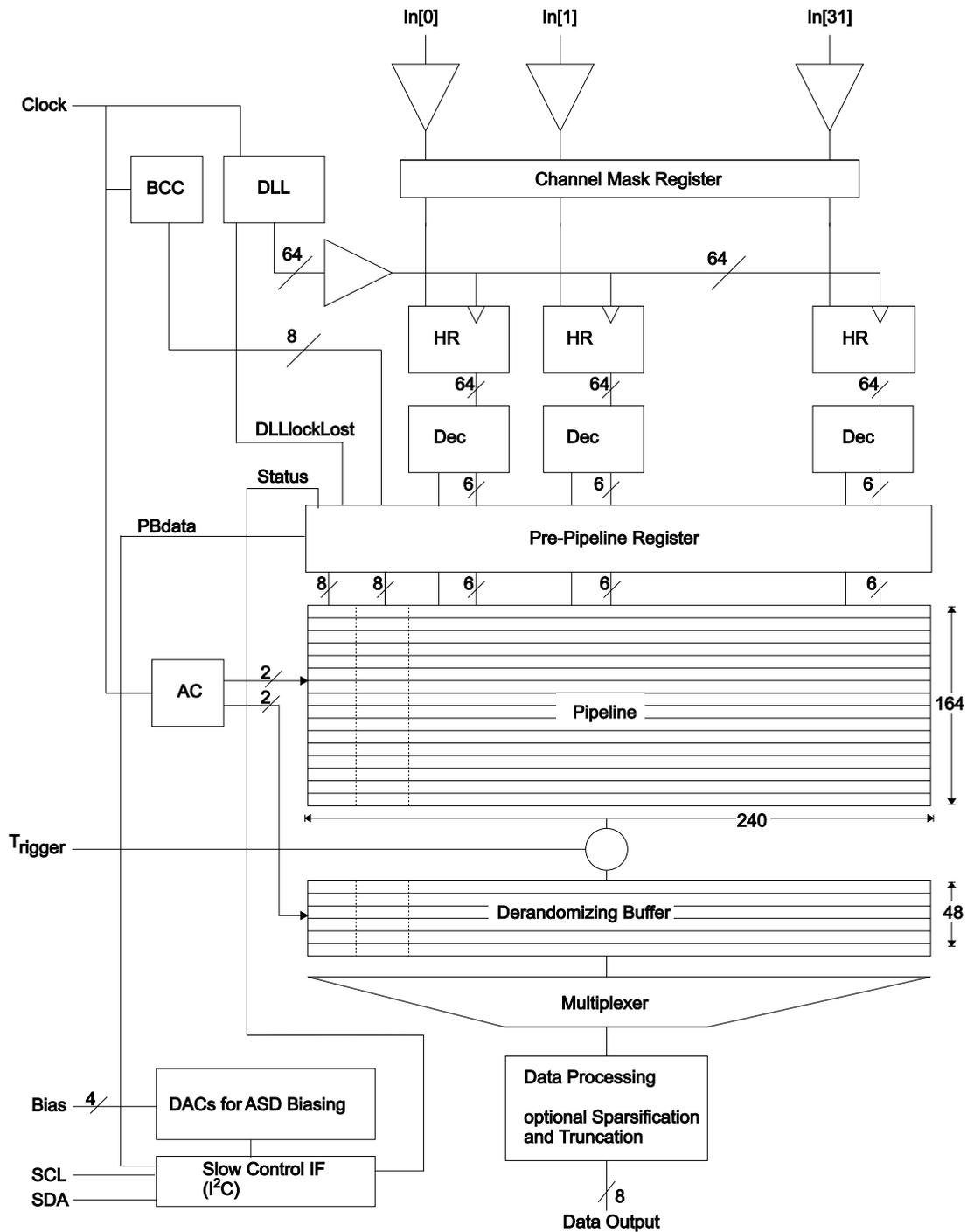


Figure 3.1: OTIS1.2 block diagram. Main data flow from input to output through TDC core (DLL, HR, decoder), pre-pipeline register, L0 pipeline plus derandomiser and data processing unit.

chronous to the LHC clock. Both parts are written in the Hardware Description Language (HDL) *Verilog* [Tho96], and while the fast control has been developed anew for the OTIS chip, the I²C programming interface of the slow control part has been taken from the Beetle [Bau02, LÖc05] chip and adapted to the OTIS needs. The slow control core provides an I²C interface for write and read access to all 66 setup and status registers of the OTIS chip.

Additionally, the I²C interface is used for slow data output. This debugging feature only uses the serial interface for triggered data output and thus introduces a second readout path that is independent from optical link and DAQ.

The fast control unit consistently integrates into the LHCb data acquisition and trigger scheme. It operates clock driven and clock synchronous to the LHC bunch crossing signal and follows all specifications given by the experiment. The control units main tasks are memory and trigger management as well as data processing and data output upon any arriving L0 trigger signal. Two different data formats are available for triggered data output. They differ in the way how each channels hit information is encoded. In the *plain hit mask* data format, the hit mask information is separated from the corresponding drift time data. This entails an event length that is dependent from the detector occupancy but allows to transfer up to three drift times per channel and trigger (given a selected search depth of 3 BX). The other data format, the *encoded hit mask* mode, adds two additional bits to each channels drift time data. This 2-bit extension is necessary to encode drift times that exceed the basic measurement range. The encoded hit mask data format only allows to transmit one hit per channel and trigger but it guarantees a fixed event length and chip operation that is independent from the detector occupancy.

Besides basic functionality, the control core also provides a memory self-test for chip level debugging and a playback operation mode that is suitable for system level debugging. Both debug modes make use of the additional pre-pipeline register banks to insert the test data into the L0 pipeline.

3.2 TDC Core

In the context of the LHCb experiment and the Outer Tracker, the term *drift time* always refers to the period of time it takes from single bunch crossing interactions until resulting detector signals. Each channel hit is assigned a digitisation time which is the sum of the time-of-flight of the traversing particle, the drift time in the detector tube and the signal propagation time towards preamplifier and TDC chip. Apart from the detector geometry, the drift time mainly depends on the operating gas. The intended drift gas mixture (Ar/CO₂) will lead to maximum drift times of about 50 ns which is twice as long as the LHCb bunch crossing interval or the basic measurement range of the TDC chip. The digital control core of the OTIS chip allows to combine up to three data sets and it thus introduces a full scale operating range that is three times the basic measurement range. The design goal, based on the interaction rate of 40 MHz, is to measure drift times with a resolution better than 1 ns. At the same time it is required that the drift time measurement, i.e. the TDC chip, does not introduce dead times during operation.

The TDC core, as an essential part of the OTIS chip, provides the circuitry for the drift time measurement. Its basic principle is to derive 64 time reference signals from the LHC bunch crossing clock. These reference signals are then used to scan and latch the discriminated detector signals into the hit register for drift time extraction. Depending on the content of the hit register, the following edge finder and encoder circuits deduce the drift times and the binary hit information. Dividing the bunch crossing interval into 64 segments is adequate for the desired resolution:

$$\frac{25 \text{ ns}}{2^6} = 0.39 \text{ ns} \quad (3.1)$$

and leads to 6 bit wide drift time codes for the basic measurement range of the TDC respectively to 8 bit codes after combination to the full scale range of three bunch crossing intervals within the digital core.

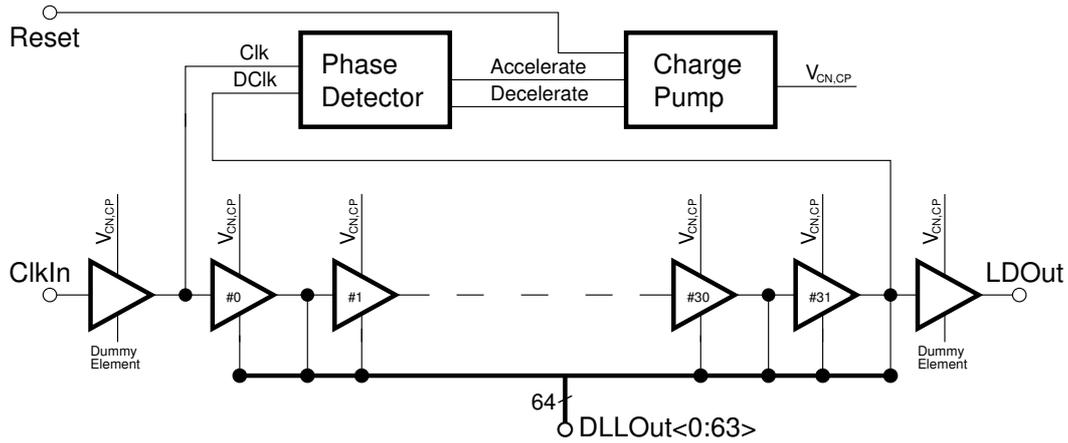


Figure 3.2: Block diagram of the DLL. The phase detector measures the phase difference between the reference clock and its delayed version and accordingly controls the delay elements propagation time by means of the charge pump.

3.2.1 Delay Locked Loop

The OTIS chip uses a voltage controlled delay chain or Delay Locked Loop (DLL) as central time reference generator for all 32 channels. Figure 3.2 shows how the delay chain, the phase detector and the charge pump form the closed-loop feedback system which has been developed for the OTIS TDC. In this implementation, the reference clock signal `Clk` propagates through a chain of voltage controlled delay elements, each contributing 2×390 ps nominal signal delay. In total, the clock signal gets delayed by approximately 25 ns or one clock cycle. Both signals, `Clk` and `DClk` are then fed into the phase detector which is the sensor of the control loop. It measures the phase difference between reference signal and delayed signal. The phase detector provides a sequence of `Accelerate` and `Decelerate` pulses, both with varying pulse widths, depending on the phase difference between `Clk` and `DClk`. The third component of the control loop, the actuator, is the charge pump which changes its filter capacitor voltage according to the outputs of the phase detector. Voltage changes at the filter capacitor result in decreasing or increasing propagation times of the delay elements, thus adjusting the frequency of the DLL. The existing control loop is designed for an operation frequency of 40 MHz and a chip temperature of 45 °C. But the control voltages dynamic range of about 1 V translates into possible operating frequencies or temperatures ranging from approximately 25-60 MHz or 20-70 °C respectively.

Generally speaking, DLLs produce a desired phase relationship between two signals (`Clk` and `DClk` in case of the OTIS TDC). The origin of those two signals can be used to set up two categories of DLL designs [Lee03]: Type I designs produce a phase relationship between a reference signal and a delayed version of this reference. For the OTIS chip, which is a Type I design, this reference signal is the LHC bunch crossing clock. Type II designs in contrast compare the reference signal with the delayed version of a second uncorrelated clock signal. While Type I DLLs are often used in clock generator and clock deskewing circuits, the Type II architectures are mainly used in clock recovery circuits. When the desired stable relationship between reference signal and delayed reference is established, the DLL is said to be in *lock state*. Accordingly the term *lock time* numeralises the time from applying clock signals to the TDC until the DLL reaches its lock state.

The following sections describe the different components of the DLL (delay element, phase detector and charge pump) and present measurement results concerning the locking of the OTIS DLL.

Delay Element

The delay elements of the OTIS DLL are composed of pairs of current starved inverters. The implementation of a single delay element is shown in figure 3.3. In total, the TDC core uses 34 such delay elements, but only the inner 32 stages add to the DLL length. The additional two elements at the beginning and at the end of the delay chain are used to adjust the capacitive load of elements no. 0 and 31. The output of the second dummy delay element (`LastDummyOut`) is available to the outside of the chip. It can be used to monitor the frequency of the DLL.

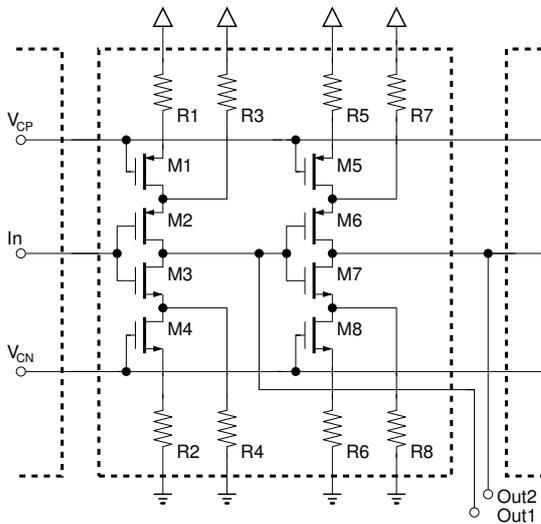


Figure 3.3: Schematic of a single delay element. Each delay stage, a pair of two current starved inverters, adds 780 ps delay nominal. The DLL uses both inverter taps.

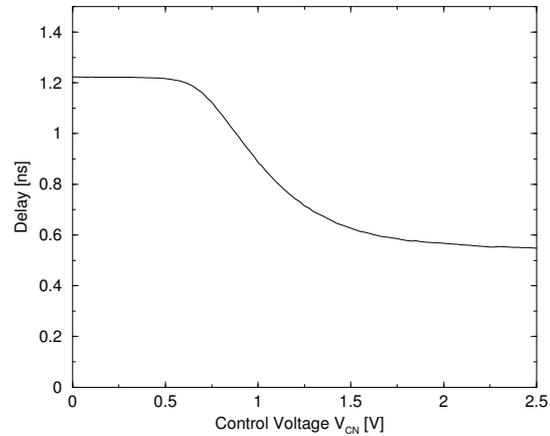


Figure 3.4: Simulation of a single delay element: signal propagation time versus V_{CN} .

The transition time of each inverter is controlled by the bias voltages V_{CP} and V_{CN} by affecting the amount of current that is allowed to pass through the inverter. Both control voltages are generated in the charge pump (see figure 3.6 and explanation below). The achievable delay range of the DLL depends on the number of delay elements and on the minimum and maximum delays of each element. In order to prevent the DLL from locking to multiples of the reference frequency, the maximum switching current through the inverters is limited by the resistors R1, R2, R5 and R6. In contrast, too small locking frequencies are prevented by providing a minimum switching current over resistors R3, R4, R7 and R8. The fact that the taps with negative polarity (`Out1`) are used as time reference signals too demands for some additional circuitry which is not shown in figures 3.2 or 3.3.

Figure 3.4 depicts simulation results showing how, under nominal conditions, the combined delay of two inverter stages depends on the control voltage V_{CN} . It is clearly visible that the resistors mentioned beforehand keep the delay elements propagation times above 0.5 ns and below 1.3 ns. This limits the possible lock frequencies of the DLL to 24.0-62.5 MHz, thus preventing locking to multiples of 40 MHz.

Phase Detector

The phase detector implementation is shown in figure 3.5. It follows standard phase detector designs [Wes94, Bak98], and as such it translates the phase difference between `Clk` and `DClk` into pulse widths of its two control outputs² `Accelerate` and `Decelerate`.

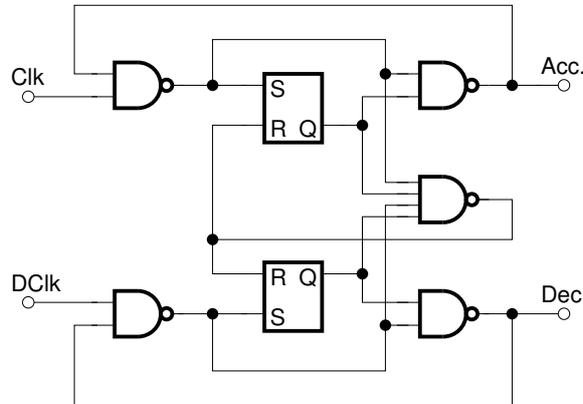


Figure 3.5: Schematic showing the implementation of the dynamic phase detector that translates phase differences at its input to pulse width variations at its output.

The basic functional principle of the phase detector is as follows: Any single falling edge of `Clk` or `DClk` sets the corresponding output `Accelerate` or `Decelerate` to 0 (assuming the two outputs of the two SR-flip-flops were already set to 1). As soon as both clock inputs are zero, the feedback of the output of the fourfold NAND gate reverses the two flip-flop outputs and causes `Accelerate` = `Decelerate` = 1. That is, both falling input clock edges activate the corresponding output signals, and additionally, the time difference between leading and trailing input clock edge determines the pulse width of the output signal that belongs to the leading input signal edge.

For example, a leading falling edge of `Clk` activates the `Accelerate` output. This output is active until the following falling edge of `DClk` triggers the reset feedback. In this example, a lagging `DClk` causes the DLL to be speeded up. A lagging of `Clk` would slow down the DLL.

After the flip-flops have been reset via the output of the fourfold NAND gate, the high-phases of both clock inputs set the corresponding flip-flop outputs to 1, thus enabling the next iteration.

Charge Pump

The `Accelerate` and `Decelerate` outputs of the phase detector are used to switch the charging and the de-charging currents for the filter capacitor `C1` within the charge pump as shown in figure 3.6 on the next page.

On the TDC chip, the filter capacitor `C1` is realised as MIMCAP, a metal-insulator-metal capacitor of approximately 20 pF. Its working voltage V_{CN} first of all directly controls the n-channel MOSFETs `M4` and `M8` of the current starved inverters. But V_{CN} is also used as input for the bias generator that generates V_{CP} to control the p-channel transistors `M1` and `M5` within the delay elements. Finally, the `Reset` input of the charge pump can be used to enforce

²Both outputs are low active.

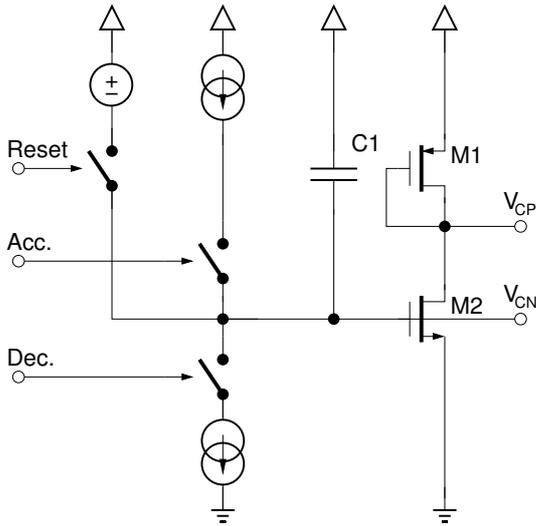


Figure 3.6: Equivalent circuit diagram of the charge pump implementation with filter capacitor and bias generator. The reset input is able to override the Accelerate and Decelerate inputs.

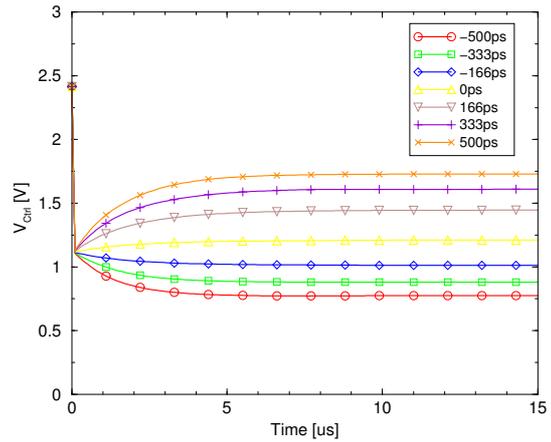


Figure 3.7: Simulation of the DLLs control voltage for the OTIS1.2 phase detector and charge pump combination: behaviour of a proportional controller.

control voltages that adjust the total propagation time of the delay chain to approximately 22 ns. The precharging of the filter capacitor results in lock times well below 1 μ s.

Figure 3.7 shows the simulation of the combination of phase detector and charge pump under nominal conditions. The different simulations apply constant phase differences between Clk and $DClk$ ranging from -500 to $+500$ ps. Figure 3.7 shows the developing of the control voltage V_{CN} over the simulation time with the applied input phase difference as curve parameter. The simulation shows that the combination of phase detector and charge pump acts a proportional controller that always exhibits a control deviation from the nominal value of zero phase difference between reference input Clk and delayed output $DClk$: the control voltage V_{CN} reaches stationary levels other than 0 or 2.5 V although the phase difference (as given by the simulation) still exists.

3.2.2 DLL Locking

The drift time measurement, precisely the interpretation of the TDC cores output, relies on the assumption that the DLL is properly locked to 40 MHz. The TDC core itself is able to check this lock state of the DLL. For this, the delay elements control voltage V_{CN} is internally compared against the two programmed output voltages of two dedicated DACs. A DLL control voltage outside of this defined interval generates a lock lost flag that is stored in the status register and is encoded to the header information of any data output sequence. Though not directly observable in the LHCb experiment, the control voltage of the DLL is accessible in the laboratory test setup. The output of V_{CN} is buffered and decoupled from the control loop. It is therefore guaranteed that the monitoring tap does not act as an antenna and thus accessing the control voltage does not influence the DLL itself. The monitoring output of V_{CN} allows to determine the DLLs lock time, its lock range and its actual lock state.

Proper DLL locking requires a dedicated reset signal. Such a specialized reset signal is not available from the LHCb TFC system. Thus the OTIS chip uses the power-up reset signal for the DLL reset. For this, the DLL reset signal is generated by the power-up reset pad (including a Schmitt trigger) together with the RC circuit external to the pad. To

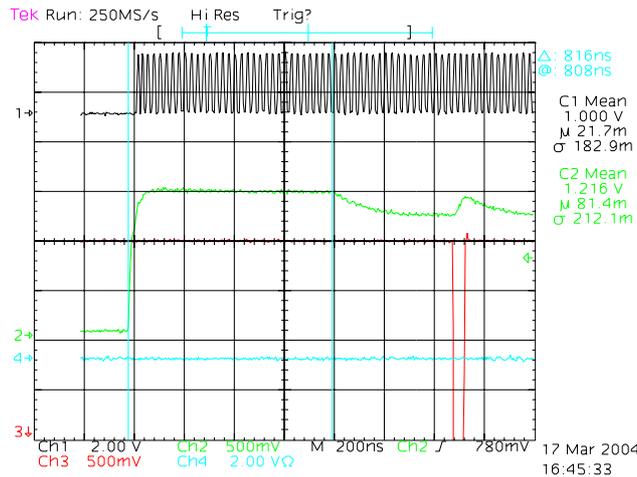


Figure 3.8: Recording of a DLL locking sequence after a power up reset. The displayed signals are `LastDummyOut` (channel 1, black) `VCN` (channel 2, green) and `DLLPadReset` (channel 3, red). Channel number 4 (blue) is unused.

be independent from rather complex power cycles in the LHCb experiment, the DLL can additionally be reset via the I²C-bus or the auxiliary DLL reset pad. The latter is only an additional option that will not be available in the LHCb environment.

Figure 3.8 shows the DLL locking sequence that follows a power cycle respectively a power-up reset. The figure displays `LastDummyOut` (channel 1, black) which is the monitoring output of the delayed clock signal, `VCN` (channel 2, green), `DLLPadReset` (channel 3, red) which is the auxiliary DLL reset input and an unused channel (number 4, blue). For clarification, no clock signal is applied to the chip during (and for some undefined time after) the power cycle. As a consequence, the signals `LastDummyOut` and `VCN` are at 0 V. As soon as the chip receives a clock signal, the control voltage rises to its precharge value of approximately 1.4 V. Then, after the reset signal went inactive, `VCN` adjusts to the lock state value within less than 1 μ s. In the situation shown in figure 3.8, the levelling of the DLL is interrupted by a reset signal from the auxiliary reset pad.

3.2.3 Hit Register

As soon as the lock state is reached, the DLL outputs `DLLOut<0:63>` divide each bunch crossing interval into 64 smaller intervals for the drift time measurement. Figure 3.9a shows how each DLL output is used to clock one of the 64 flip-flops within the hit register. The data inputs for all registers originate from the different detector channels. This way, at the end of each bunch crossing interval, each channels hit register holds a picture of the detector signal. The following edge finder and encoder circuits therefrom extract the corresponding drift times. These in turn are represented by the position of the leading edge of the channels signal that is stored in the hit register.

Another possible approach uses the detector signal as clock input and the DLL outputs as data inputs for the hit registers. In this second scenario, every channels hit register stores the state of the DLL at the incidence of an arriving detector signal. The corresponding drift time is then represented by the position of the falling edge found within the hit register (see figure 3.9b). The OTIS chip implements the first approach as it consequently follows the clock driven chip architecture.

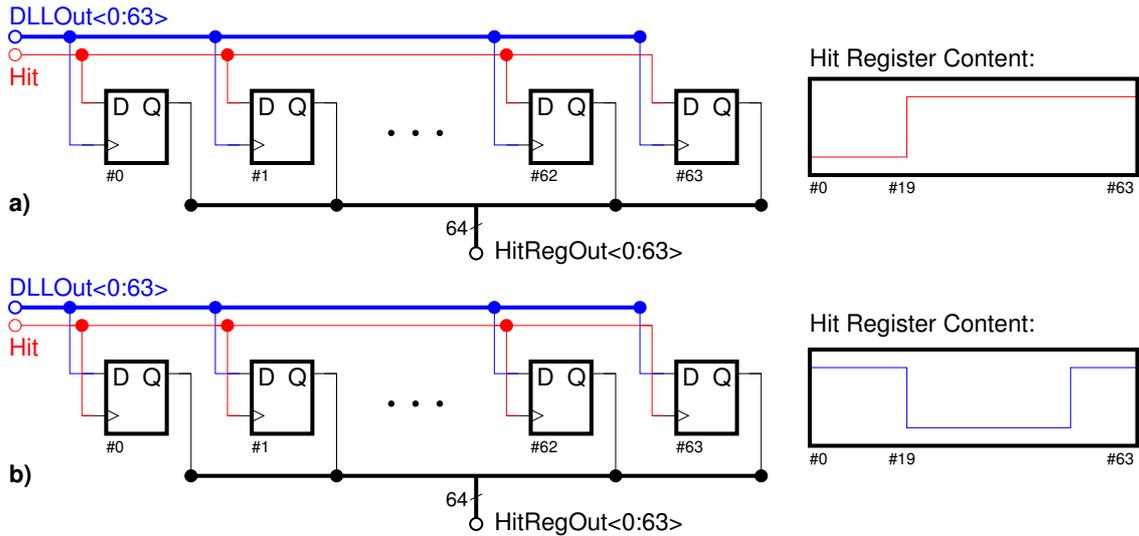


Figure 3.9: Two possible hit register configurations: a) the DLL outputs scan the detector signal: the position of the 0-1 transition is used for drift time extraction (used in OTIS); b) the detector signal stores the DLLs state: the position of the 1-0 transition is used for drift time extraction (not used in OTIS).

3.2.4 Hit Detection & Drift Time Encoding

Figure 3.10 shows the implementation of the hit detection and drift time encoding circuit that follows the hit register.

The hit register stores a picture of the detector signal and the position of its leading edge is extracted by using interconnected AND gates which have one inverting input each. Always one hit register output connects to two adjacent AND gates. The wrap around from the last hit register output to the inverting input of the first AND gate assures that hit detection is possible for bin number 0 too. This combinational logic is transparent for changes of the hit register content. This and the fact that the LHCb experiment requires dead-time-free operation of all front-end electronics devices³, requires to implement the drift time encoder as two single 32-to-5 encoders. This way, without blocking further data recording, it is guaranteed that both encoder outputs do not change for at least one half of the clock cycle period. The following intermediate storage of drift time and binary hit information from the encoder outputs finally allows to analyse the results from both halves without interference from data sampling from the following bunch crossing interval. The necessary clock signals CK1 and CK2 are derived from selected DLL taps.

The combinational edge finder circuit implicates ambivalent results when the hit register stores two or more input pulses within the span of one clock cycle. But well-defined outputs are guaranteed as the front-ends minimum double pulse resolution is 25 ns [Dre01]. Additionally, as mentioned above, the directly following encoder stage is split into two halves. This would therefore require that two distinct detector pulses fall within 12.5 ns to provoke ambiguous results. If both, upper and lower half of the hit register do store detector pulses, then always the pulse that results in a smaller drift time is preferred by the priority encoder. Additional to the drift time encoding, both encoder blocks provide binary hit detection flags which are used to generate the select signal for the output multiplexer. As each encoder only

³Neither detector signal processing nor trigger processing are allowed to introduce dead time.

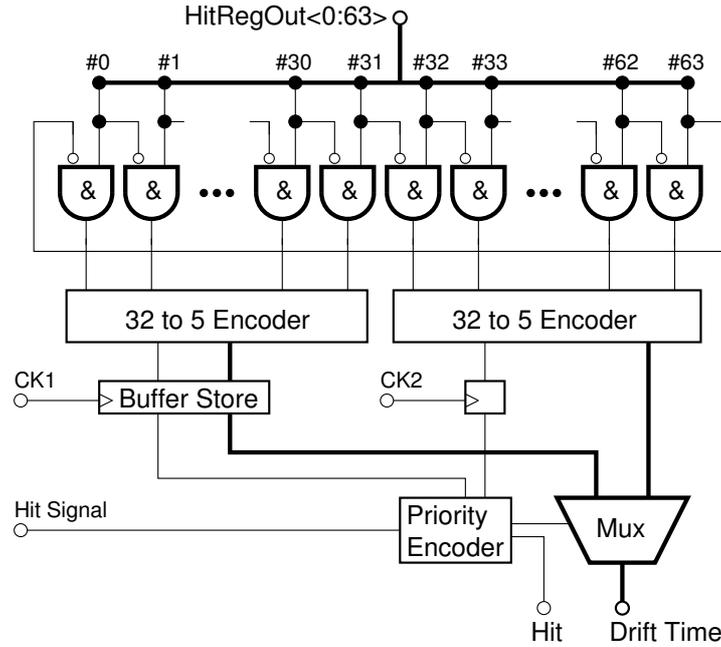


Figure 3.10: Block diagram of the hit detection and drift time encoding circuit. The twofold implementation of the encoder enables dead time free operation.

covers one half of the basic measurement range (12.5 ns or 5 bit), the resulting drift times need to be expanded by one additional bit. This is done in the output multiplexer by simply using the select signal itself as expansion bit. The resulting drift time code output is 6 bit wide (0-63) and represents drift times that range from 0 ns to 25 ns.

In total, the TDC core generates 6+1 bit drift time and hit information per clock cycle and channel. This results in a data volume of

$$40 \text{ MHz} \times 32 \times 7 \text{ bit} = 1.12 \text{ GB/s.} \quad (3.2)$$

The drift time and hit information of all 32 channels allocates 224 bits (out of 240 bits) in the following pre-pipeline register.

3.3 Pre-Pipeline Register

Interfacing the TDC core to the L0 pipeline, the pre-pipeline register serves as input buffer for the pipeline memory. Its main purpose is to synchronise and to combine data from the TDC and the control cores before writing to the L0 memory. Furthermore, the pre-pipeline register is used as data source for test patterns and arbitrary data while the OTIS chip operates in playback or memory self-test mode.

The dimension of the pre-pipeline is 3×240 bits or one dedicated register bank for the LHCb operation mode and two register banks for playback mode and memory self-test. All three register banks are implemented as flip-flops from the standard cell library and the register width of 30 bytes exactly matches the input width of the following pipeline memory. As pre-pipeline register and L0 pipeline both operate at 40 MHz, their data throughput rate is 1.20 GB/s. During normal operation, the pre-pipeline register stores a new set of detector data and status information for every clock cycle. As this data originates from the TDC

Bit No.	239	48	47	16		
Bit Content	Drift Times			Hit Mask		
Alignment	CH0	...	CH31	CH0	...	CH31

	15-14	13	12	11	10-8	7-0
	Status Information					
	0	SEU	DLL	PB	0	BX No.

Table 3.1: Bit content of the pre-pipeline register in LHCb operation mode.

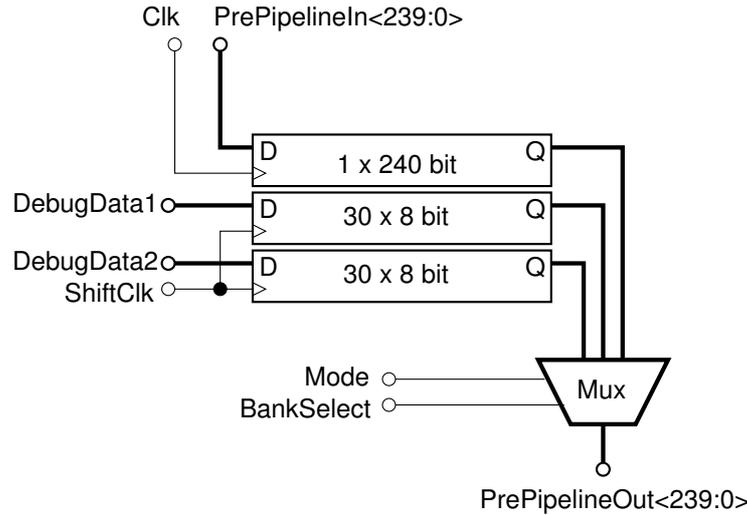


Figure 3.11: Block diagram of the pre-pipeline register.

core and the digital control core, the pre-pipeline register is mainly used as synchronisation stage but it also allows to arrange all bits in a way that is suitable for the following data processing: the channel-wise sorted hit and drift time information gets rearranged into a block of channel hit information and a block of drift-time data. Table 3.1 lists how data is arranged in the pre-pipeline register (fig. 3.11).

In the playback mode, the additional two register banks are used to store two independent sets of user defined data which are alternately written to the pipeline memory. For experimental setup at the laboratory, the data set selection can optionally be controlled by using the **BankSelect** input. The playback mode offers the possibility to setup and test the complete readout chain including the OTIS chips, optical transmission and DAQ without the need to operate the detector modules as data source. Both debugging mode register banks are arranged as shift registers. This allows to load the user-defined data byte by byte into the pre-pipeline register by using the I²C interface. As a means of consistency check, it is possible to read back the first byte after having stored all 30 playback bytes (not shown in fig. 3.11). In the memory self-test mode, the pre-pipeline register holds two pre-defined test patterns. Here, the digital control core drives data load and data set selection. Again, user interaction via the **BankSelect** pad is possible and can be used to provoke failing memory self-tests.

The two clock signals that drive the pre-pipeline register (**Clk** and **ShiftClk**) originate from two different clock domains according to the corresponding data sources. In normal

operation mode, most of the pre-pipeline data originates from the TDC core. The driving storage clock `Clk` is therefore derived from a selected DLL tap. The playback mode or the memory self-test are both driven by the digital control core. The pre-pipeline shift register clock `ShiftClk` is therefore controlled by the digital core of the OTIS chip. Figure 3.11 does not include the buffer tree that is necessary to drive the clock signal to all 240 flip-flops of each pre-pipeline register bank.

3.4 Pipeline and Derandomizing Buffer

In the LHCb experiment, three trigger stages (L0, L1 and HLT) reduce the rate of visible interactions⁴ from 10 MHz to the rate of accepted events of 200 Hz [TDR10]. In case of front-end electronics, such as the OTIS chip, the latency between data sampling and the generation of an L0 trigger accept signal is 4 μ s fixed. That is, every set of detector data needs interim storage in the L0 pipeline until being accepted or rejected. The average L0 trigger rate over a large time window is expected to be 1.1 MHz. But possible trigger rate fluctuations and the fact that up to 16 consecutive accept signals will be allowed by the Readout Supervisor (RS) [Jac01, Jac00], require a derandomizer buffer that stores accepted data sets before their processing can actually start.

The specifications for LHCb L0 front-end electronics [Chr01] allow to implement two dedicated RAM blocks for pipeline and derandomizer or to combine both into a single RAM instantiation. The analogue pipeline of the *Beetle* chip [Bau02, L c05] for example combines L0 pipeline and derandomizer to avoid copy operations on the sensitive analogue data. The drawback of this method is the huge overhead in the memory management which must inhibit write operations to triggered but not yet processed memory entries. This results in a non-contiguous behaviour of pipeline write and read pointer and demands for larger ring buffer size than the sum of pipeline and derandomizer buffer depth itself. The OTIS chip on the other hand uses two physically separated arrays of dual port SRAM cells to realise pipeline and derandomizer buffer. Copy operations on the digitised data are trouble-free and the memory management only needs to provide two pairs of write and read pointers for pipeline and derandomizer respectively.

The two memory blocks on the OTIS chip have been developed and tested in the context of a diploma thesis [Sro01]. The implementation follows standard SRAM designs [Pri97] and includes I/O amplifiers and address decoders. Their dimensions are 164 \times 240 bit for the pipeline memory and 3 \times 16 \times 240 bit for derandomizer buffer. Both blocks offer independent read and write ports which treat all 240 bits of every memory row as a single data word. Hence, from the control cores point of view, pipeline and derandomizer reduce to two one-dimensional arrays of 164 and 48 rows. The dedicated use of the pipeline output as input for the derandomizer buffer allows to create hard-wired interconnections between both memory blocks. This simplifies copy operations on accepted data sets. The derandomizer buffer is equipped with a latching output stage, i.e. data from the last read cycle is valid until new data from a new derandomizer buffer address is read. The digital control core benefits from this feature as it allows to save intermediate storage capacity at the cost of some additional read cycles.

Figure 3.12 on the next page shows the schematic drawing of a single SRAM cell with bit lines (`DI`, `DO`) and select lines (`WS`, `RS`). This figure shows the horizontally arranged write and read select lines that control write and read operations to all memory cells in one row in parallel. Extra buffers are inserted into the select lines to account for the exceptional large

⁴An interaction is defined to be visible if it produces at least two charged particles with sufficient hits in the vertex locator and the trigger stations to allow reconstruction.

word size. The bit lines vertically connect all memory cells within one column. The input side of the bit line is driven by the input amplifiers and the output side ends at the output amplifiers.

Internally, both memory blocks operate self-timed. That is, the processes that form the basis of write or read cycles, for example the switching of the bit line precharger or address decoder enabling, are coordinated and scheduled within the memory. The timing of all internal memory signals has been chosen carefully in order to minimise power consumption and to guarantee proper functionality at the desired speed of operation. On the `OTISMem1.0` prototype chip, the asynchronous SRAM has proven to be fully functional up to an operation frequency of 100 MHz. Nevertheless, the integration of pipeline and derandomizer buffer into the OTIS chip requires some additional interfacing circuitry in order to meet all timing specifications that are given by the memory design. Actually the problem is to interface the asynchronous SRAM blocks with the clock synchronous pre-pipeline register and the digital control core. The timing requirements to be met at the memory interface are listed and illustrated in table 3.2 and in figure 3.15 on the next page. The signals to be considered are data input, the write and read addresses and the enable signals for write, copy and read cycles. Within the memory, the write, copy and read cycles are triggered by the falling edges of the corresponding enable signals. This is why the data input for example is allowed to change after the write enable signal has been set to $W = 1$ (see table 3.2). However, the time from write enable high to data valid τ_{WHDV} should be less or equal than 2 ns in order to keep power consumption low.

All timing requirements at the memory interface can be expressed with respect to transitions of the four memory and derandomizer address buses. On the other hand, the control core provides clock synchronous address bus transitions. Therefore, one possible solution to realise all timing requirements is to derive the enable signals from the corresponding clock synchronous gate signals which are produced by the control core too. Figures 3.13 and 3.14 show the schematic view and the functional simulation of two interconnected flip-flops which serve as enable signal generator. In this example the digital control core provides a `WriteGate` pulse which is active for one clock cycle. The rising edges of `Clk1` and `Clk2` then define the phase alignment and pulse width of the resulting `WriteEnable` signal. The timing requirements given by pipeline and derandomizer buffer can now be fulfilled by choosing the appropriate clock signals `Clk1` and `Clk2`. The OTIS chip uses this enable signal generator to produce the enable signals for the memory write, copy and read cycles. Delay lines are used to derive the corresponding clock signals from the clock input.

3.5 Slow Digital Control Core

The two digital control cores that are integrated in the OTIS chip serve for operation parameter setup plus chip monitoring (Slow Control) and sequential control plus data processing (Fast Control). Both digital parts are separated in the layout due to the separation in the clock domain they operate at. The fast control part is driven by the 40 MHz LHC clock. Contrary, the slow control core operates at the 400 kHz I²C clock that is asynchronous to the LHC clock. The following paragraphs characterise the Slow Control core. A description of the Fast Control core follows in chapter 4.

In addition to the 40 MHz data collection path, a dedicated communication and control path will be used between the the various components of the LHCb detector and the Experiment Control System (ECS) [TDR7]. Both paths are independent from each other in order to ease error detection and error correction in the readout system. The ECS system foresees I²C or JTAG protocols for the communication with the front-end devices. The OTIS

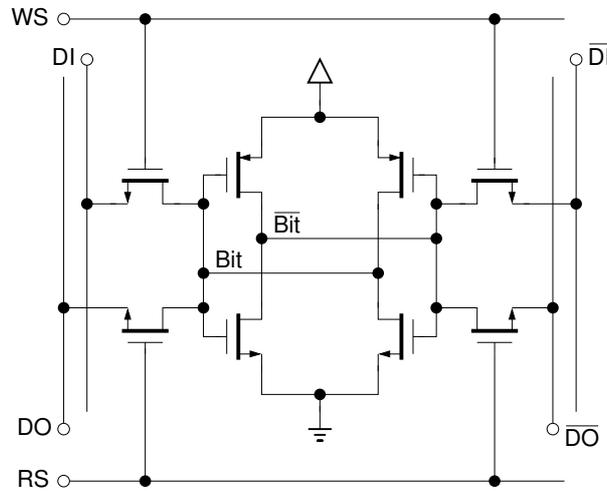


Figure 3.12: Schematic of a single dual port SRAM cell. The write and read select lines (WS, RS) each connect to all cells of one memory row. The bit lines (DI, DO, \overline{DI} , \overline{DO}) each connect to all cells of one memory column.

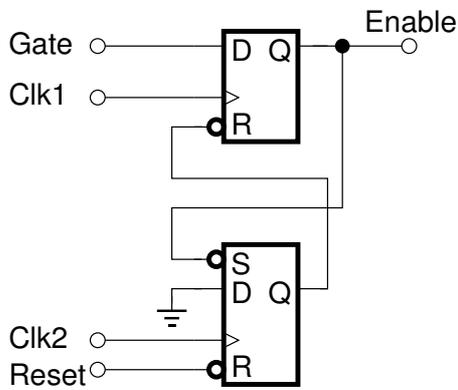


Figure 3.13: Schematic view of the enable signal generator. Two DLL derived clock signals are used to generate memory satisfying enable signals from clock synchronous gate signals.

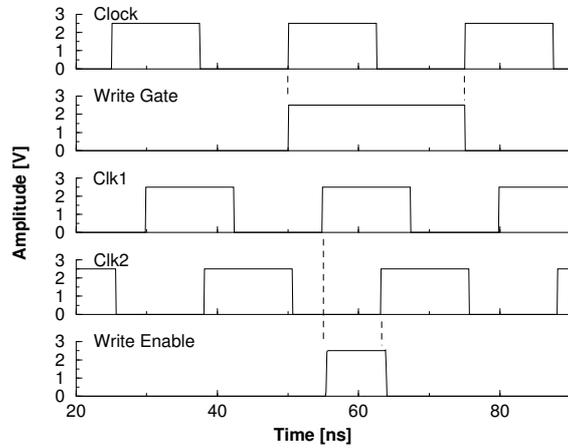


Figure 3.14: Functional simulation of the generator circuit. The Clk1 and Clk2 signals define width and phase alignment of the enable signal.

3 Chip Architecture

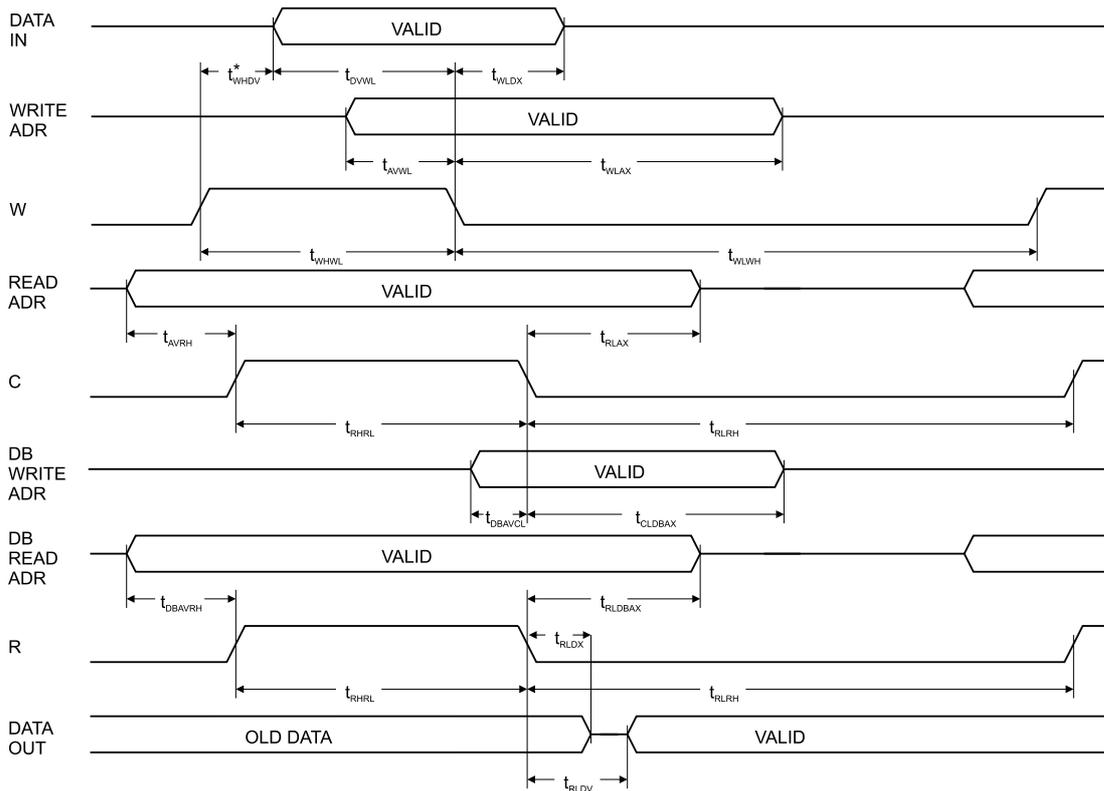
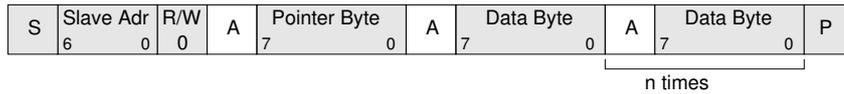


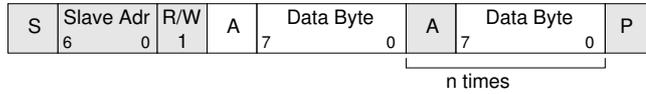
Figure 3.15: SRAM timing diagram. Graphical representation of the timing requirements for pipeline write, pipeline to derandomizer copy and derandomizer read cycles. [Sro01]

Variable	Description	Best	Worst	Unit
t_{WHDV}^*	write enable high to data valid	≤ 1.0	≤ 2.0	ns
t_{DVWL}	data valid to write enable low	≥ 1.5	≥ 3.0	ns
t_{WLDX}	write enable low to data transition	≥ 1.5	≥ 3.0	ns
t_{AVWL}	address valid to write enable low	≥ 1.5	≥ 3.0	ns
t_{WLAX}	write enable low to address transition	≥ 4.0	≥ 8.0	ns
t_{WHWL}	write enable high to write enable low	≥ 3.5	≥ 7.0	ns
t_{WLWH}	write enable low to write enable high	≥ 7.5	≥ 15.0	ns
t_{AVCH}	address valid to copy enable high	≥ 1.5	≥ 3.0	ns
t_{CLAX}	copy enable to address transition	≥ 2.0	≥ 4.0	ns
t_{DBAVCL}	DB address valid to copy enable low	≥ 1.0	≥ 2.0	ns
t_{CLDBAX}	copy enable low to DB address transition	≥ 3.5	≥ 7.0	ns
t_{CHCL}	copy enable high to copy enable low	≥ 3.0	≥ 6.0	ns
t_{CLCH}	copy enable low to copy enable high	≥ 8.0	≥ 16.0	ns
t_{DBAVRH}	DB address valid to read enable high	≥ 1.0	≥ 2.0	ns
t_{RLDBAX}	read enable low to DB address transition	≥ 1.5	≥ 3.0	ns
t_{RHRL}	read enable high to read enable low	≥ 2.5	≥ 5.0	ns
t_{RLRH}	read enable low to read enable high	≥ 5.0	≥ 10.0	ns
t_{RLDX}	read enable low to data transition	$= 1.0$	$= 2.0$	ns
t_{RLDV}	read enable low to data valid	$= 3.5$	$= 7.0$	ns

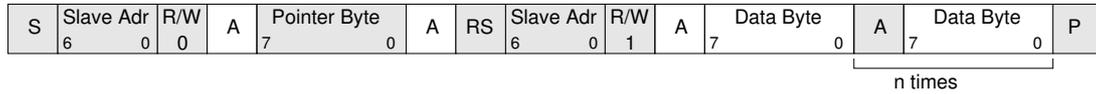
Table 3.2: SRAM Timing Requirements. [Sro01]

Write mode:**Read mode:**

Preset pointer



Pointer set followed by immediate read-out

**Figure 3.16:** I²C Write and Read Sequences.

chip uses the I²C protocol which is a simple bi-directional 2-wire bus (serial data (SDA) and serial clock (SCL)) for efficient inter-IC control developed by Philips [Phi00]. The I²C-bus is multi-master capable, but only one master device at a time is allowed to initiate any data transfer. Slave devices need to be addressed uniquely before responding to data transfers. All devices attach to the I²C-bus through wired-AND connections. Data on the I²C-bus can be transferred at rates up to 100 kbit/s and the number of interfaces connected to the bus is solely dependent on the bus capacitance limit of 400 pF or the allocation of the 7-bit address range⁵.

The data transfer on the I²C-bus is initiated by the master device. That is the master device generates the clock signal and addresses the slave devices. The communication is byte oriented and the most significant bit (MSB) is always transferred first. In the OTIS chips, every register access is controlled by the *Pointer* register which in turn addresses single data registers. After the byte transfer to or from any selected data register, the register access pointer automatically advances to the subsequent data register. This allows continuous access to adjacent registers. Even though the register selection changes within the context of a programming sequence, the content of the pointer register remains unchanged. This can be used to implement simple read-after-write data consistency checks.

Figure 3.16 shows the transfer sequences of a I²C read and write access. The master device initialises the I²C-bus (S) and transmits the slave device's address followed by a direction bit (R/W) indicating transmission or request of data. The addressed slave device responds with an acknowledge bit (A), then the data bytes follow. All byte transfers are completed by an acknowledge bit. In write mode (R/W=0), the OTIS chip always interprets the first data byte as pointer byte. The data transmission can continue as long as each data byte is acknowledged by the selected slave device. Any data transmission will stop when the bus master sends the stop condition (P). In read mode (R/W=1), two possibilities exist: reuse of the previously set pointer register or reprogramming of the pointer register followed by an immediate readout. If the pre-set pointer register is used, the data transfer starts after bus initialisation and acknowledge of the slave device addressing. In contrast to the write mode, the master device acknowledges each received data byte. If the pointer register is set

⁵The I²C-protocol offers 7-bit and 10-bit address ranges. The OTIS chips only use the 7-bit address range which offers 112 valid addresses ranging from 8 to 119.

Address	Name	Type	Bit Assignment/Description	
0	PosID0	read only	7 - 4 3 - 0	0 TDCID[11:8]
1	PosID1	read only	7 - 0	TDCID[7:0]
2	I2CID	read only	7 6 - 0	0 I2CID[6:0]
3	Revision	read only	7 - 6 5 - 3 2 - 0	0 Chip Version (3'b001) Chip Revision (3'b001 resp. 3'b010)
4	StatusReg	read/clear	7 - 4 3 2 1 0	0 SEU Buffer overflow DLL lock lost Memory self-test failed
5	ReceivedT	read/clear	7 - 0	Number of received triggers
6	RejectedT	read/clear	7 - 0	Number of rejected triggers
7	EventID	read only	7 - 0	EventID
8	SEUCntr	read/clear	7 - 0	Number SEUs detected
9	ReadMode	read/write	7 6 5 4 3 2 1 - 0	0 Previous drift time DataValid (1=on, 0=off) Comma (1=on, 0=off) Truncation MultiHit / SingleHit Number of Events per trigger
10	DebugMode	read/write	7 - 5 4 3 - 1 0	Service pad signal select (see table 4.5) Service pads (1=on, 0=off) Debug modes (see table 4.3) Debug mode (1=on; 0=off)
11	DLLReg	read/write	7 - 1 0	0 DLL reset (1=active, 0=off)
12	Latency	read/write	7 - 0	Latency register
13	Offset	read/write	7 - 4 3 - 0	BX counter wrap-around BX counter offset
14	Reserved0	read/write	7 - 0	Without any functionality
15 - 18	ChannelMask	read/write	7 - 0	Channel mask register
19	Reserved1	read/write	7 - 0	Without any functionality
20 - 23	DLLDAC	read/write	7 - 0	DLL DAC register
24 - 27	ASDDAC	read/write	7 - 0	ASD DAC register
28, 29	PBData	read/write	7 - 0	Playback data
30 - 65	ReadFIFO	read only	7 - 0	Slow event data readout

Table 3.3: Status and configuration registers of OTIS1.2 [Dep04]

anew, the read sequence starts as a write sequence. But after the slave device acknowledges the pointer byte, the bus-master continues by sending a repeated start condition (RS) again followed by the slave address. After acknowledging, the slave device sends data according to the pointer register selection (including the auto-incrementing register addressing) until the bus-master terminates the transfer.

The register bank itself is part of the slow control core of the OTIS chip. In total it contains 66 addressable registers (see table 3.3). The register bank provides read-only registers and registers with full read and write access. The read-only registers hold static information such as TDC-ID or revision number and non-static information such as chip status or the number of received L0 trigger signals. The user cannot alter the content of the static registers, but any write access to the non-static read-only registers resets them to zero. In principle, each addressable register is able to store 1 byte. But among the configuration registers with full read and write access, the `PBData` registers are organised as shift registers. These are able to store playback data (hit mask and drift time data) for 32 channels. The auto-increment mechanism of the pointer byte is deactivated for the `PBData` shift registers. This requires reprogramming of the pointer register before the subsequent `ReadFIFO` registers can be accessed.

3.6 Bias Voltage Generators

The OTIS chip additionally integrates eight 8-bit DACs (Digital to Analogue Converter). Four of these DACs are internally used for bias and threshold voltage generation for the comparators that check the lock state of the DLL. The other four DACs generate the threshold voltages for the `ASDblr` discriminator chips that connect to the input side of the OTIS chip.

The internal usage as voltage source for lock state monitoring in principle only requires to cover the dynamic range of V_{Ctrl} (800 mV to 1800 mV) with a resolution of 5 bit. In case of the threshold voltage generation for the `ASDblr` chips, the maximum and minimum output voltages should be as close to power rails of 0 and 2.5 V as possible. This allows to set the `ASDblr` threshold for maximum comparator trigger rate (the zero reference of the threshold input is set to approximately 100 mV [UP02]) or to reliably suppress all detector pulses.

A DAC step-size of ≈ 10 mV (8 bit DAC resolution) corresponds to a charge of about 0.12 fC. This is adequate for the `ASDblr` chips which show a maximum channel-to-channel variation in the threshold characteristics of ± 0.4 fC for a threshold voltage that corresponds to a charge of 2 fC [Slu03].

The DAC design that is used in the *Beetle* chip can be reused for implementation in OTIS chips as it fulfils the requirements mentioned above [Sex01, Bau02]. Its implementation uses a $R-2R$ configuration with a dynamic range close to 2.5 V at a resolution of 8 bit. Thus, the nominal DAC LSB bin size V_{LSB} calculates to

$$V_{LSB} = \frac{2.5V}{2^8} = 9.8 \text{ mV}.$$

The DAC outputs for the ASD threshold voltages need to be buffered: the track comparator threshold inputs of the ASD chips draw currents up to 10 μ A. The implemented output buffers can handle currents from -30 to $+50$ μ A. Figure 3.17 illustrates results from the simulation of a single DAC output buffer at nominal conditions. This simulation measures how the difference (y-axis, in mV) between the programmed DAC voltage and the actual buffer output depends from the DAC output (x-axis, in V) itself. The parameter for the set of curves is the buffered output current that ranges from -30 to $+50$ μ A. The buffer limits the dynamic range of the DAC and thus contributes to the nonlinearity of the output.

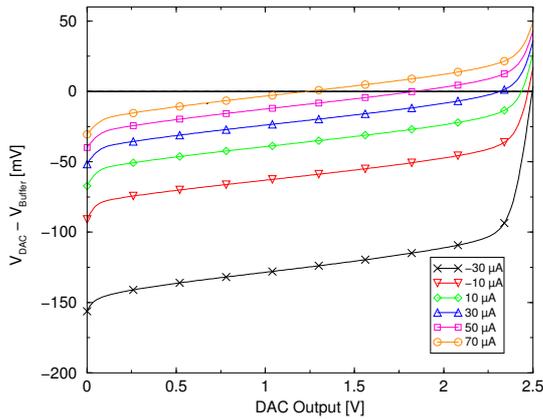


Figure 3.17: Simulation of the ASD-DAC output buffer. The difference between DAC and buffer output voltage is shown as a function of the DAC output voltage with the output current as parameter.

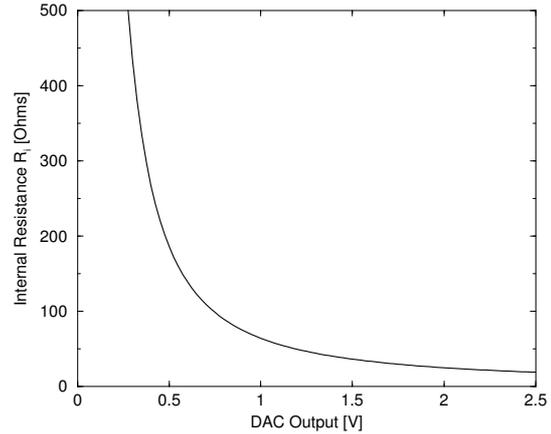


Figure 3.18: Simulation of the internal resistor of the ASD-DAC output buffer.

Figure 3.18 shows the simulation of the internal resistance R_i of the output buffer depending on the DAC output. The minimum internal resistance at $V_{\text{DAC}} = 2.5 \text{ V}$ is

$$R_{i,\min} = 18.8 \Omega.$$

Above a DAC voltage of $V_{\text{DAC}} = 325 \text{ mV}$, the internal resistance R_i of the output buffer can be described by $R_i[\Omega] = 65.5 \cdot V_{\text{DAC}}[\text{V}]^{-1.47}$ with an error of less than 10%.

The DACs that are used internally do not allow direct measuring access. But the succeeding lock lost detection circuit allows to confine the DLLs control voltage V_{CN} into a range of two least significant DAC bits. This of course includes the characteristics of the comparator circuit as well as indefinite signal variations of the DLLs control voltage. When measured externally, V_{CN} shows a variation of less than 25 mV at room temperature and 40 MHz operation frequency. This again includes an unknown characteristic of the decoupling stage that allows to access V_{CN} from outside the chip. Nevertheless a measured upper limit of 12.5 mV per DAC LSB sounds reasonable. For the usage in the LHCb environment, the lock lost comparator levels should be close to the dynamic range of V_{CN} in order not to diminish the DLLs lock range.

The threshold voltages for the ASDbldr chips in contrast can be accessed directly after the output buffers. Figure 3.19 shows the linear characteristic of the buffered threshold voltage output following the content of the corresponding DAC register. For this example the output buffer drives a 130 k Ω load against **gnd**. The minimum and maximum output voltages are $(77 \pm 14) \text{ mV}$ and $(2.42 \pm 0.02) \text{ V}$ for register content 0x00 and 0xFF respectively. Figure 3.19 shows only every 10th error bar to simplify matters. Diagram 3.20 shows the differences in the output voltages for adjacent register settings. In other words, the figure presents the 255 different bin sizes. Figure 3.20 again omits the single error bars (20 mV) to simplify matters. The calculated mean DAC bin size results to

$$V_{\text{LSB}} = (9.2 \pm 1.3) \text{ mV}$$

and the differential non-linearity (DNL), being defined as the difference between maximum and minimum bin size is

$$\text{DNL} = (7.7 \pm 3.1) \text{ mV}.$$

The relatively large error of the DNL figure results from the error propagation of the DNL calculation.

The internally used DACs and the DAC and buffer combinations that generate the ASDblr threshold voltages have proven to meet the requirements. The lock lost detection circuitry reliably flags control voltages that are out of range, and the threshold voltage generation provides buffered voltages from a range close to the supply voltage rails.

In the Outer Tracker detector, one OTIS chip provides the threshold voltages for always four ASD front-end chips. It is therefore recommended to integrate threshold voltage scans into an automated test environment. These scans should at least test every single DAC register bit once plus the minimum and maximum settings (0x00 and 0xFF).

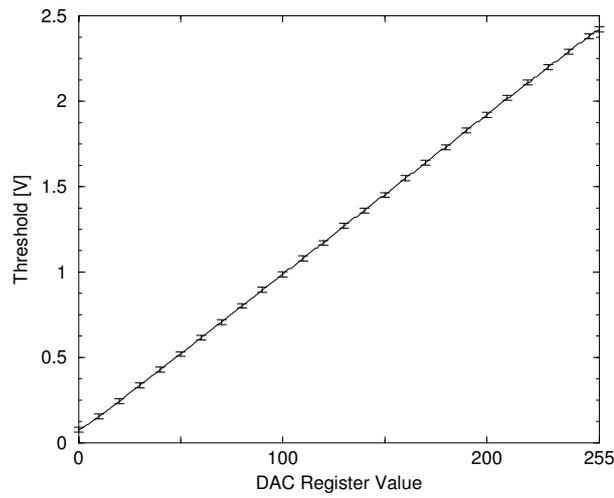


Figure 3.19: Recording of the output characteristic of the buffered ASDblr threshold DAC driving a $130\text{ k}\Omega$ load against gnd .

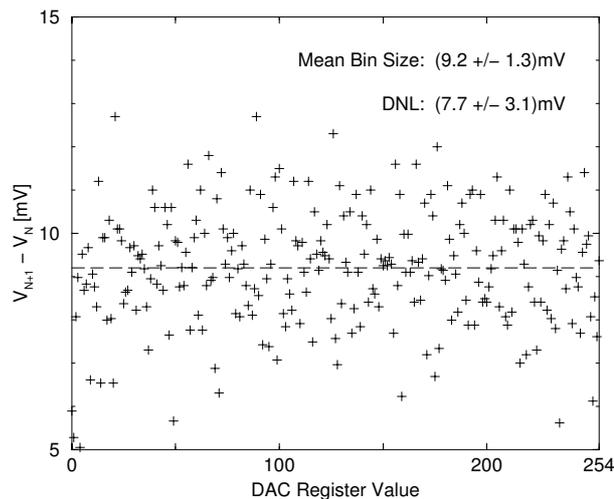


Figure 3.20: Distribution of the DAC bin sizes.

4 Fast Control Unit

The second digital control unit of the OTIS chip, the *Fast Control* core, provides sequential control for the whole chip. This includes memory and trigger management as well as data processing and data output. The fast control core additionally integrates the functionality for synchronisation and integrity checks plus the interface for a slow I²C-bus data output path that is independent from the standard 40 MHz data output path.

In contrast to the sequential control unit of the *Beetle* chip [Bau02], which is partly based on the digital core of the *Helix* chip [Tru00], the fast control core of the OTIS TDC is a new development. It is designed to comply with the requirements for LHCb L0 front-end electronics [Chr01, Chr04b] and integrates the OTIS chip into the LHCb Outer Tracker detector electronics.

The specifications foresee clock driven operation at 40 MHz. The maximum L0 trigger rate is 1.1 MHz and the accept signals arrive with a fixed latency of 160 clock cycles. The maximum number of consecutive L0 accept signals is 16. Table 4.1 summarises the key parameters of the LHCb front-end electronics.

Feature	Parameter
Clock driven design	—
Bunch Crossing Clock	40.08 MHz
L0 Trigger Latency	160 Clock Cycles
Max. L0 Trigger Rate	1.1 MHz
Consecutive L0 Trigger	Max. 16
L0 Gap	None
Samples per L0 Trigger	1, more if required
L0 Derandomizer Buffer Depth	16 Events
Derandomizer Readout Time	Max. 900 ns

Table 4.1: Features and Key Parameters of LHCb front-end Electronics

If required, the specifications allow to extract more than one data sample per trigger from the L0 buffer. This will be the case for the Outer Tracker detector, as the maximum drift times to be measured exceed one bunch crossing clock period. The expected maximum drift times in the Outer Tracker detector are 50 ns. To account for those large drift times, the OTIS TDC is able to transfer up to three data samples per trigger from the pipeline to the derandomizer buffer. But, in accordance with the specifications, the trigger processing is still dead time free (i.e. no L0 gap introduced) and the derandomizer buffer readout time is still limited to 900 ns.

The following sections describe how the fast control core manages the L0 pipeline and derandomizer buffer. The trigger handling mechanism is introduced as well as the two basic operation modes together with their output data formats. Additionally, the building blocks for synchronisation (bunch crossing counter) and integrity checks (memory self-test) are explained.

4.1 Memory Management

The LHCb-wide delay of 160 clock cycles between data taking and an L0 trigger decision requires an L0 pipeline for intermediate data storage in every detector readout chip. Triggered data sets are transferred from the pipeline to the derandomizer buffer, where the event data is stored until processing. The implementation of pipeline and derandomizer is described in chapter 3.4.

The memory management unit can treat pipeline and derandomizer as two one-dimensional arrays of size 164 (resp. 48). Both need write pointer (WP, DBWP), read pointer (RP, DBRP) and two enable signals (write enable, read enable) as control inputs. The built-in copy function between pipeline and derandomizer buffer allows to hard-wire the pipeline read enable signal with the write enable signal of the derandomizer buffer. Thus, the fast control core only needs to provide two pairs of read and write addresses plus single write, copy and read enable signals to control both, the L0 pipeline and the derandomizer buffer.

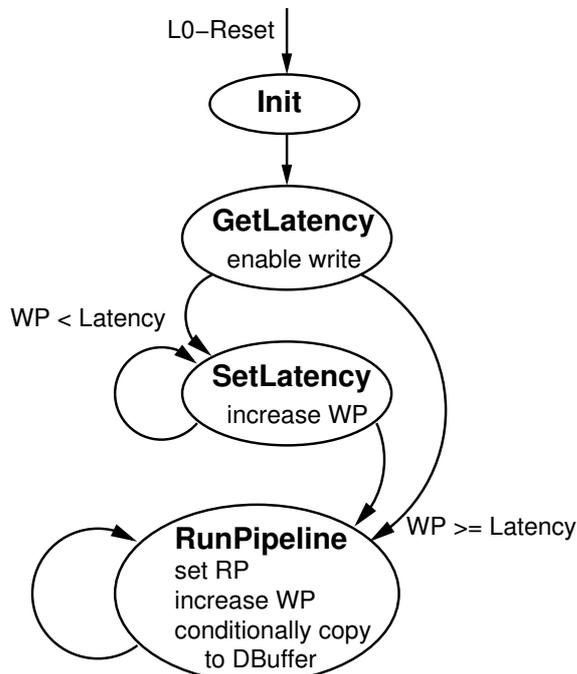


Figure 4.1: State diagram of the finite state machine that controls L0 pipeline and derandomizer buffer.

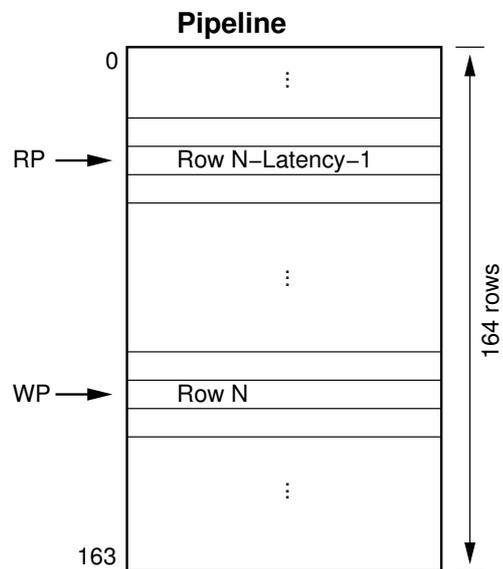


Figure 4.2: Snapshot of the L0 Pipeline. Write and read pointer have the distance Latency.

Figure 4.1 shows the Finite State Machine (FSM) which controls pipeline and derandomizer buffer. It operates clock synchronous and enters an initialisation state with every L0 reset signal. This state resets the pipeline address pointers WP and RP plus the derandomizer buffer write pointer DBWP. The derandomizer read pointer DBRP is controlled from the state machine that handles data processing and data output (see section 4.4).

The next state **GetLatency** enables pipeline write operations and reads the programmed latency from the slow control core. Only this state reads the latency, thus, any change in the programmable latency requires an L0 reset signal to become active. The operation mode of the OTIS chip is treated in the same way: reprogrammed fundamental chip parameters need an L0 reset to become effective. The **GetLatency** state is reached in the first clock cycle after an L0 reset signal. Additionally pipeline write operations are enabled from this state on. This way, the OTIS chips start taking data at the earliest possible point in time after

an L0 reset.

The intermediate state `SetLatency` is in use as long as the distance between `WP` and `RP` is less than latency pipeline rows. In this state only the pipeline write pointer advances to following rows, the read pointer stays in its reset position. L0 trigger signals are not accepted in this state.

The following FSM state (`RunPipeline`) is reached as soon as the pipeline write and read pointer show the correct distance. This state, which only loops to itself, finally accepts L0 trigger signals and conditionally copies the triggered data sets to the derandomizer buffer. The `RunPipeline` state advances the pipeline pointers `WP` and `RP` in parallel and sets new derandomizer buffer write addresses if required.

The `SetLatency` state will not be reached if the latency is set to zero. In this case, the pipeline read pointer directly follows the write pointer. The maximum latency is reached when the read pointer just precedes the write pointer. This is the case when the latency register is set to 162¹.

Figure 4.2 depicts a snap-shot of the pipeline and shows the two pipeline pointers addressing row `N` (write pointer) and row `N-Latency-1` (read pointer). In this situation, the actual detector data sample is stored to pipeline address `N`. If a trigger occurs in this cycle, then the content of row `N-Latency-1` gets transferred to the derandomizer buffer. This triggered data set has been stored `Latency+1` clock cycles earlier. Starting from the situation shown, a trigger in the following clock cycle would read from pipeline row `N-Latency`, which holds a newer data sample than the previous row. Both pointer overflow from address 163 to address 0. Any pipeline content gets overwritten after 164 clock cycles.

4.2 Trigger Management

In order to measure drift times that extend the range of single bunch crossing intervals, the OTIS chip can be set to transfer 1, 2 or 3 pipeline row contents per trigger into the derandomizer buffer. If for example the TDC chip is programmed to measure drift times up to 50 ns and a particular channel shows no hit in pipeline row `M` but a hit (plus drift time `T`; $0 \text{ ns} \leq T < 25 \text{ ns}$) in row `M+1`. Then a trigger on row `M` plus the following transfer of both rows `M` and `M+1` to the derandomizer buffer would be interpreted as drift time `T+25 ns`.

Single pipeline row transfers to the derandomizer buffer are always initiated directly by incoming L0 trigger signals. Multiple transfers that cover 2 or 3 bunch crossing cycles are always composed of 1 directly and 1 or 2 indirectly initiated transfers. The pipeline control circuit suppresses multiple transfers of any single pipeline row during one trigger pointer circulation. Figure 4.3 shows a snap-shot of the derandomizer buffer and an associated vector that marks directly triggered derandomizer buffer entries. In the situation shown, the measurement range is set to 2 bunch crossing intervals and the derandomizer buffer contains data that corresponds to three trigger signals. The first L0 accept signal extracted samples 15 and 16 from the pipeline. The second and third trigger caused sample 32, 33 and 34 to be copied into the derandomizer buffer. In this example, the measurement range of 50 ns and the sequence of trigger signals cause that the data sample no. 33 is shared between two events.

While the buffer entries that hold sample 15 and 16 are released at the end of the corresponding data output sequence, the derandomizer row that stores sample 33 will not be released until the third data output sequence of this example ends. This efficient management of the derandomizer buffer combined with the derandomizer depth of 48 rows allows

¹The slow control core allows to set latency values greater than 162. But the fast control core disregards values that outrange the physical dimension of the pipeline: 162 is used instead.

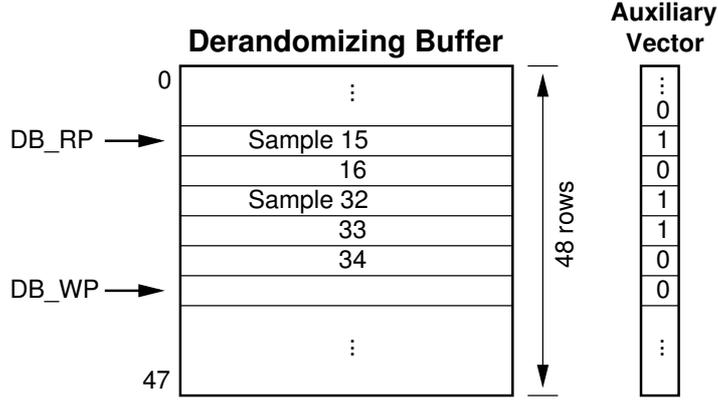


Figure 4.3: Snapshot of the derandomizer buffer plus its associated auxiliary vector that marks directly triggered buffer entries. The measurement range is set to two bunch crossing intervals.

the OTIS chip to handle more than the required 16 consecutive L0 trigger signals - even for the case of a 75 ns measurement range (3 data samples per trigger).

The fill level of the derandomizer buffer strongly depends on the trigger signal distribution and the selected measurement range. The following assumptions help to describe the processes of memory allocation and deallocation upon the reception and processing of trigger signals. This in turn allows to calculate the fill level at bunch crossing n for any given LHCb compliant sequence of trigger signals. Such a sequence \mathfrak{T} can be expressed as the sorted list of the K bunch crossing numbers T_i that represent the trigger signals arrival time at the chip:

$$\mathfrak{T} = \{T_1; \dots; T_K\}. \quad (4.1)$$

It is $T_i < T_{i+1}$ for all $1 \leq i < K$ and, without loss of generality, the first trigger signal can be chosen to occur at bunch crossing number one: $T_1 = 1$. As every incoming trigger signal potentially transfers up to 3 data sets from the pipeline to the derandomizer buffer, the search window SW is defined according to the measurement range MR :

$$SW = \begin{cases} 1 & 0ns \leq MR < 25ns \\ 2 & 0ns \leq MR < 50ns \\ 3 & 0ns \leq MR < 75ns. \end{cases} \quad (4.2)$$

With this, the number $A(i)$ of derandomizer buffer rows that are allocated by trigger number i is given by

$$A(i) = \begin{cases} SW & i = 1 \\ \min\{T_i - T_{i-1}; SW\} & 1 < i \leq K. \end{cases} \quad (4.3)$$

That is, the first trigger always allocates SW rows of the derandomizer buffer, all following allocations depend on the search window depth and the distance to the preceding trigger. The allocation process therefore depends on the trigger history. Trigger signal i can at most allocate SW rows of the derandomizer buffer, but this number drops to $T_i - T_{i-1}$ if this distance is less than the search window depth. For $SW = 1$, the allocation always spans one row. In contrast to the history dependence of the allocation process, the deallocation of derandomizer buffer rows always depends on the distance between trigger number i and the

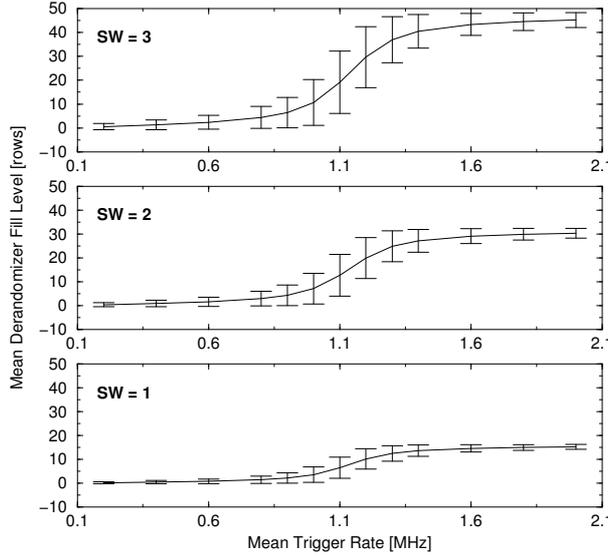


Figure 4.4: Simulation of the derandomizer buffer fill level for varying trigger rates and three search window sizes. The error bars represent the RMS of the mean derandomizer fill level at the corresponding trigger rate.

following trigger $i+1$:

$$D(i) = \begin{cases} \min\{T_{i+1} - T_i; SW\} & 1 \leq i < K \\ SW & i = K. \end{cases} \quad (4.4)$$

Again, the maximum number of affected rows is SW . Both $A(i)$ and $D(i)$ use the index of the trigger signals as parameter. The equivalence of the total number of allocated and deallocated rows for any given LHCb compliant trigger sequence follows from

$$\sum_{i=2}^K A(i) = \sum_{i=1}^{K-1} D(i). \quad (4.5)$$

The allocation of derandomizer buffer rows always happens at the reception of incoming trigger signals. In contrast, the deallocation only takes place after the complete processing of the actual trigger signal. This fact is neglected by the above described deallocation process $D(i)$. The calculation of the derandomizer buffer fill level needs to account for this and it therefore requires to derive a list of release times \mathfrak{R} from the trigger list \mathfrak{T} . The release times R_i of \mathfrak{R} represent those bunch crossing numbers that mark the end of the processing of trigger number i . The deallocation process $D(i)$ takes place at bunch crossing R_i . The calculation instructions to derive \mathfrak{R} from \mathfrak{T} are:

$$R_1 = 36 \quad \text{and} \quad R_i = \begin{cases} 36 + R_{i-1} & T_i \leq R_{i-1} \\ 35 + T_i & T_i > R_{i-1}. \end{cases} \quad (4.6)$$

The calculation instructions account for the fixed readout time of 36 clock cycles and the fact that trigger processing may be delayed until pending readout sequences have finished.

Now, with known \mathfrak{T} and \mathfrak{R} , respectively with T_i and R_i that describe the reception and the processing of trigger number i , the derandomizer buffers fill level F at a given bunch

crossing number n is specified by

$$F(n) = \sum_{T_i \leq n} A(i) - \sum_{R_j \leq n} D(j). \quad (4.7)$$

That is, at bunch crossing number n , the fill level calculates from the sum of all allocated rows reduced by the sum of all deallocated rows until BX n . The complexity of the fill level calculation comes from the different number of addends in minuend and subtrahend of the given formula.

Figure 4.4 shows the results from derandomizer buffer fill level simulations. The three diagrams, one per search window size, show the mean fill level for varying trigger rates. The simulation generates LHCb compliant random trigger sequences that are then applied to the derandomizer model described above. As this model does not include the actual size of the derandomizer buffer, the random generator is restricted such that it only produces trigger signals when there are not more than 15 pending triggers. The given error bars represent the RMS of the mean derandomizer fill level at the corresponding trigger rate.

4.3 Bunch Crossing Counter

A complex detector system such as the LHCb detector requires proper time alignment of all sub-detectors. This includes compensation of time of flight from the interaction point plus signal propagation delays. Without global time alignment, different detector components capture signals from different bunch crossing interactions. In the same way, the arrival of the L0 trigger accept signals must be in perfect synchronisation throughout the whole detector. This in turn assures that the correct event data gets extracted from the L0 pipelines of all sub-detectors.

After installation of the required timing relations, the detector synchronisation needs to be checked and maintained during operation. An effective means of control is to attach bunch crossing identifiers and L0 trigger numbers to all data as it enters the L0 pipeline respectively upon extraction from the L0 derandomizer buffer. This enables any later data processing stage to check the data tags against given reference values. The L0 trigger numbers simply represent the number of received trigger accept signals. These allow to detect the loss of triggers or event fragments, whereas the bunch crossing numbers allow extensive synchronisation checks.

Due to the limited number of bytes in the data output header (see section 4.4), only the eight least significant bits of the bunch crossing counter can be used to tag captured data sets. The bunch crossing counter must still consist of 12 bit because of the differences compared to the proposed data tagging scheme: data tagging at the input of the L0 pipeline requires valid bunch crossing numbers **Latency** clock cycles before the bunch crossing reset signal flags the start of a new machine cycle. But the L0 reset signal can not be used to reliably reset the bunch crossing counter because it is not guaranteed that every machine cycle starts with a L0 reset. Therefore the OTIS bunch crossing counter must be able to follow the LHC bunch crossing structure including the overflow at the end of a machine cycle.

The OTIS chip bunch crossing counter implementation follows the LHCb specifications. It reflects the bunch crossing structure of 3564 intervals per LHC machine cycle what results in a 12 bit wide synchronous counter with reset and preload inputs. The specifications propose data tagging at the input of the derandomizer buffer. This introduces a bunch crossing counter reset signal that is delayed **Latency** clock cycles compared to the L0 reset signal. On the OTIS chip, in contrast to the proposed scheme, the bunch crossing numbers are attached

to the data sets at the input of the L0 pipeline. This way, the bunch crossing counter reset signal is used to preload the counter to *Latency*. The resulting bunch crossing numbers do exactly show the expected behaviour. To provide maximum flexibility, the bunch crossing counter implementation allows to adjust the counter overflow mark and the counter preload value by means of the *Offset* register. The overflow mark is defined by the LHC machine cycle which is 3564 bunches. Possible changes in the bunch structure can be compensated by adjusting the upper 4 bits of the *Offset* register. The counter overflow mark range of values is then $3556 \leq N_{\text{overflow}} \leq 3571$. The register content `OffsetReg[7:4] = 4'b0111` selects the nominal value: overflow from 3563 to 0. In the LHCb experiment, a bunch crossing reset signal flags the beginning of a new LHC machine cycle. As the OTIS chip tags all data sets at the input of the L0 pipeline, the bunch crossing reset signal is used as preload input of the bunch crossing counter. Instead of resetting to zero, the preload signal sets the counter to *Latency*. Again, this preload value is adjustable. The lower 4 bits of the *Offset* register allow to set the preload value from *Latency* up to and including *Latency*+15.

Overflow Mark: $3556 + \text{OffsetReg}_{\text{upper half byte}}$
 Latency Offset: $\text{Latency} + \text{OffsetReg}_{\text{lower half byte}}$

The following sample code is an extract of the *Verilog* module that describes the actual implementation of the OTIS bunch crossing counter. The code fragment shows how the overflow mark and the preload value is calculated once a L0 reset occurs (lines 5 and 10 et seqq.). The actual bunch crossing counter follows from line 15 on.

Verilog code sample: extract from bunch crossing counter module.

```

1 // 12bit to 8bit reduction.
2 assign BunchCr[7:0] = BunchCrInt[7:0];
3
4 // L0Reset reads latency and offset.
5 always @ (negedge notL0Reset)
6   LatencyOffset[11:0] = {4'b0000, LatencyReg[7:0]}
7   + {8'b00000000, OffsetReg[3:0]};
8
9 // L0Reset reads roll-over.
10 always @ (negedge notL0Reset)
11   RollOver[11:0] = 12'b110111100100
12   + {8'b00000000, OffsetReg[7:4]};
13
14 // Bunch Crossing Counter.
15 always @ (posedge Clk or negedge notL0Reset) begin
16   // L0Reset forces BX to 0x000. First Clycle starts with 0x001.
17   if (!notL0Reset) begin
18     BunchCrInt[11:0] = 0;
19   end else begin
20     // BXReset sets BX to Latency + Offset.
21     if (!notBXReset)
22       BunchCrInt[11:0] = LatencyOffset[11:0];
23     // Overflow to zero at end of machine cycle + offset.
24     else if (BunchCrInt[11:0] == RollOver[11:0])
25       BunchCrInt[11:0] = 0;
26     // Increase counter.
27     else
28       BunchCrInt[11:0] = BunchCrInt[11:0] + 1'b1;
29   end
30 end

```

Extract from the functional simulation of the BX counter.

	Time	C	Resets			BX	
			Pwr	L0	BX		
1							
2							
3	2330000ps	1	1	1	1	8	
4	2337500ps	0	1	0	1	0	// L0 Reset
5	2350000ps	1	1	0	1	0	//
6	2362500ps	0	1	0	1	0	//
7	2370500ps	0	1	0	1	0	//
8	2375000ps	1	1	0	1	0	//
9	2387500ps	0	1	1	1	0	
10	2400000ps	1	1	1	1	1	
11	2412500ps	0	1	1	1	1	
12	2425000ps	1	1	1	1	2	
13							
14	6330000ps	1	1	1	1	158	
15	6337500ps	0	1	1	0	158	// BX Reset
16	6345000ps	0	1	1	0	158	//
17	6350000ps	1	1	1	0	159	//
18	6362500ps	0	1	1	1	159	
19	6375000ps	1	1	1	1	160	
20							
21	8762500ps	0	1	1	1	255	// 8bit Overflow
22	8775000ps	1	1	1	1	0	//
23	8787500ps	0	1	1	1	0	
24	8800000ps	1	1	1	1	1	
25	8812500ps	0	1	1	1	1	
26	8825000ps	1	1	1	1	2	
27							
28	91462500ps	0	1	1	1	235	// 12bit Overflow
29	91475000ps	1	1	1	1	0	//
30	91487500ps	0	1	1	1	0	
31	91500000ps	1	1	1	1	1	
32	91512500ps	0	1	1	1	1	
33	91525000ps	1	1	1	1	2	

The above listing is an extract from the output of the functional simulation of the bunch crossing counter. The different columns are (from left to right) simulation time, clock, power-up reset, L0 reset, BX reset and bunch crossing number (8 bit). Omissions from the original simulation output are marked with blank lines. The four parts of the simulation show the behaviour of the bunch crossing counter during L0 reset (BX number set to zero), BX reset (BX number set to Latency) and at 8 bit (overflow from 255 to 0) respectively 12 bit overflow (from 235 to 0).

Figure 4.5 presents the histogram of the 8 bit wide bunch crossing numbers as extracted from randomly triggered data output sequences. Provided that the bunch crossing counter generates the correct numbers, such a histogram must show an equal distribution of the extracted bunch crossing identifiers. The smaller number of entries in the last 20 bins of fig 4.5 originates from the LHCb bunch structure in combination with the width of the OTIS bunch crossing counter. The LHCb bunch structure requires the bunch crossing counter to overflow from 3563 to zero instead of overflowing from 4095. Additionally, the 12 bit bunch crossing numbers of the OTIS chip get reduced to 8 LSBs in the output data stream. This generates less entries in the bins 236 to 255 as indicated by the remainder of the integer division

$$\begin{aligned}
3563 \bmod 256 &= 3563 - \left\lfloor \frac{3563}{256} \right\rfloor \cdot 256 \\
&= 3563 - 13 \cdot 256 = 235.
\end{aligned}
\tag{4.8}$$

A change of the overflow mark by means of the **Offset** register, changes the number of bins that carry less entries in accordance with the remainder of the integer division of the overflow mark by 256.

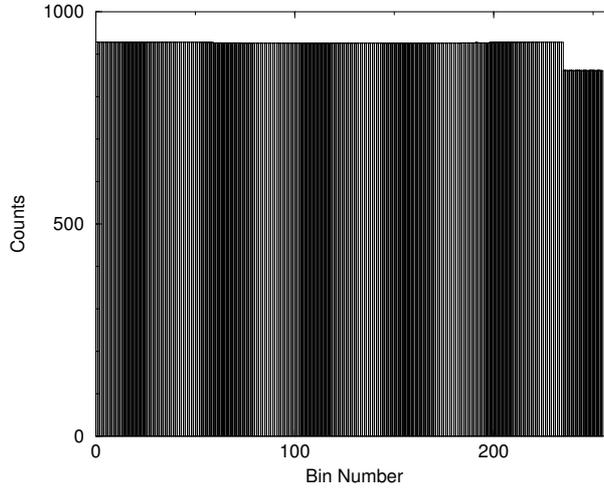


Figure 4.5: Distribution of bunch crossing numbers for a random trigger sequence. The missing entries of the last 20 bins are caused by the BX counter overflow from 3563 to 0 in combination with the output width reduction from 12 to 8 bit.

4.4 Data Processing and Data Output

Next to memory and trigger management, the digital control core steers data processing and data output. The task of this part of the control unit is to read triggered data sets from the derandomizer buffer and to prepare and execute data output. Two different data output formats exist. They differ in the encoding of the hit information and in the number of possible hits that can be transferred per channel and trigger. Both data formats fulfil the LHCb requirements for L0 front-end electronics. The following sections outline the requirements for the data output interface, describe the integration of both operation modes and give in detail descriptions of the two available data formats.

The OTIS chip operates synchronous to the LHC machine clock of 40 MHz. As a consequence, the chips TDC core can only measure drift times in the range from 0 ns to 25 ns. But the control core of the OTIS chip is able to associate drift times from 1, 2 or 3 bunch crossings with one trigger signal. This allows to extend the measurement range from the span of one bunch crossing (or 25 ns) to 2 or 3 bunch crossings (50 ns or 75 ns). If the operating range is set to 1 BX, then an arriving trigger signal selects data that has been captured *Latency* clock cycles before. A measurement range of 2 or 3 BX requires not only 1 but 2 or 3 pipeline read cycles. Here again, the incoming trigger signal addresses and reads a data set that is *Latency* clock cycles old. But the following read cycles (which are still associated with the actual trigger signal) address newer pipeline entries. The corresponding drift times still range from 0 ns to 25 ns but can be interpreted as long drift times (25-50 ns or 50-75 ns) since these samples are *Latency-1* or *Latency-2* clock cycles old.

If the measurement range exceeds 25 ns, then triggered pipeline rows may contain 2 or 3 hits per channel. The control circuit can not resolve this ambiguity. Instead, the selected output data format decides whether only the first hits drift time (see *Encoded Hitmask Mode*) or the drift times of all hits (see *Plain Hitmask Mode*) are transferred of chip.

The integration into the LHCb data taking scheme requires not to exceed a maximum readout time of 900 ns or 36 words per event. Only this readout limit plus a derandomizer

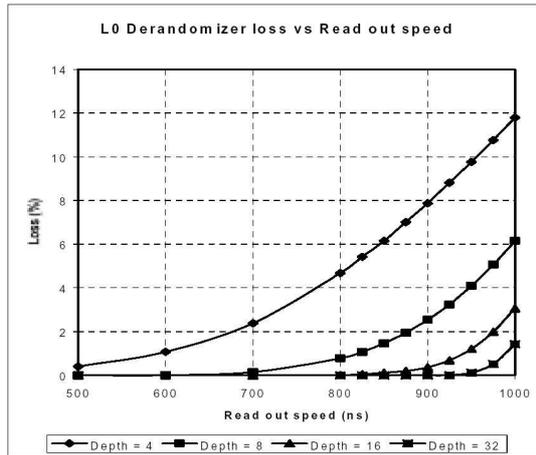


Figure 4.6: Simulated event loss as a function of the derandomizer depth and the read-out time. [Chr01].

buffer depth of 16 or more events result in an event loss below 1% at a 1 MHz trigger rate [Chr01]. The figure 4.6 shows the simulated event loss as a function of the readout length. This simulation compares different derandomizer buffer sizes and shows that for 900 ns readout time and a 16 stage derandomizer the expected loss stays below 1%.

A 900 ns readout time and a data size of 8 bit per channel allows for 4 extra bytes to be transmitted besides the drift time data. Hence an 8 bit wide output interface operating at 40 MHz is suitable for the OTIS chips. This additionally allows to combine data from always four OTIS chips for serialisation with the following GOL chip. The specifications do not fix the time necessary to prepare the readout of a new event when the derandomizer buffer has been empty. Obviously this preparation time must not exceed 900 ns. But pending readout sequences have to start immediately after the actual event readout ends.

4.4.1 Header Data Format

In either readout mode (plain or encoded hitmask) four header bytes precede the data output stream. These header bytes contain the chip identification number, operating parameters, error bits, trigger and bunch crossing numbers (see figure 4.7). The chip identification number (cf. the chips I²C address) is 12 bit wide and uniquely identifies every OTIS chip in the LHCb experiment. The chip addressing scheme follows the geometrical aspects of the Outer Tracker detector [Wie03] and guarantees, that at least two bits are non-zero, facilitating data stream synchronisation in the following L1 DAQ stage. Five header bits are used to indicate actual operating parameters. These are read mode (2 bits), measurement range (2 bits) and a 1-bit-flag that is used to distinguish detector data from playback data. One of the following two error bits is exclusively used to flag a full derandomizer buffer. This bit is set when -based on the measurement range- the available capacity of the derandomizer is less than the size of one triggered data set. The other error bit is used to represent the disjunction of lost DLL lock, SEU detection and failed memory self-test. The header byte sequence is completed with 4 LSBs of the Event ID counter and 8 LSBs of the bunch crossing counter. These are only fractions of the corresponding counters and therefore only allow for consistency checks within the scope of 16 L0 trigger signals respectively 256 bunch crossing cycles.

As the readout preparation time is not specified, the OTIS chips provide the possibility to insert an extra byte in advance of the event readout. This *Comma* byte (0xFF) possibly eases

Header Data Format (OTIS1.2)

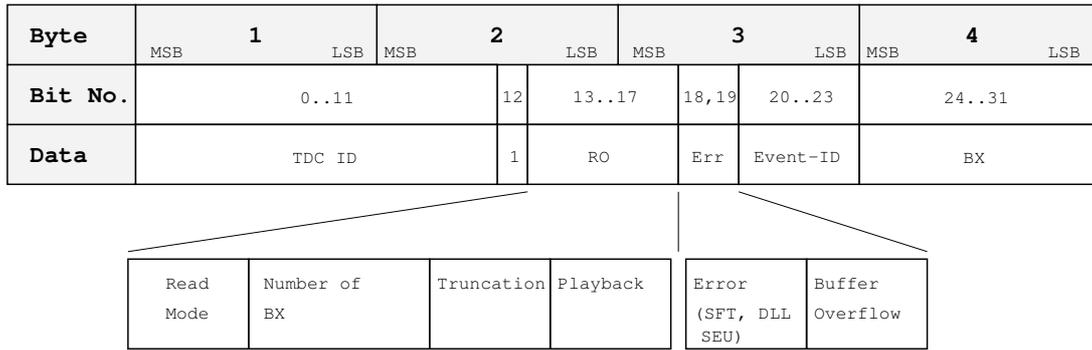


Figure 4.7: Header data format.

data stream synchronisation. The comma byte is neither needed nor allowed and therefore not inserted in-between two successive event readouts. The OTIS chips additionally provide a *Data Valid* flag which is always set for ongoing data output sequences (including the comma byte).

4.4.2 Encoded Hitmask Mode

In the encoded hitmask mode, the drift time bytes immediately follow the header bytes (see figure 4.8). In this mode only one drift time per channel and trigger is transmitted. In case that a channel shows multiple detector hits within the selected measurement range, then always the hit that results in the smallest drift time (i.e. the first hit found within the measurement range) is selected and read out from the chip.

As mentioned before, the basic measurement range of the TDC core spans one bunch crossing period. This range needs to be expanded due to the expected drift times of about 50 ns. The expansion of the measurement range is done by a per channel combination of up to three data sets that originate from three adjacent bunch crossings. The resulting extended drift time data is composed of the 6 bit wide *Fine Time* and the 2 bit wide *Coarse Time*. The fine time represents the unmodified result of the drift time measurement within the TDC core. The coarse time identifies the corresponding bunch crossing window within the extended measurement range. Two bit coarse time encoding additionally allows to flag the *No-Hit* situation. The OTIS chips by default clear the fine time bits of any single channel if it does not show a hit. It is possible to switch off this behaviour². In any case only drift time data ranging from 0x00 to 0xBF is considered to represent valid detector data.

If the drift time measurement range is set to one bunch crossing, then the data processing unit makes use of the latching functionality of the derandomizer buffers output port. This setting then only requires one derandomizer buffer read cycle. For a search window size of two or three bunch crossing periods, the number of derandomizer buffer read cycles rises according to the hit arrangement over the measurement range and the channels. Read cycles may thus happen until processing of the last channel starts. This requires that derandomizer buffer entries are only released at the end of the corresponding output sequence and only if this particular data set does not belong to any other L0 trigger accept within the search window of the primary trigger.

²Allowing drift time data to exceed 0xBF has been introduced in order not to lose detector data in case that the TDC core would wrongly suppress hit information but not the corresponding drift time data.

Output Data Format (SingleHit Mode)

Bit:	0..31	32..39	40..47	...	280..287
Data:	Header	Drift Time 0	Drift Time 1	...	Drift Time 31

Drift Time Encoding

Hit Position	Drift Time Encoding
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	11XXXXXX

Figure 4.8: Encoded hitmask mode data format. The drift time bytes immediately follow after the header bytes. The two most significant bits of each drift time byte represent the hits position within the selected search window size. The data output frame length is fix (36 bytes).

The encoded hitmask mode is by definition independent from the channel occupancy. In this mode the OTIS chips could even handle 100% occupancy without introducing dead time. The header data is partly and the drift time data completely byte-aligned. This simplifies data handling in the following DAQ stage to a great extend. The data output starts at the first clock cycle after the reception of the L0 trigger signal and the data transfer exactly takes 36 clock cycles to complete. The encoded hitmask mode fully complies the given specifications.

4.4.3 Plain Hitmask Mode

In the plain hitmask mode the four header bytes again precede the transmission of the channel hit and drift time information. But in contrast to the encoded hitmask mode, this mode allows to transmit three hit and drift time combinations per channel and trigger. More precisely, the plain hitmask mode allows to transmit one hit and drift time pair per channel and per bunch crossing interval that the measurement range is composed of.

In this operation mode the amount of data goes beyond the scope of the allowed readout time, especially when the measurement range covers two or three bunch crossing periods. This is why the plain hitmask mode uses zero suppression. The data processing unit dynamically discards detector channels that have not been hit. In the encoded hitmask mode, which does not use zero suppression, the byte positions within the data stream imply the corresponding channel number. This cannot be used in the plain hitmask mode because of the zero suppression. The solution is to transfer the binary hit information non-zero suppressed and separated from the (zero suppressed) drift time information. This way the bit positions within the hitmask imply the channel number and allow to relate the following drift time data to the corresponding channel numbers.

Figure 4.9 shows the three resulting data formats for measurement ranges of 25 ns, 50 ns and 75 ns. When the search window is greater than 25 ns, then the binary hit information is transferred such that the channel number iterator loops before the bunch crossing number iterator. The zero suppressed drift time data follows in the order specified by the preceding

Output Data Format (MultiHit Mode, 1BX/Trigger)

Bit:	0..31	32..63	64..71	...	64+(8n)..71+(8n)
Data:	Header	1 Hitmask	Drift Time 0	...	Drift Time n

Output Data Format (MultiHit Mode, 2BX/Trigger)

Bit:	0..31	32..95	96..103	...	96+(8n)..103+(8n)
Data:	Header	2 Hitmasks	Drift Time 0	...	Drift Time n

Output Data Format (MultiHit Mode, 3BX/Trigger)

Bit:	0..31	32..127	128..135	...	128+(8n)..135+(8n)
Data:	Header	3 Hitmasks	Drift Time 0	...	Drift Time n

Figure 4.9: Plain hitmask mode data format. The binary hit information is transferred before the thereby specified channels drift time information. The data output frame length depends on the search window size and on the detector occupancy.

hitmasks. The drift time data itself is 6 bit wide. Nevertheless, single channel data is still byte aligned because the advantage of simplified data handling compensates the smaller net data rate.

This zero suppressed operation mode entails a data format whose frame length is dependent from the selected measurement range and from the detector occupancy. To still comply with the LHCb specifications, the data processing unit offers the possibility to truncate the data output after 900 ns (or to fill it with zeros until 900 ns are reached). This option keeps the OTIS chips in synchronisation throughout all Outer Tracker detector modules. In case that the truncation option is switched on, single channels drift time information may be lost, but it is guaranteed that the binary hit information of the full measurement range is transmitted completely.

When using the plain hitmask mode together with the truncation option, i.e. the frame length is set to 36 bytes, the search window size SW reduces the maximum number of transmitted drift times per channel DT_{max} by $4 \times SW$:

$$DT_{max} = 32 - 4 SW. \quad (4.9)$$

This is because of the 32 bits of channel hit information that must be transferred per bunch crossing period the search window consists of. On the other hand, the single hit TDC allows for one hit per channel and search window size. Hence, the mean channel occupancy \overline{Occ} the OTIS chip can handle, defined as the quotient of available drift time capacity and acceptable hits, is:

$$\overline{Occ} = \frac{DT_{max}}{32 SW} = \frac{32 - 4 SW}{32 SW} = \frac{1}{SW} - \frac{1}{8}. \quad (4.10)$$

Table 4.2 lists the resulting figures for the mean channel hit occupancies that the OTIS chip can cope with in plain hitmask mode before single drift times get lost due to the truncation option.

Measurement Range	Drift Time Capacity		Mean Channel Occupancy	
	non-padding	padding	non-padding	padding
1 BX	28	37	87.5%	100.0%
2 BX	24	32	37.5%	50.0%
3 BX	20	26	20.8%	27.1%

Table 4.2: Channel occupancy threshold before truncation sets in. For a search window size of 3 BX, the less compact non-padding version of the plain hitmask mode is able to sustain 20.8% mean channel occupancy before the output data sequence exceeds 36 bytes.

Like the encoded hitmask mode, the plain hitmask mode releases no longer required de-randomizer buffer entries at the end of the data output sequence (independent from the truncation option). In this mode, first the chronological order of the detector data (in terms of bunch crossings) and then the channel number decide the order of the data output stream. This results in at maximum six (three times hitmask plus three times drift time data) de-randomizer buffer read cycles. In the encoded hitmask mode, where the data output order is determined by the channel number, the number of required derandomizer buffer read cycles depends on the chronology of the detector data.

4.4.4 Data Alignment in the Plain Hitmask Mode

The plain hitmask mode faces the problem of transferring 6 bit wide drift time data over an 8 bit interface. This section summarizes the discussion that led to the decision not to use the more compact approach of spreading the drift time data over the byte frames. Instead, the OTIS chips use the 8 bit data frames to transmit 6 bit drift time data.

The byte-padding version of the plain hitmask mode would need to cover many special cases that arise from the byte frame breaking data alignment. The most challenging point is that the total number of drift times to be transmitted is not known until all hitmasks have been read from the derandomizer buffer. Assumptions on the channel occupancy distribution are not possible and possibly big imbalances must not disrupt the composition of the output data stream.

Though all simulations of the byte-padding hitmask mode showed the full functional range, the Verilog code may still contain faults or imperfections due to incomplete test coverage. Furthermore, the synthesis result consumed more chip area than intended, but this problem has been solved by exploiting the inherent periodicity of the byte-padding data transfer.

For the user's point of view, the lower net data rate is compensated with a remarkable simple data handling. The data processing stage that follows the OTIS chip receives byte aligned data similar to the encoded hitmask mode. This allows straightforward processing without the need of additional data rearrangement. The usage of the plain hitmask mode in the LHCb environment demands to make use of the truncation option. Then, depending on the selected measurement range and on the detector occupancy, single channel drift times may get lost. Table 4.2 lists the threshold values for the channel occupancy which the OTIS chips can process without losing drift time data due to truncation. Additionally, the table quotes the amount of drift times that the plain hitmask mode can transmit within 900 ns. It is clearly visible that the implemented non-padding version offers less net data rate than the byte-padding version would be able to achieve. Especially when the measurement range is set to 25 ns the byte-padding version would be able to operate at 100% channel occupancy. But even at the largest measurement range of 75 ns the non-padding version is able to operate at as much as twice of the expected occupancy without losing drift time information. The

average occupancy expected in the LHCb Outer Tracker is smaller than 10% [Ber05].

4.5 Debugging Features

The OTIS chips integrate several test and debugging tools. These provide simple monitoring functionalities but also discrete functionalities such as memory self-test, playback operation mode and a slow readout path via the serial I²C-interface.

All debugging features are controlled with the `DebugMode` register (see tables 4.3 and 4.5). Therefore only I²C-communication is required for their setup. Most of the debugging features outputs are again readable via I²C-interface or they are encoded in the data output header bytes. Only the online monitoring of the chip-internal control signals requires direct access to the two service pads `WPWrap` and `RPWrap`. Though connected to the OTIS-PCB, there is no feedback channel available for the two service pad signals in the LHCb experiment. Both, memory self-test and playback operation mode offer the possibility of user interaction through the `BankSelect` pad. Again, this pad will not be accessible when integrated into the LHCb environment. The use of `WPWrap`, `RPWrap` and `BankSelect` is therefore limited to an experimental setup in the laboratory and the chip test prior to assembly. Table 4.3 lists all possible debug mode combinations offered by the OTIS chips.

DebugMode [3:1]	Debug Feature	Option
3'b001	I ² C Readout	—
3'b010	Memory Self-test	auto bank select
3'b011	Memory Self-test	manual bank select
3'b100	Playback Mode	auto bank select
3'b101	Playback Mode	auto bank select, I ² C RO
3'b110	Playback Mode	manual bank select
3'b111	Playback Mode	manual bank select, I ² C RO

Table 4.3: List of possible debug feature combinations. The playback mode does accept trigger signals while the memory self-test does not. The I²C readout always only catches the first triggered data output sequence after being enabled.

4.5.1 Memory Self-test and Playback Mode

The memory self-test and the playback operation mode both use the pre-pipeline register to bypass the detector data flow. Instead they insert arbitrary data into the pipeline. In both cases the pre-pipeline register stores two different data sets that are alternately written to the pipeline. If used, the `BankSelect` input steers the data set selection. The playback mode can be used to operate and test the data output path without the need of inserting detector data. Instead, the pre-pipeline register holds two independent sets of arbitrary hit and drift time information. Only the binary hit information and the drift time data for 32 channels is user controllable. The status information and the bunch crossing numbers are generated and inserted to the pipeline as in normal operation mode. The playback mode accepts L0 trigger signals and can be used with the plain or the encoded hitmask output data format. In any case, the use of the playback mode is flagged in the header bytes of all triggered data output sequences. This is needed to avoid accidental mixing of detector and playback data. When the `BankSelect` pad is accessible, user interaction is possible by selecting data sets according to the sequence of the incoming trigger signals.

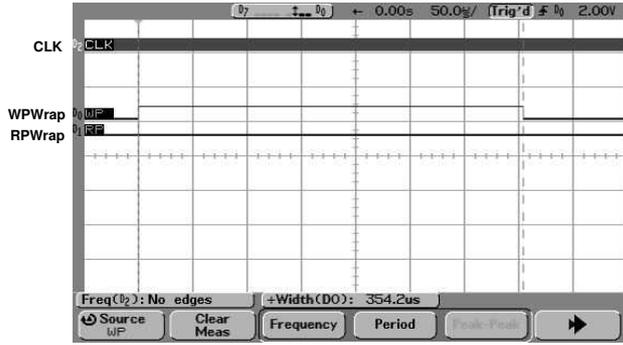


Figure 4.10: Recording of the SFTBusy and the SFTFailed flags during memory self-test. The screenshot shows the clock signal and the two service signals indicating active self-test (WPWrap) and self-test failure (RPWrap).

Temperature	Max. Frequency
-15 °C	75 MHz
5 °C	72 MHz
20 °C	70 MHz
35 °C	69 MHz
55 °C	65 MHz

Table 4.4: Maximum memory self-test operating frequency for different ambient temperatures.

Both memory self-test and playback mode operate at the nominal frequency of 40 MHz. Both are controlled by the experiment control system via the I²C-bus. While the playback mode accepts L0 trigger signals but disregards detector signals, the memory self-test does not accept trigger signals during operation. The self-test mode writes a checkerboard pattern into all pipeline cells. Single pipeline rows are then copied to the derandomizer buffer, read back and checked against known reference patterns. A second cycle with the opposite pattern follows the first run. A memory self-test run takes 14167 cycles or 354.175 μ s to complete: The processing time consists of **StartUp** (1 cycle), **PrePipeline** register setup (60 cycles) and two turns each consisting of **Init** (1 cycle) and 164 times **Write**, **Copy**, **Read** and **Check** (43 cycles). Again user interaction via the **BankSelect** pad is possible. This can be used to provoke failing memory self-tests. If any derandomizer buffer read cycle fails to yield the expected result, then the self-test stops and reports the negative output to the status register. A failing memory self-test is additionally flagged in the header bytes of any following data output sequence.

Figure 4.10 shows the recording of the two service pad signals WPWrap and RPWrap plus the clock signal during one memory self-test sequence. The timescale is 50 μ s per grid according to the processing time of the memory self-test. The two service pads show the SFTBusy and the SFTFailed signals which are labeled as WP and RP. During the error-free processing of the memory self-test, as shown in fig. 4.10, the busy flag is set but the failed flag remains unset. In case that an error occurs, i.e. the output data does not match the reference data, the failed flag gets set and the self-test process stops (the busy flag then returns to zero).

Built in self-test (BIST) implementations that use simple checkerboard patterns usually underperform at defect identification or defect localisation. Nevertheless such a BIST offers an adequate functional fault coverage of 94 % [Kim99] at reasonable implementation effort and execution time (complexity $O(n)$).

The memory self-test processes that were initiated during the measurement period did not reveal any errors. But as a crosscheck, failing memory self-tests have been provoked by using the manual data set selection via the **BankSelect** pad. The memory self-test proofed correct operation up to a clock frequency of 65 MHz at an environmental temperature of 55 °C (see table 4.4) what is consistent with the maximum memory speed.

4.5.2 I²C Data Output

When operating at the laboratory, the chips output interface (8 bit parallel at 40 MHz) requires rather complex data acquisition systems. But the optional use of the I²C-interface for data output allows to perform simple tests with a limited experimental setup. Even in the LHCb environment, the I²C-readout may be of use during the commissioning phase when the optical links or the DAQ system is possibly not yet available. The data output via I²C-interface can be used additional to the normal operation mode or it can be combined with the playback mode. Its implementation uses a FIFO register of 36 bytes to store a single data output sequence. The restriction to 36 bytes requires to switch on the `Truncation` option when operating in the plain hitmask mode. On the other hand, this artificial truncation to 36 bytes can be used to test this option of the plain hitmask mode. When switched on, the FIFO register captures the next triggered data output sequence and holds the data ready for I²C-readout. Following trigger signals do not need to be blocked, because the I²C-readout requires to be disabled and re-enabled before the FIFO data will be overwritten by a next data output sequence. When taking the I²C-bus protocol overhead (chip and register addressing, register setup) into account, an I²C FIFO read cycle consists of 45 words³. The I²C-bus clock is 400 kHz and thus the maximum I²C-readout rate is approximately 1 kHz.

4.5.3 Control Signal Monitoring and Counter Registers

The two service pads `WPWrap` and `RPWrap` provide online monitoring access to chip internal status and control signals. Several pairs of important internal signals are multiplexed to the two service pads according to the content of the `DebugMode` register (see table 4.5). These signals provide runtime information of the OTIS chips and allow the examination of the pipeline and derandomizer buffer pointer, the start and stop of a data output sequence or the fill level of the derandomizer buffer. The other service pad selections refer to the debug modes itself and provide information about memory self-test, playback mode or I²C-readout.

DebugMode [7:5]	Monitoring Information	Pad <code>WPWrap</code>	Pad <code>RPWrap</code>
3'b000	Zero-crossing of Pipeline write and read pointer	Write Pointer	Read Pointer
3'b001	Zero-crossing of DBuffer write and read pointer	Write Pointer	Read Pointer
3'b010	Memory self-test	Self-test busy	Self-test failure
3'b011	Playback operation mode	PB mode enabled	BankSelect
3'b100	Readout sequence	Start of sequence	End of sequence
3'b101	DBuffer fill level	Buffer empty	Buffer full
3'b110	I ² C-readout status	I ² C-readout enabled	FIFO has data
3'b111	DLL lock status	<code>VCtrl ≤ DLLDAC3</code>	<code>VCtrl ≥ DLLDAC0</code>

Table 4.5: List of the online available status information. The service pads `WPWrap` and `RPWrap` are not accessible in the LHCb environment due to the lack of a dedicated feedback channel.

Due to internal wire routing, capacitive load and the multiplexing circuit, the outputs of the service pads show a signal propagation delay of $\Delta t \leq 10$ ns with respect to the external clock signal (see fig. 4.11). This still allows correlation to the corresponding clock cycle and therefore the analysis of the programmed latency or the length of a data output sequence.

³Each word consists of 8 data bits and 1 acknowledge bit.

The OTIS chips do count the number of accepted and rejected L0 trigger signals as well as the number of completed data output sequences. 8 LSBs of each counter are available through the `ReceivedT`, `RejectedT` and `EventID` registers. The first two counter registers can be reset through an I²C-write access. The `EventID` register is reset via the L0 `EventID` reset signal. If there is no pending readout (i.e. the derandomizer buffer is empty) and none of the counter registers has been individually reset, then `ReceivedT = EventID` applies (except for possible counter overflows). For the same conditions, the total number of trigger signals sent to the OTIS chips must be equal to `ReceivedT + RejectedT`. In principle, the `ReceivedT` and the `EventID` registers do count the same occurrences, but the difference is based on the integration of the counters in two different state machines: the pipeline control and the readout control state machine. In contrast to the service pads, the counter registers are not suitable for online monitoring. This is because the I²C-access is operating asynchronous to the LHC clock signal.

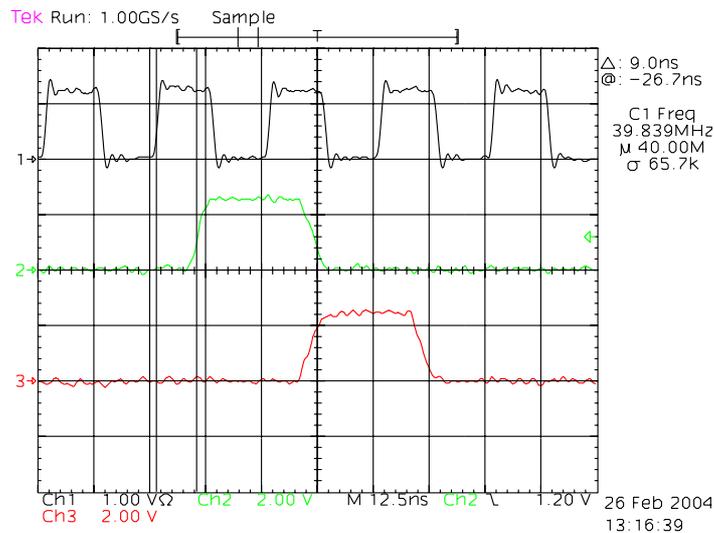


Figure 4.11: Timing of the service pad outputs with respect to the external clock signal (OTIS1.1). Channel 1: Clock. Channel 2: Zero-crossing of the pipeline write pointer. Channel 3: Zero-crossing of the pipeline read pointer.

5 Chip Characterisation

The goals of this study are, besides development and integration of the OTIS control core, the initial startup and the characterisation of the different test- and prototype chips of the OTIS project¹. This chapter focuses on measurements with the actual version of the TDC chip OTIS1.2. Results from measurements with previous chip versions are not listed herein.

The scope of the measurements at the laboratory includes acceptance tests and performance measurements. The acceptance tests basically address the functional range of the two digital cores (e.g. I²C data transfer, main operation modes or debug features) but they also deal with the TDC core of the OTIS chip (e.g. lock lost detection). The performance measurements mostly regard the analogue TDC core and result in figures for the differential and integral non-linearity (DNL, INL). The test setup at the laboratory provides the infrastructure for chip operation and data acquisition but does not include detector modules, ASD discriminator chips or the GOL serialiser chip. At maximum three OTIS chips can be operated in parallel in this setup. In the meantime, the OTIS chips also proved to operate error free in a medium scale cosmic ray test setup that included detector modules and ASD discriminator chips and in a full scale test beam setup that additionally included the GOL serialiser chips, optical data transmission and DAQ. The tests are summarised in chapter 6.

This chapter starts with the description of the two experimental setups that were used for the laboratory chip tests. Then selected results from the acceptance and performance tests are presented.

5.1 Experimental Setup

Chips from a pilot run or a Multi-Project Wafer (MPW) production are delivered as single bare dice. These need to be mounted and connected to a Printed Circuit Board (PCB) before measurements can start. A PCB has been developed for this purpose (see schematic in appendix A).

Figure 5.1 shows the OTIS chip mounted and connected to the test carrier. Conductive adhesive glues the chip to the PCB and connects the chip substrate to **gnd**. Bond wires (25 μm diameter) provide the connections to all inputs and outputs of the chip.

The test PCB is able to accommodate one chip plus the external blocking components for the supply voltages. Apart from the chip and an optional output signal buffer, the test board only carries passive components such as pull-up resistors, LVDS terminating resistors, block capacitors and choke coils. The PCB provides strips to interface to every input and output of the OTIS chip and it features jumper based configuration of the quasi-static chip inputs such as the TDC- or I²C-identification numbers. Furthermore the carrier makes the output signals of the TDC chip available on a dedicated interface ready to connect to a logic analyser system.

Figure 5.2 shows a schematic representation of the laboratory test setup. The chip operation without LHCb Timing and Fast Control system (TFC), without detector modules and dedicated data acquisition requires to emulate the experimental environment.

¹A detailed record of all chips manufactured for the OTIS project can be found in appendix C.

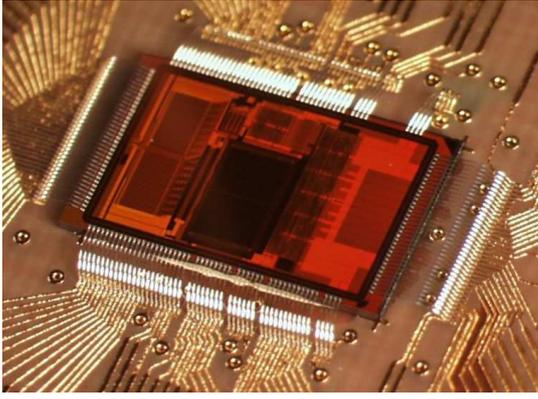


Figure 5.1: Device under test: OTIS Chip glued and connected to the test PCB.

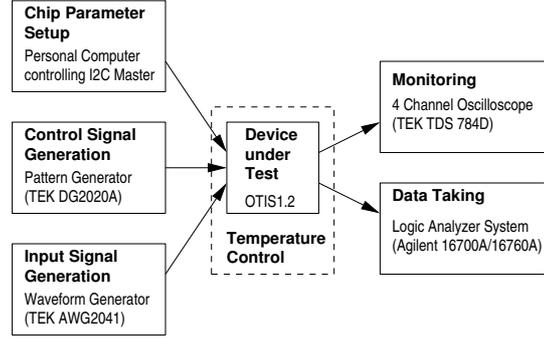


Figure 5.2: Schematic view of the laboratory test setup.

Name	Explanation	Min.	Typ.	Max.	Unit
vdd, vdd_* ²	Positiv digital supply	2.2	2.5	2.7	V
vdda	Positiv analog supply	2.2	2.5	2.7	V
gnd	Detector ground	-0.2	0	0.2	V

Table 5.1: DC characteristics of the OTIS chip

DC Characteristics and Signal Levels The OTIS chip needs two positiv operating voltages: analog and digital supplies of nominal +2.5V with respect to Ground (**gnd**, 0V) each. The operational range of **vdda** and **vdd** is predetermined by the manufacturing process. Minimum, maximum and nominal values for the supply voltages are listed in table 5.1.

The OTIS chip has 3 different types of I/O pads: I²C, CMOS and LVDS. The signal levels for these pads are given in table 5.2. Commercially available I²C devices usually operate at +3.3V or +5V. The OTIS chip therefore features 5V compliant I²C-pads. The chip can directly interface with commercial 3.3V or 5V I²C-controllers.

Control Signal Generation The control signals (clock, resets and trigger) and the discriminated detector signals are produced by a pattern and a waveform generator. The I²C-bus communication is driven by a bus master device that is controlled through a personal computer. Both signal generators are compatible with the LHCb requirements: 40 MHz clock speed, 1 MHz trigger rate and up to 16 consecutive trigger signals can be produced as well as input signals with variable pulse width and adjustable rate.

The input signals can either be generated by the pattern generator or the waveform generator. The first option provides an adjustable but then fixed-phase alignment between clock signal and trigger³ or input signal. The second option, where both generators run independently from each other, can be used to produce input signals with varying phase alignment with respect to the clock signal.

Various parameters of chip operation can be controlled within this experimental setup. The pattern generator for example produces a low jitter clock signal (<50 ps_{p-p} at 200 MHz, typical) and allows frequency adjustment in kHz steps within the desired range from 30 to 50 MHz. The generator outputs can be shifted against the clock signal in quarter period steps and two dedicated channels allow for additional delays from 0 to 20 ns in 0.1 ns steps.

²any power supply net having a name starting with **vdd_**

³The OTIS chip uses the negative clock edge to sample the trigger signal

I ² C							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	7.0	2.5	V
output	—	—	0.0	—	—	2.5	V
CMOS							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.4	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
LVDS (100Ω termination)							
	offset voltage			differential voltage			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	0.0	2.5	1.2	0.1	2.5	0.2	V
output	—	—	1.02	—	—	1.38	V

Table 5.2: Specification of signal levels

The setup furthermore allows to individually set the different supply voltages for the OTIS chip and to control the environmental temperature.

Data Acquisition and Monitoring A four-channel oscilloscope is used for the monitoring of additional signals such as the debugging signals from the service pads, the DAC outputs or the V_{ctr1} or `LastDummyOut` signals from the DLL.

As a substitute for the L1 data acquisition stage that would follow the OTIS chip in the experiment, the described setup uses a logic analyser system for data processing and data storage. This system allows to selectively store triggered data output sequences, to examine transferred header and data bytes or to build histograms of single-channel drift time data.

Random Trigger Generation The described experimental setup lacks the possibility to generate random trigger sequences. But operating one or more OTIS chips with randomly generated trigger signals is helpful for testing the digital control core of the chip, especially the memory and trigger management parts. In the LHCb experiment, the trigger signals are distributed through the TFC system which transmits the trigger signals in phase to the rising clock edge. A random trigger generator should therefore produce random sequences of clock synchronous pulses at an overall rate of 1 MHz. For this purpose a second setup is used. This setup includes a noise source plus discriminator for pulse generation (see figure 5.3).

Compared to the above mentioned setup, the FPGA based ACEX board [TI02] (figure 5.4) is used for clock and reset signal generation instead of the pattern generator. The ACEX board is an educational multi-purpose test PCB that is designed for prototyping and data acquisition in combination with a personal computer. It features on-board SRAM and oscillator, it allows VGA output or to interface to a PCI bus and it provides LVDS and single ended connections to the CPLD. In the OTIS chip test setup, the FPGA provides control signal generation and trigger pulse synchronisation. It is additionally programmed to calculate and display the accumulated trigger rate and to count and display the number of trigger signals produced since the last reset. In this second setup, the chips under test again receive their register setup through the computer driven I²C-master, and again, a logic analyser

5.2 Acceptance Tests

A newly developed and highly integrated system such as the OTIS chip needs extensive verification before producing a successor version or before starting the large-scale production. During this phase chip testing centres around detection of design errors and faults in the circuit. Due to the large amount of applicable test vectors, the pilot run testing is time-consuming and consists of a large number of single, not automated test sequences. Towards large-scale production, the test sequences evolve into an automated test procedure that allows to select the chips that are qualified for use in the detector modules.

The following paragraphs present a selection of results from acceptance tests with the chip version OTIS1.2. These tests cover the chips basic functionality range and are likely to be included in the automated test procedure on the wafer prober station.

5.2.1 Power Consumption

The power dissipation in the LHCb detector is of big concern because of the need for a cooling system to compensate heating. Current estimations result in a power dissipation of about 25 W per Outer Tracker front-end box [Slu02]. This includes the ASDblr, OTIS and GOL chips and the low-voltage regulators.

Table 5.3 lists the electric power consumption of the analogue and digital power nets of the OTIS chip. After a power up reset, when all configuration registers are set to zero,

Status	Powernet	I [mA]	P [mW]
Power Up	vdda	2 ± 1	
	vddd	223 ± 5	
	Total	225 ± 5	563 ± 13
Operating	vdda	4 ± 2	
	vddd	263 ± 10	
	Total	267 ± 10	668 ± 30

Table 5.3: OTIS chip power consumption after power up and during operation.

the total power consumption is 563 ± 13 mW. It is assumed that in this state the OTIS chip does not receive a clock signal and that the threshold of all ASDblr DACs is set to 0 V. During operation, i.e. the OTIS chip is configured, receives a 40 MHz clock as well as detector and trigger signals and the ASDblr threshold levels are set to 500 mV, the total power consumption of the chip is 668 ± 30 mW. The figures given in table 5.3 are based on a random sample of five OTIS1.2 chips that all operate at room temperature. The measuring error of the amperemeter is $\pm 2\%$.

First results from the routine tests of the ATLAS preprocessor ASIC and the Beetle chip show that narrow confines for the chips power consumption can be used as exclusion criteria for the chips under test. It should be considered to search for and to use similar cuts in the measured power consumption as exclusion criterion for the OTIS wafer test too. First of all this would help speeding up the test procedure, because following tests can be skipped if a chips power consumption outranges the defined interval. Second, with a test coverage of less than 100% in mind, predefined cuts in the power consumption may exclude defective chips too.

5.2.2 DLL Locking

Figure 5.6 presents the developing of the control voltage V_{ctrl} of the DLL with the lock frequency for different temperatures. The stated temperatures refer to the ambient temperatures that are controlled by an oven which surrounds the test PCB. To represent the actual temperatures at the surface of the chip, 15 to 20°C must be added to the surrounding temperature.

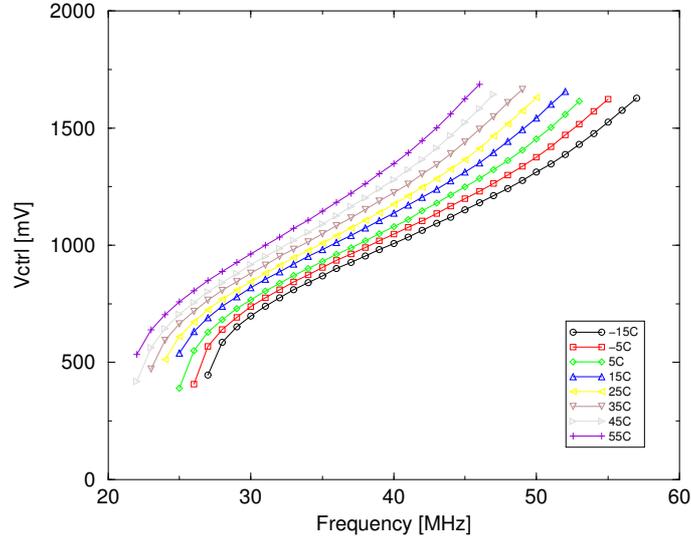


Figure 5.6: DLL control voltage as a function of the locking frequency with ambient temperatures as curve parameter. The DLL reliably locks from 28 MHz to 45 MHz for a temperature range from -15°C to 55°C.

The dynamic range of V_{ctrl} of approximately 1 V ranging from 600 to 1600 mV combined with temperatures ranging from -15°C to 55°C results in a frequency range from approximately 28 to 45 MHz in which the DLL reliably locks. For the chip temperature of 45°C, which the design is based upon, the locking frequencies range from 24 to 50 MHz.

Once the DLL reached a stable lock state, it has never been observed that the TDC core loses its lock. For all temperatures, the upper bound of the locking frequency range tends to be lower than expected. The downward shift of the upper frequency limit is possibly a first sign of the DLL length mismatch found by the performance measurements that follow in section 5.3.

Proper DLL locking should be investigated within an automated test procedure. This should include initial DLL locking after power up as well as re-locking after an external (I²C) DLL reset. Additionally the DLLs control voltage should be measured while in reset and while in lock state. Under controlled conditions (namely ambient temperature and operating frequency), the control voltage allows to rate the impact of process parameter variations. But as the chip internal DACs and comparators depend on process variations too, the logging of the control voltage should not rely on the internal lock lost detection circuitry. The automated test setup should therefore include appropriate analog to digital converters (ADCs).

5.2.3 Plain Hitmask and Encoded Hitmask Mode

Figure 5.7 shows an exemplary recording of a data output sequence of the OTIS chip while operating in the plain hitmask mode. The visible section of the recording spans 50 clock cycles and between markers G1 and G2 the data from 36 clock cycles is shown. Next to the eight data bits that are labelled from Data 0 (LSB) to Data 7 (MSB), the figure additionally presents the DataValid signal plus the two service pad signals that are programmed to indicate start and stop of any data transfer.

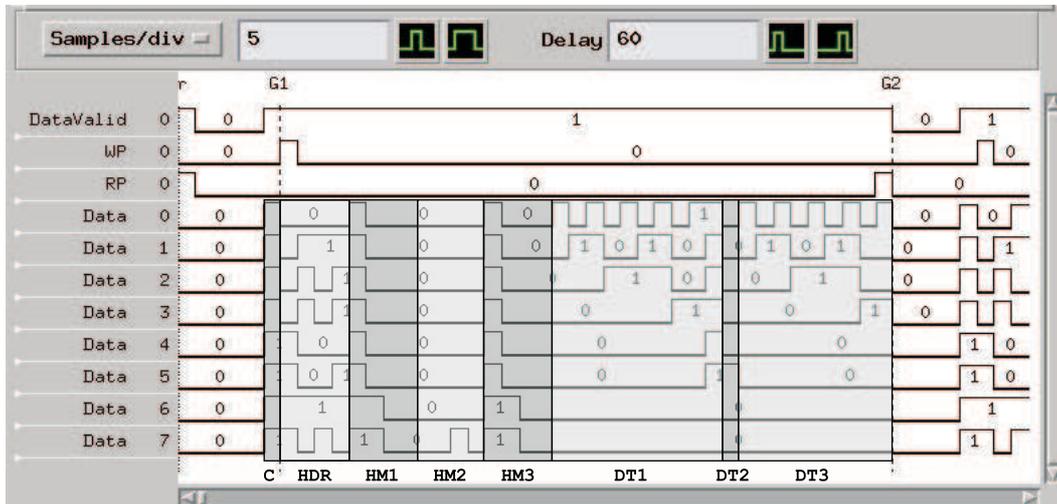


Figure 5.7: Recording of a data output sequence while operating in the plain hitmask mode. The different header, hitmask and drift time sections are alternately greyed for the ease of orientation.

While the service pads only provide signals for monitoring purposes, the DataValid output actually drives the DataAvailable input of the GOL chip. This is why the DataValid signal encloses the Comma byte (0xFF left to marker G1) but the start and stop signals from the service pads do not.

Figure 5.7 presents output data that results from the processing of arbitrary playback data in the plain hitmask mode. The triggered data output starts with the Comma byte followed by four header bytes (labeled HDR at the bottom of fig. 5.7). The three blocks of four data bytes each represent the binary channel hit information covering the full search window size of three bunch crossings. Now, in the order that is given by the hitmasks, the corresponding drift times follow. The structure of the pre-pipeline register only allows to use two different sets of playback data. In this case, the applied playback data is:

Data Set	1					2
Channel	0	1	...	8	9	16
Drift Time	1	2	...	9	63	32

All channels that are not listed in the above table, have no drift time assigned and are therefore suppressed in the plain hitmask mode. The two data sets are alternately written to the pipeline, and any arriving trigger signal results in a transmission of either 12 or 21 drift times. For the recorded data sequence, the trigger and search window combination resulted in 21 drift time bytes. However the data transmission omits the last byte (BX 3, channel

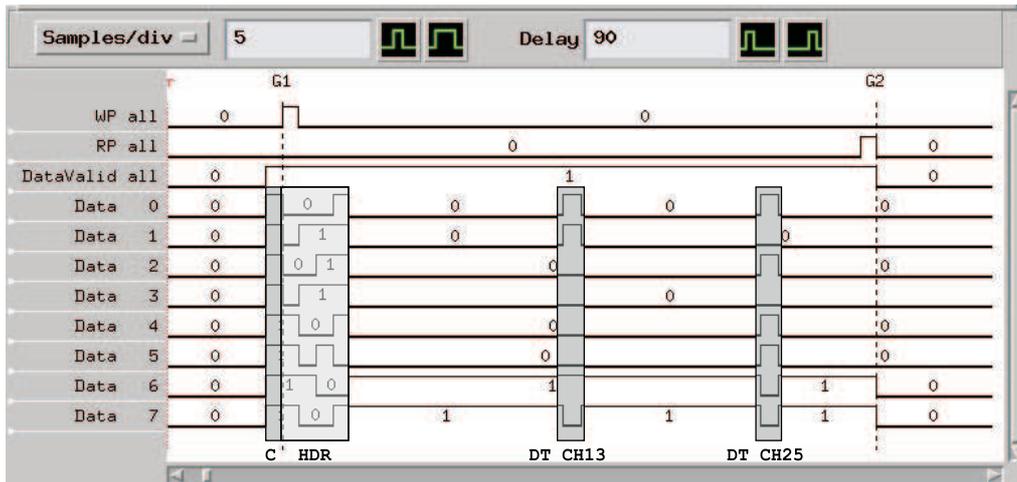


Figure 5.8: Recording of a data output sequence while operating in the encoded hitmask mode. The four header bytes are followed by 32 drift time bytes. Only the channels 13 and 25 show a valid hit and drift time code: `0x43` and `0x35`, all other channels show the out of range code `0xC0`.

9, drift time 63) because of the selected truncation option that prevents exceeding the given readout frame of 36 bytes.

Figure 5.8 shows a sample data recording for the encoded hitmask mode. Here, 32 bytes of combined hit and drift time information follows the four header bytes. All channels but two show the out-of-range code `0xC0`. Only the bytes that represent channels number 13 and 25 carry valid drift times: `0x43` (or 26.2 ns) and `0x35` (or 20.7 ns).

The data processing part of the OTIS chip has been checked in detail for both operation modes (plain and encoded hitmask mode) for all three possible search window sizes. More than 10^{11} trigger signals have been applied to the chips. The processed channel hit and drift time data either resulted from measurement within the TDC core or originated from the pre-pipeline register bypassing the analogue part of the chip. The applied trigger sequences range from manually initiated single trigger signals to regularly or randomly generated triggers. In all cases, the processing unit generated the expected data output sequences. That is, correct output frame length and correct encoding of the header data, the hit and the drift time information.

5.2.4 Drift Time Scan

The results from an exemplary drift time scan is shown in figure 5.9. The diagram shows the measured and encoded drift times of one channel for externally generated input signals. The applied signals show a time alignment that ranges from -2.6 ns to $+77.4$ ns with respect to the reference clock signal. For this recording, the OTIS chip operated in the encoded hitmask mode with a search window of three bunch crossings. The resulting drift time codes seamlessly touch at the two bunch period boundaries and give the no hit information (out of range code `0xC0`) for input signals that are out of the measurement range.

The first full-scale prototype chip OTIS1.0 showed missing drift time codes in the second half of the basic measurement range. Weak driver strengths and underestimated parasitic capacitances were identified to lead to timing violations within the TDC core and at the interface between TDC core and pre-pipeline register. This resulted in missing drift time codes despite the correct input signal sampling and correct generation of the corresponding

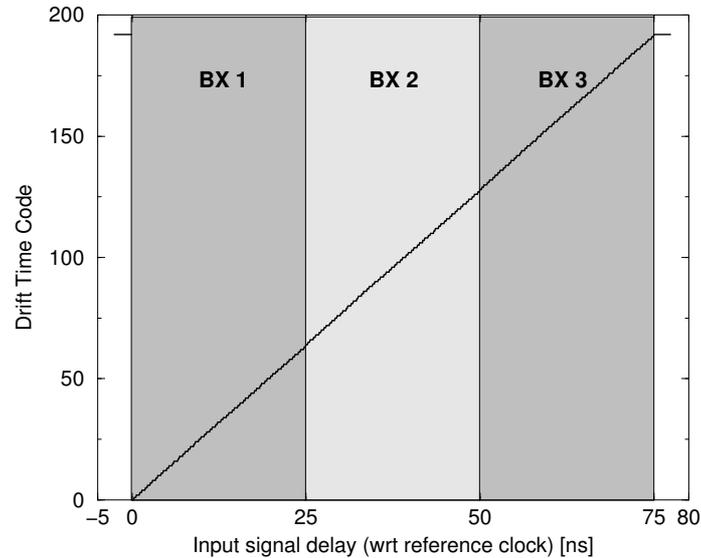


Figure 5.9: Resulting TDC output codes for input signals that cover the full scale range. Outside of the greyed measurement range, the drift times show the out of range code 0xCO.

binary hit information. Simulations helped tagging driver strength and parasitic capacitances as sources of failure. The simulation results could successfully be confirmed with a FIB (Focused Ion Beam) patched chip, which allowed external adjustment of the incorrect interface timing. The FIB circuit modification cut through two clock lines and created two new connections instead, thus allowing for external clock line control. See section 5.5 for more details concerning the FIB patch.

An automated test setup should check for the correct encoding of the header information plus, depending on the selected operation mode, the correct encoding of the hit and drift-time information. Special trigger sequences in combination with arbitrary playback data allow detailed checks of both data formats including tests regarding the LHCb requirements (e.g. dead time free operation or fixed readout time).

5.2.5 Trigger Handling

The correct operation of the trigger managing part of the digital control is not directly accessible for test opposed to for example the correct encoding of the header information. Nevertheless, indirect consistency checks have been done by using the different counter registers the OTIS chips provide. The random trigger test setup for example checked if the number of generated trigger signals matches the sum of the received and rejected trigger counters. This and other consistency checks that include counter registers of the OTIS chip are limited by the fact that the counters are only 8 bit wide. Additional to the received and rejected trigger numbers, known trigger sequences have been used to check if the therefrom generated data output sequences showed the expected bunch crossing and event identification numbers. This allows for the statement that accepted trigger signals correctly act on the provided data sets.

Three times two OTIS chips have proven to operate for more than 10 hours (consuming more than $4 \cdot 10^{10}$ random trigger signals) each without losing any trigger signal. The readout

interfaces of the chips did not run out of sync for both operation modes. Additionally, the counter registers of both chips were identical and added to the expected values.

In the LHCb experiment, the readout supervisor will not issue trigger signals that would cause an overflow of the derandomizer buffer. But the described random trigger test setup does not check for or suppress trigger sequences that overflow the buffer. For that case, the TDCs control core declines the acceptance of trigger signals as soon and as long as there is not enough free capacity left in the derandomizer to store the next triggers data sets. The decision to reject a trigger signal is solely based on the actual derandomizer buffers fill level and the selected search window size. This scheme also rejects trigger signals that would transfer less data sets to the derandomizer than the search window depth indicates.

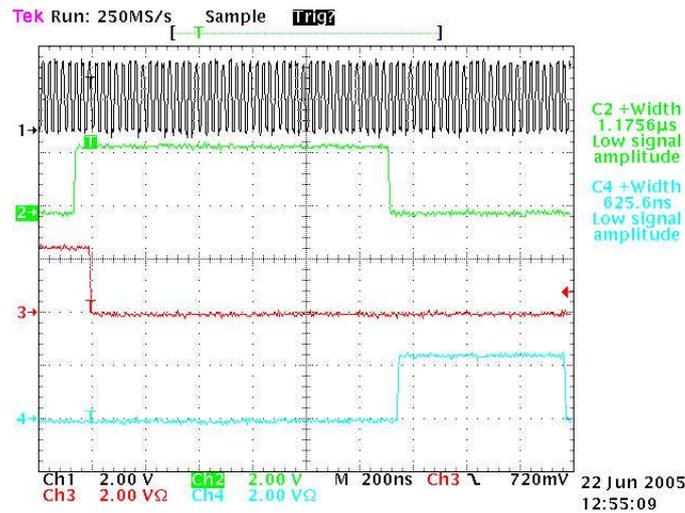


Figure 5.10: Recording of 47 subsequent trigger signals that fill the chips derandomizer buffer (encoded hitmask mode, 2 BX search window size). The displayed signals are: clock (channel 1), trigger (channel 2), BufferEmpty (channel 3) and BufferFull (channel 4).

Correct trigger rejection depends on the correct fill level calculation. This can be checked by observing the BufferEmpty and BufferFull flags at the service pads while applying trigger sequences that are known to overflow the derandomizer. Figures 5.10 and 5.11 show recordings of these two service pad signals plus the corresponding trigger and clock signals. For recording 5.10 the OTIS chip operated in the encoded hitmask mode with a search window size of two bunch crossings. Starting from an empty derandomizer buffer, the chip receives 47 consecutive trigger signals (recorded on channel 2; positive width ≈ 1175 ns or 47 clock cycles). The first trigger signal causes the BufferEmpty signal (channel 3) to change from one to zero, that is the derandomizer buffer is not empty any longer. The time difference between the rising edge of the trigger signal and the falling edge of the BufferEmpty output results from the trigger sampling of the TDC chip and the output delay of the service pad. Upon reception of the 47th trigger signal, the BufferFull signal (channel 4) changes from zero to one, i.e. the memory allocation of trigger number 47 fills the derandomizer buffer to an extent that there is no capacity left to store a next data set of a following trigger. In fact, after reception of trigger number 47, the derandomizer fill level is 47: the first trigger allocates two rows and the 46 following (consecutive) triggers allocate 46 rows. Additionally one row can be freed within 47 clock cycles due to the completion of one data output sequence. A fill level of 47 does not provide enough derandomizer rows for a next triggers data set which would allocate two rows in this operation mode.

The positive width of `BufferFull=1` is 25 clock cycles what exactly corresponds to the completion of readout sequence number two which happens 72 clock cycles after the reception of the first trigger signal. Recording 5.10 does not show the clearance of the derandomizer buffer. This in fact happened $42.3\ \mu\text{s}$ after the trigger signals started to fill the derandomizer buffer what corresponds to 47 complete readout sequences.

Figure 5.11 shows a similar recording for a sequence of 17 separated single trigger signals. The separation of the trigger signals is such that every trigger allocates the maximum of three rows in the derandomizer buffer. For this recording, the chip operated in the plain hitmask mode with a search window size of three bunch crossings and activated truncation option. The truncation of the readout sequences in the plain hitmask mode uniformly sets the length of all readout frames to 36 bytes. This in turn allows exact fill level calculations. Again, the first trigger signal allocates the first three rows from the derandomizer and thus sets the fill level to 3. Every following trigger further allocates three rows and adds 3 to the fill level. The fill level, after the reception of the 16th trigger is 45 (one set of three rows has already been freed) and the 17th trigger of this example fills the derandomizer buffer. Again the positive width of `BufferFull=1` and the negative width of `BufferEmpty=0` correspond to the times until the second respectively the 17th readout sequence finishes.

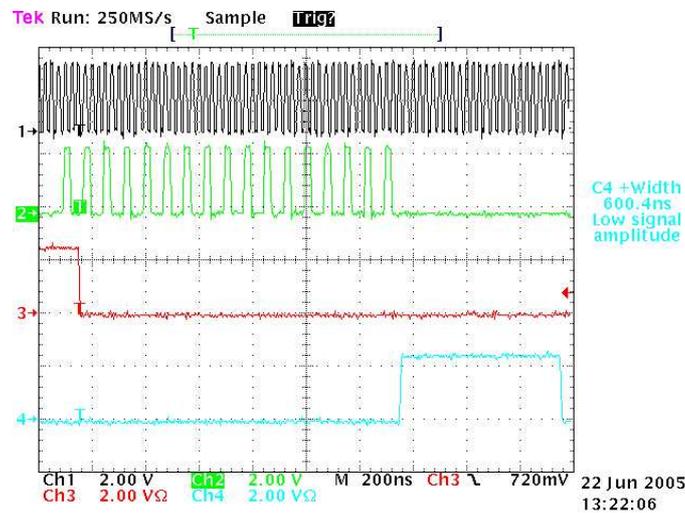


Figure 5.11: Recording of 17 separated single trigger signals filling the chips derandomizer buffer (plain hitmask mode, 3 BX search window size). The displayed signals are: clock (channel 1), trigger (channel 2), `BufferEmpty` (channel 3) and `BufferFull` (channel 4).

The tests concerning the derandomizer buffer and its correct overflow for a given predetermined trigger sequence can be combined with the test procedure that checks the output data encoding. When combined, both tests cover the default data path through the OTIS TDC (pre-pipeline register, L0 pipeline, derandomizer buffer and control core) and include the longest signal paths of the control core (fill level calculation). It is strongly recommended to include derandomizer overflow checks in an automated test setup.

5.3 Performance Tests

The performance tests mostly deal with the TDC core of the OTIS chip. They result in figures for the resolution, the integral and the differential nonlinearity of the drift time

measurement of the TDC. Hence, the performance measurements provide information about the chips qualification for its use in the LHCb experiment.

While the acceptance tests deal with predetermined test vectors, for example a given trigger sequence or a known correlation between clock and input signal, the determination of performance figures relies on the application of a large number of input signals with random phase relationship with respect to the clock signal. An equal distribution of the input signals then ideally causes an equal distribution of the measured drift times. This allows to calculate the bin sizes of the DLL and further, it allows for the determination of the differential and integral nonlinearity. Clock, trigger and other control signals are still generated by the Tektronix Pattern Generator, the random input signals are generated by a second, independently running signal generator (Tektronix Arbitrary Waveform Generator). This way, input and control signals are derived from two different reference oscillators. Thus both signals show a varying phase relationship. The setup operates at a trigger rate of 1 MHz and a input signal rate of approximately 5 MHz. This allows to build drift time histograms with 10^6 entries within seconds.

5.3.1 DLL Jitter

Delay locked loops are by design sensitive to jitter on the reference clock signal [Lee03]: the phase detector can not distinguish between jitter on the reference input or the delayed signals input. Therefore a reference signal jitter can temporarily be amplified until it propagates through the DLL. Thereafter, the control loop accordingly adjusts the propagation delay of the DLL.

The OTIS chip provides access to the delayed reference signal after the last dummy delay stage `LastDummyOut`. This allows to measure the jitter that is introduced by the DLL. The period jitter measurement uses two consecutive rising signal edges as start and stop of the oscilloscopes data sampling. The histogram of the switching points of the second edges then directly allows to extract the jitter figures of the DLL. These numbers represent the RMS calculation of the difference of each period from the waveform average and the peak to peak difference between smallest and biggest measured periods.

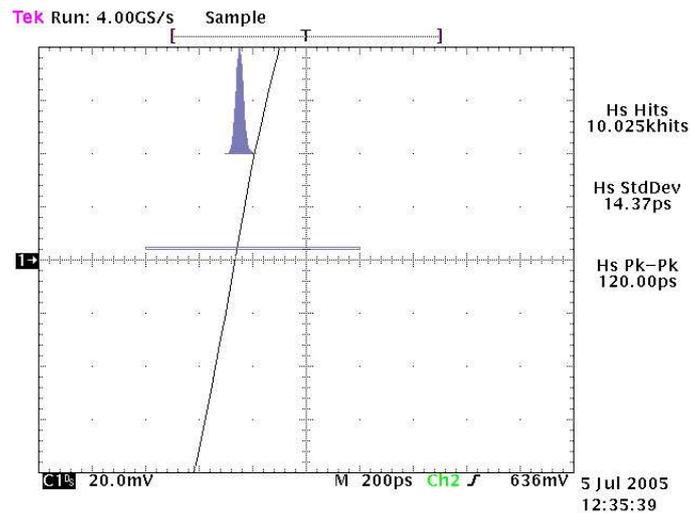


Figure 5.12: DLL period jitter measurement. The display only shows a detail of the rising edge of `LastDummyOut`, the zero-point defining `Clk` signal is blanked out.

Figure 5.12 shows the screenshot of a sample jitter measurement. The picture displays the magnified `LastDummyOut` signal (channel 1) plus the gaussian shaped histogram together with the underlying histogram limits box. Figure 5.12 does not show the triggering clock signal that defines the virtual zero-point of this measurement. Though present, this signal has been blanked from the screen output in order not to decrease the oscilloscopes sampling rate.

The resulting histogram contains 10025 entries that populate 30 bins. At the given time base of 200 ps per axis grid, the histogram bin size evaluates to 4 ps. The RMS jitter of the presented example evaluates to $J_{\text{RMS}} = 14.4$ ps and the peak-to-peak jitter to $J_{\text{P-P}} = 120$ ps. Table 5.4 lists two more results from the jitter measurements that vary in the configuration of the two edges that define the measuring period. The amount of underlying data samples always exceeds 10^4 and the bin size of all three histograms is 4 ps.

Measurement		J_{RMS} [ps]	$J_{\text{P-P}}$ [ps]
from	to	(10^4 samples)	(10^4 samples)
n^{th} Clk	$n+1^{\text{st}}$ Clk	14.9	116
n^{th} Clk	n^{th} LDO	14.4	120
n^{th} LDO	$n+1^{\text{st}}$ LDO	14.6	116

Table 5.4: Results from different Clk and DLL jitter Measurement. The quoted values are dominated by the resolution of the measurement setup.

The use of the oscilloscopes histogramming function results in RMS jitter figures that are smaller than the given oscilloscopes (single shot) time measurement accuracy of 37.5 ps. That is, at the present setup, the measurement of the clock signal jitter and the period jitter of the output signal of the DLL is dominated by the oscilloscopes sampling accuracy. The DLL does not visibly add to the incoming clock jitter within one clock cycle.

5.3.2 Code Density Tests

A code density test (CDT) is a commonly used measuring procedure that uses histogram testing to determine the nonlinearity parameters of the design under test. For data converter circuits such as ADCs or TDCs, these parameters are the differential and the integral nonlinearities (DNL and INL). During this code density test, equally distributed input signals are applied to the TDC that in turn generates a corresponding distribution of digital codes at its output.

Deviations from the expected output code distribution result in various errors that can be described with the extracted DNL and INL parameters. The differential nonlinearity characterises the differences in the sizes of the least significant bits of the characteristic curve of the TDC. The integral nonlinearity in turn measures the maximum deviation of the TDCs real characteristic curve from its ideal transfer characteristic. Both figures are most commonly quoted in picoseconds respectively in least significant bits.

The OTIS TDCs basic measurement range is 25 ns with a resolution of 6 bit. Additionally, the digital control core allows to measure time intervals up to 75 ns by using two extra bits that indicate the full scale range (FSR) multiplier. But as only information from the time measurement unit is relevant for the CDT, it can be restricted to only use the six least significant bits of the output codes of the TDC. That is, the histogram needs 64 bins to cover the basic measurement range of the TDC.

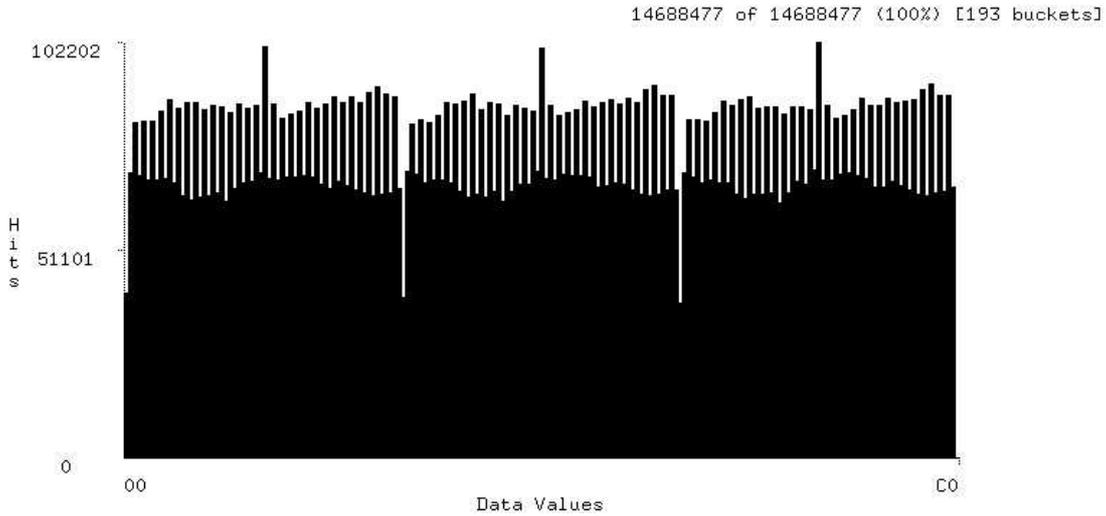


Figure 5.13: Sample full scale range drift time code histogram. The diagram shows the expected even-odd bin size structure but also unexpected deviations in bin no. 0 and 31 (repeating three times due to the 3 BX measurement range).

The present setup allows to build histograms with a bin population of the order 10^5 within seconds. Again, clock and control signals are provided by the pattern generator, while the second, free running generator produces the input signals for the TDC. The logic analyser system is responsible for data acquisition and only needs minor adjustments when the operating parameters of the TDC (address, readout mode, channel numbers) change.

DLL Bin Sizes

A sample histogram of output codes is shown in figure 5.13. This histogram shows the recordings of a single channel (OTIS1.2, chip 4, channel 15) while operating at an ambient temperature of 35°C . This histogram contains 1.5×10^7 entries spread over 192 bins (the reduction to the 6 bit wide measurement range of the TDC has not been accomplished yet).

The histogram entries represent the bin size structure of the TDC f always one small and one large bin. This structure is due to the different capacitive load between even and odd numbered inverter stages within the delay chain of the DLL. It has not been intended to balance the even-odd asymmetry of the time bins.

The DLL is designed such, that the delay chain starts with a large and stops with a small time bin. It appears that the first histogram bin from this recording tends to show less entries than the mean small time bin does, though it is considered to be a large time bin. Other measurements confirm this behaviour for the channels 0 to 15. Similarly, the bin number 31 tends to show more entries for the first half of the TDC channels. The second half of channels in principle shows the same behaviour but less distinct. A detailed explanation of the rational causing these effect follows below.

Granted that all 64 time bins exactly cover the basic measurement range of 25 ns, the single time bin sizes t_i (in ns) can be calculated by multiplying the fraction of the number of entries for bin i to the total number of histogram entries by 25 ns:

$$t_i = \frac{N_i}{\sum_i N_i} \cdot 25 \text{ ns} \quad (5.1)$$

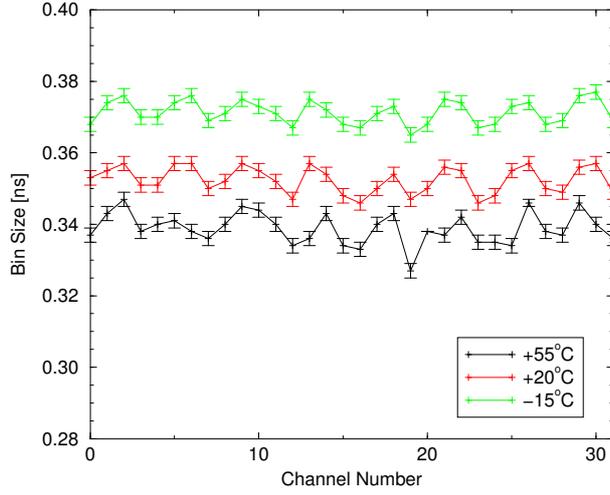


Figure 5.14: Measured bin sizes (small bins) vs. channel number for different ambient temperatures.

Without excluding bin 0 or bin 31, the mean small and large bin sizes results to In both

$$\begin{aligned} \text{TDC-Bin}_{\text{small}} &= 342 \pm 2 \text{ ps and} \\ \text{TDC-Bin}_{\text{large}} &= 438 \pm 2 \text{ ps.} \end{aligned}$$

cases the quoted errors originate from the statistical uncertainties $\sqrt{N_i}$. All the resulting (small) bin sizes for channels 0 to 31 are shown in figure 5.14 as a function of the channel number and three ambient temperatures as parameter. Each bin size characteristic exhibits a periodic structure that repeats every fourth channel. This can be explained with the layout of the buffer trees that drive the DLL taps for always four channels. The bin sizes drop by approximately 35 ps when the ambient temperature rises from -15 to +55 °C. As the bin size calculation assumes a fixed DLL length of 25 ns, the corresponding large bin sizes grow by the same amount for this temperature step.

Differential Nonlinearity

The histogram of the drift time codes can be corrected for the even-odd-time bin asymmetry by using the ratio of the mean numbers of bin entries for large and small time bins as scale factors. With this bin size correction, the deviation of bin number 0 even grows: being a large bin by design, its number of entries get further scaled down.

Starting from the CDT distribution of fig. 5.13), the resulting bin size corrected histogram is shown in the upper half of figure 5.15. The lower half of this figure shows the therefrom calculated bin size differences between bin number i and its preceding bin $i-1$ (note the wrap around from bin 0 to bin number 63). Now the DNL calculates as the sum of the maximum bin size difference and the absolute value of the minimum bin size difference:

$$DNL = |\max\{\Delta_i\}| + |\min\{\Delta_i\}| \quad (5.2)$$

For this sample, the DNL evaluates to

$$\begin{aligned} DNL &= (1.11 \pm 0.04) \text{ bin or to} \\ DNL &= (440 \pm 20) \text{ ps.} \end{aligned}$$

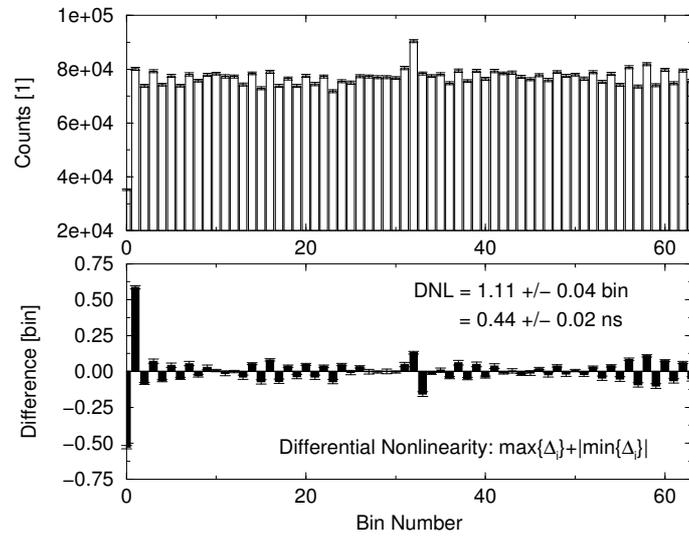


Figure 5.15: Bin size corrected drift time code histogram and differences between subsequent bins (chip 4, channel 15).

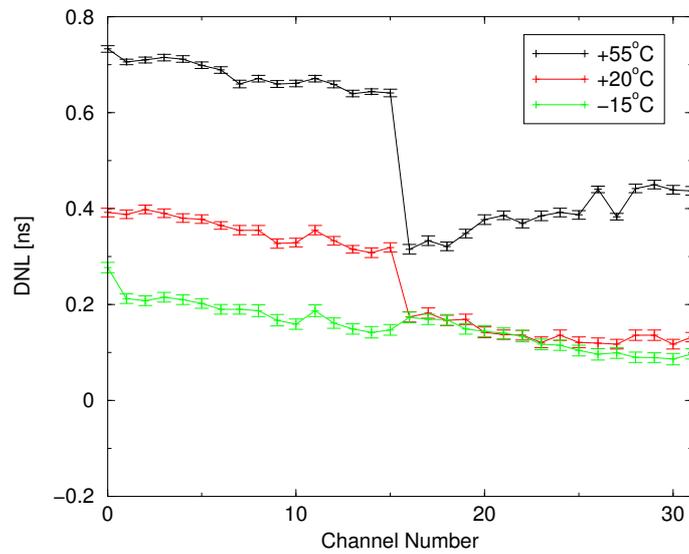


Figure 5.16: Differential nonlinearity vs. channel number for three different ambient temperatures.

The DNL figures of the channels 0 to 15 are determined by the already known bin size deviations of the first time bin. For the channels 16 to 31, this time bin 0 deviation only dominates the DNL for ambient temperatures greater than approx. 20°C. Below that temperature unclassified bin size variations contribute to the DNL figures.

The relatively large differential nonlinearity is of no consequence for the intended application of the OTIS chip in the LHCb Outer Tracker. The measured drift times can be corrected for example by using look-up tables in the following L1 electronics stage.

Diagram 5.16 presents each channels DNL figure (in ns) as a function of the channel number and three ambient temperatures as curve parameter. The temperature dependent step between channel 15 and 16 is the described change in the DNL dominating effects for the second half of channels.

Integral Nonlinearity

The upper part of figure 5.17 shows every CDT histogram bin count number added to the previous bin entries (black crosses). The underlying straight red line represents the linear regression of those data points. That is, the regression line reflects the TDCs ideal full scale range linear digitisation characteristic. The integral nonlinearity now equals the maximum absolute value of all data point differences from this regression line:

$$INL = \max\{|\Delta_i|\}. \quad (5.3)$$

In this example the INL calculates to

$$INL = (0.29 \pm 0.01) \text{ bin}.$$

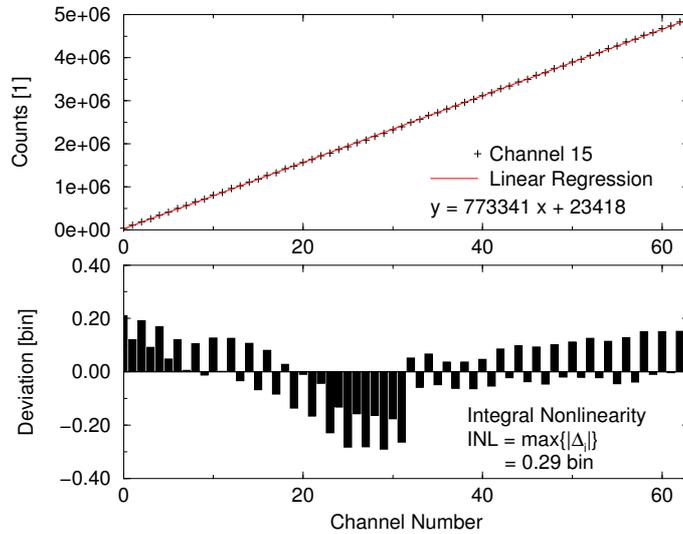


Figure 5.17: Best fit straight line through the accumulated histogram bin counts plus resulting differences between measurement data and linear regression. (chip 4, channel 15)

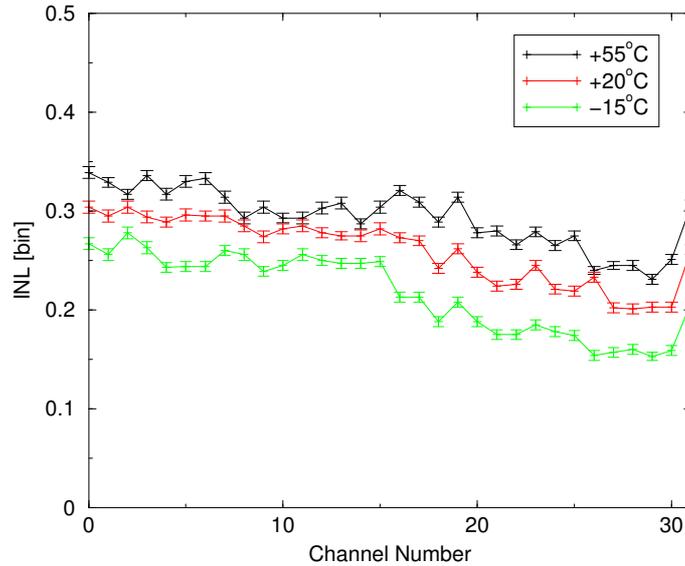


Figure 5.18: Integral nonlinearity vs. channel number for three ambient temperatures(chip 4).

Figure 5.18 shows the integral nonlinearities (in bin sizes) of all channels as a function of the channel number with three ambient temperatures as curve parameter. Like for the differential nonlinearities, the chips maximum INL is determined from channel number 0.

5.3.3 Time Bin 0/31 Deviation

The above described code density tests have revealed a systematic bin size deviation of bin numbers 0 and 31 of the histogram of the drift time codes. The differences compared to the expected bin sizes depend on the ambient temperature and the channel number. The chip supply voltage or the operating frequency can additionally affect the deviations (see below).

Two design features have been found to be responsible for the observed time bin deviations. The following paragraphs explain the two characteristics, describe a possible impact on drift time measurement and outline the design changes that correct the bin size deviations on next chip version OTIS1.3.

Design Features of the Phase Detector

First of all, in the delay locked loop, the two input paths of the phase detector (C1k and DC1k) are not properly balanced. This results in a small persistent phase difference between the two clock signals. Additionally, the phase detector and the charge pump of the DLL act as a proportional controller (see chapter 3.2.1) that always exhibits a small control deviation from the nominal value of zero phase difference between C1k and DC1k. The resulting offset from the nominal value leads to a misalignment of the lock frequency of the DLL respectively the propagation time of the single delay elements.

The excess in each delay elements propagation time accumulates to a DLL length that is greater than 25 ns. This - together with the fact that the DLL is not free-running - implicates that a new clock edge enters the delay chain before the previous clock edge reaches the last DLL tap. This affects the size of the first time bin because of the hit finder circuit that assigns hits to time bin 0 based on the content of the two involved hit registers (HR₆₃ and HR₀, see figure 3.10). Only the combination HR₆₃=0 and HR₀=1 evaluates to the drift time

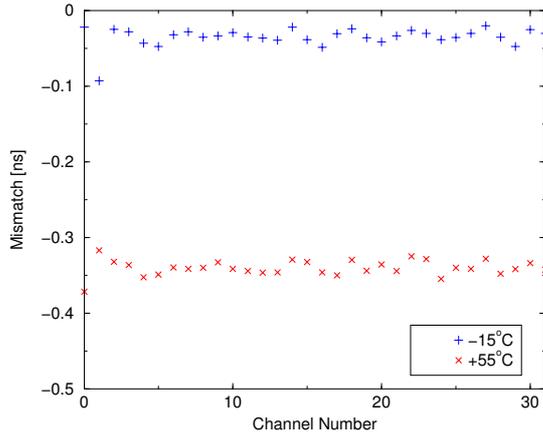


Figure 5.19: Measured time bin 0 length mismatch vs channel number for two ambient temperature.

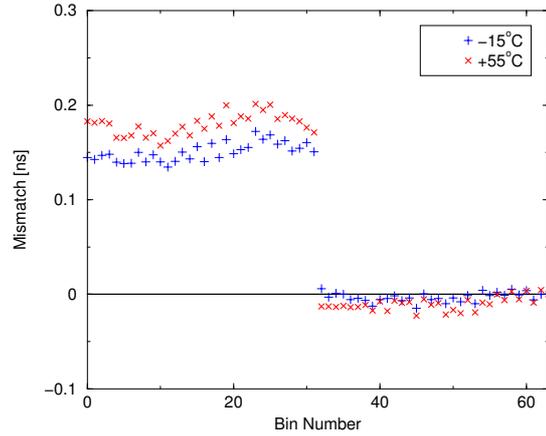


Figure 5.20: Measured time bin displacement between channel 15 and 16 vs. bin number for two ambient temperatures.

code 0. But exactly this hit register configuration is suppressed when the clock edge arrives late at DLL tap 63 with respect to the arrival of the following clock edge at DLL tap 0.

Figure 5.19 shows the measured length error of time bin 0 (in ns) for all 32 channels and two ambient temperatures (40 MHz clock frequency). The diagram shows a noticeable mean length error of approximately 35 ps at -15°C . This error rises to 340 ps for an ambient temperature of 55°C . The error is then close to the nominal size of a time bin.

Design Feature in the Channel Routing

The second design feature refers to the layout of the hit signal traces. The routing shows differences between the first and the second half of channels: the length of the hit signal trace between HR_{31} and HR_{32} changes by approximately $500\ \mu\text{m}$ from channel 15 to channel 16. This routing mismatch has been accidentally introduced during hit signal routing.

The routing difference between upper and lower half of channels effectively broadens the time bin 31 for the channel numbers 0 to 15 compared to the corresponding time bin of the other half of channels. As a consequence, the positions in time of bins 0 to 30 change between channel 15 and 16. Figure 5.20 depicts this circumstance: the measured time bin shift (in ns) between channel 15 and 16 is shown as a function of the bin number for two ambient temperatures. At a temperature of -15°C (resp. $+55^{\circ}\text{C}$), the measured mean time bin displacement between lower and upper channel half is approximately 150 ps (resp. 180 ps).

Visualisation of the Design Features

Both shortcomings of the OTIS1.2 design sufficiently explain the observed deviations of the TDC bins 0 and 31. The above mentioned effects are visible in figures 5.21 and 5.22 which show size and position of the different time bins (stacked on top of each other) for all 32 TDC channels for -15°C and $+55^{\circ}\text{C}$ (see next page).

The DLL length error effects that the time bin 0 is smaller than the average bin size, whereas the differences in the hit signal routing cause the bin position shift between channel 15 and channel 16.

It must be stated that for nominal operating conditions (i.e. 40 MHz clock frequency and 45°C ambient temperature), both effects only cause a manageable performance loss.

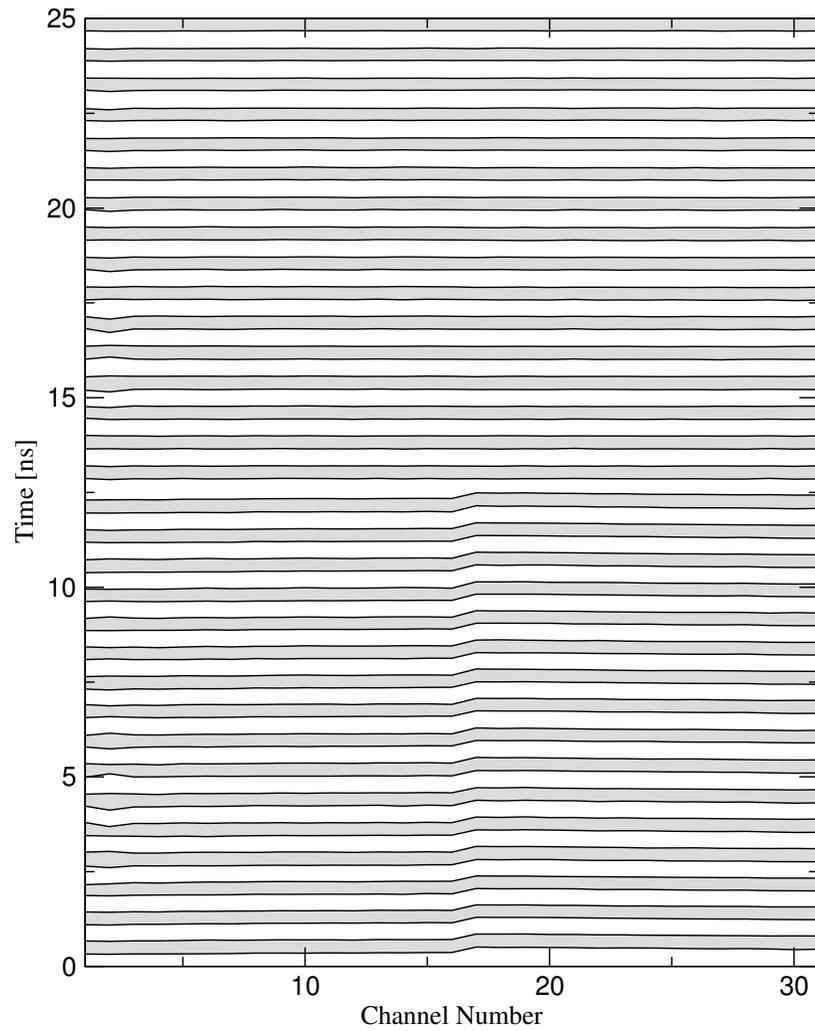


Figure 5.21: Time bin size and position at -15°C surrounding temperature.

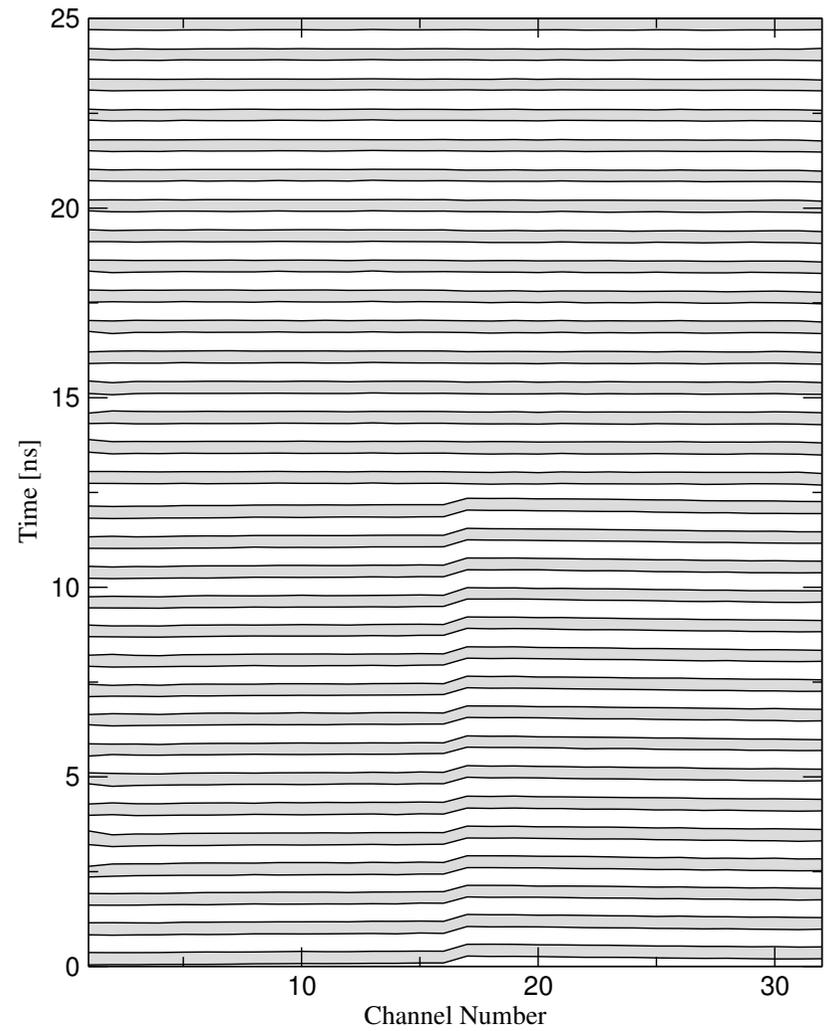


Figure 5.22: Time bin size and position at $+55^{\circ}\text{C}$ surrounding temperature.

Possible Impact on the Drift Time Measurement

The observed mismatch of the DLL length has a possible impact on the drift time measurement: above a clock frequency of 42 MHz or above 55°C, it happens that the overall DLL length error exceeds the size of one time bin. This worst case scenario will then lead to false positive hit detection during TDC operation because of the same mechanism that is responsible for the scaling down of time bin 0.

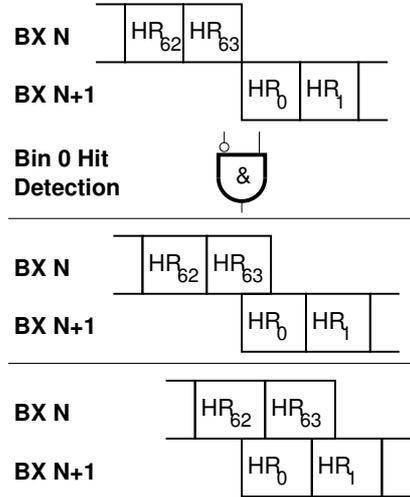


Figure 5.23: Implications of the DLL Length Mismatch.

Time Slot	BX N		BX N+1	
	HR ₆₂	HR ₆₃	HR ₀	HR ₁
1	0	0	0	0
2	1	0	0	0
3	1	0	1	0
4	1	1	1	0
5	1	1	1	1

Table 5.5: False positive hit detection in case the DLL length error exceeds the length of one time bin. The hit register configuration that triggers the false positive hit detection is typed in bold-face.

Figure 5.23 and table 5.5 illustrate the impact of an DLL length mismatch. The top part of figure 5.23 represents the ideal case: time bin 0 (HR₀) of bunch crossing N+1 starts at the end of time bin 63 of the previous bunch crossing. Note that the hit register sampling always happens at the end of the corresponding time bins. Only the combination of HR₆₃=0 and HR₀=1 leads to a hit detection in time bin 0.

In the middle part of figure 5.23, the DLL length mismatch leads to an overlap of time bin 63 (BX N) with time bin 0 (BX N+1). This results in a scale down of time bin 0 as the hit register configuration (HR₆₃=0 and HR₀=1) is suppressed.

In the bottom part of figure 5.23, the time bin overlap exceeds the size of one time bin. That is the content of HR₆₃ of bunch crossing N is defined after the sampling of HR₀ of the following bunch crossing. This situation is shown in table 5.5. The table rows (or time slots) display the evolution of the hit register content during an arriving hit signal. The hit register configuration (HR₆₃=0 and HR₀=1) that results in a hit in time bin 0 appears in row number 3 only because HR₀ of bunch crossing N+1 is defined prior to HR₆₃ of the previous bunch crossing. This way, all hit signals that belong to bunch crossing N but also last until bunch crossing N+1 will cause a false positive hit detection for bunch crossing N.

Workaround and Design Change

Measurements show that the mismatch of the DLL length (and therefore possibly false hit detection) depends on the operating frequency and the analogue supply voltage. As the operating frequency is fixed to 40 MHz, one possible workaround could be to increase the analogue supply voltage.

Figure 5.24 shows the development of the measured mismatch of time bin 0 (in bins) for varying analogue supply voltages (chip 4, channel 17, 55°C). In this measurement, the time

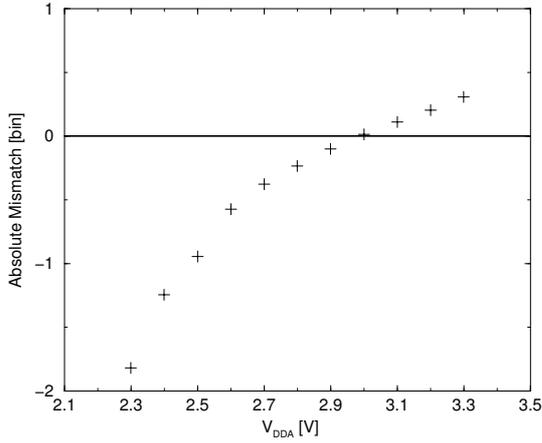


Figure 5.24: Evolution of the time bin 0 deviation with the positive analogue supply voltage.

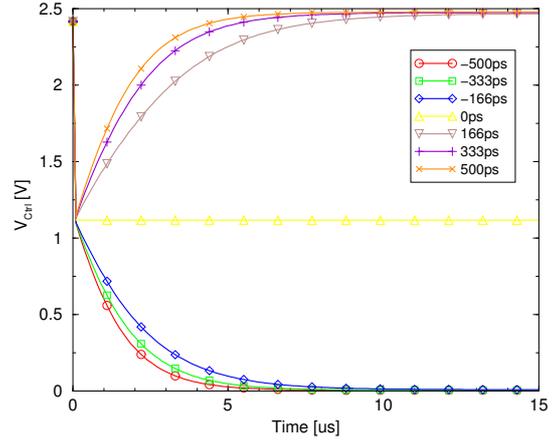


Figure 5.25: Simulation of the DLLs control voltage for the OTIS1.3 phase detector and charge pump combination: the integrating part of the controller translates a fixed input phase difference in a control voltage that rises/falls until the power supply rails.

bin 0 reaches its nominal size for an analogue supply voltage of approximately 3 V.

For the succeeding chip version OTIS1.3 the design of the phase detector has been modified: imbalanced paths have been cleared and the feedback of the fourfold NAND gate (see figure 3.5) now additionally gates the control outputs *Accelerate* and *Decelerate*. The simulation of the redesigned phase detector and the charge pump now shows an integrating behaviour. A corresponding simulation is shown in figure 5.25: the diagram depicts the control voltage of the DLL V_{Ctrl} as a function of the simulation time and different static phase differences at the input. The fixed misalignment of the two phase detector inputs (as given by the simulation) causes V_{Ctrl} to rise/fall until it reaches the power supply rails.

5.3.4 Resolution

The nominal bin size of the OTIS TDC is $\frac{1}{64}$ of the LHC clock period or 391 ps. However, as both inverter taps of each delay element are used, the 64 TDC bins show a periodic structure of always one large and one small time bin. Code density tests, that measure the mean bin sizes by the application of a large number of random input signals, resulted in 438 ± 2 ps and 342 ± 2 ps mean bin sizes for large and small bins respectively.

The resolution of the TDC was determined by applying an input signal and a delayed version of its own in pairs to two adjacent channels. The TDC then measured two drift times with a nominal difference that is determined by the used cable delay. The histogram of the measured cable delay was then used to calculate the mean signal delay and its RMS.

This setup again relies on a large number of input signals that are not correlated to the system clock. Additionally the signal generator must be able to drive the multidrop connection to the OTIS TDC without introducing too much jitter and without significant loss of signal quality. The Tektronix Waveform Generator is suitable for this purpose: the generator is able to provide the desired signal levels and it can be setup such that the output signals of the generator equally cover the measurement range of the TDC.

Figure 5.26 presents the result from a sample time interval measurement. In this case the selected cable delay introduced approximately 16.7 ns delay between the two input signals. The figure depicts the resulting distribution (y-axis scaled to the total number of entries)

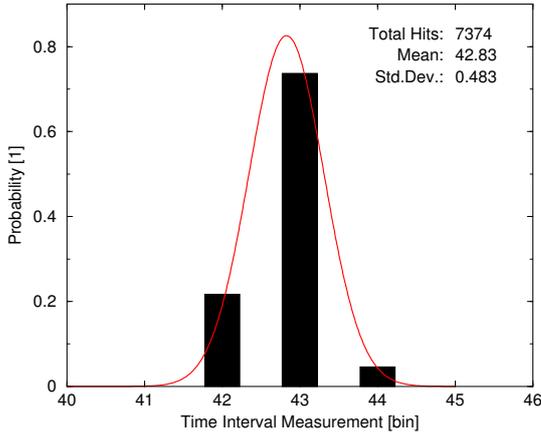


Figure 5.26: This diagram shows the histogram of the measured drift time codes for a given input time interval. Additionally the gaussian shaped curve for the extracted parameters μ and σ is shown.

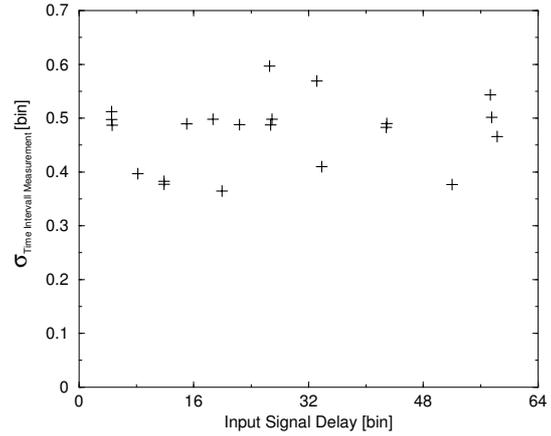


Figure 5.27: This picture shows the compilation of the calculated σ from all different time interval measurements.

of the time intervals that were measured by the OTIS chip: 7374 measurements occupy three histogram bins. The mean time interval calculates to $\mu=42.83$ bin with a mean square deviation of $\sigma=0.48$ bin. The red curve in figure 5.26 represents the corresponding Gaussian distribution.

All mean square deviations from similar measurements but with varying cable delays and for varying TDC channels are summarised in figure 5.27. Their mean value is $\sigma_{\Delta T} = 0.47$ bin or 184.4 ps. This time interval measurement consists of two independent drift time measurements and thus the single channel TDC resolution σ_{TDC} calculates to

$$\sigma_{TDC} = \frac{1}{\sqrt{2}} \cdot \sigma_{\Delta T} \approx 130 \text{ ps.}$$

σ_{TDC} is an upper limit for the TDC resolution because this consideration does not include the contribution of the jitter of the two input signals.

5.4 Total Ionising Dose Irradiation Test

The OTIS TDC chip was part of a total ionising dose irradiation campaign in February 2005 at the X-ray irradiation facility of the CERNs microelectronics group [MIC]. Two chips were subject to irradiation and accumulated a total dose of 1 Mrad(SiO₂) (chip A) and 10 Mrad(SiO₂) (chip B) [Tru05].

For the selected operating conditions, an accelerating voltage of $U_{\text{tube}} = 40$ kV and a tube current of $I_{\text{tube}} = 60$ mA, the dose rate DR at a distance of 1 cm from the collimator is given by:

$$DR [\text{rad}(\text{SiO}_2)/\text{min}] = 92 + 631.30 \cdot I_{\text{tube}} [\text{mA}]. \quad (5.4)$$

That is, a total ionising dose of 1 Mrad is accumulated within less than half an hour. No significant changes in the power consumption or in the DLLs control voltage were found after the irradiation campaign. The measured figures for the two chips before and after irradiation are given in table 5.6. The third column states the results from the repeated measurement after $3\frac{1}{2}$ months of chip storage at room temperature. The change in the figures compared to the irradiation campaign originates from a different ambient temperature.

Chip	Dose	Parameter	Pre-Irradiation	Post-Irradiation	After 3½ Months
A	1 Mrad	V_{Ctrl}	1.10 V	1.10 V	1.20 V
		I_{dig}	—	—	250 mA
		I_{ana}	—	—	6 mA
B	10 Mrad	V_{Ctrl}	1.24 V	1.25 V	1.38 V
		I_{dig}	230 mA	224 mA	242 mA
		I_{ana}	2 mA	2 mA	5 mA

Table 5.6: OTIS1.2 V_{Ctrl} and power consumption measured before and after the irradiation campaign [Tru05].

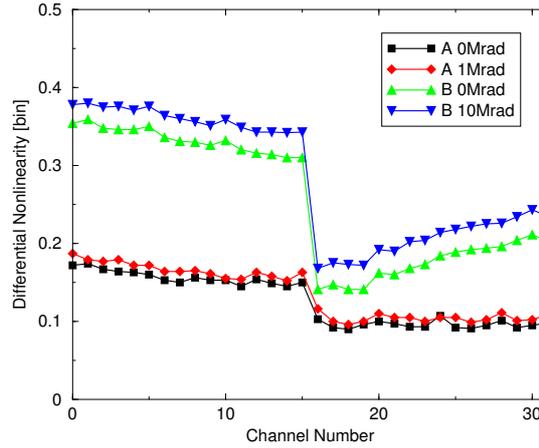


Figure 5.28: OTIS1.2 DNL measured before and after the irradiation test [Tru05].

Figure 5.28 summarises the single channels DNL measurement for both chips before and after the irradiation test. Like above, no worrying change in the performance figure was observed. The OTIS chip thus fulfils the LHCb specifications [Tru05].

5.5 Addendum: OTIS1.0 Missing Drift Time Codes

The first full-scale chip of the OTIS project OTIS1.0 did not show the expected TDC output codes: an input signal scan reveals missing codes in the second half of the basic measurement range. An example measurement is shown in figure 5.29. This diagram prints the TDC codes from a single channel depending on the phase alignment between input signal and reference clock. In the first half of the measurement range, the measured drift times reflect the rising input signal delays, but in the second half, though detecting input signals (indicated by output codes less than $0x\text{C0}$), the TDC chip outputs wrong drift times.

Series of complex measurements and simulations could identify weak driver strengths and underestimated parasitic capacitances as sources of failure resulting in misaligned data sampling at two chip internal nodes. The wrong sampling of the binary hit information that steers the multiplexing of the two encoder halves, resulted in the output of drift time codes from the first half of the measurement range (drift time codes less than $0x\text{20}$) though the applied input signals demanded for codes from the second half (codes $\geq 0x\text{20}$). Additionally, for the case of correct sampling of the binary hit information, the output driver strength

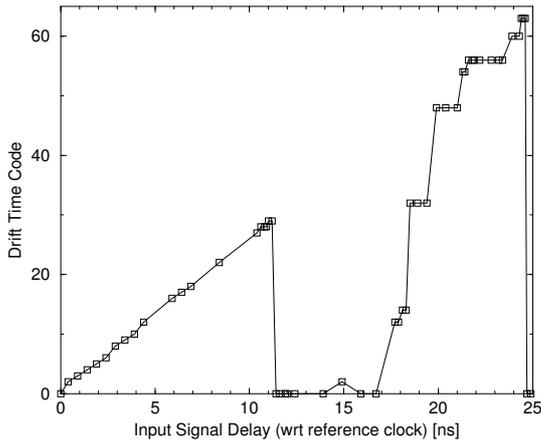


Figure 5.29: OTIS1.0: Drift time scan shows missing codes in the upper half of the basic measurement range.

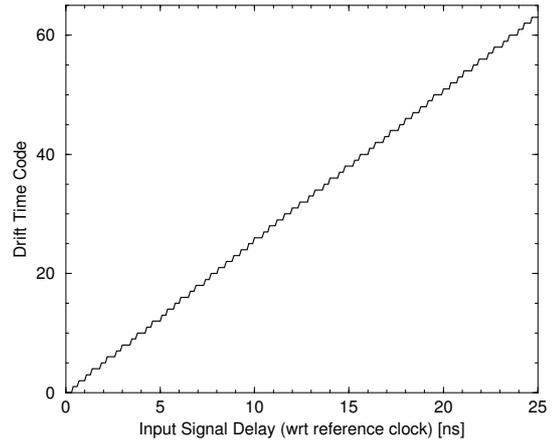


Figure 5.30: Drift time scan of the patched OTIS1.0 chip. The TDC shows the expected drift time codes for the whole basic measurement range.

of the second encoder were too weak to reliably set new signal levels before the sampling time of the pre-pipeline register. This second design flaw resulted in wrong drift time codes though correct encoder selection.

Simulations showed that the proposed corrections in the sampling points resulted in the expected drift time codes, but before starting a next chip production run, the intended changes have been checked on a FIB patched chip. The Focused Ion Beam (FIB) technology [FEI] allows local removal of materials on a sub-micrometer scale as well as local deposition of conductive or non-conductive materials thereby modifying existing integrated circuits. As in this case, FIB patching can be used for proof of concept or, depending on the intended changes, as a time saving alternative to a new chip production run.

To implement the new timing scheme, two metal line cuts decoupled the corresponding clock lines from the original clock signal distribution. The fact that all necessary metal line cuts only affected the chips topmost metal layer facilitated the chip patching. Furthermore two newly created metal lines allowed to control the hit bit and pre-pipeline registers sampling points from outside the chip. Figure 5.31 schematically shows the clock line cuts and the newly created connections. To allow a connection to the PCB, the new metal lines used the bonding pads of two decommissioned TDC channels.

Figure 5.30 shows a sample recording of a single channels drift time scan with the patched chip. The proposed timing scheme could successfully be confirmed: the TDC produces the expected linear dependency between input signal alignment and output codes for the whole measurement range. For this recording, the input signals for the drift time measurement originated from the pattern generator and scanned the TDCs working range in steps of 100 ps.

Figures 5.32 and 5.33 show photographs of the modified OTIS chip. The track shown in fig. 5.32 is of deposited tungsten, the track length is approximately $800\ \mu$. This auxiliary clock line makes the pre-pipeline sampling controllable from outside the chip by connecting to the input pad of the now unused channel 31. The connection point at the original clock lines is shown in figure 5.33. This picture shows the uncovered clock lines before the deposition of tungsten. The opening in the chips topmost passivation layer is approximately $10\ \mu\text{m} \times 25\ \mu\text{m}$.

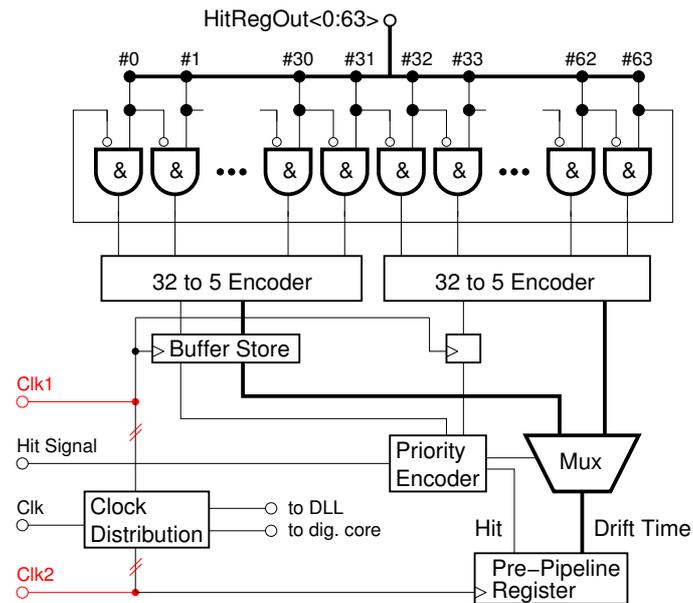


Figure 5.31: Schematic drawing of the circuit modifications (red) of the OTIS1.0 patch. The clock lines that control hit bit and pre-pipeline register sampling are decoupled from the original clock distribution.

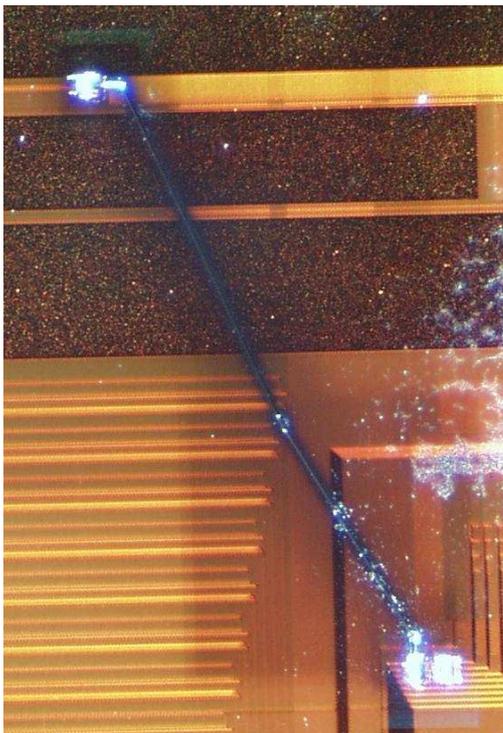


Figure 5.32: Close-up view of one patched clock line (deposition of tungsten). The track length is approximately 800 μm .

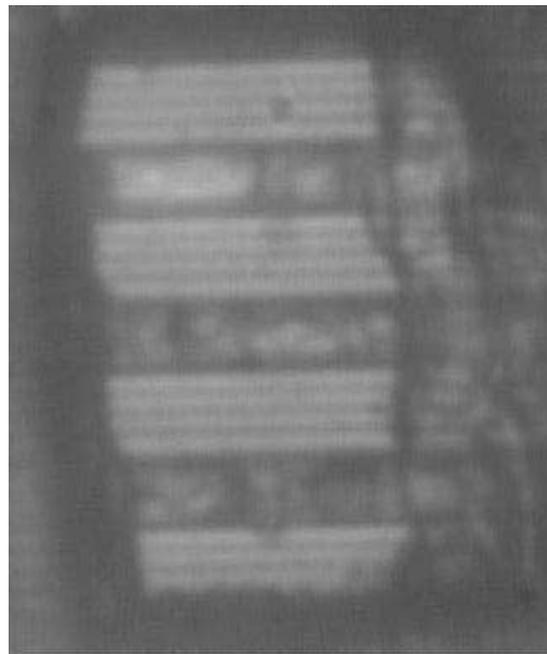


Figure 5.33: The clock lines lower right end from fig. 5.32 connects to all 16 uncovered metal lines (arranged in groups of four). The opening in the passivation layer is approximately 10 $\mu\text{m} \times 25 \mu\text{m}$.

5.6 Summary

The TDC chip OTIS1.2 successfully passed the different laboratory test procedures. The chip fulfils the LHCb requirements and is ready for mass production.

The 32-channel TDC chip measures drift times with a nominal resolution of 6 bit within the basic measurement range of 25 ns. The accuracy of the time digitisation has been measured to be 130 ps. Differential and integral nonlinearity are 440 ± 20 ps respectively 0.29 ± 0.01 bin. At excessive ambient temperatures, the performance of the TDC core suffers from the length mismatch of the DLL. For this reason a new chip version with a modified phase detector has been developed.

The digital control unit of the OTIS chip integrates memory and trigger management and provides the formatting of the triggered data. The two offered output data formats fully comply with the specifications for LHCb front-end electronics. All parts of the digital control core work as expected; no errors have been found.

Two different building blocks of the OTIS chip, the I²C-interface and the digital to analogue converter, have been adopted from the Beetle chip. The I²C-interface works as expected, the differential nonlinearity of the 8 bit-DAC has been measured to be 7.7 ± 3.1 mV.

The main test results for the OTIS1.2 chip or its discrete building block are:

Power Consumption	= 668 ± 30 mW
Radiation Hardness	up to 10 Mrad
Resolution	= 130 ps RMS
DNL	= 440 ± 20 ps
INL	= 0.29 ± 0.01 bin
Memory	fully functional
Fast Control Core	fully functional
Slow Control Core	fully functional
DNL Threshold DACs	= 7.7 ± 3.1 mV

6 Summary

Conclusion

The OTIS TDC chip is designed for the readout of the Straw Tubes of the LHCb Outer Tracker detector. The target drift coordinate resolution of $200\ \mu\text{m}$ requires that the TDC provides drift time measurement with a resolution $< 1\ \text{ns}$. The expected maximum drift times of about $50\ \text{ns}$ furthermore demand for the possibility to expand the basic measurement range ($25\ \text{ns}$) by a factor of two or three.

The measured drift times from all 32 channels are stored in the pipeline memory and in the derandomizer buffer that cover the $4\ \mu\text{s}$ trigger latency and compensate trigger rate fluctuations. Two data formats exist for the readout of triggered data sets. A digital control core manages the two memory blocks, processes the received trigger sequences and passes the formatted data to the following data acquisition stage.

In the context of this work, the following contributions have been made:

- Development of the digital control unit (including memory and trigger management, data processing, and debugging features) of the OTIS chip. Development of the interface between pipeline memory and digital control core.
- Customisation of the existing I²C-interface (implementation of the OTIS register map).
- Integration of digital control unit, I²C-interface and pipeline memory into the OTIS chip.
- Development of the PC-based OTIS programming interface. Assembly of the laboratory test environment.
- Initial start-up, test and characterisation of the different OTIS prototype chips. Intensive fault diagnostics (simulation and measurement) concerning the problem of missing drift time codes of chip version OTIS1.0. Validation of the identified cause of defect with a FIB patched version of the OTIS1.0 chip.

The latest version of the OTIS readout chip (OTIS1.2) fulfils all the requirements of the LHCb Outer Tracker detector as well as the requirements of the front-end electronics specifications of the LHCb experiment.

Outlook

Usage of the OTIS Chip in the Experiment

The TDC chip OTIS1.2 has been successfully operated in the 2005 testbeam campaign of the Outer Tracker group. The goal of the beam test was to operate mass production Outer Tracker modules with mass production electronics and to measure detector performance parameters.

The test setup included four Outer Tracker modules (with Ar/CO₂ (70:30) drift gas mixture), four Outer Tracker front-end boxes (each fully equipped with ASDblr discriminator

chips, OTIS1.2 TDC chips and GOL serialiser chip), optical receiver and TTC system for the distribution of timing and fast control signals. The trigger decision for the data acquisition has been derived from a set of scintillators and reference tracking information was provided by silicon tracker detectors.

The setup successfully operated for three weeks at the 6 GeV electron beam "22" at DESY, Hamburg, and about 150 runs with 10,000 events each were recorded. The test allowed to take drift time spectra and to determine the drift coordinate resolution or the cell efficiency. Figure 6.1 shows a sample drift time spectrum from the testbeam campaign. The presented drift time histogram has been corrected for signal propagation delays. Such drift time spectra have been used to derive the r-t-relation and the cell resolution of the straw tubes. Figures 6.2 and 6.3 present the dependencies of the drift coordinate resolution and the cell efficiency from the comparator threshold voltage. For the standard operating parameters (1550 V detector high voltage and 700 mV comparator threshold), the particle tracks were reconstructed with a resolution $< 200 \mu\text{m}$. The cell efficiency was $> 98\%$.

The 2005 testbeam campaign successfully validated the specifications of the technical design report (resolution $< 200 \mu\text{m}$) with the final module design and the complete readout chain including the OTIS chip.

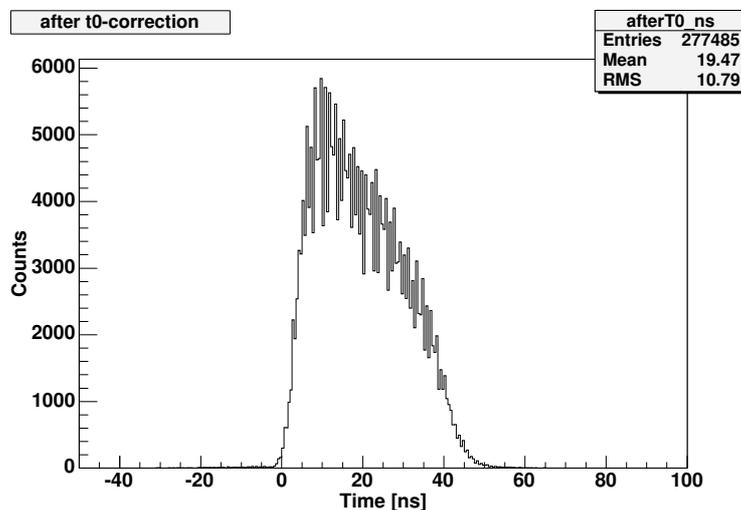


Figure 6.1: Sample drift time spectrum from the 2005 testbeam campaign. The drift times have been corrected for cable delays. 99% of all measured drift times are between 0 and 45 ns. [Haa05]

OTIS Routine Test

Currently, the chip test setup for a semi-automatic wafer prober station is under development. This setup will be used for the upcoming testing and characterisation of the OTIS chips from the mass production. The test environment provides chip operation parameter setup and generation of all control signals and test pulses that are necessary for the routine test. An FPGA will be used for the data acquisition and the validation and processing of the data output of the OTIS chip. The FPGA will for example calculate the differential non-linearity of the TDC core from a recorded drift time spectrum.

Approximately 2000 chips will be needed for the assembly of the Outer Tracker detector modules. The start of the routine test is scheduled for Q4/2005.

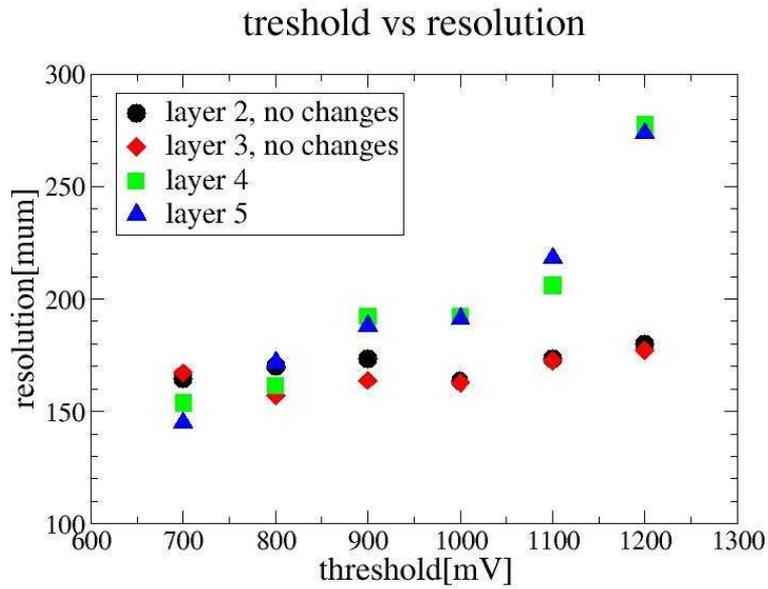


Figure 6.2: Drift coordinate resolution vs. comparator threshold. Threshold voltage variation only for module no. 3 (layer 4 and 5); standard settings for module no. 2. The resolution stays below 200 μ . [Haa05]

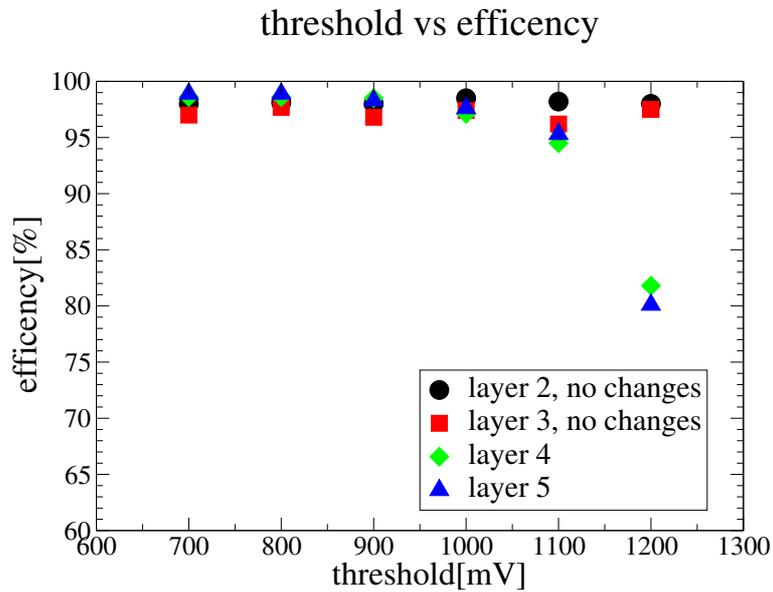


Figure 6.3: Detector cell efficiency vs. comparator threshold. Threshold voltage variation only for module no. 3 (layer 4 and 5); standard settings for module no. 2. The efficiency stays above 98%. [Haa05]

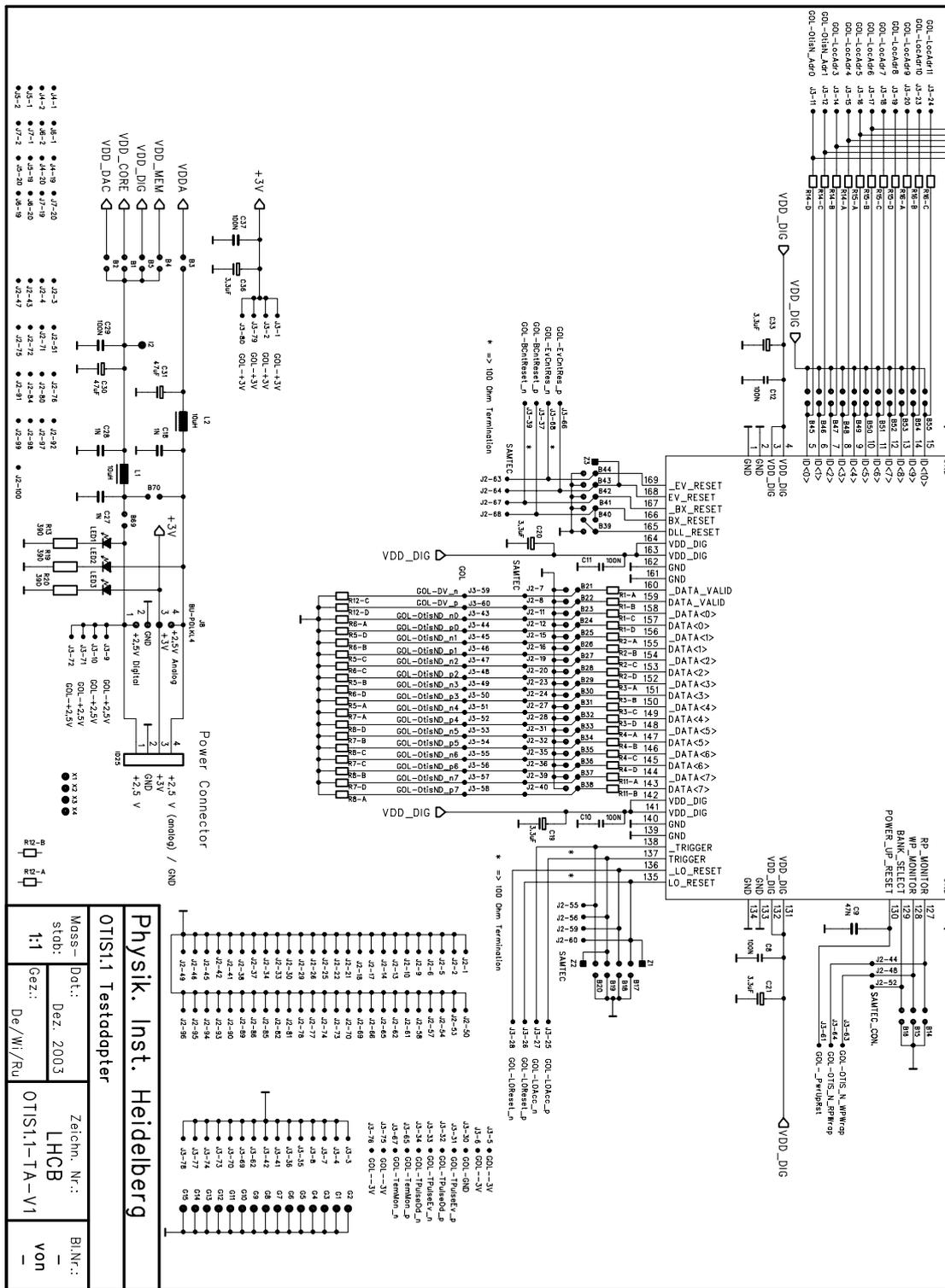


Figure A.2: Schematic of the OTIS1.2 test PCB.

B Chip Geometry and Pad Layout

The size of the OTIS1.2 chip is $5100\mu\text{m} \times 7000\mu\text{m}$. But the actual dimensions of single dies may vary due to the tolerances of the wafer cutting process. Figure B.1 shows the arrangement of the 169 pads of the OTIS chip. The given pad coordinates refer to the lower left point of origin and are measured from the central point of each pad. The bondable pad window size is $95\mu\text{m} \times 95\mu\text{m}$ and the pitch of abutting pads is $120\mu\text{m}$.

Table B.1 lists number, name, coordinates and type of all pads. The differential inputs (hit input, clock, trigger) are non-inverting, i.e. the interpretation of the input signal always follows the positive input. Resets are active-low.

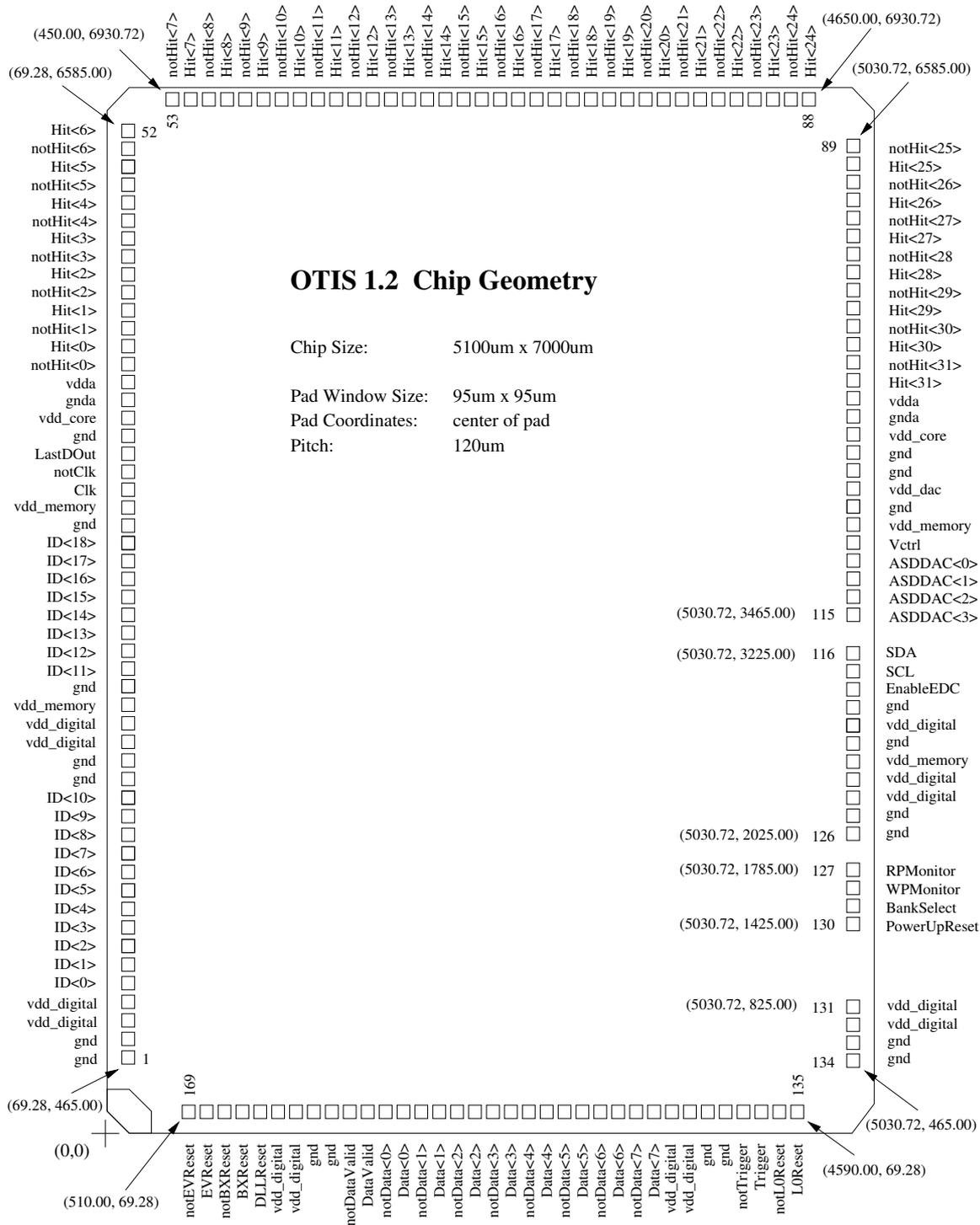


Figure B.1: OTIS1.2 Pad Layout

Table B.1: OTIS1.2 Pad Description

No.	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	465.00	input	neg. digital supply
2	gnd	69.28	485.00	input	neg. digital supply
3	vdd_digital	69.28	705.00	input	pos. digital supply
4	vdd_digital	69.28	825.00	input	pos. digital supply
5	ID< 0 >	69.28	945.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1065.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1185.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1305.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1425.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1545.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	1665.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	1785.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	1905.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2025.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2145.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2265.00	input	neg. digital supply
17	gnd	69.28	2385.00	input	neg. digital supply
18	vdd_digital	69.28	2505.00	input	neg. digital supply
19	vdd_digital	69.28	2625.00	input	pos. digital supply
20	vdd_memory	69.28	2745.00	input	pos. memory supply
21	gnd	69.28	2865.00	input	neg. digital supply
22	ID< 11 >	69.28	2985.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3105.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3225.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3345.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	3465.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	3585.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	3705.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	3825.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	3945.00	input	neg. digital supply
31	vdd_memory	69.28	4065.00	input	pos. memory supply
32	Clk	69.28	4185.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	4305.00	LVDS input (neg.)	
34	LastD0Out	69.28	4425.00		
35	gnd	69.28	4545.00	input	neg. digital supply
36	vdd_core	69.28	4665.00	input	pos. TDC supply
37	gnda	69.28	4785.00	input	neg. DLL supply
38	vdda	69.28	4905.00	input	pos. DLL supply
39	notHit< 0 >	69.28	5025.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5145.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5265.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	5385.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	5505.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	5625.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	5745.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	5865.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	5985.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6105.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6225.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	6345.00	LVDS input (pos.)	

Table B.1: OTIS1.2Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
51	notHit< 6 >	69.28	6465.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	6585.00	LVDS input (pos.)	
53	notHit< 7 >	450.00	6930.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	6930.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	6930.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	6930.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	6930.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	6930.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	6930.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	6930.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	6930.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	6930.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	6930.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	6930.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	6930.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	6930.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	6930.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	6930.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	6930.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	6930.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	6930.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	6930.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	6930.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	6930.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	6930.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	6930.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	6930.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	6930.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	6930.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	6930.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	6930.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	6930.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	6930.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	6930.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	6930.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	6930.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	6930.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	6930.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	6585.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	6465.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	6345.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6225.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6105.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	5985.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	5865.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	5745.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	5625.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	5505.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	5385.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5265.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5145.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5025.00	LVDS input (pos.)	

Table B.1: OTIS1.2Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
103	vdda	5030.72	4905.00	input	pos. DLL supply
104	gnda	5030.72	4785.00	input	neg. DLL supply
105	vdd_core	5030.72	4665.00	input	pos. TDC supply
106	gnd	5030.72	4545.00	input	neg. digital supply
107	gnd	5030.72	4425.00	input	neg. digital supply
108	vdd_DAC	5030.72	4305.00	input	pos. DAC supply
109	gnd	5030.72	4185.00	input	neg. digital supply
110	vdd_memory	5030.72	4065.00	input	pos. memory supply
111	VCtrl	5030.72	3945.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	3825.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	3705.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	3585.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	3465.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3225.00	input/output (5V open drain)	I ² C Data
117	SCL	5030.72	3105.00	CMOS input (5V)	I ² C Clock
118	EnableEDC	5030.72	2985.00	CMOS input (pull down)	Enable I ² C EDC
119	gnd	5030.72	2865.00	input	neg. digital supply
120	vdd_digital	5030.72	2745.00	input	pos. digital supply
121	gnd	5030.72	2625.00	input	neg. digital supply
122	vdd_memory	5030.72	2505.00	input	pos. memory supply
123	vdd_digital	5030.72	2385.00	input	pos. digital supply
124	vdd_digital	5030.72	2265.00	input	pos. digital supply
125	gnd	5030.72	2145.00	input	neg. digital supply
126	gnd	5030.72	2025.00	input	neg. digital supply
127	RPMonitor	5030.72	1785.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	1665.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	1545.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	1425.00	input	Power Up Reset
131	vdd_digital	5030.72	825.00	input	pos. digital supply
132	vdd_digital	5030.72	705.00	input	pos. digital supply
133	gnd	5030.72	585.00	input	neg. digital supply
134	gnd	5030.72	465.00	input	neg. digital supply
135	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notL0Reset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	neg. digital supply
140	gnd	3990.00	69.28	input	neg. digital supply
141	vdd_digital	3870.00	69.28	input	pos. digital supply
142	vdd_digital	3750.00	69.28	input	pos. digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	

Table B.1: OTIS1.2Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	
159	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
160	notDataValid	1590.00	69.28	CMOS output (neg.)	
161	gnd	1470.00	69.28	input	neg. digital supply
162	gnd	1350.00	69.28	input	neg. digital supply
163	vdd_digital	1230.00	69.28	input	pos. digital supply
164	vdd_digital	1110.00	69.28	input	pos. digital supply
165	DLLReset	990.00	69.28	CMOS input (pull up)	DLL Reset
166	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	notBXReset	750.00	69.28	LVDS input (neg.)	
168	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	notEVReset	510.00	69.28	LVDS input (neg.)	

C OTIS Chip Family

The evolution of the OTIS TDC chip project is presented below in table form. In total six chips were manufactured participating in Multi Project Wafer (MPW) productions. The pipeline and derandomizer buffer test structure has been submitted on the **BeetleSR1.0** test chip of the *Beetle* group.

The TDC chip **OTIS1.2** fulfils the specifications of the LHCb experiment and the Outer Tracker sub-detector. The chip version **OTIS1.3** has been designed to overcome the performance degradation of **OTIS1.2** at excessive temperatures.

OtisDLL1.0	Production Lot	MPW09 / October 2000
	Date	19.10.2000
	Size	2.0 mm × 2.0 mm
	Description	The DLL test chip features a 32 delay stage DLL with one tap per delay stage that drive a 32 bit wide hit register. Available monitoring outputs are V_{Ctrl} , LastDummyOut and the outputs of the phase detector.
OtisMEM1.0	Production Lot	MPW04 / March 2001
	Date	21.03.2001
	Size	4.0 mm × 4.0 mm
	Description	Test chip for SRAM and DLL. The full featured memory prototype is an array of 186×240 cells with registered output plus supplementary input data generator and output data error checker. The DLL features a 32 stage delay chain with two taps each plus a 64 bit wide hit register multiplexed to four output pins. Available monitoring outputs are V_{Ctrl} , LastDummyOut and the outputs of the phase detector.
BeetleSR1.0	Production Lot	MPW05 / May 2001
	Date	18.05.2001
	Size	2.0 mm × 2.0 mm
	Description	Test chip for the Beetle project containing one column of the OTIS pipeline-derandomizing buffer combination to test the pipeline to derandomizing buffer copy mechanism.

OTIS1.0	Production Lot	MPW07 / May 2002
	Date	15.05.2002
	Size	5.1 mm × 6.0 mm
	Description	First full scale OTIS TDC chip with 64 tap DLL, hit register, L0 pipeline and derandomizer und control core that features the encoded hitmask operation mode. Shows missing drift time codes due to timing violations between TDC core and pre-pipeline register.
OTIS1.1	Production Lot	MPW12 / November 2003
	Date	10.11.2003
	Size	5.1 mm × 7.7 mm
	Description	TDC chip version that overcomes the missing code problem but misses the plain hitmask operation mode. Other problems: large offset spread for the ASDblr threshold voltage output buffers; large fanout/capacitance between derandomizer and digital core provokes faulty bunch crossing number in the data output.
OTIS1.2	Production Lot	MPW13 / May 2004
	Date	24.05.2004
	Size	5.1 mm × 7.0 mm
	Description	This chip version includes the plain hitmask mode and fixes the bunch crossing number problem and removes the large offset spread of the ASDblr threshold voltage output buffers.
OTIS1.3	Production Lot	MPW15 / May 2005
	Date	09.05.2005
	Size	5.1 mm × 7.0 mm
	Description	Changes in the DLLs phase detector in order to overcome the the bin size deviations of the predecessor chip version.

D List of Acronyms

ASIC	Application Specific Integrated Circuit
BIST	Build In Self-Test
CDT	Code Density Test
CPLD	Complex Programmable Logic Device
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DLL	Delay Locked Loop
DNL	Differential Non-Linearity
DUT	Design Under Test
ECS	Experiment Control System
FIB	Focused Ion Beam
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
FSR	Full Scale Range
FSM	Finite State Machine
GOL	Gigabit Optical Link
HDL	Hardware Description Language
HEP	High Energy Physics
HLT	High-Level Trigger
HR	Hit Register
INL	Integral Non-Linearity
JTAG	Joint Test Action Group, common name for boundary-scan architecture defined in IEEE Standard 1149.1.
L0	LHCb Trigger Level Null
L0DU	Level-0 Decision Unit
LFSR	Linear Feedback Shift Register
LHC	Large Hadron Collider

D List of Acronyms

LHCb	Large Hadron Collider beauty experiment
LVDS	Low Voltage Differential Signal
LSB	Least Significant Bit
MPW	Multi Project Wafer
MSB	Most Significant Bit
OT	Outer Tracker
OTIS	Outer tracker Time Information System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PRBS	Pseudo Random Binary Sequence
PRNG	Pseudo Random Number Generator
RS	Readout Supervisor
RTL	Register Transfer Level
SDF	Standard Delay Format
SEE	Single Event Effect
SEU	Single Event Upset
SEL	Single Event Latch-Up
SRAM	Static Random Access Memory
TID	Total Ionising Dose
TDC	Time to Digital Converter
TFC	Timing and Fast Control
TLF	Timing Information Library File
VGA	Video Graphics Array
VLSI	Very Large Scale Integration
WLM	Wire Load Model

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