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Development and Implementation of the Control System for the Pre-Trigger System of theTransition Radiation Detector at ALICE

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Entwicklung und Implementierung des Steuerungssystems für das Pre-Trigger System des Übergangsstrahlungsdetektors von ALICE

Die Front-End Elektronik des Übergangsstrahlungsdetektors (TRD) des *A Large Ion Collider Experiment(s)* (ALICE) am *Large Hadron Collider* (LHC) am CERN benötigt ein schnelles Triggersignal mit geringer Verzögerung noch vor dem Eintreffen des globalen Triggersignals des Zentralen Trigger Prozessors (CTP). Dieses Triggersignal wird vom Pre-Trigger System des TRD bereitgestellt. Im Rahmen dieser Arbeit wurde die Software zur Überwachung und Steuerung des Pre-Trigger Systems entwickelt. Sie besteht aus Servern und Clients, die über das *Distributed Information Management* Netzwerk kommunizieren, und einer Software Bibliothek, die Funktionen und Subroutinen zur ganzheitlichen Kontrolle des Systems enthält. Außerdem definiert sie das Format, in dem die Server und die Clients miteinander kommunizieren. Desweiteren wurde eine *Finite-State Machine (FSM)* eingeführt, die die Implementierung des Systems in das Detektorkontrollsystem des TRD erlaubt. Was die Hardware betrifft, wurde das Pre-Trigger System durch den Einbau des Backup-Systems im L3 Magneten von ALICE komplettiert. Hinzu kommen der Entwurf und der Einbau zweier Stromverteilerkästen, die die Verkabelung und die Wartung der Stromzufuhr für das Pre-Trigger System vereinfachen. Außerdem wurden Tests mit dem Interface zwischen dem T0 Detektor und dem Pre-Trigger System durchgeführt, um sich des einwandfreien Betriebes zu vergewissern.

Development and Implementation of the Control System for the Pre-Trigger System of the Transition Radiation Detector at ALICE

The front-end electronics of the Transition Radiation Detector (TRD) of A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider (LHC) at CERN require a low latency trigger prior to the global trigger from the Central Trigger Processor, which is provided by the pre-trigger system of the TRD. Within this thesis, the software to control and monitor the pre-trigger system has been developed. The software consists of clients and servers, which communicate through the Distributed Information Management network, and a standard Linux shared object library, that contains the functions and subroutines to supervise the pre-trigger system as well as defining the format of communication between the clients and the servers. Moreover, a finite-state machine was introduced, which allows the implementation of the system in the Detector Control System of the TRD. Furthermore, the hardware components of the backup system of the pre-trigger system were completed and installed in the L3 magnet. In addition, two patch panels have been designed and installed, which simplify the low voltage distribution scheme for the pre-trigger system. Also, tests were carried out to ensure the proper operation of the interface between the T0 detector and the pre-trigger system.

Contents

1 Introduction

Quantum chromo dynamics (QCD) is the theory of strong interactions. Asymptotic freedom [1, 2] is a remarkable feature of QCD, i.e. the interaction between quarks weakens as quarks get closer to one another. Shortly after the idea of asymptotic freedom was introduced, it was realized that this has a fascinating consequence. Above a critical temperature and density, quarks and gluons are freed from their hadronic boundary forming a deconfined phase of matter [3, 4] – a quark gluon plasma (QGP). Our present world exists at low temperatures and densities with quarks and gluons confined to the size of hadrons. But shortly after its origin, our universe was of a much higher temperature and density. About 10 μs after the Big Bang, it is thought that all matter visible today existed as a quark gluon plasma.

Solving QCD in regularized lattice calculations, at vanishing or finite net-baryon density, predicts a cross-over transition from the deconfined thermalized partonic matter to hadronic matter at a critical temperature $T_c \approx 150$–180 MeV [5]. A similar value has been derived in the 1960s by R. Hagedorn as the limiting temperature for hadrons when investigating hadronic matter [6].

The only way to create and study such a QGP in the laboratory, is the collision of heavy nuclei at highest centre-of-mass energies. A crucial question is to what extent matter is created in these collisions, i.e. whether local equilibrium is achieved. If the system at least approximately reaches equilibrium , then temperature, pressure, energy and entropy density can be defined. The relation amongst these macroscopic parameters is given by the (partonic) equation of state.

Heavy-flavour (c, b) quarks are excellent tools to study the degree of thermalization of the initially created matter [7]. Due to their large masses ($\gg \Lambda_{\mathrm{QCD}}$), heavy quarks are dominantly created in early stage perturbative QCD processes. The overall number of heavy quarks is conserved since their heavy mass is much smaller than the maximum temperature of the medium. Thus thermal production is negligible. Also, cross sections for heavy quark-antiquark annihilation are marginal [8]. As shown in fig. 1.1, the large masses of heavy quarks are almost exclusively generated through their coupling to the Higgs field in the electro-weak sector, while masses of light quarks (u, d, s) are dominated by spontaneous breaking of chiral symmetry in QCD. This means that in a QGP, where chiral symmetry might be restored, light quarks are left with their bare current masses while heavy-flavour quarks remain heavy.

Frequent interactions at the partonic stage will cause these heavy quarks to participate in collective motion [9, 10, 11] and finally kinetically equilibrate. This lead to the idea of statistical hadronization of charm quarks [12]. Calculations predict significant changes in the production of hidden charm hadrons, e.g. J/ψ [13].

Quarkonia play a key role in research into the quark gluon plasma. In 1986, Satz and Matsui [14] suggested that the high density of gluons in a quark gluons plasma should destroy charmonium systems, in a process analogous to Debye screening of the electromagnetic field in a plasma through the presence of electric charges. Such a suppression was indeed observed by the NA50 collaboration [15] at the super proton synchrotron (SPS). However, absorption of charmonium in the cold nuclear medium also contributes to the observed suppression [16] and the interpretation

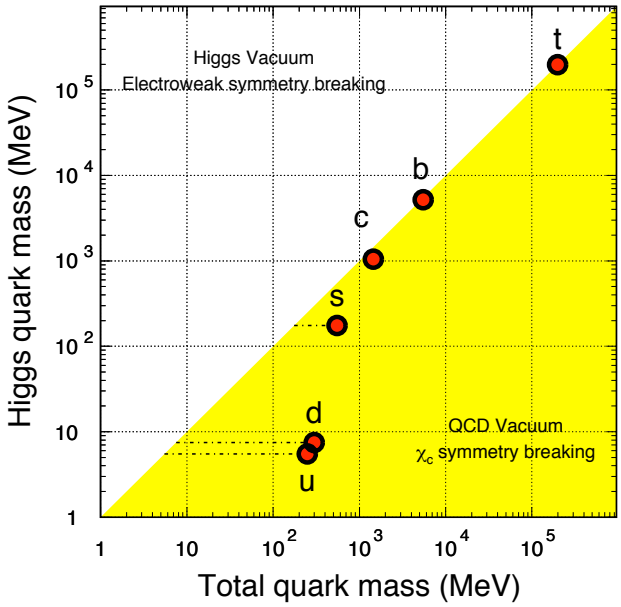


Figure 1.1: Quark masses in the QCD vacuum and the Higgs vacuum. A large fraction of the light quark masses is due to chiral symmetry breaking in the QCD vacuum while heavy quarks attain almost all their mass from coupling to the Higgs field. This figure has been taken from Ref. [7].

of the SPS data remains inconclusive.

At high collider energies, the large number of charm-quark pairs produced leads to a new production mechanism for charmonium, either through statistical hadronization at the phase boundary [12, 17] or coalescence of charm quarks in the plasma [18, 19, 20, 21, 22]. At low energy, the average number of charm-quark pairs produced in a collision is much lower than one, implying that charmonium is always formed from this particular pair. If charm quarks are abundantly produced (in the order of some tens to a few hundred), charm quarks from different pairs can combine to form charmonium, see fig. 1.2.

This mechanism works only if heavy charm quarks can propagate over substantial distance to meet their counterpart. Under these conditions, charmonium production scales quadratically with the number of charm-quark pairs [23]. Thus enhancement rather than strong suppression is predicted for high collision energies. This would be a clear signature of the formation of a quark gluon plasma with deconfined charm quarks and thermalized light quarks.

The large hadron collider (LHC) at CERN near Geneva, Switzerland, will provide collisions of nuclei with masses up to that of lead. Unprecedented high centre-of-mass energies up to $\sqrt{s_{NN}} = 5.5$ TeV per nucleon-nucleon pair for lead-lead collisions will be achieved. At these energies, heavy quarks are abundantly produced.

A large ion collider experiment (ALICE) detector at LHC will measure most of the heavy quark hadrons. Open charm hadrons are identified by their displaced decay vertex with high spatial resolution applying silicon vertex technology. The ALICE transition radiation detector (TRD) measures production of J/ψ and other quarkonia by identifying electrons and positrons from electromagnetic decays over a large momentum range.

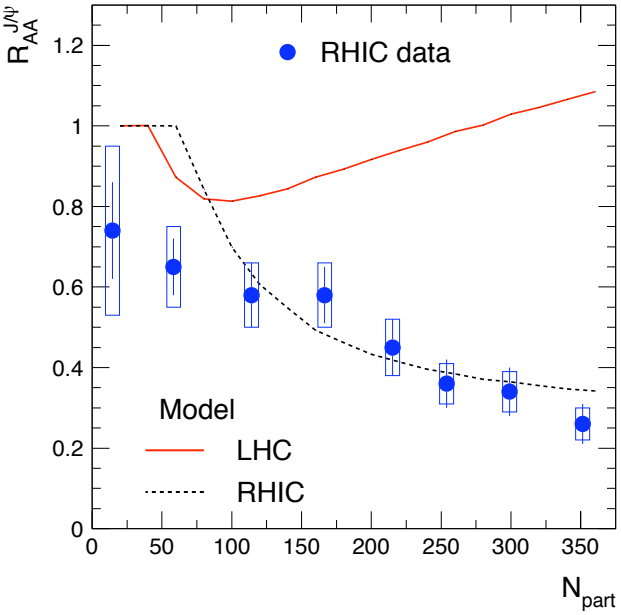


Figure 1.2: Statistical Model predictions for charmonium production relative to normalized $p+p$ collisions for RHIC (dashed line) and LHC (solid line) energies. The data point is for top RHIC energies as measured by the PHENIX collaboration [24]. This figure has been taken from Ref. [23].

The present LHC schedule plans to start with p+p collisions at energies of $\sqrt{s_{NN}} = 900$ GeV in November 2009. Shortly after, the collision energy will be increased for some weeks to $\sqrt{s_{NN}} = 7$ TeV. It is followed by a long period until the end of 2010 with runs at energies of $\sqrt{s_{NN}} = 10$ TeV. The runs at the maximum collision energy of $\sqrt{s_{NN}} = 14$ TeV are planned at the beginning of 2011. Within ALICE, the p+p collisions at energies of $\sqrt{s_{NN}} = 10$ TeV will serve as a reference to characterize the Quark Gluon Plasma in future Pb+Pb collisions. However, p+p collisions at the LHC offer unique opportunities to study other physics topics, such as diffractive scattering at high energies [25].

Diffractive scattering at high energies is dominated by pomeron exchange. Prototypes of such processes involving pomeron exchange are shown in fig. 1.3. The incoming protons exchange either one or two pomerons. The outgoing particles can be the protons with changed momenta or newly created particles. Figure 1.3 (b) shows a fusion process of two pomerons, producing a third particle, for example the vector meson J/ψ. The pomeron consists either of gluons and/or quark-antiquark pairs in a colour singlet state and has the quantum numbers of the vacuum. Therefore it radiates neither pions nor photons. In the experiment this leads to large angular regions, the so called rapiditiy gaps, where no particles are detected. In other words, rapidity gaps are defined as the absence of particles in a rapidity or pseudorapitdity region and they are a signature for the exchange of a color-singlet, such as the pomeron.

The theoretical counterpart of the pomeron, the odderon, predicted by QCD, has not yet been discovered, although processes similar to the one above are expected. Suggestions to explain the missing odderon were given [26].

To study the underlying dynamics it is necessary to analyze events with signatures of the above mentioned rapidity gaps. Special triggers are needed to select these events. Within ALICE, the TRD has a dedicated pre-trigger system, which is suited to provide such triggers. The pre-trigger

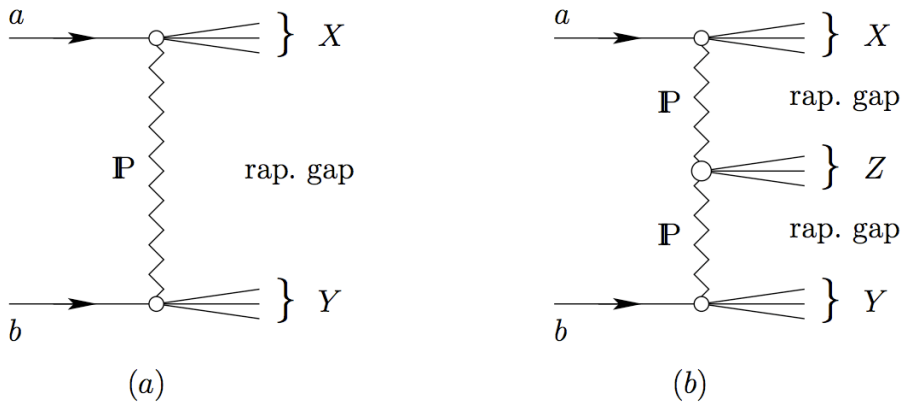


Figure 1.3: Diffractive process with (a) one rapidity gap and (b) two rapidity gaps involving a pomeron exchange. This figure has been taken from [25].

is necessary for the TRD, since the TRD requires a trigger signal to wake up the front-end electronics to start the data processing, not later than 500 ns after the collision had occured. The reason ist, that the TRD itself provides triggers for other detectors, such as the Time Projection Chamber (TPC) However, the latency of the lowest level trigger (Level-0 trigger) provided by the ALICE Central Trigger Processor (CTP) is 1.2 μs, which is too large for the TRD.

Within this thesis, the software to monitor and control the pre-trigger system of the ALICE TRD has been developed. Most hardware components of the pre-trigger system have been installed and commissioned during a previous thesis [54]. In the present thesis the hardware of the pre-trigger system was completed by installing the backup system. In addition, the low voltage power distribution scheme for the pre-trigger system was changed. For that purpose, a patch panel was designed and installed, which simplifies wiring and maintenance. Furthermore, commissioning and tests to ensure the proper operation of the pre-trigger system were carried out.

This thesis is structured as follows. Chapter 2 describes the accelerator complex at CERN and gives a brief overview of the ALICE experiment. The ALICE TRD is explained in detail in chap. 3. The conceptional design of the pre-trigger system is presented in chap. 4, its hardware components in chap. 5 and its control software in chap. 6. The detailed tests of the interface between the T0 detector and the pre-trigger system are described in chap. 7. Chapter 8 gives a summary and a outlook.

2 The LHC and A Large Ion Collider Experiment

2.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is located at the European Organisation for Nuclear Research (Conseil Européen pour la Recherche Nucléaire, CERN) near Geneva, Switzerland. The first circulating beam was seen at 10. September 2008. First collisions are expected to take place in autumn 2009. At its full capacity two counter rotating beams of protons or heavy ions are brought to collision at an unprecedented high centre of mass energy and luminosity. Due to these enormous collision energies new insights into the structure of matter and fundamental forces will be possible. The design centre of mass energy of $\sqrt{s} = 14$ TeV in p+p collisions at a luminosity of $\mathcal{L} = 10^{34}\ cm^{-2}s^{-1}$ [29] will exceed the up-to-date highest available energies of the Tevatron by a factor of 7 and the luminosity by a factor of 100. The targeted centre of mass energy of $5.5TeV$ per nucleon-nucleon pair in lead-lead collisions is 30 times higher than the collision energies gained at the Relativistic Heavy Ion Collider (RHIC) located in the Brookhaven National Laboratory (BNL), USA. The nominal luminosity in lead-lead collisions at the LHC is $\mathcal{L} \approx 10^{27}\ cm^{-2}s^{-1}$.

The LHC was constructed inside the existing tunnel of the Large Electron Positron (LEP) collider which stopped its operation in 2000. A schematic overview of the CERN accelerator system is shown in fig. 2.1.

Protons from a 90 kV duoplasmatron proton-source are accelerated in the linear accelerator LINAC2 to a kinetic energy of 50 MeV and then passed to the multi ring Proton Synchrotron Booster (PSB) where they are accelerated to 1.4 GeV. In the Proton Synchrotron (PS) they reach 26 GeV and their bunch patterns are generated. After the transfer to the Super Proton Synchrotron (SPS) the protons are accelerated to 450 GeV and injected into the LHC ring with about 27 km circumference where they reach 7.5 TeV. To keep the protons within the ring, 1232 superconducting dipole magnets are installed. They are cooled down to 1.9 K by liquid helium and provide a magnetic field up to 8.3 T. Additionally, 392 quadrupole magnets keep the beams focused.

Lead ions from an electron cyclotron resonance source are bunched and accelerated by a radio frequency quadrupole. They are selected in the charge state Pb^{27+} and further accelerated in the linear accelerator LINAC3 to 4.2 MeV/nucleon. Afterwards, they are stripped by a carbon foil and the charge state Pb^{54+} is selected in a filter line. These selected ions are further accelerated in the low energy ion ring (LEIR) to an energy of 72 MeV/nucleon. From there the ions are transferred to the PS where they are accelerated to 5.9 GeV/nucleon and sent to the SPS. In between they

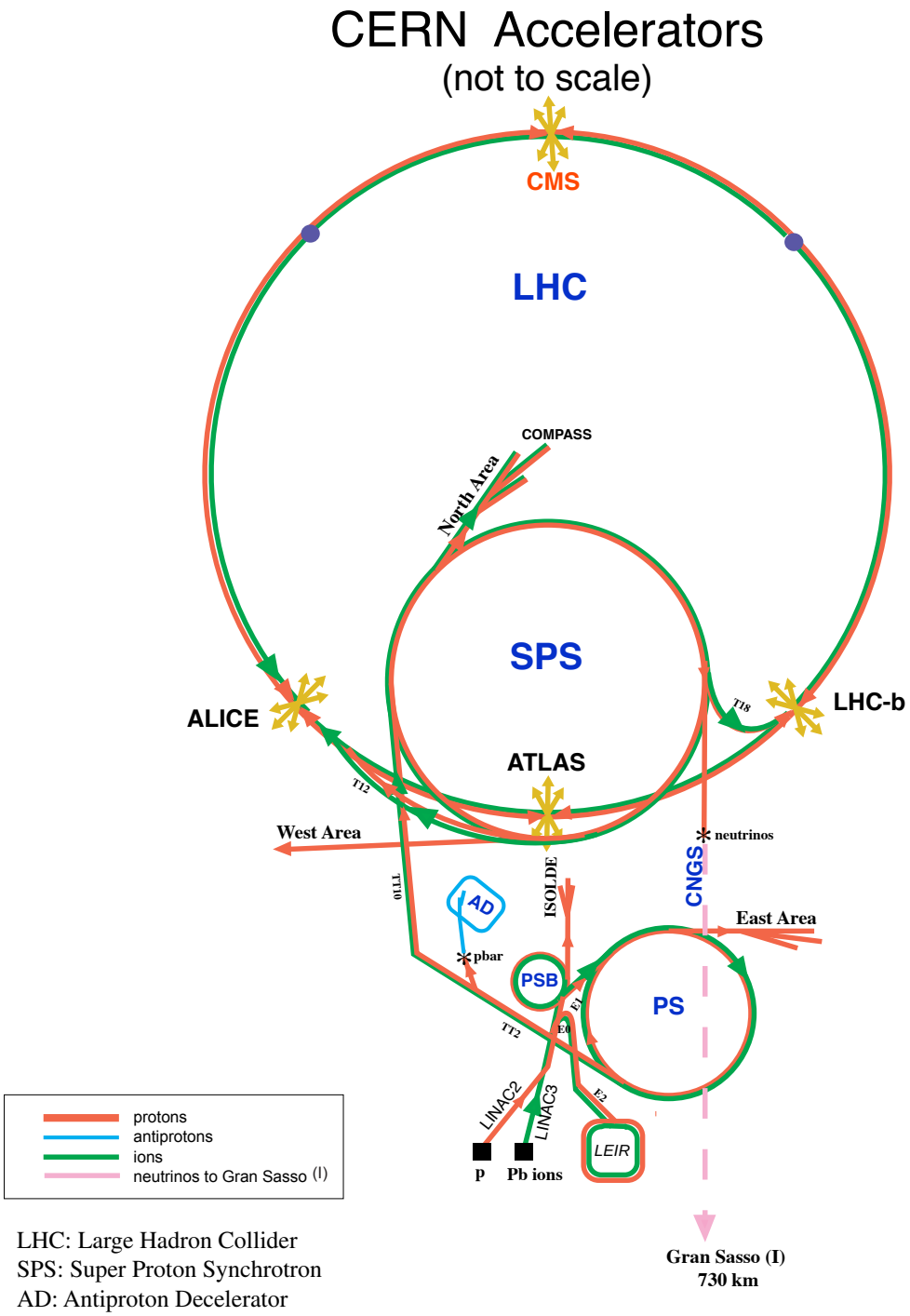


Figure 2.1: Overview of the accelerator system at CERN, taken from [30].

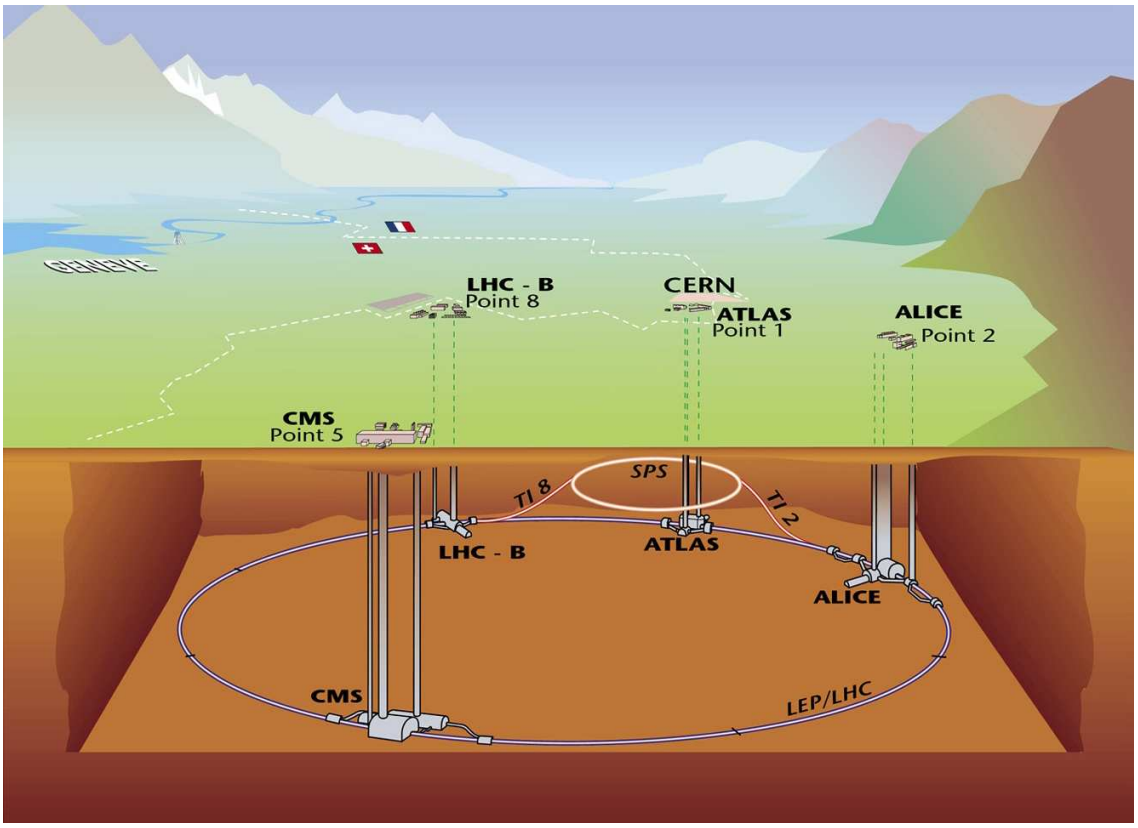


Figure 2.2: Schematic view of the Large Hadron Collider and its four experiments ALICE, ATLAS, LHCb and CMS, taken from [30].

pass another foil which fully strips the ions to Pb^{82+}. The SPS accelerates the fully stripped ions to 177 GeV/nucleon, before injecting them into the LHC where they reach a maximum energy of 2.76 TeV/nucleon.
The two beams are brought to collision at eight interaction points. At four of these the main experiments are located as indicated in fig. 2.2.

ATLAS: The main goal of A Toroidal LHC Apparatus (ATLAS) experiment is the discovery of the Higgs-Boson and the investigation of theories beyond the standard model, such as the search for supersymmetric particles and extra dimensions.

CMS: The Compact Muon Solenoid (CMS) is designed to analyze the nature of matter. In principle the CMS and the ATLAS experiments are built for the same purpose applying complement detector technologies.

LHCb: The LHC Beauty (LHCb) experiment is built to observe CP violation in B-meson systems. The results will help to understand the difference between matter and antimatter in the universe.

ALICE: A Large Ion Collider Experiment (ALICE) is the dedicated heavy ion detector at the LHC. The ALICE detector is designed to identify and characterize the quark gluon plasma. ALICE is briefly described in the next section.

2.2 A Large Ion Collider Experiment

A Large Ion Collider Experiment (ALICE) is designed to determine the identity and precise trajectory of more than ten thousand charged particles over a large momentum range from 100 MeV/c to 100 GeV/c in transverse momentum. The layout of the ALICE detector which is split into the so-called Central Barrel and the Muon arm is illustrated in fig. 2.3.
The Muon Arm covering a pseudo-rapidity range from $-2.4 < \eta < -4.0$ is dedicated to the measurement of muons. Hadrons and electrons are removed by the absorber made predominantly out of carbon and concrete. The muon tracks are bent for momentum measurement by the dipole magnet with an integrated field of 3 Tm and then detected by the tracking system which covers a total area of about 100 m^2 and achieves a spatial resolution of about 100 μm. The tracking system consists of cathode pad chambers which are arranged in five stations: two are placed before, one inside and two after the dipole magnet. The stations are made of two chamber planes. Their size ranges from few square metres for the first station to more than 30 m^2 for last station. To trigger on J/ψ or Υ a trigger system, arranged in two stations placed behind the muon filter consisting of four Resistive-Plate Chamber (RPC) planes with the total active area of about 150 m^2, is used.
The ALICE central barrel covers the kinematic region around mid-rapidity $|\eta| < 0.9$ and is surrounded by the L3 solenoidal magnet which produces a homogeneous magnetic field of up to 0.5 Tesla parallel to the beam axis. This magnetic field provides momentum dispersion for charged particles in the plane transverse to the beam axis.

The central part of ALICE is an assembly of various detectors. The detectors providing in-

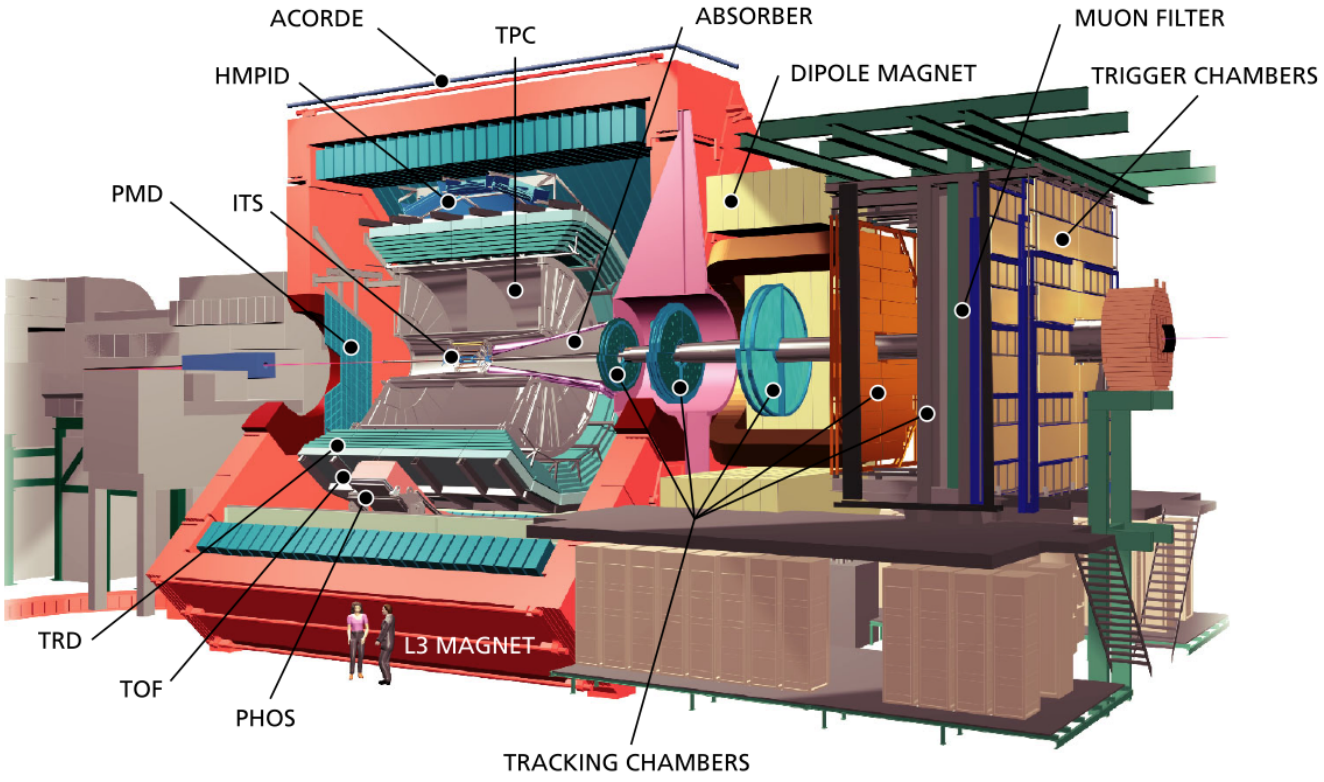


Figure 2.3: Schematic layout of the ALICE detector. This figure has been taken from [31].

formation like momentum, vertex coordinates and particle identification are the Inner Tracking System (ITS), the Time Projection Chamber (TPC), the TRD and the Time of Flight (TOF). They all cover a pseudo-rapidity range of $|\eta| < 0.9$, full azimuth and comprise the ALICE central barrel. The central barrel is used for the presented studies and is described in more detail in the following.

Inner Tracking System
The main purpose of the Inner Tracking System (ITS) is the determination of vertices with high spatial resolution. Additionally the ITS provides tracking and identification of particles with momenta down to 100 MeV/c and improves the momentum resolution of tracks with higher momentum. To cope with the large number of charged particles expected to be produced in a lead-lead collision the ITS has a high granularity and radiation hardness. To keep the distortion of tracks of charged particles to a minimum, the total thickness of ITS was optimised to be 7% radiation length. Therefore the ITS consists of six cylindric layers each of a different type: the first two layers are Silicon Pixel Detectors (SPD), followed by two layers of Silicon Drift Detectors (SDD) and two layers of double-sided Silicon micro-Strip Detectors (SSD). These six layers are located at radii $r = 4, 7, 15, 24, 39$ and 44 cm [31]. The first layer is located only 4 cm away from the beam axis, and covers almost four units of pseudo-rapidity. The two layers of SPD have a spatial resolution of 12 μm in the $r\phi$-plane and 70 μm in z-direction, the resolution of the two layers of SDD is 28 μm in z-direction and 38 μm in $r\phi$-direction while the two outer layers have a 20 μm $r\phi$-resolution and 830 μm z-resolution. The precise measurement in ITS allows the extrapolation of tracks back to the primary vertex of the collision with an impact parameter resolution better than 100 μm.

Time Projection Chamber
The Time Projection Chamber (TPC) is the main tracking detector in the central barrel ($|\eta| < 0.9$) of the ALICE experiment. The TPC provides charged particle momentum measurement and primary vertex determination with precise momentum resolution at a large tracking efficiency of 90% and two-track separation up to a p_T region of more than 10 GeV/c. Additionally correct pattern recognition of the high multiplicity Pb+Pb central collisions at the LHC energy are achieved by the TPC. Up to 20 thousand primary and secondary charged tracks per event are expected in the sensitive volume. The cylindric TPC has an inner radius of 80 cm, an outer radius of 250 cm and an overall length of 5 m, covering full azimuth. This means the ALICE TPC is with its active volume of about 95 m^3 the largest TPC ever built. The total material budget is kept at the level of 3% radiation length to ensure minimal multiple scattering and secondary particle production. The TPC cylindrical field cage of 88 m^3 size is divided by a central electrode into two drift regions. The high voltage central electrode provides a uniform electrostatic field of 400 V/cm. The whole drift volume in the cage is filled with a gas mixture of 85% Ne / 10% CO_2/ 5% N. Within this drift gas the maximum drift time is $t \sim 88$ μs. Three-dimensional space points are reconstructed from the measured drift time (z-direction) and the position on the cathode pads (x, y-direction) of the induced signal. In total, the TPC provides up to 160 space points for each particle trajectory. Additionally the TPC contributes strongly to the particle identification. Particles are identified within the TPC by their specific loss of energy due to interactions with the TPC gas. More details are discussed in the next chapter.

Transition Radiation Detector
The TRD identifies electrons with $p_T > 1$ GeV/c and provides fast trigger capability of 6 μs. More details of the TRD are described in chap. 3.

Time Of Flight
Time of Flight (TOF) detector is the most outer part of the ALICE tracking chain and extends the identification of hadrons, namely π, K, p, in a momentum range up to 4 GeV/c by measuring the time a particle needs to fly from the interaction point to a radial distance of approximately 4 m. TOF is composed of 18 supermodules surrounding the 18 TRD supermodules and covers a surface larger than 160 m^2. The TOF detector is composed of multigap resistive plate chambers (MRPC) which achieve a time resolution of 65 ps at a rate of more than 50 Hz/cm^2.

The detectors dedicated to a specific physics task are the Photon Spectrometer (PHOS) measuring high momentum photons, the High Momentum Particle Identification (HMPID) to separate koans from pions and protons and the Electro-magnetic Calorimeter (EMCAL) for the detection of high momentum electro-magnetic probes. These three detectors cover only a small part of the full acceptance. A detailed description of the individual subcomponents of ALICE is found in [32].

ALICE Coordinate System
The *global* coordinate system is defined in accordance with the LHC. The origin is defined as the arbitrary centre of the detector where the collision ideally occurs. The z-axis is parallel to the beam direction. Perpendicular to the z-axis is the transverse $r\phi$-plane in x, y-direction, where the x-axis is horizontal, and the y-axis is vertical. The system is right-handed, with positive x pointing inwards referred to the LHC ring, positive y pointing upwards and positive z pointing in the opposite direction of the muon arm. The azimuthal angle Φ increases, starting in x-direction $\Phi = 0°$ counter-clockwise viewed from z-direction. This coordinate system is generally used to locate an object described in the global view of the detector, e.g. the sub-detectors, the track vertex, etc.
Clusters and tracks are always expressed in a *local* coordinate system related to a given sub-detector (TPC super module, ITS module etc). This local coordinate system is defined as following:

- it is a right handed-Cartesian coordinate system;
- its origin and the z axis coincide with those of the global ALICE coordinate system;
- the x axis is perpendicular to the sub-detector's sensitive plane e.g. the TPC pad row, ITS ladder, TRD pad plane.

This choice reflects the symmetry of the ALICE setup and therefore simplifies the reconstruction equations. It also enables the fastest possible transformations from a local coordinate system to the global one and back again, since these transformations become single rotations around the z-axis.

Experiment Control System

A complex software hierarchy is used to monitor and control the ALICE detector. The top layer of this hierarchy is the so called Experiment Control System (ECS), shown in fig. 2.4, which acts as a mediator between the different software entities, being:

- Data Aquisition (DAQ)
- Detector Control System (DCS)
- High Level Trigger (HLT)
- Trigger System (TRG)

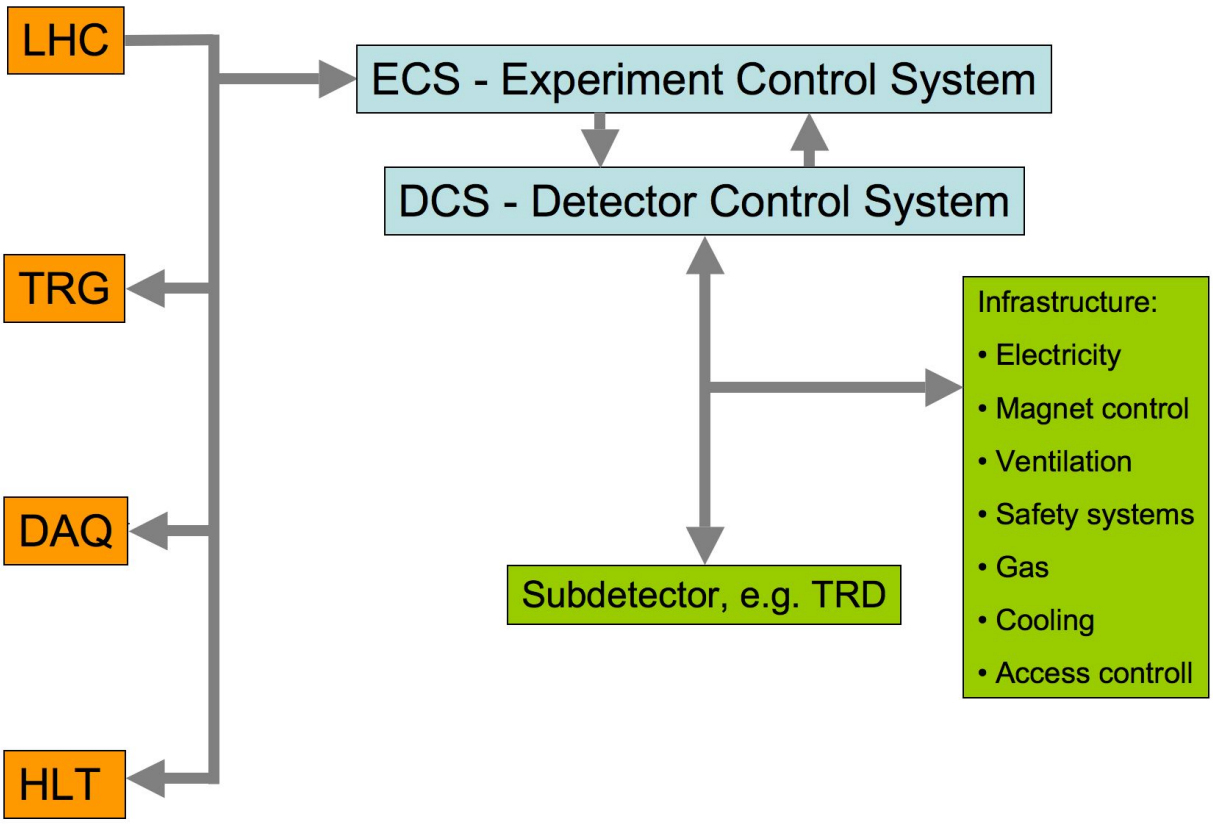


Figure 2.4: Relations between ECS, Detector, Infrastructure and other entities.

The DCS controls all hardware relating to the detectors. This is carried out by custom software embedded in the PVSS framework and is controlled via a graphical user interface from the ALICE

control room. More information is given in sect. 6.1.
The HLT analyses raw data from all detectors. It filters and compresses the data and subsequently writes it onto long term storage devices.
The Trigger System consists of the Central Trigger Processor (CTP), which provides the logic for the trigger decision, and the Trigger Distribution Network. This network transmits the different trigger signals (subsect. 3.3.1) to and from all subdetectors by using the Timing, Trigger and Control (TTC) system, developed by CERN [49].

3 The Transition Radiation Detector

3.1 Energy Loss of Charged Particles

A charged particle deposits energy if it traverses matter, e.g. if it passes through the drift chambers gas of the Transition Radiation Detector (TRD). Processes of energy loss by ionisation are described by the *Bethe-Bloch formular*. Radiative energy loss or *Bremsstrahlung* and transition radiation are further processes of energy loss. These processes depend on the particle velocity. Thus, at a given momentum it allows for the determination of its mass and hence the particle's identity.

Ionisation and the Bethe-Bloch Formula

When passing through a medium a charged particle loses energy via ionisation or excitation of the constituent atoms. The mean energy loss per path length is derived from the Rutherford formula for elastic scattering and is described by the *Bethe-Bloch formula* [27]:

$$-\frac{dE}{dx} = \frac{4\pi N_A z^2 e^4}{mv^2}\frac{Z}{A}\left[\ln\left(\frac{2mv^2}{I(1-\beta^2)}\right) - \beta^2\right] \tag{3.1}$$

The path length x in the medium is usually given in [$g\ cm^{-2}$ or $kg\ m^{-2}$] and corresponds to the amount of matter traversed. Here, m is the electron mass, z and v are the charge and velocity of the traversing particle. The relativistic velocity is given by $\beta = v/c$, N_A is Avogadro's number and I is an effective ionisation potential of the atom species of the medium, averaged over all electrons, with approximate magnitude $I = 10\ Z\ eV$ [27]. Z and A are the atomic number and mass number of the medium's atoms. The energy loss described by eq. (3.1) drops with $1/\beta^2$ for small $\gamma = E/Mc^2 = (1-\beta^2)^{-1/2}$, M being the mass of the passing particle, reaches a minimum for $E \simeq 3\ Mc^2$ and increases afterwards logarithmically with γ. The drop is due to the particle having less time to interact with the medium the faster it gets. The slow rise for high γ originates from relativistic effects, leading to an increase of the transverse electric field of the particle which enables atoms of the medium that are further away from the particle's path to interact with the particle. This effect saturates into the Fermi plateau, since the polarisation of the medium shields the electro-magnetic field of the moving particle.
The energy loss described by eq. (3.1) is independent of the particle mass M. The specific energy loss of different particles with the same momentum $p = Mv$ is used to identify the particle species if momentum of the particle is known, e.g. via the curvature of the path in the magnetic field.

Bremsstrahlung

Additionally to ionisation, particles loose energy due to radiation of photons when traversing matter. The electric field of the atomic nuclei of the medium decelerates the passing particle, resulting in the emission of a photon, therefore the name *Bremsstrahlung*.
The average energy loss per unit length is given by:

$$-\frac{dE}{dx} = 4\alpha_e N_A \frac{Z^2}{A} z^2 r_0^2 E \ln \frac{183}{Z^{1/3}} \tag{3.2}$$

$$-\frac{dE}{dx} = \frac{E}{X_0} \tag{3.3}$$

With variables and constants as in eq. (3.1) and , the classical electron radius $r_0 = \hbar/c\alpha_e M$, M donating the electron mass. Energy loss from Bremsstrahlung drops with the traversing particle's mass squared M^{-2} and rises proportional to its energy E. Therefore Bremsstrahlung is mainly seen from electrons. X_0 is the characteristic radiation length after which the energy of the particle is reduced by a factor $1/e \approx 1/3$.
For low energies the energy loss is dominated by ionisation. However the ionisation effect is almost constant for high energies, while the radiative energy loss rises with E Bremsstrahlung becomes the dominating effect. For electrons the critical energy at which both effects contribute equally is:

$$E_c \simeq \frac{600}{Z}\ MeV. \tag{3.4}$$

Transition Radiation

Another radiative effect is transition radiation (TR). It is produced if an ultra-relativistic particle crosses the boundary surface of two media with different dielectric constants, fraction indices n, respectively. The electro-magnetic field of a charged particle changes with the dielectric constants of the medium by which it is surrounded. Since the electric field is continuos at the boundary region the field of the charged particle has to change, hence radiation is emitted. A qualitative description of transition radiation is obtained from classical electro dynamics by using the model of a mirror charge of the particle within the medium with opposite charge and equal distance to the boundary surface. The actual particle and its mirror self form a dipole evolving in time since the particle is moving towards the boundary and so is its mirror charge. Therefore radiation is emitted in an angle of $\Theta \propto 1/\gamma$. The typical energy of an emitted photon is $E_\gamma \simeq \gamma\hbar\omega_p$ with the plasma frequency of the corresponding medium $\omega_p = \sqrt{4\pi\alpha n_e/m_e c^2} = 28.8\sqrt{\rho\frac{Z}{A}}$.
Since the transition radiation is related to $\gamma = \sqrt{1/1-\beta^2}$ whereas other energy loss effects depend on β, transition radiation is a great tool to identify particles in higher momenta regions. For the momenta at which particles reach the TRD, electrons are the only particles with $\gamma > 1000$ and therefore produce transition radiation making TR a good tool to identify electrons.
On the other hand, the mean number of emitted transition radiation photons per boundary surface is with about $\frac{1}{137} = \alpha_e$ rather low. Within a TR detector many boundary surfaces are therefore used, realised as foil sequences, micro fibers or other materials providing a large number of boundary surfaces. The number of TR photons is, though, limited and saturates for many

boundary surfaces, because of interference effects. For regular foil sequences analytic calculations are possible which are not possible for other radiator types.

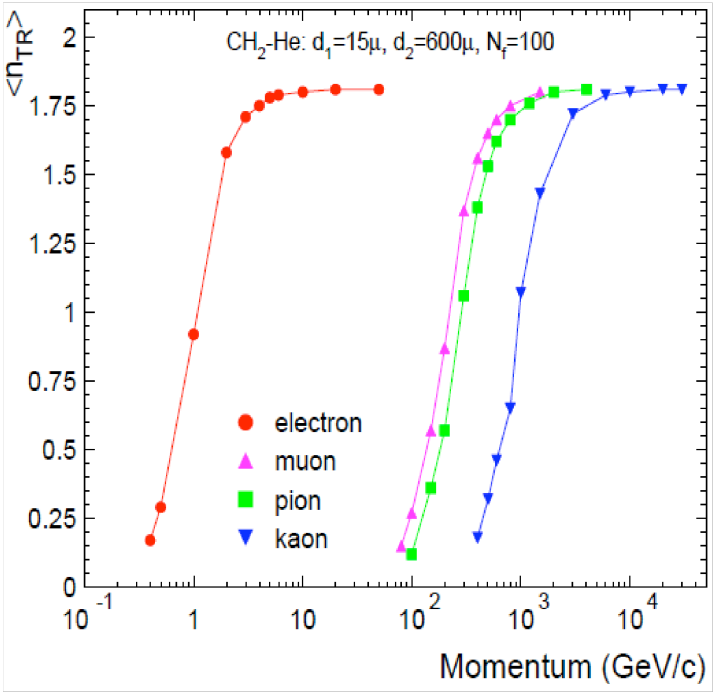


Figure 3.1: The mean number of transition radiation photons produced by various particles versus momentum. The mean number rises and saturates quickly after a threshold momentum is reached.

3.2 Detector Design

The ALICE TRD is located between the Time Projection Chamber (TPC) and the Time of Flight (TOF) in the radial range from 2.9 m to 3.7 m in the ALICE spaceframe with an overall length of 7 m. It consists of 540 gas detector modules arranged in 18 supermodules mounted in radial direction. Each supermodule is divided into 6 layers in radial direction and 5 stacks in beam direction. Hence one supermodule consists of 30 detector modules.
Part of each of the 540 modules is a sandwich radiator and a multiwire proportional chamber, whose drift region filled with 85% Xe and 15% CO_2. The multiwire proportional chamber includes the drift region and the amplification region. The drift region has a width of 3 cm and the amplification region as another part of the module 0.7 cm.
In the sandwich radiator as many boundary surfaces as possible are used to reach a higher yield of transition radiation. Nevertheless, stacks of foils do not provide sufficient mechanical stability and additional supply structures would be needed to strain the foils. The supply structures would lead to large inactive areas which not only reduce the acceptance of the TRD but also spoil the possible results of detectors behind the TRD. The solution found for the ALICE TRD radiator is a combination of foam and fibres providing the optimal combination of TR efficiency and mechanical stability. Figure 3.2 shows the principle design of the radiator sandwich. The supporting structure with good transition radiation production rate is made out of a polymethacrylimide foam, called

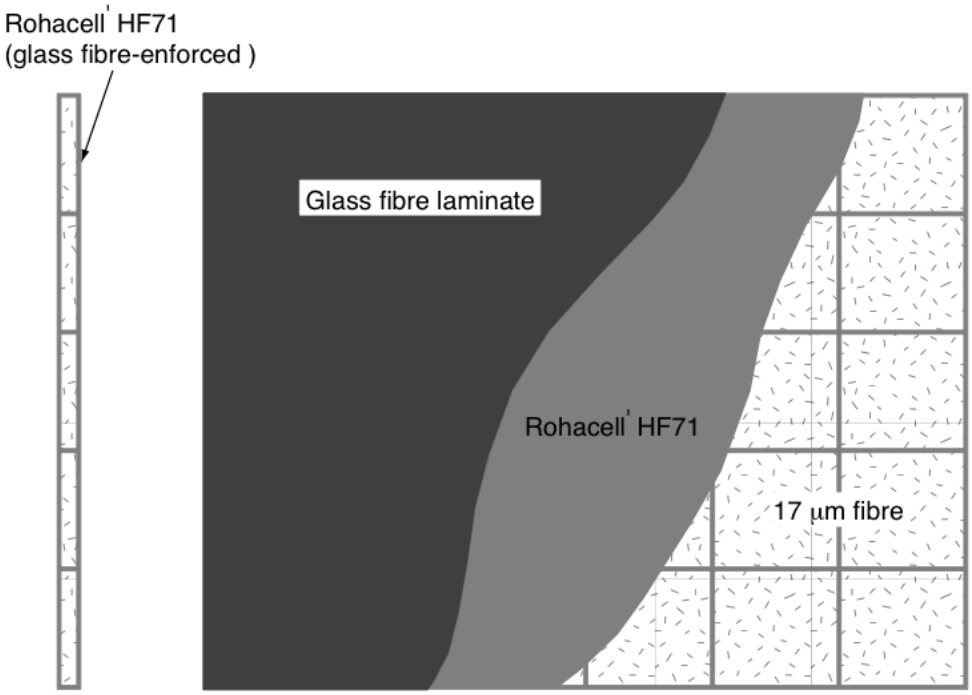


Figure 3.2: Schematic design of a ALICE TRD sandwich radiator providing the optimal combination of TR efficiency and mechanical stability. This figure has been taken from [32].

Rohacell HF71 of 8 mm thickness reinforced by glass fibre sheets. The inner volume of the sandwich cells is filled with polypropylene fibre mats being the main radiator material. Scanning electron microscope images of both materials are shown in fig. 3.3.

Since it is not possible to calculate the energy loss of such materials analytically, simulations of the detector response parametrisations are used. In the case of the ALICE TRD the behavior of the radiator is modeled by a foil stack in good agreement with measured results.

The design of the ALICE TRD as well as the signal creation is schematically shown in fig. 3.4. The large cluster at the beginning of the drift chamber originates from a transition radiation photon of the electron. Electrons produced by ionisation energy loss (dE/dx) and by transition radiation absorption drift along the field lines toward the amplification region where they produce avalanches around the anode wires. These avalanches induce a signal on the cathode pads. The insert in the right figure shows the distribution of pulse height over pads and time bins spanning the drift region for a measured electron track. The local coordinate system shown is the coordinate frame of a single readout chamber with the z-direction parallel to the beam axis.

3.3 Readout Chain and Data Aquisition

3.3.1 Trigger Sequence

Data taking, its processing and storing depends on a trigger sequence monitored by the Central Trigger Processor (CTP) of ALICE. The trigger sequence and the initiated actions concerning the TRD are summarized in fig. 3.5 and serves as example for the trigger sequence. A number of detectors produce a signal, the so called "L0 contribution" based on the input of their front-end

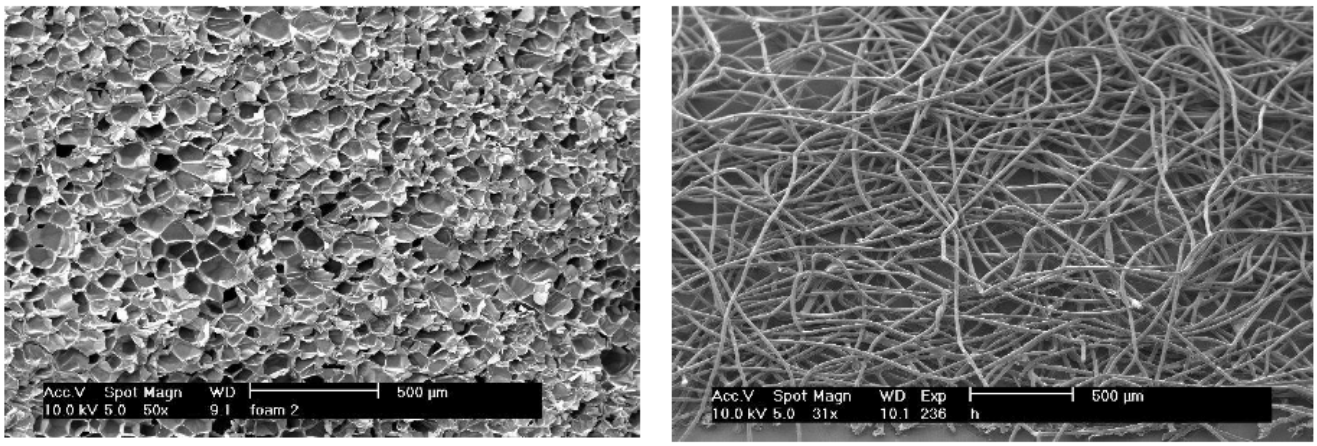


Figure 3.3: Scanning electron microscope images of the used radiator materials: Rohacell HF71 foam (left) and fibres mat (right). This figure has been taken from [32]

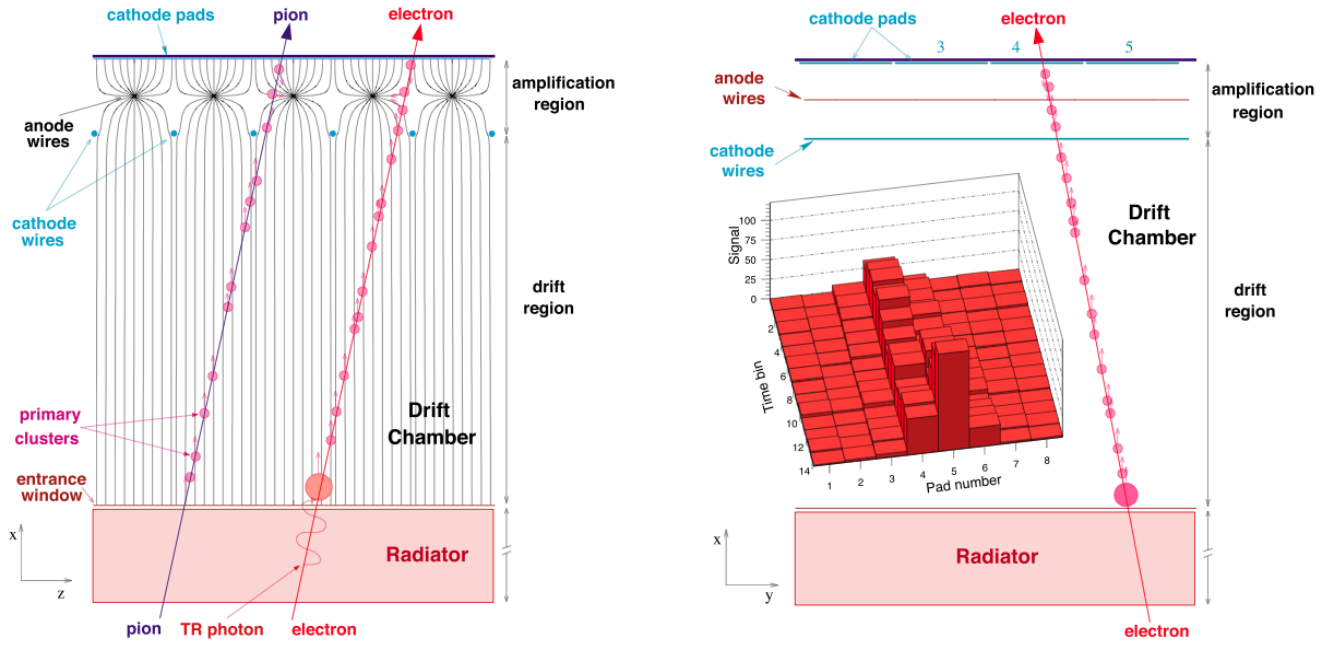


Figure 3.4: The principle of the ALICE TRD. The figure on the left shows the projection in the plane perpendicular to the wires. The figure on the left shows the projection in the bending plane of the ALICE magnetic field. In this direction the cathode plane is segmented into the pads from 0.635 to 0.785 *cm* width. The insert shows the distribution of pulse height over pads and time bins spanning the drift region for a measured electron track. This figure has been taken from [32].

electronics, which is sent to the CTP. The CTP derives upon this input the L0 trigger which is sent to the front-end electronics of all subdetectors, arriving there approximately 1.2 μs after the collision and triggering the further processing of the event. Among others, the detectors used are the Time of Flight detector, the TRD, T0, V0 and the Silicon Pixel Detector.
Based on the trigger inputs from all detectors after 6.1 μs, the CTP produces the L1 trigger. The L1 trigger is expected to arrive at the front-end electronics after (6.5 $\pm$ Δt) μs. Δt is a configurable margin. If L1 does not arrive within this time interval, the subdetectors regard this as the abort of the trigger sequence, consequently stopping the processing of the current event. In opposite case, a set time after the L1 trigger arrives, the subdetectors send information to the CTP containing event identification and trigger details.
After evaluating the past-future protection condition, which is a measure to prevent pile-up and

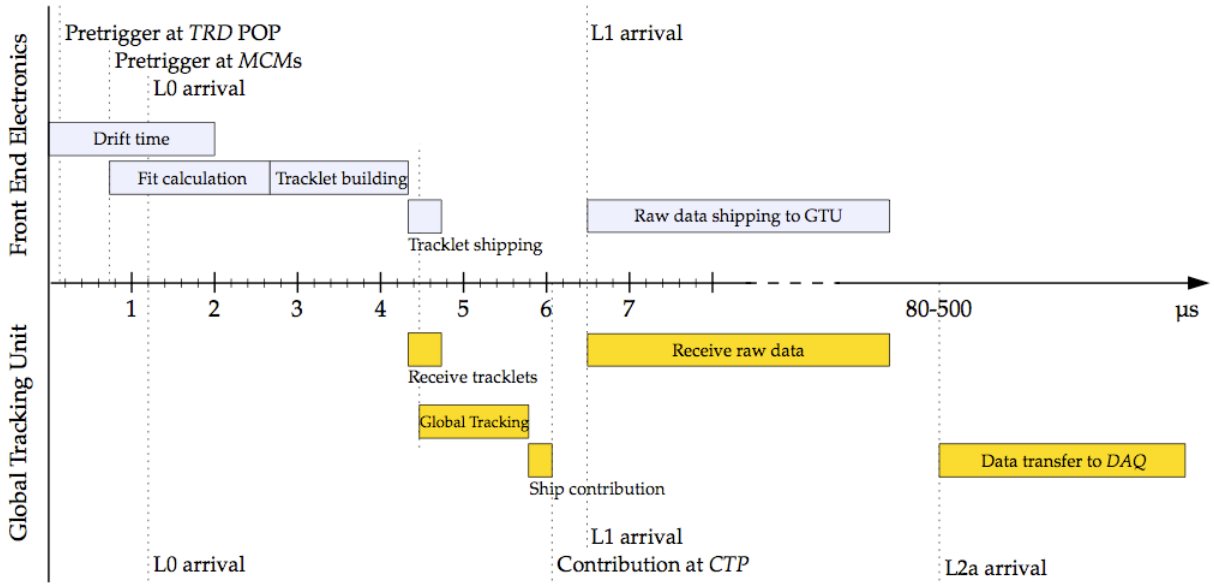


Figure 3.5: Timetable of triggers and initiated actions of the Front-End Electronics and the Global Tracking Unit in a non-interleaved trigger sequence.

overlapping events, the CTP provokes the transmission of either a 'L2 accept' or a 'L2 reject' signal. The 'L2 accept' starts the shipping of the raw event data to the Data Aquisition unit and is expected to arrive at the front-end electronics in the time window between 80μs and 500μs after the collision.
As a further trigger stage the High Level Trigger reconstructs the event online and decides on its permanent storage. Due to the vast amount of raw data and limited bandwidth to the Data Aquisition unit, the High Level Trigger filters and compresses the event. Depending on the event size, up to 30 events per second are stored.

3.3.2 Front-End Electronics

The part of the detector reading out the signals from 540 chambers are the so called front-end electronics. Each chamber is mounted with readout boards equipped with up to 18 special chips.

The chips, called Multi Chip Module (MCM), consist of two parts: the PASA and the Tracklet Processor (TRAP) chip.
The PASA reads out 18 channels preamplifying and continuously shaping the analog signal arriving from the chamber. This happens regardless of the trigger level. The Tracklet Processor chip is the digital part of the Multi Chip Module. One of its functions is the tracklet building.
A tracklet is a fit to the track of the traversing particle. The tracklet building is only activated after receiving a L0 trigger. All tracklets of a half-chamber are shipped via optical fibers to the Global Tracking Unit (GTU), which merges tracklets to tracks. The different stages for building a tracklet are shown in fig. 3.6. Upon the result of the reconstruction by the Global Tracking Unit, the L1 trigger contribution of the Transition Radiation Detector is sent to the CTP. Shortly after the L1 trigger arrives at the front-end electronics and requests the shipment of the raw data from the front-end electronics to the Global Tracking Unit, it is buffered until a 'L2 accept' arrives. The data is then shipped to the Data Aquisition unit.
The timing of triggers and front-end electronics actions are summarized in fig. 3.5. To reduce heat

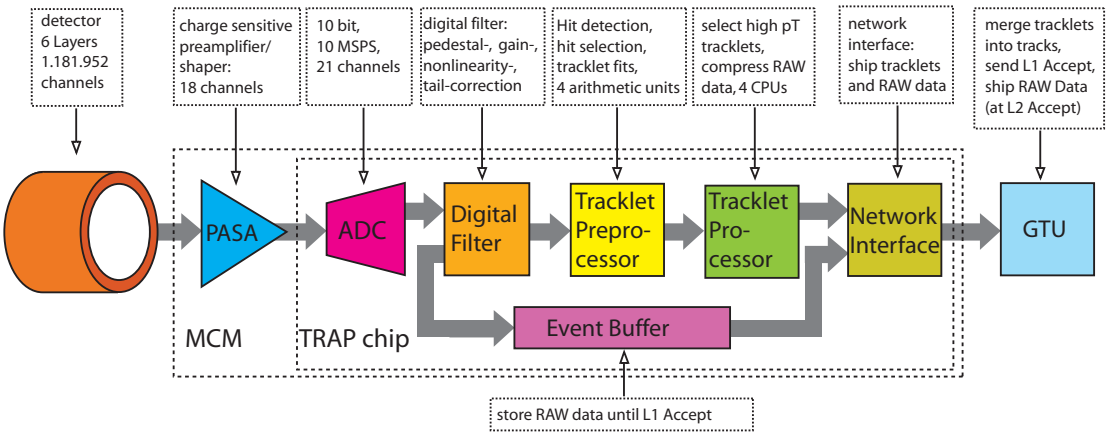


Figure 3.6: Readout chain of Front-End Electronics of the Transition Radiation Detector

and noise production on the readout boards the electronics are reduced to a minimum. Therefore the event buffer in each chip is of limited size. It stores up to 900 ns of raw data. Assuming that the L0 trigger of the Central Trigger Processor, issueing the readout of the Multi Chip Module (MCM) raw data, arrives 1.2 μs after the collision, an overflow occures. Data obtained from electron clusters near to the readout pads is already overwritten by data from clusters with a long drift time. Therefore, unlike other detectors, the TRD needs a trigger signal prior to the L0 signal of the CTP. This signal is called pre-trigger signal and is generated by the pre-trigger hardware. In order to achieve a fast trigger signal, the hardware is located inside the L3 magnet near to the beam pipe and the signal is derived from the detector signals of the fast V0 and T0 trigger detectors and the Time of Flight detector. Further details are given in chap. 5.

The control and configuration of the MCMs is realized with a custom designed board, the Detector Control System (DCS) board [41]. On each chamber of the TRD is one of these boards. It is attached to a readout board and has the dimensions of 14.5 cm x 9 cm. The board has several interfaces, such as Slow Control Serial Network (SCSN), Joint Test Action Group (JTAG) and ethernet. A small Linux system runs on it and it is accessible via ethernet with the Secure

Shell (SSH) protocol.
The MCMs are accessible via SCSN and they are, together with the DCS board, logically arranged in a ring. The DCS board send commands to individual MCMs by sending it to the first MCM in the ring and forwards it to the next chip in the ring until it reaches its destination. If one of the MCMs in the ring breaks down, it is possible to bridge that one to sustain the command chain. The JTAG is used to recover DCS boards, which have a serious failure in the firmware. The DCS boards are arranged in a JTAG chain and the neighbouring DCS board reprograms the errorneous one by uploading the firmware. The DCS board was not exclusively designed for the TRD and is used also in many other places in ALICE, for example in the pre-trigger system. More information on this topic are given in the doctoral thesis of T. Krawutschke [42].

3.4 Charged Particle Identification

The ALICE experiment identifies particles over a large range of momenta from about 0.1 GeV/c up to a few tens of GeV/c. This is schieved by combining the information obtained by the different sub-detectors, ITS, TPC, TRD, TOF and HMPID, which are optimised for smaller momentum ranges as illustrated in fig. 3.7.

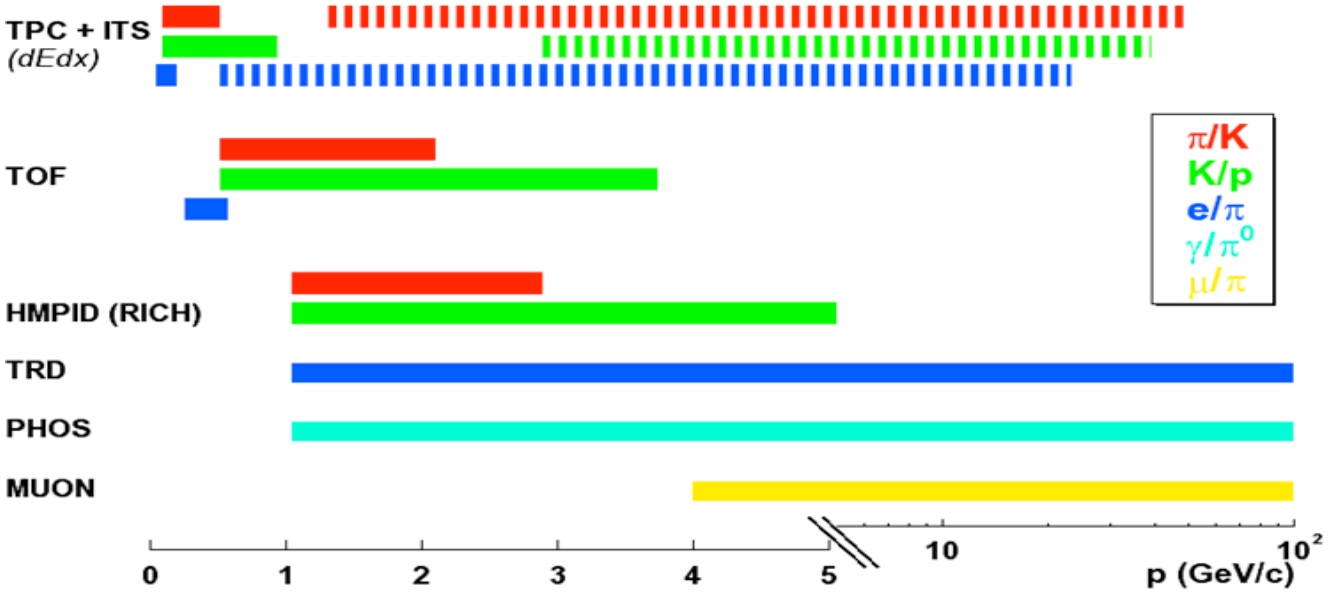


Figure 3.7: Particle identification in ALICE: momentum range and detectors used. This figure has been taken from [33]

First a brief overview of the particle identification (PID) methods and capabilities, e.g. found in [31] for the four main central barrel sub-detectors is given, followed by more detailed information about PID with the TRD.

- *ITS* uses energy loss in the non-relativistic ($1/\beta^2$) region, therefore particle identification of low momentum particles and reconstruction of secondary vertices is possible.

- *TPC*: Charged particles ionise the gas of the detector. The Bethe-Bloch equation eq. (3.1) relates the velocity β of a particle to its mean energy loss per path length, dE/dx. The Time Projection Chamber (TPC) is designed to provide dE/dx information with a resolution better than 7%. Combining dE/dx and momentum information yields the particle identity.

- *TRD* uses the production of transition radiation by electrons additional to ionisation energy loss. It is designed to detect electrons at higher transverse momenta $p_t > 1$ GeV/c and helps substantially to improve the e/π separation, as discussed in more detail in the next section.

- *TOF* uses the time of flight a particle needs to traverse a defined path length. Time of Flight (TOF) is used for separating kaons and pions up to $p_T < 3$ GeV/c and kaons and protons up to $p_T < 5$ GeV/c.

Each of the sub-detectors gives a standalone particle identification. When a track is reconstructed in more than one sub-detector simultaneously, the particle identification is improved by combining the single detector PID information.

Particle Identification with the TRD

Particles entering the TRD drift chamber, as well as transition radiation photons they produced, ionise the gas in the chamber and create electron clusters. The transition radiation photon is absorbed shortly after entering the drift chamber due to the chosen gas mixture. The primary particle constantly generates electron clusters on its way through the chamber.
The final signals produced at the cathode pads as described above are read out at a 10 MHz sampling rate such that the signal height on all pads is sampled in time bins of 100 ns. Figure 3.8 shows the measured average signals of pions and electrons with and without transition radiation versus the drift time. For small drift times the average pulse height increases rather strongly, it is about twice as high as for time bins in the mid-region. This is due to the signal coming from the amplification region. The following plateau originates from the drift region. The signal from transition radiation of the electrons arrives preferentially later, in higher time bins, since the radiation photons are produced at the entrance of the detector and therefore any signal deriving from them has the longest distance to travel until it is read out.

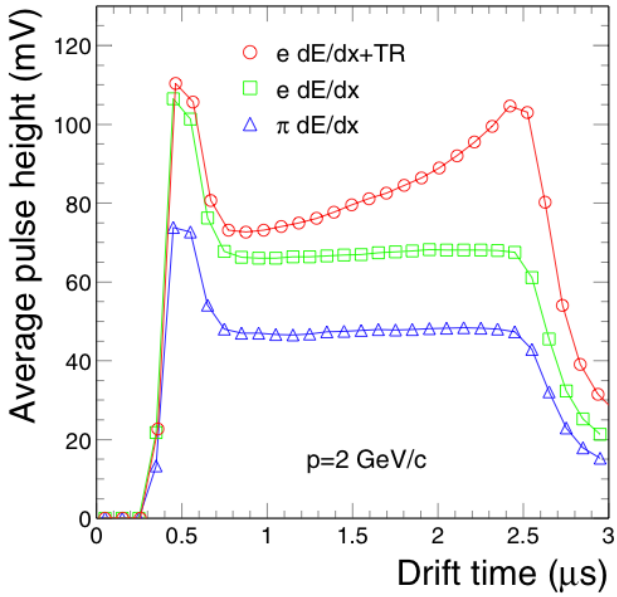


Figure 3.8: Average pulse height versus drift time for electrons (upper and middle) and pions (lower). The different pulse heights indicate the different ionization energy (dE/dx) loss of electrons (green rectangles) and pions (blue triangles). The characteristic peak at larger drift times of the electron (red circles) is due to the absorbed transition radiation. This figure as been taken from [32].

In the following the main purpose of the TRD being the seperation of electrons and pions is discussed.
However, the principle of identifying other particles like muons, koans and protons is the same

and look-up tables for each of them exist.
The first approach is the:

LQ-Method

For this ***L***ikelihood method the total deposited energy shown in fig. 3.9, produced charge ***Q*** respectively, in one TRD layer is taken into account. Electrons and pions have the probability

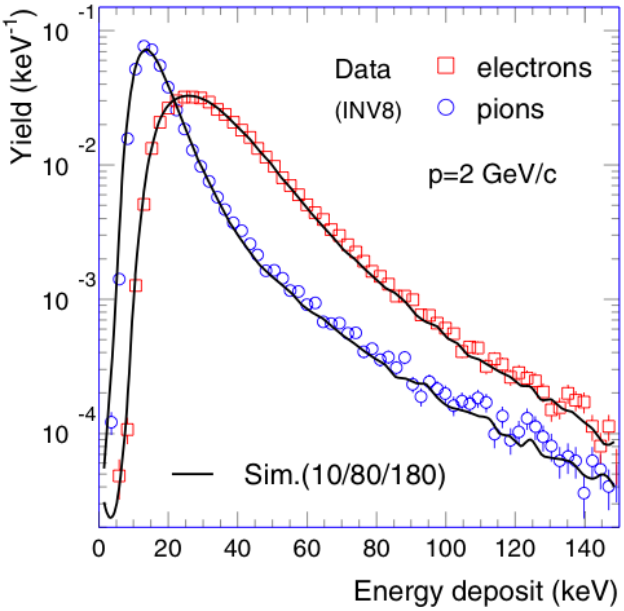


Figure 3.9: Integrated energy deposit for pions and electrons for a momentum of 2 GeV/c. The symbols represent the measurements, the lines are calculations. This figure has been taken from [34].

$P(E_n)$ to deposit the energy E_n in each layer. The total probability of an electron to produce a set of measured values is defined by:

$$P_e(E) = \prod_{n=1}^{6} P^n(E_n|e) = \sum_{n=1}^{6} P(E_n|e) \tag{3.5}$$

where the sum has to be taken over all $n = 6$ layer and the probability P is assumed to be the same in every layer. For pions the analog expression is:

$$P_\pi(E) = \prod_{n=1}^{6} P(E_n|\pi) \tag{3.6}$$

The probability or likelihood that the energy E is deposited by an electron is hence given by:

$$L_e(E) = \frac{P_e(E)}{P_e(E) + P_\pi(E)} \tag{3.7}$$

This likelihood distribution is illustrated for 2 GeV/c electrons and pions in fig. 3.10. The purple band indicates the region to which 90% of all electrons belong and is taken as a baseline value.

This is the definition of the *electron efficiency* meaning that 90% of all electrons are identified correctly. For 90% electron efficiency a pion efficiency of 1% or a pion suppression (factor) of 100 is achieved, meaning that only one out of 100 pions is misidentified as an electron.

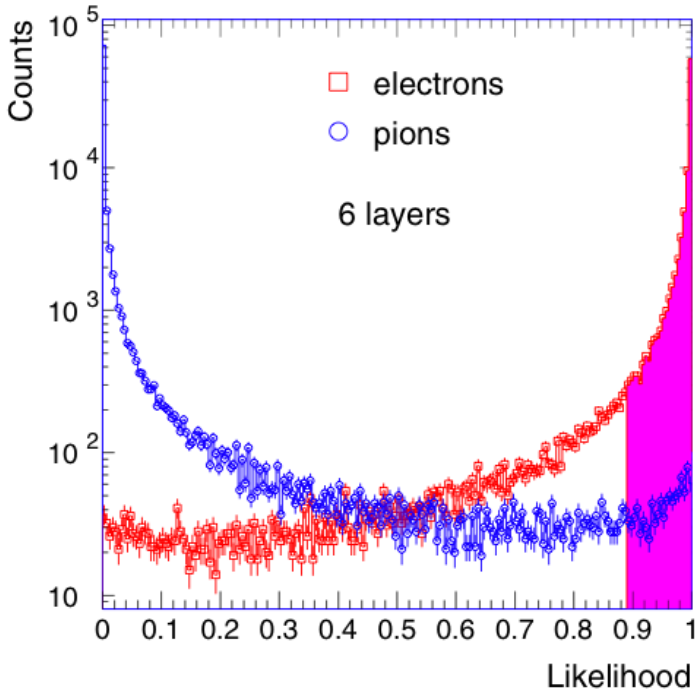


Figure 3.10: Distributions of the likelihood (to be an electron) for electrons and pions of 2 GeV/c, obtained from the total energy deposit. The shaded area corresponds to 90% electron efficiency. This figure has been taken from [34].

Factors influencing the pion efficiency are:

1. The chosen electron efficiency. The pion efficiency improves substantially by almost an order of magnitude when lowering the electron efficiency from 0.9 to 0.7. Nevertheless, the improvement of the pion suppression does not compensate the loss of this amount of electrons since e.g. the quarkonia yield depends quadratically on the electron yield.

2. The number of layers ergo the amount of information available for the probability calculations. Not every track leaves useable PID information in each layer, because of the statistical character of energy loss and the geometric acceptance. The, with about a factor of two per layer, strong dependence of the pion efficiency on the number of layers used in the PID calculations is shown in fig. 3.11 for fixed electron efficiency and particles with momentum $p = 2$ GeV/c.

3. The momentum of the particle. The momentum dependence of the pion rejection is shown in fig. 3.12. The data points (red) indicate that the pion efficiency increases from momenta larger than 2 GeV/c on. At $p = 6$ GeV/c the pion rejection is about a factor 2 worse than it is at 2 GeV/c. In this regime, the transition radiation yield, which almost saturates, no longer compensates the relativistic rise of the pions deposited energy (dE/dx).

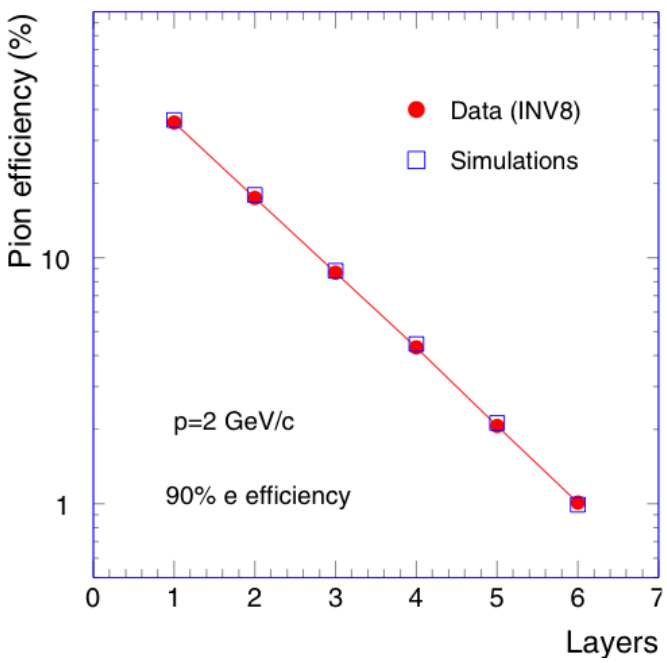


Figure 3.11: Pion efficiency as a function of the number of layers for a momentum of 2 GeV/c. This figure has been taken from [34].

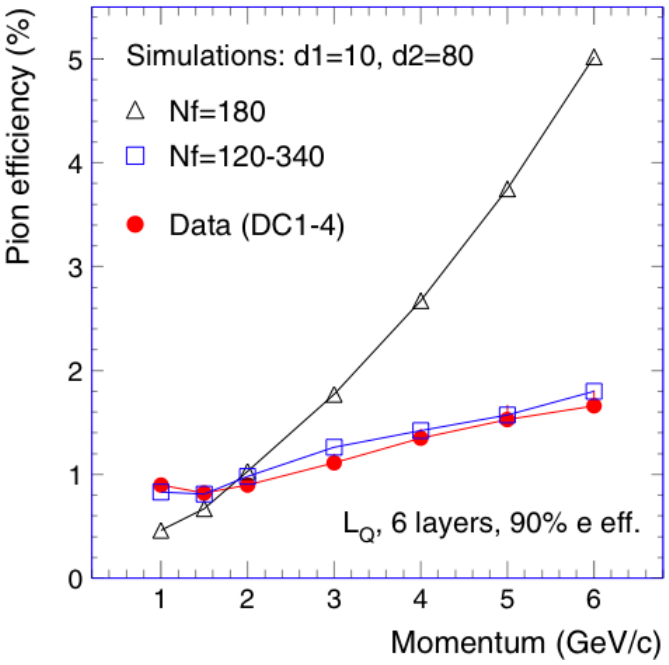


Figure 3.12: Measured and simulated pion efficiency as a function of momentum. This figure has been taken from [34].

LQX-Method

The upper mentioned straight forward method is not making use of the important temporal distribution of the deposited energy. The maximal amplitude originating from the transition radiation of an electron is measured in higher time bins. With including this information to the integrated charge measurement a additional dimension is added to the particle identification approach, resulting in a bi-dimensional likelihood or L_{QX} method. The probabilities eq.(3.5) and eq.(3.6) are adapted to

$$P_e(E) = \prod_{n=1}^{6} P^n(E_n|e) \cdot \prod_{n=1}^{6} P^n(X_n|e) \tag{3.8}$$

$$\tag{3.9}$$

leaving the likelihood definition eq. (3.7) unchanged. With the L_{QX} method the pion suppression is improved by $15-30$ % compared to the one dimensional L_Q method as illustrated in fig. 3.13.

NN-Method

Although the LQX method is already a great improvement and the default pre-set way in the used AliRoot version it does not use all the information that is recorded by the detector, since only the drift time information and not the amplitude of the signal in each time bin is used. Including this additional information is however not as easy as the step from the LQ to the LQX method, since the signals in each time bin along a track are strongly correlated. The reasons herefore

are the intrinsic detector signal and the response of the front-end electronics used to amplify the signals. A possibility to find an algorithm that uses all the available information is given by neural networks.
Neural networks (NN) are used for a variety of tasks, not only in particle physics, since they provide some properties that are hardly achieved in the binary world of computing. Analogous to natures example neural networks in computing consist of many simple parts so called neurons which each just performs simple operations. In the technical approach these are processors calculating weighted sums and are organised in several layers.
Since the NN method could not be used in this study, further details are refered to [35] and [36].

Comparing the pion suppression rate of the LQ, LQX and the NN method as done in fig. 3.13 shows that the neural network approach further improves the results of the LQX method by a factor of 3-5.

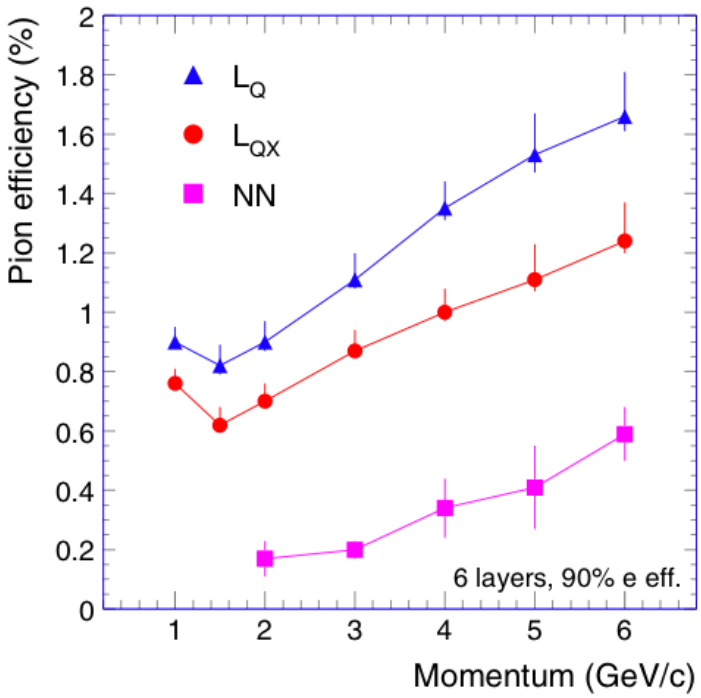


Figure 3.13: Measured pion efficiency as a function of momentum for three different methods: likelihood based on total charge (LQ), bi-dimensional likelihood based on total charge and the position of the maximum time bin amplitude (LQX), and neural network (NN). This figure has been taken from [34].

Combined Particle Identification

To benefit from all the particle identification information from all the sub-detectors a automatic mechanism to combine signals according to different probability densities is used.
The scheme chosen for ALICE is combining PID signals with a Bayesian approach which also allows to complete the above discussed single detector PID.
So far only the properties of a detector, the detector response functions, that do not depend on external conditions have been taken into account. The a priori probability of a particle species

to even be present in the considered event is included in the improved probability $w(i|s)$ to be a particle of type i ($i = e, \mu, \pi, K, p, \dots$) if a signal s is observed in a sub-detector:

$$w(i|s) = \frac{r(s|i)C_i}{\sum_{k=e,\mu,\pi,\dots} r(s|k)C_k}, \tag{3.10}$$

where $r(s|i)$ is the detector response function and C_k the, not with $r(s|i)$ correlated, a priori probability of the considered particle type. The probabilities $w(i|s)$ are often called PID weights. If the whole system consisting of N detectors is considered the combined PID weights W are in the approximation of uncorrelated single detector PID measurements, given as:

$$W(i|s_1, s_2, \dots, s_N) = \frac{C_i \prod_{j=1}^{N} r(s_j|i)}{\sum_{k=e,\mu,\pi,\dots} C_k \prod_{j=1}^{N} r(s_j|k)} \tag{3.11}$$

This definition grants the advantages

- If one or several of the detectors does not identify a particle its contribution cancels out in eq. (3.11), since all $r(s|i)$ are set equally to 0.2 for this detector.
- If several detectors get PID information, their contributions are accumulated with proper weights and therefore improve the combined PID.
- Since the a priori probabilities C_i of particles are not known during reconstruction only the probabilities determined by the single-detector response functions $r(s|i)$ are stored in the event summary data (ESD, Chap.**??**). The final PID decision is then postponed to the physics analysis, enabling further cuts on the quality of the particle identification.

Further, the PID depends on the chosen performed physics analysis. Nevertheless, as shown in [37] varying the true weights by 10% has only an effect of less than 3%.

The combined PID procedure in ALICE is summarised in three steps:

1. The calibration software calculates the single detector response functions $r(s|i)$.
2. The reconstruction software calculates the combined PID response, with the above features and writes the results into a file.
3. Within the analysis software the a priori probabilities C_i are estimated and the PID weights $W(i|s)$ are calculated after event and track selection.

4 Conceptional Design of the Pre-Trigger System

This chapter introduces the basic idea and design of the pre-trigger system.

The lowest level trigger (L0) from the Central Trigger Processor (CTP) of ALICE arrives approximately 1.2 μs after the interaction. The L0 trigger latency is too large to fulfil the timing restrictions for the TRD, as explained in subsect. 3.3.2. The pre-trigger system produces a faster trigger signal and sends it prior to the L0 trigger to the TRD. This is technically realized by generating the trigger signal inside the L3 magnet and mixing the pre-trigger signal with the ALICE trigger signals, as shown in fig. 4.1 and fig. 3.5. The pre-trigger signal is derived from the signals of fast detectors, being:

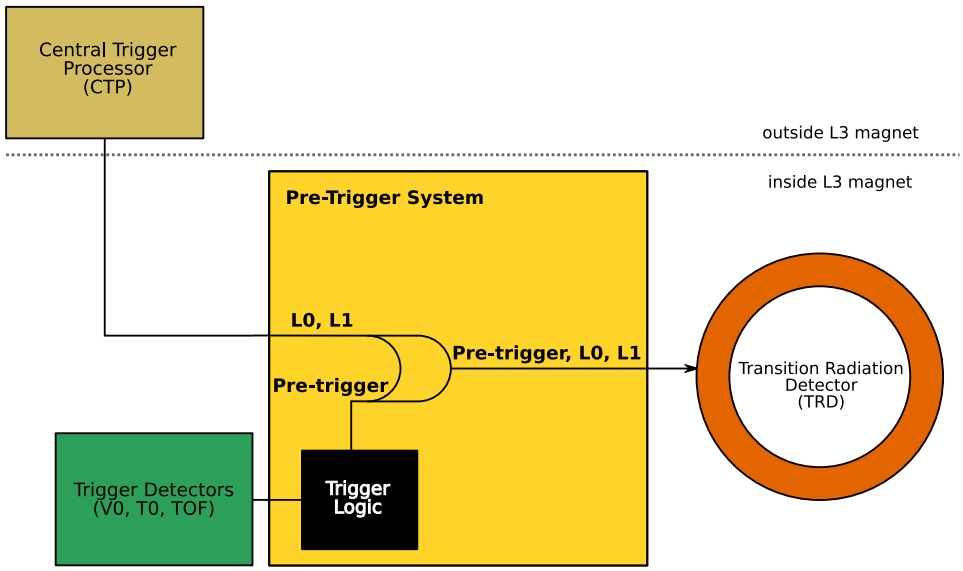


Figure 4.1: Concept of the pre-trigger system. The standard trigger signals from the CTP are merged with the pre-trigger signal derived from fast trigger detectors. The resulting trigger sequence, beginning with the pre-trigger, is then sent to the TRD.

- The T0 detector, consisting of two rings around the beam pipe with twelve Cherenkov radiators equipped with twelve corresponding photomultiplier tubes for each ring. The two rings are located on opposing sides relative to the interaction point.

- The Time of Flight detector, a mulitgap resistive plate detector arranged in 18 supermodules around the TRD supermodules in a cylindrical ring with a radius of 3.70 m.
- The V0 detector, made of two rings of plastic scintillators around the beam pipe on each side of the interaction point, producing signals with 32 photomultiplier tubes on each side.

The pre-trigger system evaluates the signals of the fast detectors mentioned above for each bunch-crossing and generates the pre-trigger signal for TRD with the least possible latency.

4.1 The Generation of the Pre-Trigger Signal

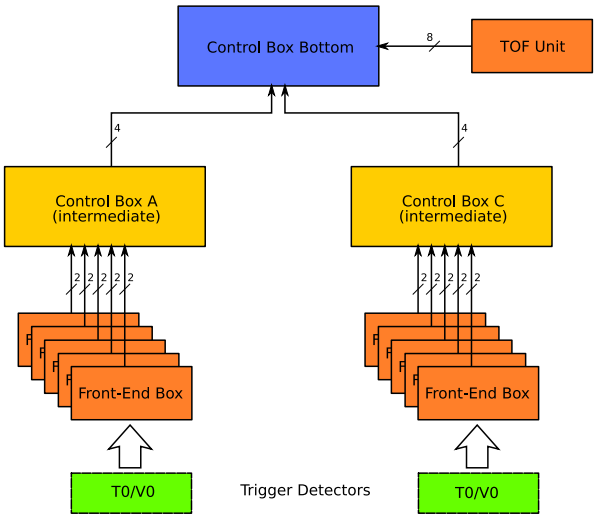


Figure 4.2: The hierarchy of the pre-trigger system. In the lowest level the front-end boxes, followed by the intermediate control boxes, and on top the control box bottom. The numbers represent the number of trigger bits sent for each bunch crossing of the LHC (40.08 MHz).

The major requirement for the pre-trigger signal is the arriving at the TRD front-end electronics not later than 700 ns after the interaction. The implementation of the logic leading to a trigger decision should be very fast and flexible to take several event scenarios into account. A completely flexible trigger decision requires to gather the full information of all trigger detectors (T0, TOF and V0) in one place inside the L3 magnet. Since that is not realistic, it was decided to distribute the system inside the magnet and pre-process the individual detector signals at satellite stations, as shown in fig. 4.2. The implementation of three stages of lookup tables, illustrated in fig. 4.3, keeps the flexibility while fulfiling the speed and distribution requirement.

The three levels of lookup tables are reflected by the hardware hierarchy (shown in fig. 4.2) and each component of the pre-trigger system listed below hosts one lookup table.

- The front-end boxes are at the lowest level of the pre-trigger system, the interface to the trigger detectors. Those front-end boxes collect the signals from up to twelve detector units and send a two bit large trigger element to the next level, the intermediate control boxes.

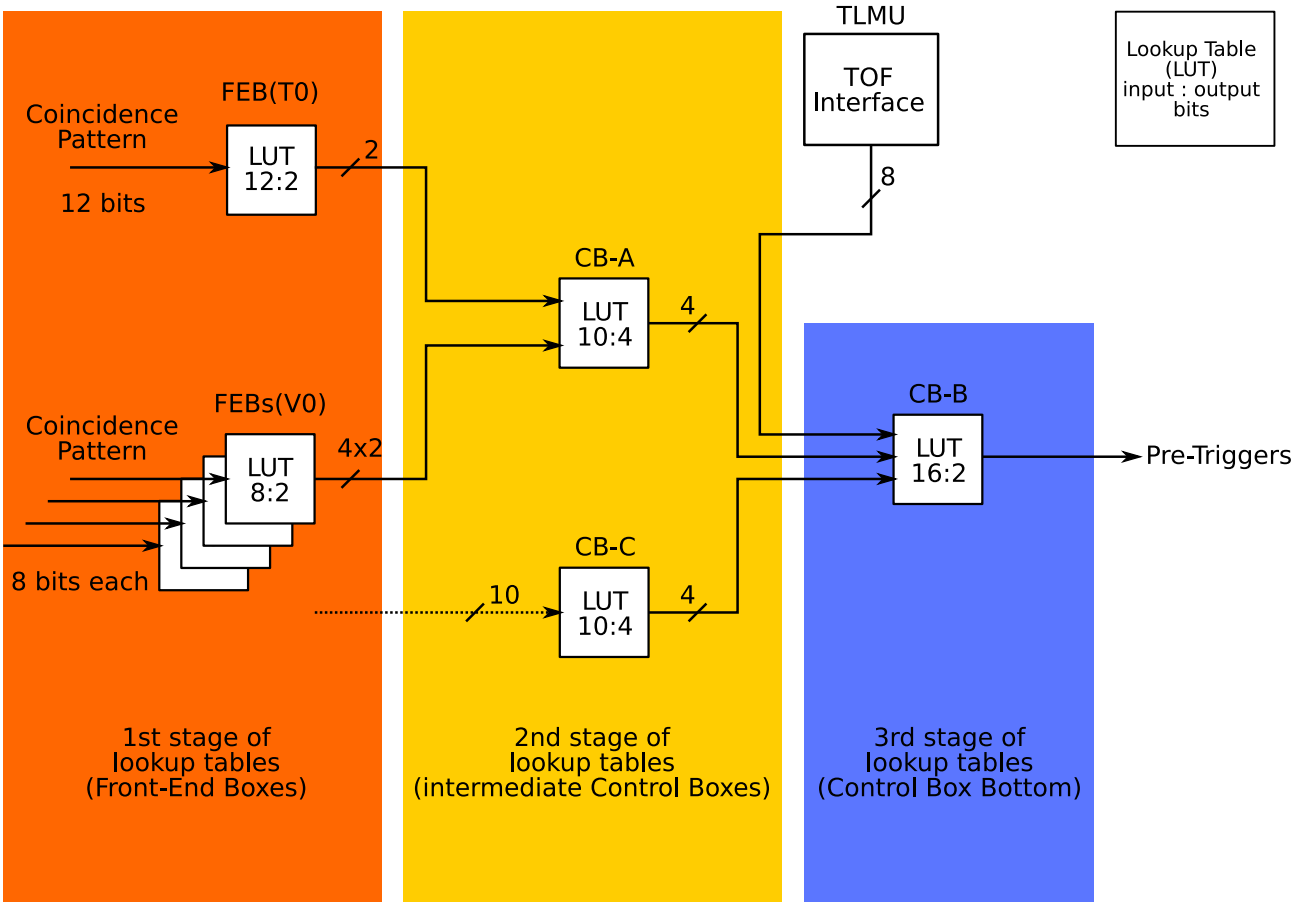


Figure 4.3: The three stages of lookup tables implement a configurable trigger logic in the pre-trigger system.

- Two intermediate control boxes, each combining the information of five front-end boxes, produce themselve a four bit large trigger element and send this to the third level, the control box bottom. Furthermore, they control of the front-end boxes.

- The control box bottom is at the highest level in the trigger logic, collecting the trigger information from the intermediate control boxes and the Time of Flight detector interface. Upon this information the trigger logic in the control box bottom decides, whether or not it generates the pre-trigger signal. In addition, it ensures the correct timing of the pre-trigger signal and the subsequent trigger signals from the Central Trigger Processor (CTP) (L0 and L1).

Each of these components is explained in detail in the following chapter.

At the first stage of the lookup tables, close to the trigger detectors, twelve photomultiplier tubes produce twelve analog signals, which are digitized by discriminators at every LHC clock cycle. Those twelve bits are fed to a fully programmable lookup table, whose output has two bits and is defined by the user for every possible input pattern. The two bits allow two different trigger logics. The output of several such lookup tables are pre-processed at the second stage

lookup table. The 4-bit outputs of two second stage lookup tables, together with maximum eight bits from the TOF Unit, are fed to the final lookup table at the third stage. Based upon the output of this table, the pre-trigger system decides, whether it generates a pre-trigger or not. The contents of the lookup tables are defined according to the physics motivation of the current data taking run of ALICE.

The mapping of the individual bits of the input pattern for each lookup table is documented in appendix B.

5 Hardware for the Pre-Trigger System

This chapter describes the pre-trigger system hardware, the functionality and location of its components and their relations in detail. Also, the logics implemented in each component are explained. Most of the logic circuits are written in the programming language VHDL (Very High Speed Integrated Circuit Hardware Description Language) [43] and implemented in Field-Programmable Gate Arrays (FPGA). Finally, the powering scheme of the pre-trigger components is described.

5.1 Overview of the Hardware

As described in the previous chapter, the pre-trigger system consists of several components inside and outside the L3 magnet. This section introduces the various components and their relations to other components of the system. The system can be split into a lower and a upper hierarchy for simpler explanation. Figure 5.1 shows the lower part of the hierarchy close to the detectors, while fig. 5.2 shows the upper part of the hierarchy, connecting to the Central Trigger Processor (CTP), the Global Tracking Unit (GTU) and to the TRD.

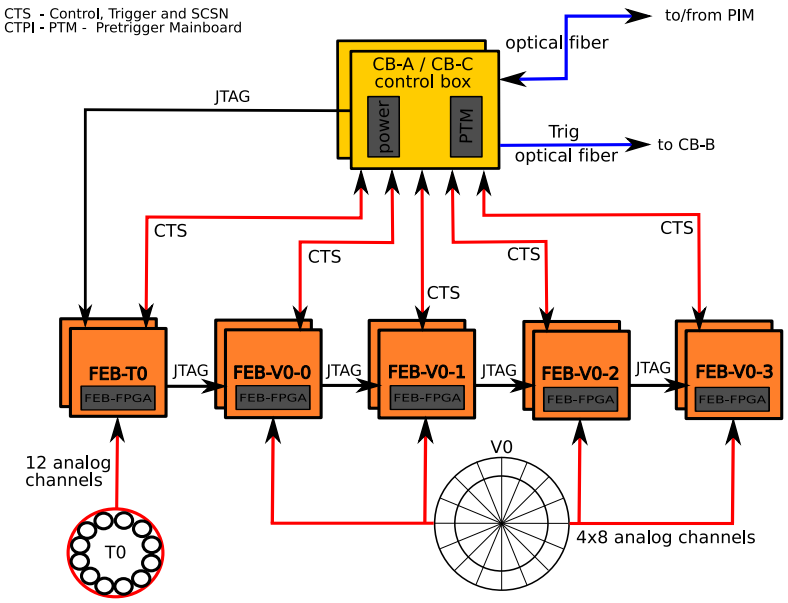


Figure 5.1: The connections between the intermediate control box, either A- or C-side, the PIM, the CTP, the front-end boxes and the detectors.

The lower hierarchy of the pre-trigger system consists of the following components:

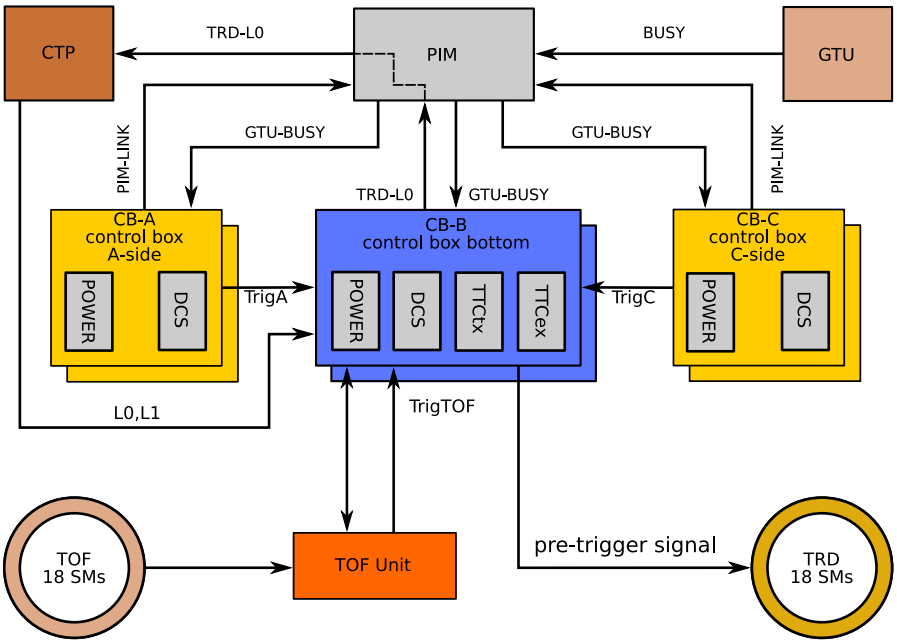


Figure 5.2: The control box bottom and its peripherals. Connections to the intermediate control boxes and the TOF Unit transmit trigger elements, which are combined to the pre-trigger signal, which is forwarded to the TRD. The pre-trigger interface module forwards a busy signal from the GTU to the control box bottom and transmits trigger related information to the CTP.

- 10 front-end boxes (FEB), five on each side of the interaction point, placed in the vicinity of the T0 and V0 detectors to receive those detector signals and produce trigger elements.
- 2 control boxes (CB–A and CB–C) control the front-end boxes. The configuration and the collection of trigger elements of the front-end boxes are peformed by these control boxes. Both control boxes send trigger elements to the third control box (CB–B). Thus, they are referred to as the intermediate control boxes.

Figure 5.1 shows the connection scheme of the intermediate control boxes and their connections to other components of the pre-trigger system.

One front-end box collects and digitizes up to twelve analog signals provided by the trigger detectors. The T0 detector provides twelve analog signals, this means one front-end box is used. The V0 detector has four sectors each equipped with eight photomultiplier tubes, therefore four front-end boxes are in use for this detector.

Five front-end boxes are connected to each intermediate control box. The category 6 high quality individually shielded twisted pair cables (CAT6, often used in ethernet systems [45]) is used for the communication between the control boxes and front-end boxes. Optical fibers connect to the PIM and to the control box bottom (CB–B).

- 1 TOF Unit receiving signals from the Time of Flight (TOF) detector and producing trigger elements.
- 1 control box (CB–B), controlling the TOF Unit. The configuration and the collection of trigger elements of the TOF Unit are performed by the control box bottom. It also collects

trigger elements from the other two control boxes (CB–A, CB–C) and performs a final trigger decision and sends it to the CTP and the TRD. Thus the two other control boxes are called intermediate control boxes and CB–B is called master control box.

- 1 pre-trigger interface module (PIM) located in the racks below the muon arm in C-side outside the L3 magnet. This is the interface of the pre-trigger system to the GTU and the CTP.

The control box bottom (CB–B) is at the top of the pre-trigger system hierarchy. The interconnection of the control box bottom to the intermediate control boxes, to the CTP and to the GTU through the pre-trigger interface module and to the TRD is illustrated in fig. 5.2. The trigger elements from the intermediate control boxes and from the TOF Unit are collected at the CB–B. These inputs are used to derive the pre-trigger signal, which is then transmitted to the TRD. This signal is also sent to the CTP as Level-0 (L0) contribution from the TRD. The CTP provides the ALICE global triggers, consisting of different trigger levels (Level-0, Level-1 and Level-2) to all ALICE detectors as well as to the control boxes. The GTU of the TRD sends a busy signal to the CB–B, in case the TRD is not ready for receiving triggers, thus preventing the generation of further pre-trigger signals. The CTP and the GTU are both located outside the L3 magnet. The pre-trigger interface module (PIM) translates the signals from the pre-trigger system for the GTU and the CTP and vice versa.
All installed hardware components of the pre-trigger system are built redundantly (primary and backup system), except for the TOF Unit.

5.1.1 Physical Location of the Pre-Trigger Boxes

The location of each component of the pre-trigger system is sketched in fig. 5.3. The labels of most components contain the suffix *A* or *C* to indicate, whether they are installed on A- or C-side of the L3 magnet. For example, CB–A and CB–C sit on A-side and on C-side respectively, and the CB–B is located approximately 2 m below the beam pipe close to the magnet door at C-side and is hanging at the bottom of the backframe.

The following sections give precise descriptions of the individual components in ascending order following the pre-trigger hierarchy, starting with the front-end boxes followed by the TOF Unit and the control boxes.

5.2 Front-End Boxes

The front-end boxes (FEB) are the interface between the trigger detectors and the pre-trigger system. Ten front-end boxes are installed in the ALICE cavern close to the T0 and V0 detectors inside the L3 magnet. Their design is identical except for the number of input channels used. One front-end box is shown in fig. 5.4 and the block diagram of such a front-end box is shown in fig. 5.5.

A front-end box is built of custom designed preamplifier cards and two printed circuit boards, which are used for the primary and the backup system. The maximum number of installable preamplifier cards is twelve. The main components of each printed circuit board are a differential

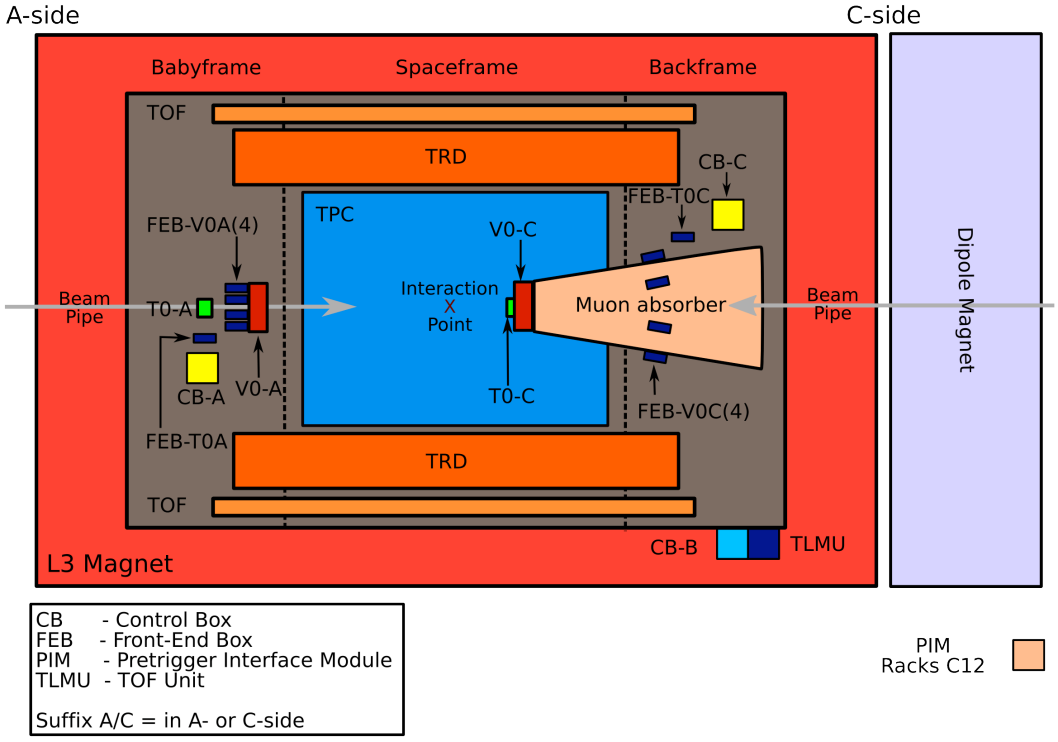


Figure 5.3: Location of the pre-trigger components in- and outside of the L3 magnet.

signal receiver, a discriminator and a FPGA, as shown in fig. 5.5.

The analog signals from the detector are fed to a preamplifier card. This card gives three outputs:

- A buffered output without amplification. This output signal is transmitted to the front-end electronics of the T0 and V0 detectors located outside the L3 magnet.
- One amplified output with an amplification factor of 10. This output is also used in the V0 and T0 front-end electronics.
- One differential signal output with an amplification factor of 5 for each polarity, dedicated for the use in the pre-trigger system.

The differential signal from the amplifier is converted to a single ended signal on the front-end box mainboard and converted to a digital signal by a leading edge discriminator. The discriminated signal is fed into the FPGA.

Inside the FPGA the signal is fed to the Synchronizer & Alignment module. It samples incoming signals with an internally generated 160 MHz clock and compensates the delays between the individual channels. The coincidence pattern of these twelve signals is fed to the lookup table (LUT). The 2-bit output of this table is further processed by the Serializer module multiplexing it into a one bit serial output line, which is then forwarded to the intermediate control box.

All aspects of the processing of those signals are defined by setting parameters in the registers of the FPGA, such as the discriminator threshold, a programmable delay setup for the alignment, the contents of the lookup table and many more. Writable registers are also readable for validation.

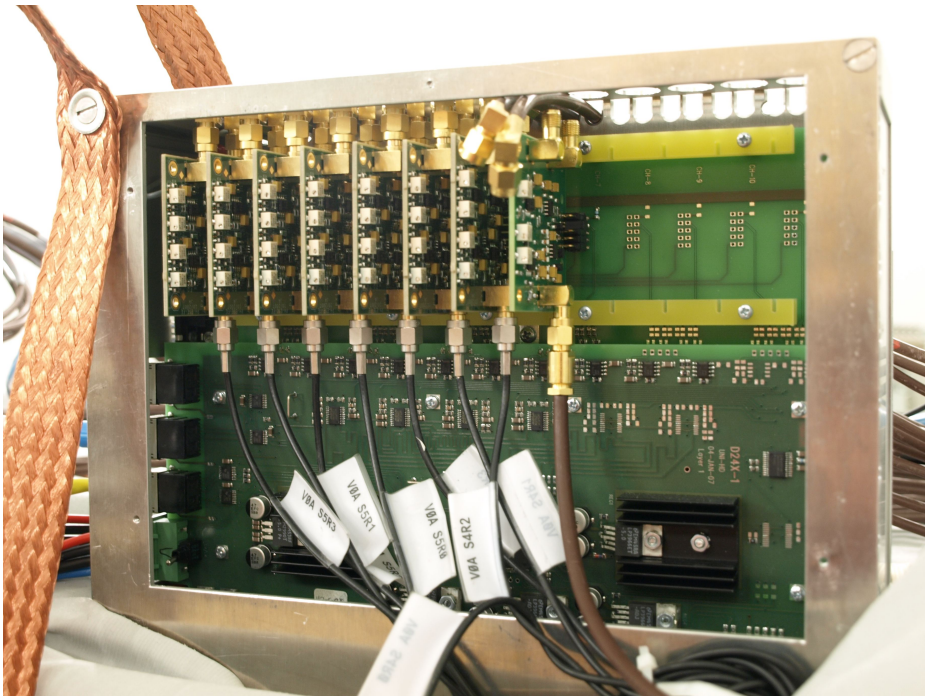


Figure 5.4: A front-end box, equipped with eight preamplifier cards for the V0 detector.

Besides the configuration registers, there are counters implemented in the internal RAM of the FPGA. They count the occurrence of various signals, such as the clock signal and signals seen in individual channels. To obtain these values, it is necessary to stop the counting, reading the values from the memory and writing them to registers. Setting certain configuration registers triggers this readout process. A complete list of the currently defined registers is given in [54].

The registers are configured and controlled by the control box. An eight-pin CAT6 cable is used to carry the control signals (SCSN-IN/OUT and Select), the LHC clock signal and the trigger output to the control box. Since the logic standard used for all these signals is LVDS, a maximum of four signals is transmitted with one CAT6 cable.

The LHC clock signal is used to generate the internal 160 MHz clock. The Select line from the control box to the front-end box is used to define whether the FPGA is in configuration mode or in triggering mode. In the configuration mode, the SCSN-OUT/Trigger line is used for SCSN-OUT and the control box communicates with front-end box to read and write registers in the front-end box. However if the FPGA is set to triggering mode, the communication via SCSN is not possible and front-end box sends the trigger elements to control box. The latter mode is used during data taking.

Additional CAT6 cables (labelled JTAG) from the control box to one of the front-end boxes and between those are used for uploading the FPGA design. Using JTAG for device programming means using the devices' JTAG boundary scan capabilities [44]. Multiple JTAG devices (the five FEB FPGAs) are daisy-chained and programmed from a single JTAG controller on the DCS board.

The front-end box has dimensions of 26.5 cm width, 20.5 cm height and 7.5 cm depth.

The V0 detector has 32 channels on A and 32 channels on C-side. Therefore, four front-end

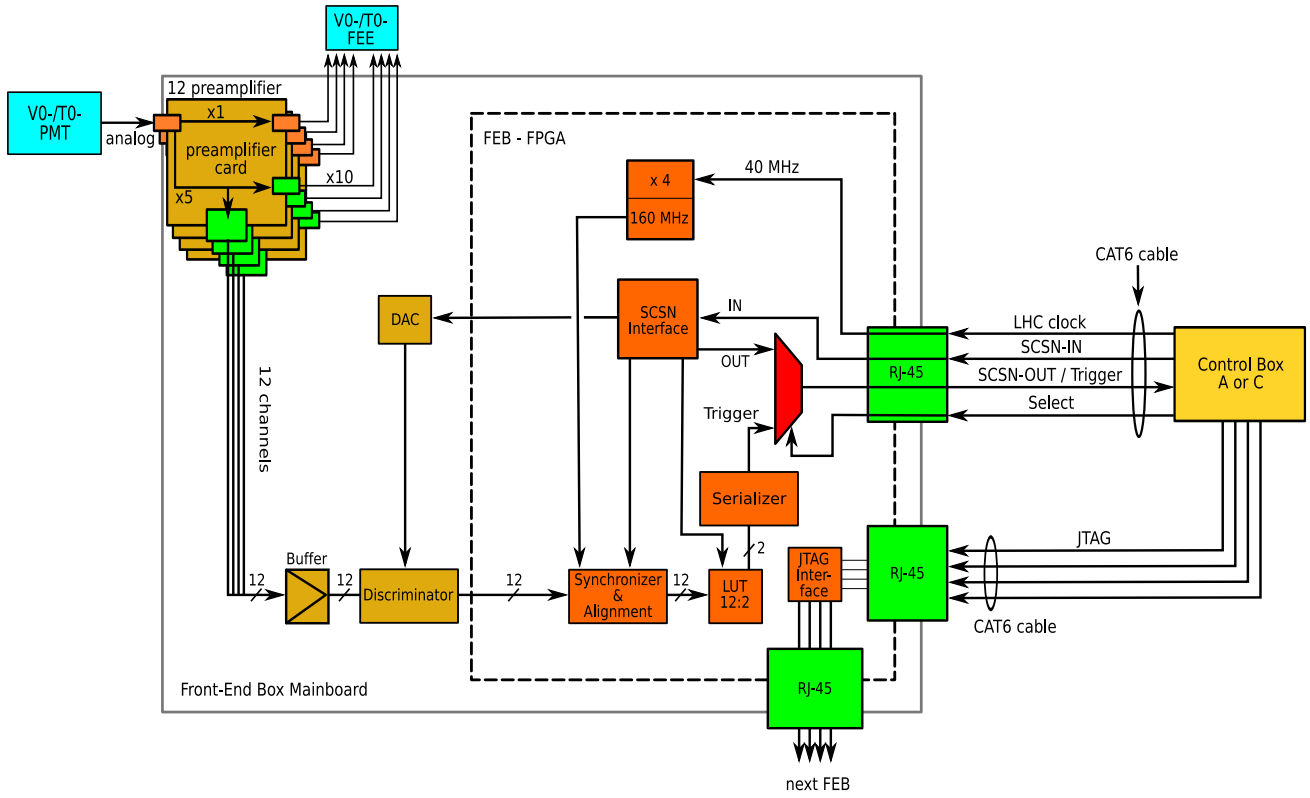


Figure 5.5: Block diagram of a front-end box.

boxes on each side equipped with eight preamplifier cards are installed. The T0 detector provides twelve channels on each side, this means one front-end box for the T0 detector for each side is installed.

More detailed information about the FPGA design is given in [54].

5.3 Time of Flight Unit

The official name of this box is TOF Logic Multiplicity Unit (TLMU), however in this thesis it is called TOF Unit for simplicity. The TOF Unit is the interface between the the TOF detector and pre-trigger system and is directly attached to the control box bottom inside the L3 magnet. The TOF detector with 18 supermodules and 32 bits per supermodule provides 576 bits per bunch crossing. A FPGA that can process such a big number of input channels is rare, thus it was decided to use the Virtex4 FPGA [47] with over 600 input pins.

The functionality of the TOF Unit is shown in fig. 5.6. The 576 bits arrive as differential signals and are converted to LVTTL [46] signals before they are processed in the FPGA.

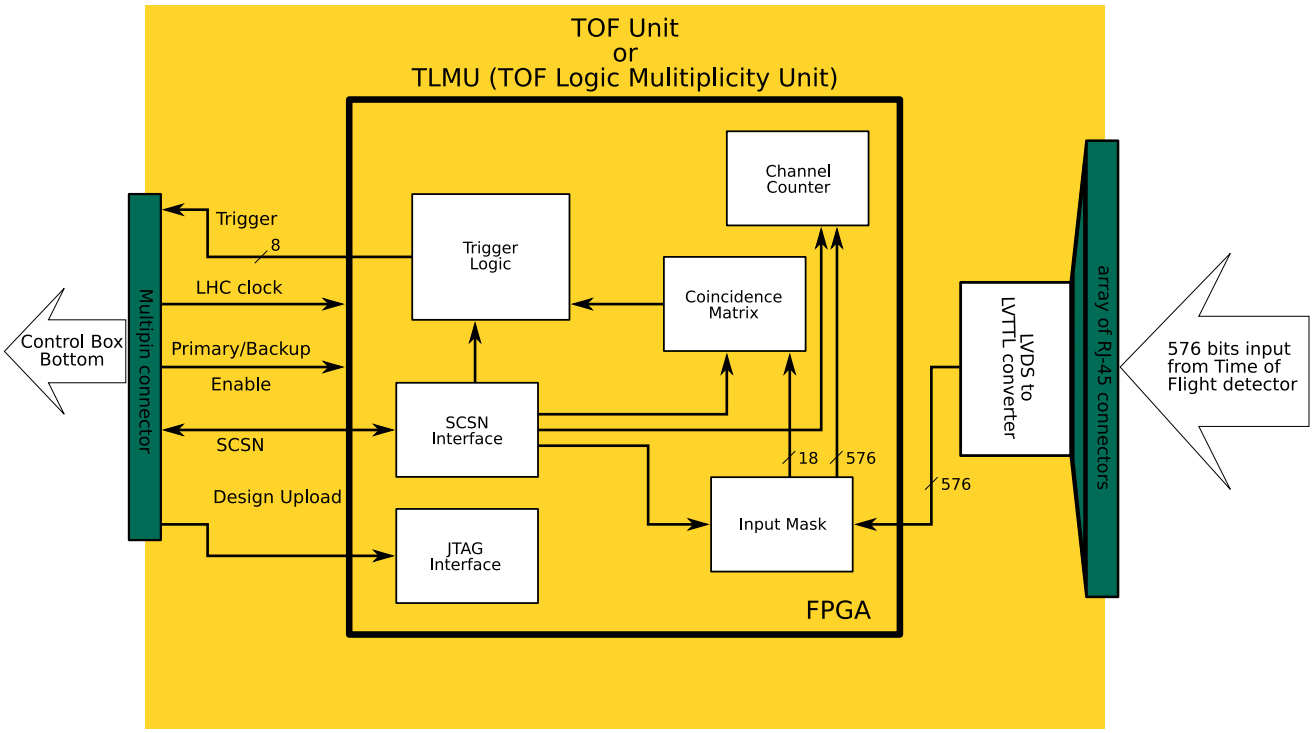


Figure 5.6: Block diagram of the TOF Unit. Its logical function in the pre-trigger tree is similar to the front-end boxes' but differs from the hardware used to process the incoming 576 bits.

The 576 input bits are fed to an Input Mask module which masks out input bits. The typical reason of masking is because the input bit is noisy or not properly working. For each input bit is an independent counter with 48-bit depth implemented. These Channel Counters are incremented every clock cycle, when the corresponding input bit is one. The Input Mask module also provides the logical "ORs" of the 32 bits of one supermodule, in total 18 bits.

This 18-bit pattern is compared to a Coincidence Matrix, an 18 times 18 dimensional symmetric matrix implemented in the memory of the FPGA, which specifies the desired coincidences of hits in different supermodule. This matrix is illustrated in fig. 5.7. Each matrix element represents the coincidence of two signals of two supermodules. Not all matrix elements are needed and the number of memory addresses used is reduced to 153. The diagonal of the coincidence matrix represents the coincidence of a supermodule with itself. In the example matrix given in fig. 5.7 the TOF Unit only sends a positive trigger decision to the control box bottom, if supermodule six is hit at the same time as one of the supermodules 14, 15 or 16.

The logic and modules shown here are the minimum implementation of a trigger logic. In future, there will be more modules, such as a multiplicity counter and even more Coincidence Matrices of different type which are used simultaneously. The Trigger Logic module will be then

more complex, taking more inputs of such kind into account.

The TOF Unit is controlled by the control box bottom. All communication lines are combined in one cable with 50-pin SCSI-2 compatible connectors at the ends. This includes four lines for JTAG connection, two lines for the serial connection (Slow Control Serial Network (SCSN)), eight trigger lines, two spare lines going in, two spare lines going out and a clock line, transmitting the LHC clock signal. The upload of the design, distribution of the LHC clock signal and the setting of registers in the FPGA is done in the same way as in the front-end boxes. There are eight lines for trigger transmission to the CB–B. This limits the number of triggers to the CB–B to eight.

Unlike all other components of the pre-trigger system, the TOF Unit has no backup system. The TOF Unit is connected to the primary and to the backup system of the control box bottom and in case one of these fails, the TOF Unit switches to the other system. The enable line added in the connection between TOF Unit and the control box bottom indicates, which system is currently working. Detailed schematics of the TOF Unit can be found in [55].

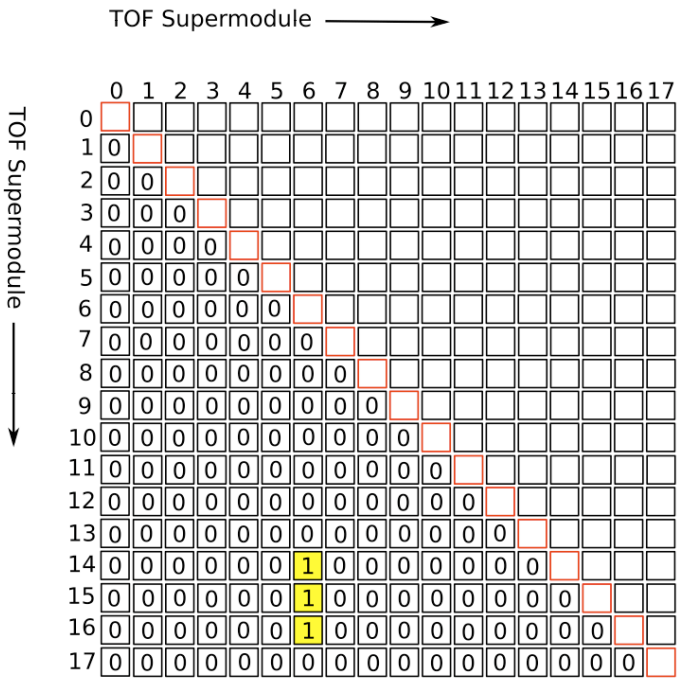


Figure 5.7: Example configuration of the coincidence matrix. The number filled entries are mapped to a memory address, either containing an "0" or an "1" for enabling the trigger condition.

5.4 Control Boxes

The control boxes serve for controlling, generating a pre-trigger signal and monitoring the pre-trigger system. In total three of them are installed inside the L3 magnet. They are called CB–A, CB–B and CB–C, depending on their function and location.

The intermediate control boxes CB–A and CB–C monitor and control the connected front-end boxes and collect trigger signals from them. The CB–B combines the trigger signals from TOF

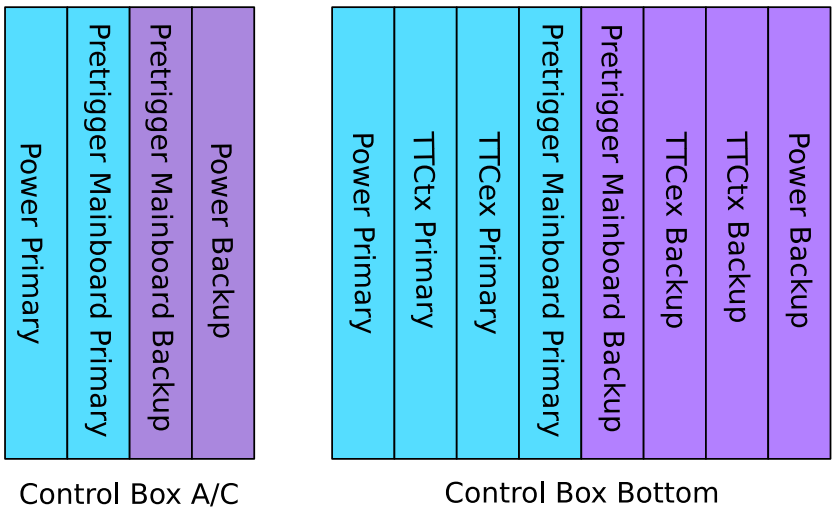


Figure 5.8: A schematic view of the hardware modules in the control boxes.

Unit, CB−A and CB−C, performs the final trigger decision and produces the pre-trigger signal. The connections between CB−A, CB−C, CB−B and other components of the pre-trigger system is shown in fig. 5.1 and fig. 5.2.

Figure 5.8 shows the layout of CB−A/C (left) and the CB−B (right). Every control box has four modules, two pre-trigger mainboards and two power modules, and the CB−B has in addtion four more modules (Timing, Trigger and Control (TTC)), which are explained later in subsect. 5.4.2. The power module has voltage regulators and stabilizers. It is connected to a power supply unit sitting outside the L3 magnet, which actually provides the power for the pre-trigger system. The power domains for the primary and backup system in each box are separated, this means there are dedicated power modules for each primary and backup system. Figure 5.9 shows a pre-trigger mainboard for an intermediate control box. It is a modular design with individual printed circuit boards (PCBs) for the various functionalities and interfaces of the mainboard.

The FPGA Sub-Board is mounted on top of the PCB stack visible in the center of fig. 5.9. Its Xilinx Spartan3 FPGA implements the full logic for the processing of signals rom all pre-trigger sub-components and the generation of triggers for the TRD front-end electronics. It is connected through a double-row of pins to the DCS board and the base board, which are both visible behind the FPGA sub-board.

The Adapter Card is seen on top of the picture, directly attached to the FPGA sub-board. In the given picture, six RJ-45 connectors are mounted on the adapter card, corresponding to the five front-end boxes plus the JTAG connection to one of the front-end boxes. The adapter card is different for the pre-trigger mainboards in the control box bottom and the intermediate control boxes. They are shown in fig. 5.10. This is the only difference in the hardware of the pre-trigger mainboard between the intermediate control boxes and the control box bottom.

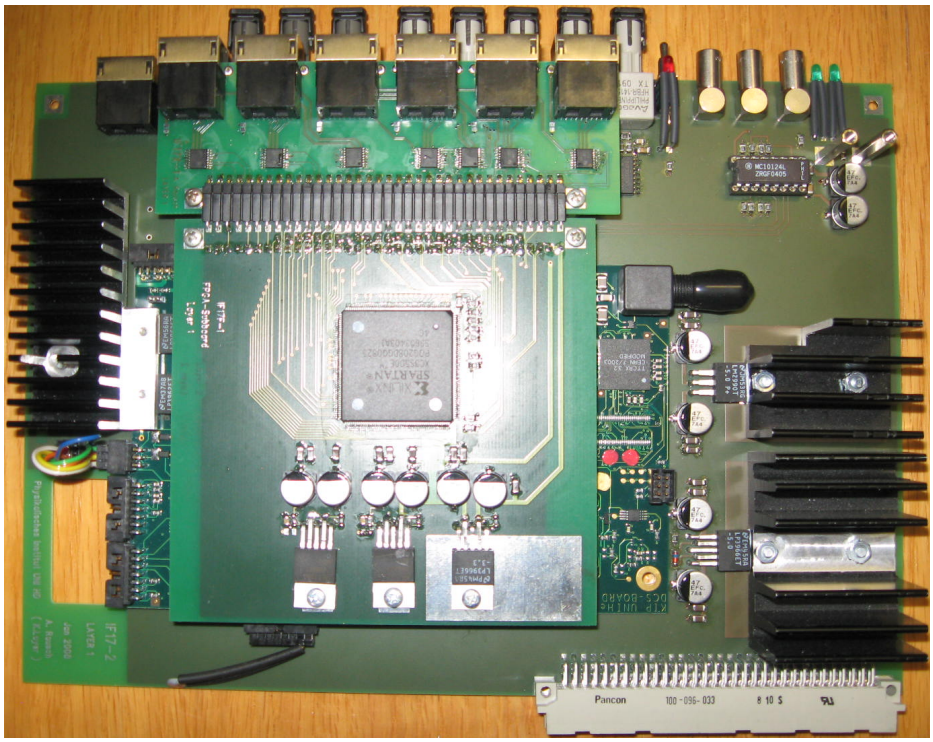


Figure 5.9: The pre-trigger mainboard. It has dimensions of approximately 23 cm × 18 cm. The FPGA sub-board is seen in the center. The adapter card with six RJ-45 connectors is directly attached to the FPGA sub-board. Eight optical connectors are visible behind the adapter card on top of the picture. The black covered optical receiver of the DCS board is visible on the right.

The DCS Board is between the FPGA sub-board and the base board. It contains an FPGA with an embedded ARM processor running a Linux operating system. The use of Linux allows easy access and control of all connected pre-trigger components, such as the FPGAs and the configuration chains. The software to control the pre-trigger system runs on the Linux system and is accessible through ethernet. The corresponding connector is in the top left corner, mounted on the base board. The DCS board has an optical receiver through which it receives the LHC clock signal and the trigger signals from the CTP.

The Base Board supports all other components and provides services such as power and I/O devices. It has several optical in- and outputs along with three Lemo connectors and a RJ-45 connector for network connection. All connections are forwarded to a double-row of metal pins, which are shared by the DCS board and the FPGA sub-board.

The pre-trigger mainboards and their connectors are used differently by the intermediate control boxes and the control box bottom. Their detailed description is given separately in the next two subsections.

5.4.1 Control Boxes in A- and C-side

The control box A and C (CB–A, CB–C) collect trigger elements from five front-end boxes and produce trigger elements and send them to the control box bottom (CB–B). The block diagram

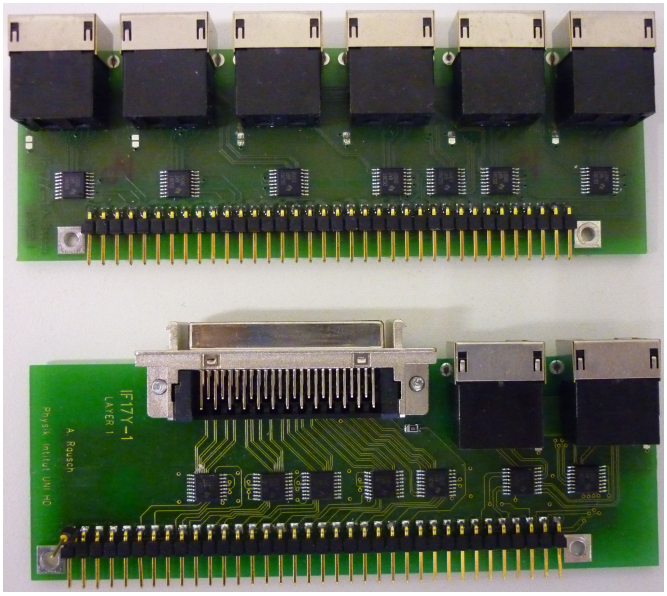


Figure 5.10: Adapter cards. They are directly connected to the FPGA sub-board. The upper card connects the front-end boxes to CB–A and CB–C. The card on the lower part of the picture connects the TOF Unit and the CB–B.

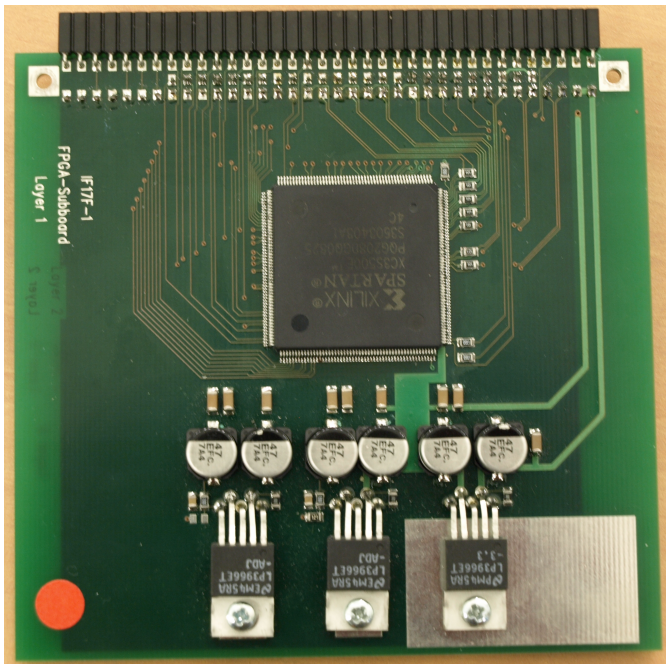


Figure 5.11: FPGA sub-board. The FPGA mounted on the board contains logic to process the arriving signals through which the trigger decision is made. The dimensions of the board are about 10 cm x 10 cm. The I/O pins of the FPGA are connected to two rows of pins on the upper end of the board. The lower row is the connection to the pre-trigger mainboard on which the sub-board is mounted. The upper row of pins connects to the corresponding adapter card.

of the pre-trigger mainboard for CB–A and C is shown in fig. 5.12.

The equipped DCS board has a Linux operating system, which is accessible via ethernet. The DCS board receives the LHC clock signal and the trigger levels from the CTP through the optical receiver module *TTCrx*, which decodes the incoming optical signals. After conversion, these signals are forwarded directly to the FPGA sub-board containing the trigger logic. The software to read and write the registers of the control box FPGA via the SCSN runs on the Linux system.

The FPGA design for the FPGA mounted on the pre-trigger mainboard and for the connected FEB-FPGAs is uploaded via two JTAG lines, which are prepared for these. The JTAG line to the front-end box is routed to the RJ-45 connector *FEB-JTAG* on the adapter card. On the adapter card are in addition five RJ-45 connectors for the individual connections to the five front-end boxes. This adapter card is shown on top of fig. 5.10.

There are five optical transmitters. Three of them are connected to the PIM. Another one transmits the trigger element to the CB–B and the remaining transmitter is spare. In addition, three optical receivers are installed. The CB–A and CB–C use only one of these for receiving the busy signal from the GTU [60]. It indicates that the TRD is not ready for receiving triggers while processing data.

Figure 5.12 shows the simplified block diagram of the control box and the FPGA. The control boxes in A- or C-side collect 2 bits per bunch crossing from each connected front-end box. The total

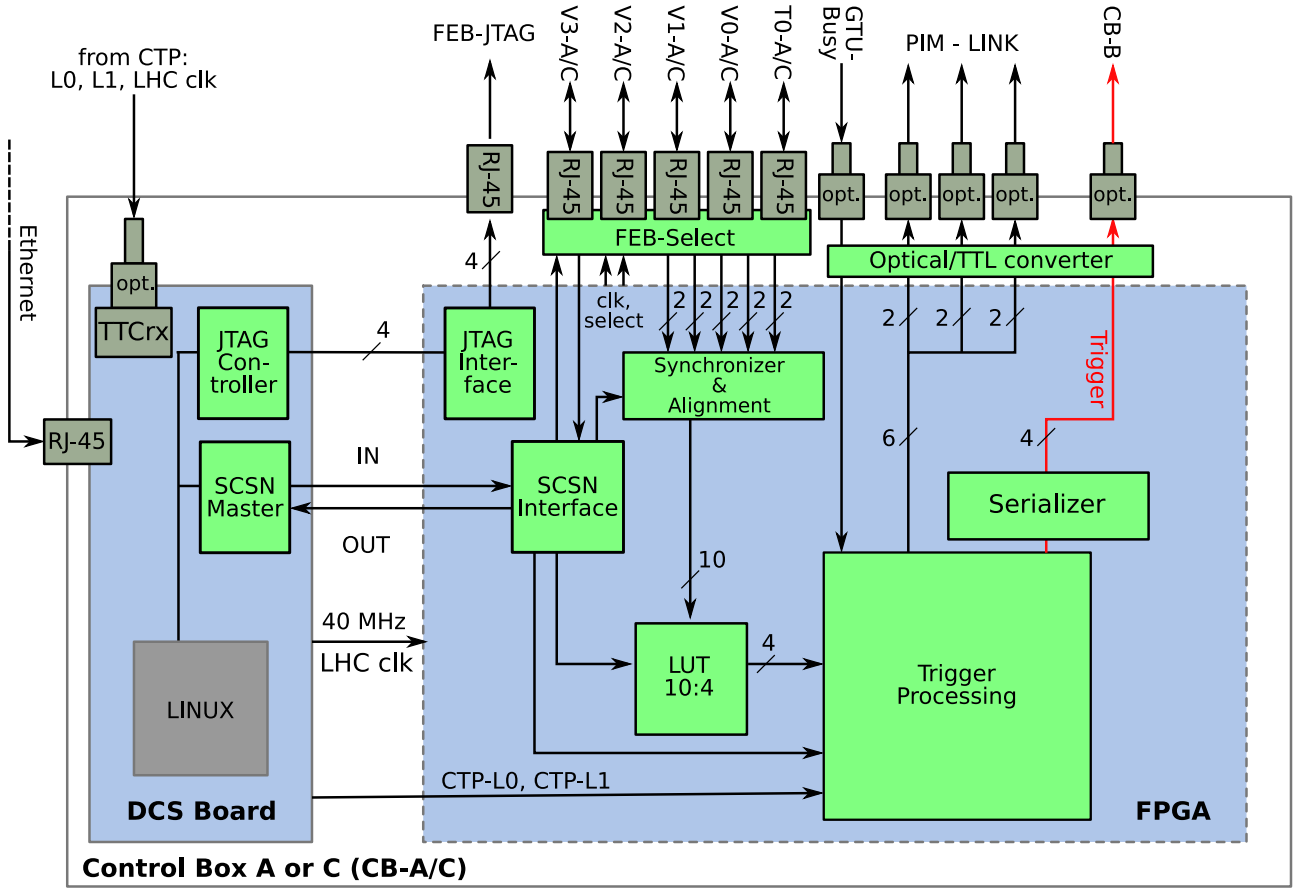


Figure 5.12: Block diagram of the pre-trigger mainboard for CB–A and CB–C. It has a DCS board, a FPGA and interfaces for the PIM, the CB–B, the GTU and the front-end boxes.

number of trigger elements to process is 10 bits for each control box. These 10 bits are synchronized and aligned in the Synchronizer & Alignment module in the same way as the detector signals in the front-end boxes. They are afterwards evaluated by the lookup table (LUT) and the 4-bit result is sent to the Trigger Processing module. At the moment, the Trigger Processing forwards these 4 bits to the CB–B via the optical transmitter labelled *CB-B*. In future, the Trigger Processing module will be more complex. It will send six bits to the CTP and will take for the trigger decision also other inputs into account, such as the GTU-Busy and the global triggers from the CTP. Those features are not implemented so far.

5.4.2 Control Box Bottom

The CB–B is the at top of the pre-trigger hardware hierarchy. It derives the pre-trigger signal from the input of CB–A, CB–C and the TOF Unit.

The block diagram for the pre-trigger mainboard of the control box bottom (CB–B) is shown in fig. 5.13. The reception of the LHC clock and the global trigger levels, the upload of the FPGA design to the FPGAs of the pre-trigger mainboard and the TOF Unit and the access to

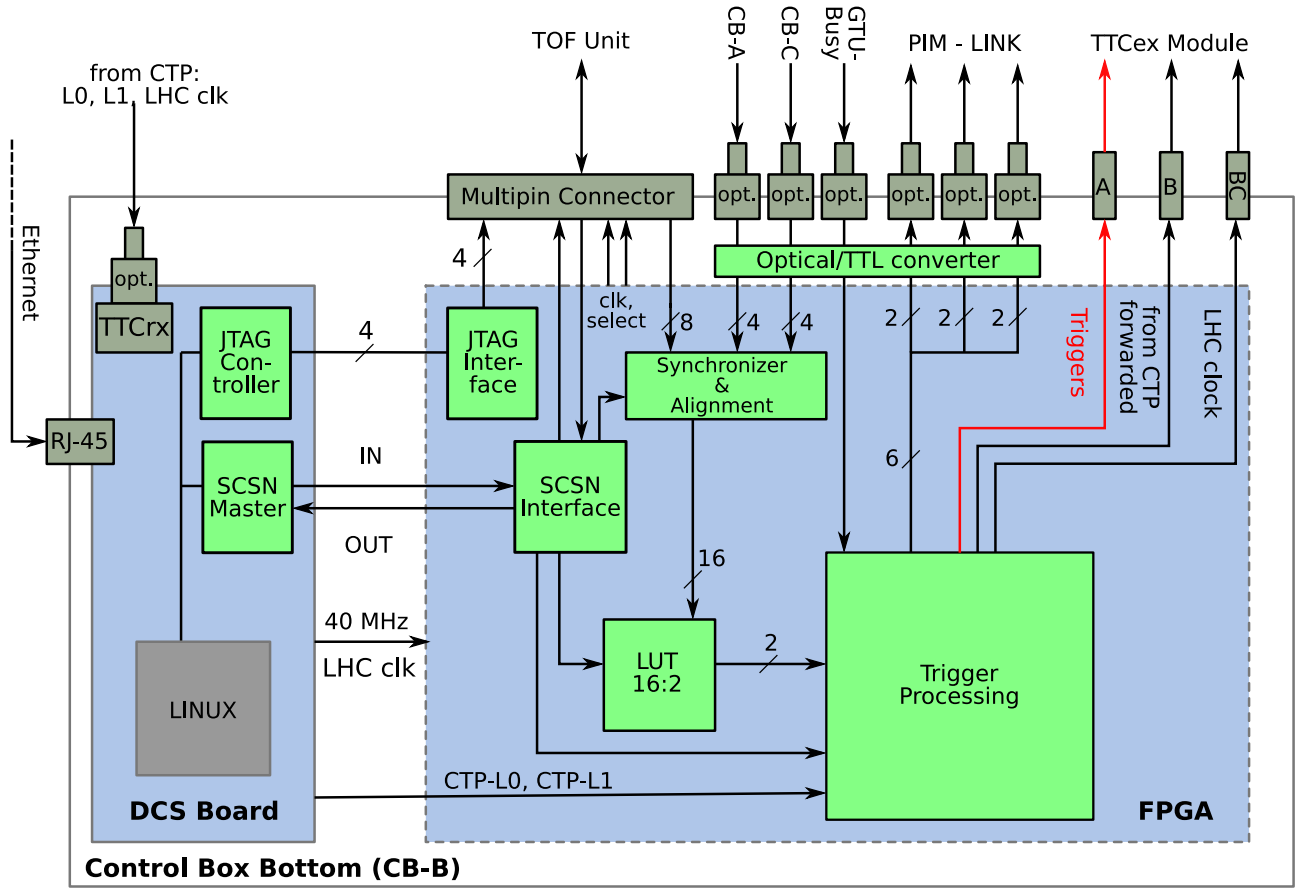


Figure 5.13: Block diagram pre-trigger mainboard of the control box bottom (CB–B). It has a DCS board, FPGA sub-board and special interfaces for the TOF Unit, CB–A, CB–C and TTC modules (channel A, B and BC).

the registers of both FPGAs is done in the same way as in the other control boxes.

The connection to the TOF Unit is made with a 50-pin SCSI-2 compatible cable, shown in the bottom of fig. 5.10 and was already mentioned in sect. 5.3.

The CB–B collects trigger elements, 16 bits per bunch crossing, through two optical inputs (*CB-A* and *CB-C*) and through the SCSI-2 compatible connector from the TOF Unit. These inputs are synchronized and aligned in the same way as in the other control boxes and are then fed to the top level lookup table (LUT). The 4-bit output of the lookup table is fed to trigger logic, along with the ALICE trigger signals (L0 and L1) and the GTU-Busy signal.
The trigger logic decides upon these inputs whether a pre-trigger signal is produced or not. For example, a high GTU-Busy signal indicates that the TRD is currently processing data and is not ready to receive any triggers. Thus, the trigger logic prevents further trigger signals to the TRD [54]. In total six bits of trigger information are sent to the pre-trigger interface module via three optical outputs. From there, these bits are forwarded to the CTP.
To distribute the pre-trigger, the subsequent ALICE triggers and the LHC clock signal to the supermodules of the TRD, the CB–B uses two Lemo connectors to send these signals to the

Timing, Trigger and Control (TTC) modules. The third Lemo connector is used to forward the B-channel of the CTP. As shown in fig. 5.8, these four additional (in comparison to the other control boxes) TTC modules are sub-components of the TTC system, which is used LHC wide [49]. The modules used in the CB−B are the TTCex and the TTCtx modules.
In the TTC system architecture, it is possible to transmit three signals over one optical fiber. These signals are encoded in one serial data stream and sent to a receiver, such as a detector.

The A channel transmits trigger signals.

The B channel transmits serial data commands. This channel is not used by the pre-trigger system at the moment.

The BC channel transmits the LHC clock signal. The frequency is 40.08 MHz.

Since the TTCex has only 10 optical outputs, an additional TTCtx is used for the 18 supermodules of TRD. This module fans out the given input from TTCex.

5.5 Pretrigger Interface Module

The ALICE CTP accepts LVDS signals as trigger contribution inputs from the trigger detectors. However, since the CTP is located outside the L3 magnet and CB−B is located inside the magnet, a direct connection between CB−B and the CTP by LVDS may cause difficulties, such as ground loops and noise, which arise from different grounding points far away from each other. Therefore, it was decided to use only optical signal transmission between the outside and the inside of the magnet, and the Pretrigger Interface Module (PIM) was prepared to convert signal types between optical and LVDS.

The PIM is located in the rack C12 below the muon arm of the ALICE detector. Figure 5.14 shows the PIM, which consist of three sub-modules:

1 **PIM-FPGA module** is connected to the CTP and to the GTU, receives a busy signal from the GTU and sends trigger information to CTP.

2 **PIM-Optical modules** are split into one for the primary and one for the backup system. They receive and send optical signals from and to the control boxes.

The PIM enables the communication between the control boxes on one side and the CTP and the GTU on the other side.Each of the two pre-trigger mainboards of a control box connects with 4 optical fibers to either the primary or backup PIM optical. Three fibers transmit in total 6 bits trigger information from the control boxes to the PIM and one transmits the GTU-busy signal to the control boxes. The GTU-busy signal is used only in the CB−B.

5.6 Low Voltage Power Distribution

The pre-trigger components are powered by several PL512 power supplies manufactered by the Wiener company [56]. The power supplies have up to four floating channels capable to deliver a maximum of 20 A at 15 V.

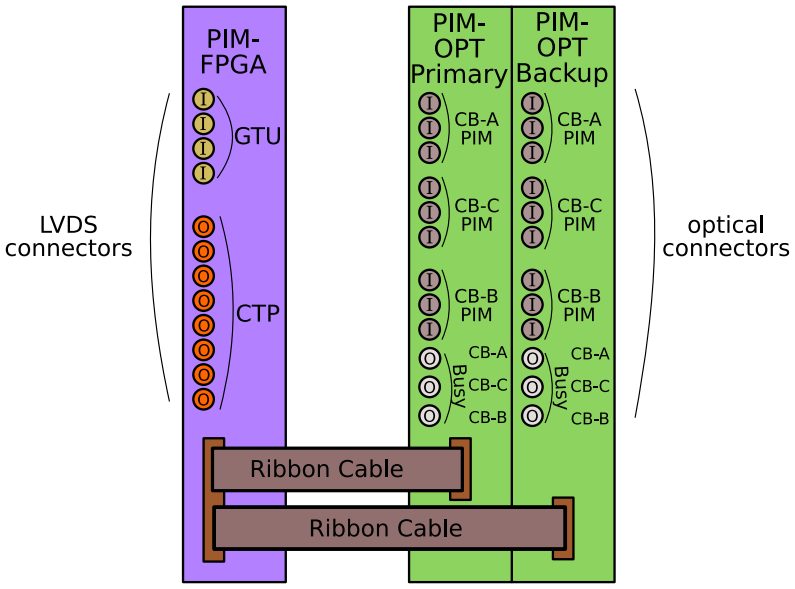


Figure 5.14: Diagram for the pre-trigger interface module (PIM) front panels. The pre-trigger interface module acts as translator between the GTU and the CTP on one side and the control boxes on the other side. The 'I' and 'O' in the circles stand for Input and Output.

In A-side one power supply supports the corresponding front-end boxes of the V0 detector and another supports the control box and the front-end box of the T0 detector, see fig. 5.15. The control box bottom, the TOF Unit and the pre-trigger components in C-side are powered by the other two power supplies. The TTC modules, which are part of control box bottom, need ±12 V in addition. So these power supplies have a larger number of channels to take the different voltages into account, as shown in fig. 5.16.

The power supplies are located in the galeries above the ALICE detector outside the L3 magnet.

While the study for this thesis, the powering scheme for the pre-trigger components on A-side was changed for easier access and maintenance. Therefore, a new patch panel (PP-PTA) was designed and installed approximately 1.5 m below the beampipe. Initially, it was planned to keep the possibility to power up all front-end boxes with separated low voltage channels to eliminate noise, which arise from ground loops. Later it was tested to power up the system on A-side with common channels, which showed no problems of such kind. The modified connection scheme is described below.

In between the power supplies in the galeries above the ALICE detector and the pre-trigger components on A-side are two patch panels, called PP0 and PP-PTA. From the galeries, cables with a cross section of 10 mm^2 are routed down to the PP0, sitting at the end of the miniframe.

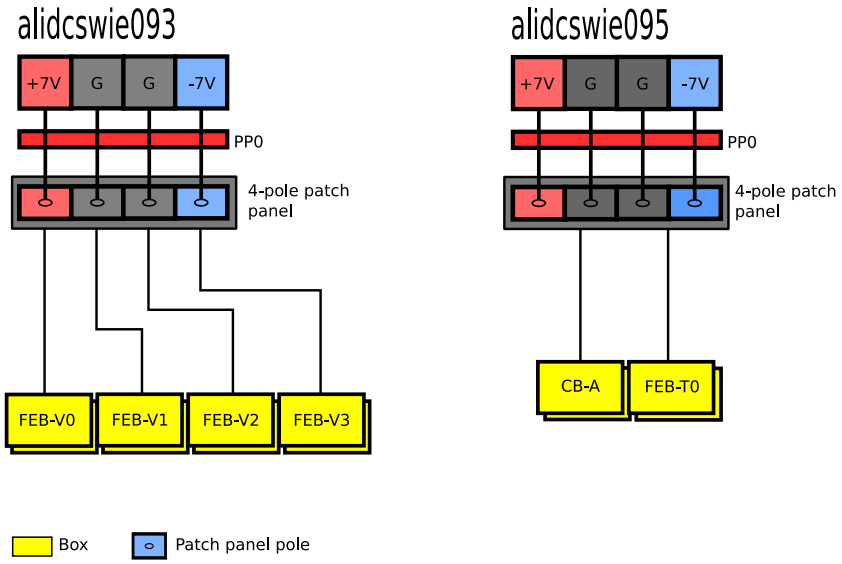


Figure 5.15: The altered low voltage power distribution scheme in A-side.

From here, cables of the same cross section run through the miniframe to the newly designed patch panel PP-PTA. The cabeling scheme from this patch panel to the front-end boxes was changed recently.

The cables between the patch panel and the front-end boxes of T0 and V0, have five cores with an individual cross section of 6 mm^2. The two black wires carry ground, the brown positive and the blue negative potential. One wire is spare. Thirty centimeters before the front-end boxes, each line is split up in two 2.5 mm^2 lines for primary and backup system powering. The ends are 4 pinned plugs with 2 grounds in the middle. The control box on A-side is located next to the new patch panel. The short distance allows to use thinner 2.5 mm^2 wires. The power plugs are identical to the ones for the front-end boxes and follow the same pin mapping.

The next improvement for A-side would be to power the primary system and the backup system individually by one power supply each. For this, the existing multicore cables (five cores) have to be exchanged by cables with the double number of cores.
A more detailed wiring diagram is given in the appendix. The preamplifier cards in the front-end boxes are powered by different power sources maintained by the V0, respectively the T0 group. The power pin mapping for the preamplifier cards can be found in the appendix C.

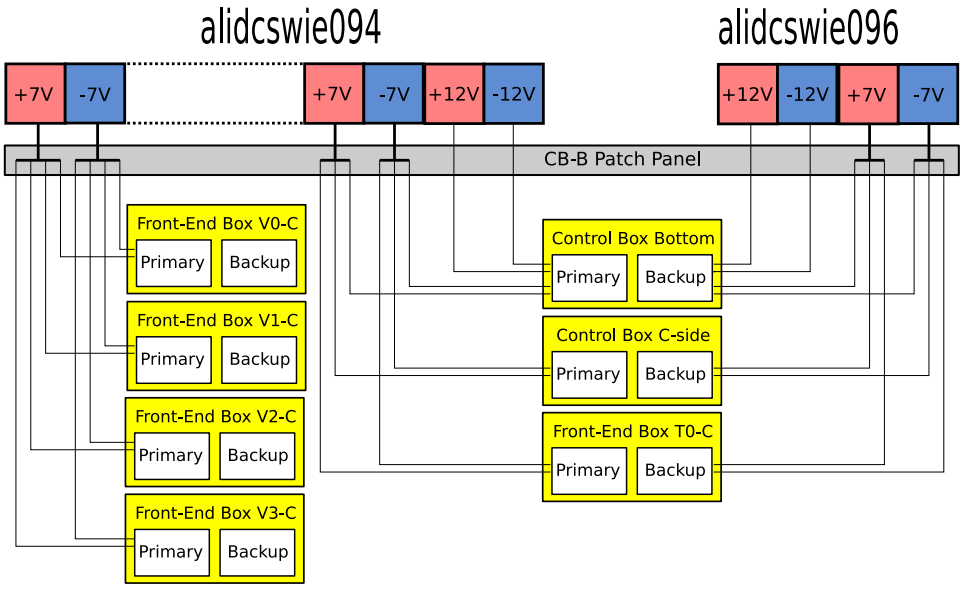


Figure 5.16: The low voltage power distribution scheme in C-side.

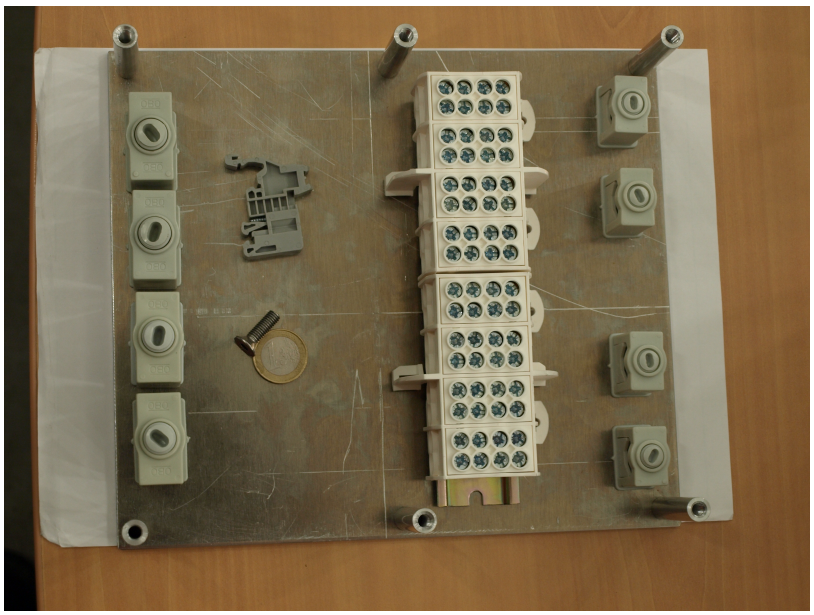


Figure 5.17: The redesigned patch panel with dimensions of approximately 21 cm x 26 cm. Two of these are installed in the cavern 1 m below the beampipe near to the front-end boxes on A-side. The eight white units in the middle fan out the power delivered by one power supply, coming from the right side. Each unit has two input slots and two output slots. Two neighbouring white units are connected together composing four poles (+5V, ground, ground, -5V) with four output slots each. The grey clamps reduce the mechanical force applied to the patch panel. An aluminium plate is mounted on top for protection.

6 Software for the Pre-Trigger System

This chapter describes the software to monitor and control the pre-trigger system. When the study for this thesis has been started, the configuration of the entire pre-trigger system was performed by executing shell based scripts by hand on a Linux system [54]. To change a parameter, starting and stopping the triggering, it was necessary to log in the Linux system running on the Detector Control System (DCS) board, using Secure Shell (SSH) and to execute prepared scripts. The overall state of the pre-trigger system was only known to the user who executed these scripts. Consequently, there had been strong desires to develop a system to automatize the configuration process for users, who do not have exhaustive knowledge of the pre-trigger system, and at the same time to enable display of the system status.

The software developed during the study of this thesis is to make such desires possible. The pre-trigger system can be configured within the ALICE detector control framework. All configuration, which is necessary to start the run, is executed automatically in back-ground and the user just has to pre-select the configuration before the system starts the automatic configuration.

As one of the most strongest tools to develop such a system, a finite-state machine was introduced to the system. The developed software is extensible and allows an easy modification of the current set of commands, if necessary.

All pre-trigger related software including the design of the FPGAs resides in the subversion repository for the TRD [53].

Naturally, as it is usual in many complicated control systems, the pre-trigger system software consists of many different hierarchies, and itself is part of a complex ALICE detector control system hierarchy. In the following sections, the ALICE detector control system hierarchy is shortly introduced, and it is shown how the pre-trigger software fits in such architecture, and then each component of the developed software is described.

6.1 The ALICE Detector Control System

The ALICE DCS is developed on base of the software framework PVSS [50]. PVSS is a SCADA system [51], a software which manages automatically very complex systems, such as plants and factories, from few or even only one computer. Such software gathers information from all components of the system and acts automatically to operate the system. Usually, a finite-state machine [40], implemented in the SCADA software, defines, what actions have to be taken under which conditions. The idea of a finite-state machine is shortly introduced in subsect. 6.1.2. Normally, the SCADA software displays information about the system and allows intervention by human through a graphical user interface. The following subsection introduces the overall hierarchy of the ALICE SCADA system.

6.1.1 Overview

As shown in fig. 6.1, the ALICE DCS system to monitor and control the detector consists of three layers, such as the supervision layer, the process control layer and the field layer.

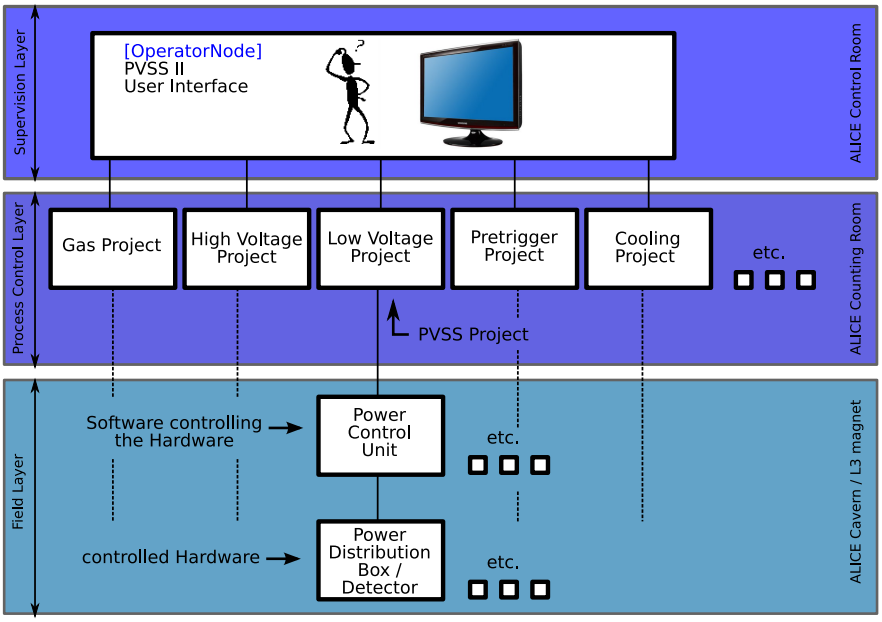


Figure 6.1: The ALICE DCS hierarchy, which consists of three layers: (i) the supervision layer, where a graphical user interface allows a user to monitor and control the all sub-components, (ii) the process control layer, where the PVSS project for a given sub-component prepares commands and receives information from that, and (iii) the field layer, where sub-component specific software is in direct control of the hardware. This hierarchy is exemplified by the low voltage system of the TRD.

Supervision Layer The human supervision and operation of the TRD takes place in the supervision layer. A graphical user interface based on the complex software framework PVSS is used here. It displays information received from underlying PVSS projects and sends commands given by the user to these projects. It runs on a Windows XP computer, called the "operator-node".

Process Control Layer For each sub-component necessary to operate the detector, such as electrical power, cooling, gas and the front-end electronics, exists a PVSS project (in fig. 6.1, the low voltage project). The PVSS project bundles the information retrieved from the corresponding hardware sub-components and provides this information to the graphical user interface. The PVSS projects peform commands given by the user by forwarding them to the sub-components in the field layer (in the given figure, the power control unit). Furthermore, the PVSS projects use software tools, such as logging and archiving facilities, configuration databases and alarm handlers. PVSS projects in the process control layers are running on Windows XP computers, which are called "worker-nodes". The associated software components used by PVSS projects are running usually in many computers accessible via the network, and those are mostly Windows XP and Linux computers.

Field Layer The hardware of the sub-components and the software to control it are associated with the field layer. This software executes received commands and retrieves information from the hardware and sends it to the corresponding PVSS project.

To develop the necessary software library used for communication between the process control layer and the software components controlling the pre-trigger hadware was the major task for the work described in this thesis.

The concept of a finite-state machine is used here to encapsulate the fine details of the individual sub-components and is used in all layers of the ALICE DCS. What finite-state machines are and how they are used in the ALICE DCS is introduced in the next subsection.

6.1.2 Finite-State Machine

A finite-state machine is an abstract model describing the behaviour of an object, which has a finite number of states, possible actions available at each state, and transitional states between those states [40]. Behaviour in this context means, how the system reacts to actions at a given state. Practically, in this thesis the finite-state machine is an software object, which stands for the lower level components of the system (such as hadware or lower level finite-state machines) and hides the details of the system. For example, most electrical devices, such as simple lamps, have the states *ON* and *OFF*. This case can be described as a state diagram, as shown in fig. 6.2. The transition states between those states could be called *SWITCHING ON* and *SWITCHING OFF*. The actions depend on conditions, in this example, whether the machine is needed or not. The possible actions therefore are `SWITCH ON` and `SWITCH OFF`.

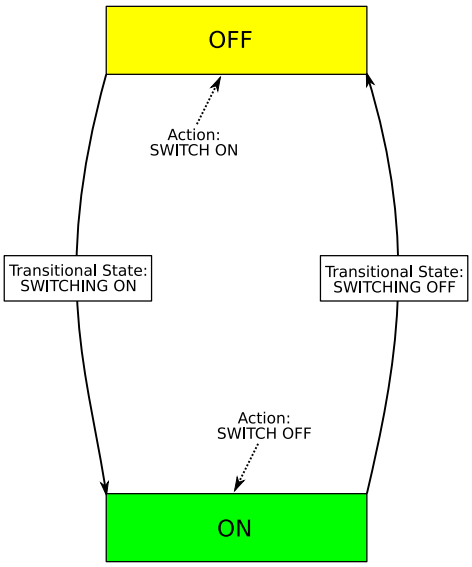


Figure 6.2: State diagram of a finite-state machine with two states.

Considering a more complex machine with several sub-components, each sub-component has an

individual finite-state machine and the state of the whole machine depends on the states of the sub-components.

Such architecture is used to synchronize all sub-detectors of ALICE towards a state, in which the detectors are ready to take data and is implemented in the DCS. The TRD is one of the sub-components of the ALICE DCS. The TRD itself is a finite-state machine and its state depends on the states of the sub-components of the TRD, such as the high voltage system, the low voltage system, the gas system, the cooling system, etc.

Since there are many control software components in ALICE DCS system, it is necessary for all of them to have a common way to communicate and transfer data among them. In ALICE, following other experiments and the LHC, it was decided to use the Distributed Information Management (DIM) network developed at CERN [48], which is introduced in the next subsection.

6.1.3 Distributed Information Management

The Distributed Information Management (DIM) was developed by CERN [48] and is network protocol at the user level using the TCP/IP network protocol. The DIM framework is compatible to several programming languages such as FORTRAN, C, C++, Java and Python. It provides libraries for those programming languages, and also for different system architectures, such as Intel i386 CPUs, Power PC, and ARM processors. The protocol and the library absorb the system architecture dependence and therefore allows the intercommunication among different system. Thus, it is well suited for a mixed environment, where many individual software components are developed.

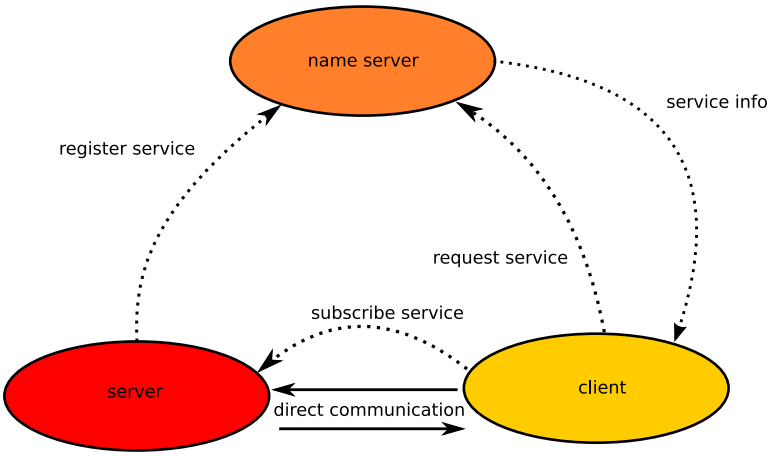


Figure 6.3: The DIM framework follows the client-server paradigm. The server registers its services at a name server to be visible to clients. The client requests a specific service and receives the necessary information from the name server to connect the server. The direct communication is user-defined.

The DIM network consists of a server, a client and a name server. The simplest example is shown in fig. 6.3. The DIM server registers the services at a name server in order to be visible to DIM clients. The name server keeps the present servers and their services available. The client requests a specific service and receives the necessary information from the name server, to communicate with the server. Using that information, the client subscribes to the server to send data to the client or to execute a given command. The data exchanged between the client and the server is defined by the user.

There are three different types of services typically provided by DIM servers.

DIM Service provides (regulary updated) information. In ALICE, for example, this information is typically temperature, pressure, power consumption, etc..

DIM Command service is used to receive commands from a client. A command can be of any type of data, such as integer numbers, strings or C-structs, and the user has to define their meanings.

RPC Service has both functions; receiving commands from a client and returning data to it. RPC stands for "Remote Procedure Call".

In ALICE, the DIM network is used to monitor device states, using service channels and send state transition commands using command channel. RPC channels are used, where both functions are needed at once.

6.2 The Detector Control System for the Pre-Trigger System

The Detector Control System (DCS) for the pre-trigger system reflects the standard architecture of the ALICE DCS with the three software layers and is shown in fig. 6.4. In this figure, the architecture is exemplified with the intermediate control boxes and the connected front-end boxes. The corresponding diagram for the master control box (CB—B) and the TOF Unit looks basically the same.

The DCS for the pre-trigger system consists of following main components:

Pre-Trigger Slim Server (PTSS) forms together with pre-trigger hardware the field layer of the pre-trigger system. Six pre-trigger slim server run on six DCS boards in three control boxes. Three servers are used for the primary and three servers are used for the backup system. Each of these DIM servers providing a Remote Procedure Call (RPC) service directly controls components of the pre-trigger hardware. It executes commands received from the pre-trigger finite-state machine daemon and reports to it, if the execution was successful or not.

The Pre-Trigger Finite-State Machine Daemon (PTFSMD) implements the finite-state machine of the pre-trigger system, as explained in sect. 6.3. It is either a DIM client to the pre-trigger slim server or a DIM server for the pre-trigger PVSS project. The daemon translates the transitions between states into commands specific for the pre-trigger system and sends them to the pre-trigger slim servers. Also, it is aware of the overall system status by collecting information from all pre-trigger slim servers and reports on it upon request.

The daemon runs on a Linux computer, called worker-node 005. Together, the pre-trigger finite-state machine daemon and the pre-trigger PVSS project form the process control layer in the pre-trigger system.

The Pre-Trigger PVSS project is part of TRD PVSS project. It is a DIM client and communicates with the pre-trigger finite-state machine daemon. It forwards instructions (from the user) to the pre-trigger finite-state machine daemon and displays aquired information on the graphical user interface. The project is still being developed.

The idea to develop these pre-trigger slim server and the pre-trigger finite-state machine daemon was proposed by an author, at the beginning of the work for this thesis, and developments have been started. More details, how those are implmented, work and communicate with each other are precisely described in the following sections.

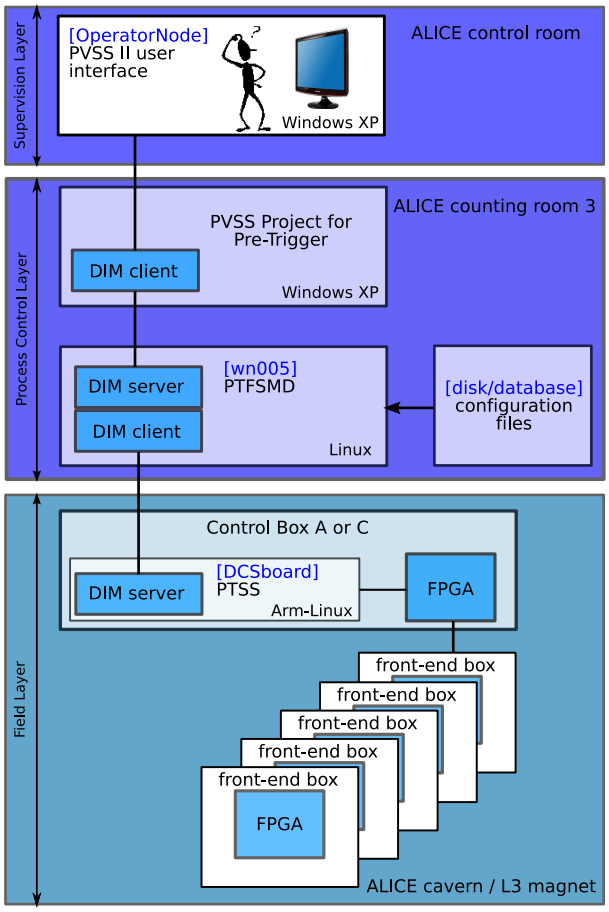


Figure 6.4: The Detector Control System for the pre-trigger system. The user configures and surveys the pre-trigger system with a graphical user interface displaying the status of the system. The pre-trigger project requests commands and information via the DIM network from the software in the process control layer, the here as server appearing pre-trigger finite-state machine daemon. The daemon itself connects as DIM client to the software controlling the hardware, the pre-trigger slim server. This software performs the commands and sends information back to the daemon, who forwards it to the pre-trigger project, displayed in the graphical user interface.

6.3 The Pre-Trigger Finite-State Machine Daemon

The pre-trigger finite-state machine daemon (PTFSMD) is a DIM implements a finite-state machine and controls the pre-trigger slim servers. It uses the DIM network for communication. It is written in C++ and runs on a Linux computer. The PTFSMD communicates with the PVSS project for pre-trigger and the pre-trigger slim servers controlling the pre-trigger hardware. To fulfil this task the PTFSMD is not only a DIM client to the pre-trigger slim server, it is also a DIM server as indicated in fig. 6.4.

The state diagram of the finite-state machine as it is implemented in the PTFSMD, is shown in fig. 6.5. The blue rectangular boxes represent static states, in which the finite-state machine stays until a transition command arrives or a critical error happens. The yellow round boxes are the transitional states, where the finite-state machine executes the pre-defined procedure and changes automatically into the next static state without receiving additional commands from outside. The white rectangular boxes with dashed arrows pointing at static states are the transition commands to provoke a transition into another state. Exceptional is the red "ERROR" state, to which the finite-state machine can go from any previous state.

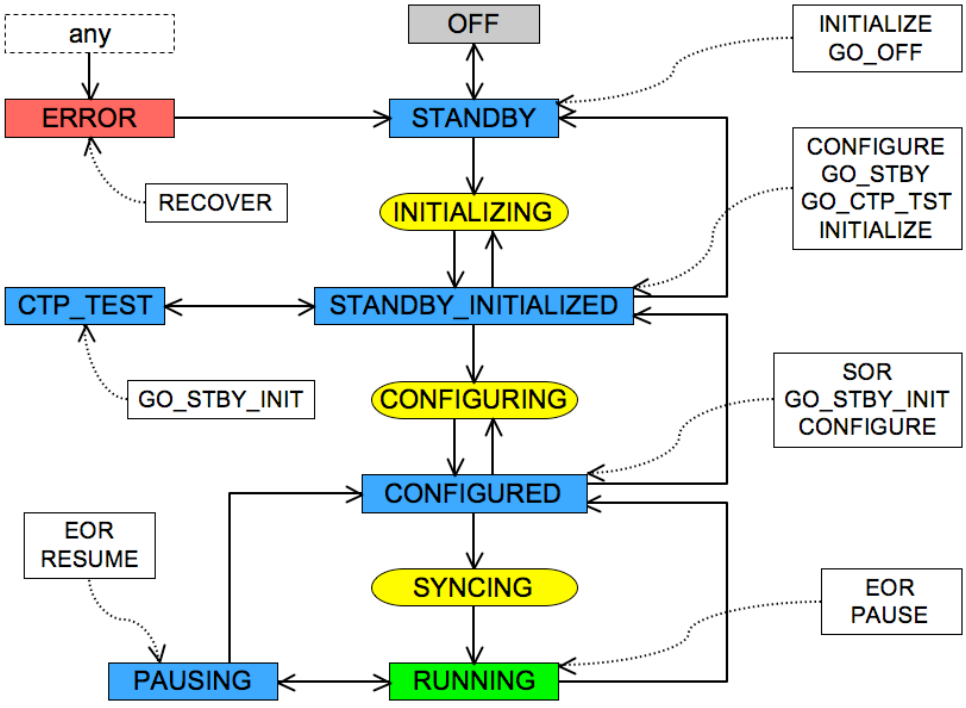


Figure 6.5: State diagram of the finite-state machine for the pre-trigger system, implemented in the pre-trigger finite-state machine daemon.

The precise description of all states is given below.

OFF All pre-trigger hardware is switched off.

STANDBY All components of the pre-trigger system are powered. The pre-trigger slim servers in every control box are up and running, ready to be initialized. The following transition commands accepted in this state are:

- `GO_OFF`
- `INITIALIZE` provokes the transitional state *INITIALIZING*.

INITIALIZING Transitional state, in which the FPGA designs are uploaded.

STANDBY_INITIALIZED The FPGA designs for the front-end boxes, the control boxes, and the TOF Unit are loaded. Possible transition commands accepted in this state are:

- `GO_STBY` means to go back to *STANDBY* state.
- `INITIALIZE` provokes the *INITIALIZING* state.
- `GO_CTP_TST` brings the system in *CTP_TEST* state, described later.
- `CONFIGURE` provokes the transitional state *CONFIGURING*.

CONFIGURING Transitional state, in which all configuration registers of the FPGAs are set, such as the delay of the input channels, the lookup tables and the trigger timing parameters. All counters are set to zero.

CONFIGURED The system is fully ready for operation, but the run is not started yet. If no errors occur, the system returns to this state after individual runs.

- `GO_STBY_INIT` returns the system to the *STANDBY_INITIALIZED* state.
- `CONFIGURE` reconfigures the run parameters by provoking the *CONFIGURING* state.
- `SOR` initiates the start of the run. It changes to the transitional state *SYNCING*.

SYNCING Transitional state, in which the pre-trigger system provokes the sychronisation of the tracklet processor on all readout boards and sets the front-end electronics in a state ready to receive triggers.

RUNNING The pre-trigger system starts issueing pre-triggers and forwards the ALICE trigger signals in proper order. Available commands accepted in this state are:

- `EOR` signalizes the end of the run and returns the system to *CONFIGURED* state.
- `PAUSE` sets the system in *PAUSING* state and temporarily stops the triggers.

PAUSING Triggering is temporarely stopped during a run. It leaves that state, if following commands arrive:

- `RESUME` returns the system to *RUNNING* state, restarting the production of pre-triggers.
- `EOR` initiates the end of the run and returns the system to the *CONFIGURED* state.

ERROR Any severe error puts the system in error state. A full recover sequence beginning at *STANDBY* has to be performed. Only the command `RECOVER` is accepted to reset the system and brings it to the *STANDBY* state.

CTP_TEST Special state, in which the connection to the Central Trigger Processor (CTP) is tested.

During the transitional states, the PTFSMD prepares the necessary commands for the PTSS and puts them in a special data format. This format is defined in the pre-trigger software library, described later. This data is then sent to the PTSS using its RPC channel, and the daemon awaits the answer to these commands. The answer is information about execution of the issued commands and is also put into a special data format, similar to the one used for the commands. The information in the answer is used to define the state in which the pre-trigger system is at the moment. The PTFSMD decides next action according to that answer, and if necessary change the states. For example, if PTSS fails to execute commands given by PTFSMD, it returns error codes to the PTFSMD, which might change the current state to the ERROR state.

6.4 The Pre-Trigger Slim Server

The pre-trigger slim server (PTSS) has the role to receive configuration commands from PTFSMD, executes the configuration commands, and returns their results to the PTFSMD. For receiving and returning the commands and results, the DIM RPC channel is used. Therefore PTSS has DIM server inside. PTSS is written in C++. Before running on the on the six DCS boards on every pre-trigger mainboard, it must be downloaded from a repository, dedicated for DCS board. This repository provides executables, libraries and other software for the DCS board as packages. The software to manage, download and install these packages is called *iPKG* [62] and is similar to the widely used package managers for Linux systems, but simpler, due to the limited hardware resources of the DCS board.

PTSS is started automatically by an entry in a script, which is automatically executed while the boot up of system of the DCS board.

The dedicated data format for the communication between the client, such as PTFSMD and PTSS has been defined. All commands, parameters and FPGA configurations are put into this data format and are sent to the PTSS. Usually, all performed commands are either read and write operations on registers of the connected FPGAs or the upload of the FPGA design, via the JTAG protocol. To execute those operations on the FPGAs, the PTSS uses two devices on the DCS board, namely the SCSN Master and the JTAG controller. The PTSS carries out the received commands and prepares an answer, containing information about errors and successfully executed commands and sends this data to the PTFSMD using its RPC service. The answer is also in a special data format, similar to the format of the arriving commands.

The list of available commands sent to the PTSS can be split up in different realms.

SCSN Commands There are three basic commands for access the registers of the FPGA via SCSN [42]:

- `SCSN_read` issues via a given SCSN line (to the different FPGAs of the control box, front-end boxes or the TOF Unit) the readout of a given register and returns the stored value.

- `SCSN_write` issues the writing of a given value to a given register of the targeted SCSN device (such as the FPGAs).
- `SCSN_reset` resets the SCSN interface of the targeted device to a defined state.

Control Box Commands All commands use the basic SCSN commands where the selected SCSN line (to the FPGA of the control box) is fixed. Besides the corresponding commands for reading, writing and resetting, there are additional commands available:

- `CB_read` Is equal to `SCSN_read` with SCSN line fixed to FPGA of the control box.
- `CB_write` is equal to `SCSN_write` with SCSN line fixed to FPGA of the control box.
- `CB_reset` is equal to `SCSN_reset` with SCSN line fixed to FPGA of the control box.
- `CB_read_many` uses the basic `SCSN_read` command with fixed SCSN line to read out a given range of register in the FPGA of the control box.
- `FEBS` Sets or unsets a given front-end box connected to the control box in configuration mode, as mentioned in sect. 5.2. The registers of the front-end box FPGA are only accessible, if the front-end box was selected through this command. Only one front-end box at a time is accessible.

Front-End Box Commands Same commands as the ones for control boxes are available, except of the select command.

- `FEB_read` Is equal to `SCSN_read` with SCSN line fixed to FPGA of the front-end box.
- `FEB_write` is equal to `SCSN_write` with SCSN line fixed to FPGA of the front-end box.
- `FEB_reset` is equal to `SCSN_reset` with SCSN line fixed to FPGA of the front-end box.
- `FEB_read_many` uses the basic `SCSN_read` command with fixed SCSN line to read out a given range of register in the FPGA of the front-end box.

Miscellaneous Commands Various other commands.

- `JTAS` Selects the JTAG line on the DCS board prepared for the FPGA of the control box or the front-end box.
- `PXSV` Programs a targeted FPGA by uploading a given design file via the JTAG controller of the DCS board.
- `COUR` Starts the transfer of the RAM counters to prepared registers of the FPGA in either the control box or the front-end box and returns all or a specified counter.
- `RUNI` Retrieves for a given box, either front-end box or control box, all information associated with the configuration of the trigger logic and the values of the counters. Usually, this command will be issued just before the start of a run or shortly after the end of a run.

The design of the FPGA of the TOF Unit was decided to modify significantly and is currently under development. Therefore, at the moment only the basic FEB_read/write/reset commands are available to configure the registers of the TOF Unit FPGA. More commands will be defined for that purpose and there are plans for even more, such as a automatic configuration of the lookup table.

The precise description of the format of the exchanged data, in which the above listed commands are encoded, is discussed in sect. 6.5 and a complete list of currently defined commands and their necessary arguments is given in the sect. D.

6.5 The Pre-Trigger Library

The functions and subroutines developed for the pre-trigger system within this thesis are collected in a standard Linux shared object library, called *libptrg*. It is written in C++. The library also defines the format of communication between the pre-trigger slim server and the pre-trigger finite-state machine daemon.

The files contained in the library are listed below.

CheshireCat.h/cc contain the code for basic read and write operations via SCSN. The code to access the registers of the FPGA via SCSN has been ported from the TRD front-end electronics software and was optimized for use in the pre-trigger system. Furthermore it was adapted to be used in C++ code.

ptdat.hh/cc contain the definition of the data format from the client to the server (commands). Those files also contain the functions to prepare and read that data format.

ptssdat.hh/cpp contain the definition of the data format from the server to the client (results). Those files also contain the subroutines to prepare and read that data format. In addition, the code contain the functions to execute commands received from a client.

playxsvf files contain code, which was ported from a software tool for programming Xilinx FPGAs. The code was adapted for use in the *libptrg* and is used to program the FPGAs in the pre-trigger system.

run_info.hh/cc contain the definitions and functions to retrieve and convert information associated with the configuration of the FPGA and the implemented counters into XML.

pt_ui.hh/cc contain the user interface classes to be used by clients.

The precise description of the data format for the communication between client and server defined in the *libptrg* is given in the following two subsections and is illustrated in fig. 6.6.

6.5.1 Data Format from Client to Server

To compose a set of commands to be executed by the PTSS, the client uses the format shown on the left side in fig. 6.6.

The data format consists of an array of unsigned integer values with 32 bits width for each element. This array is prepared by the client to be sent to the PTSS via the DIM RPC channel.

This array is split into several blocks and the first block in the array is called *ptdat_header*, which has information about the data format itself, such as the total size, the number of appending commands and their associated arguments, the number of appending files and so on. The *ptdat_header* is followed the first command block. It consists of a *ptdat_command* and the associated arguments for that command. The *ptdat_command* identifies the command by an integer

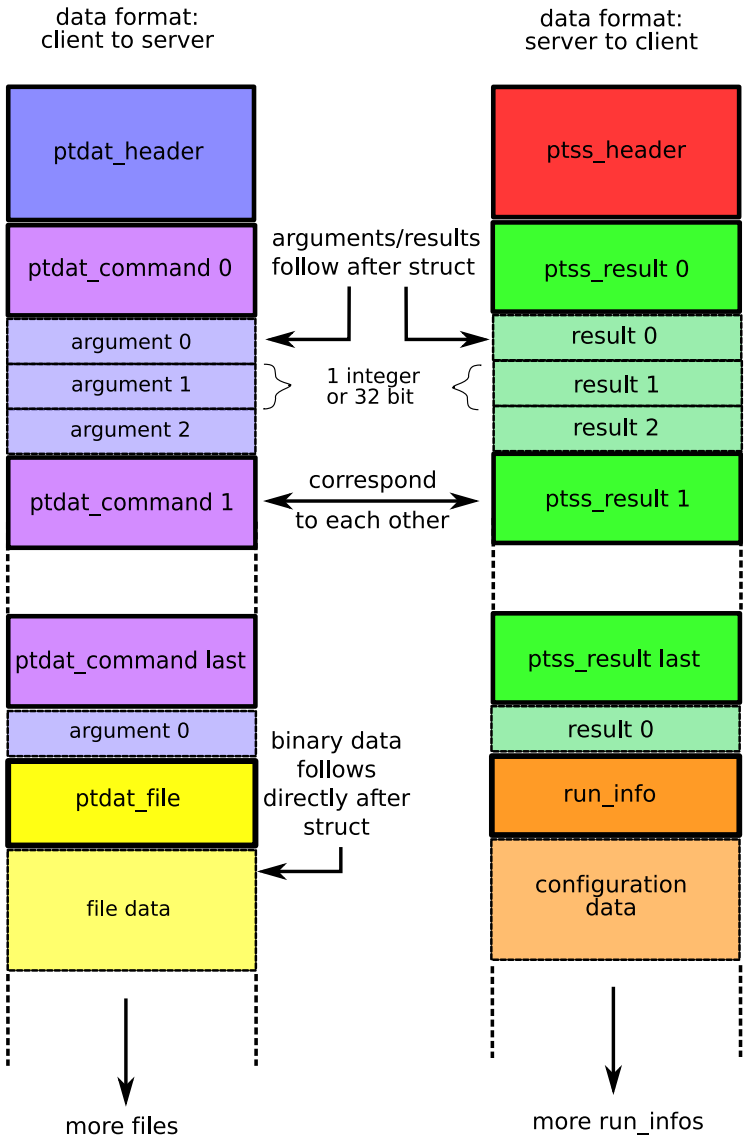


Figure 6.6: Diagram illustrating the user defined format of communication between DIM client and server. The DIM client uses the array format shown on the left side to prepare a set of commands and sends this data to the server. The server prepares an answer to the received commands by using the array format on the right side and sends the prepared data to the client.

number and contains the number of associated arguments. Then the arguments follow. The next command block follows directly the last argument of the previous command block. This pattern continues for all commands to be sent to PTSS.

Instead of sending pre-defined command and arguments, there is a requirement to read binary data from a file and send it to PTSS, such as a FPGA configuration file. This binary data is prepared in the same manner as the commands and is appended at the end of the array. The *ptdat_file* block holds information about the associated data and is directly followed by the binary data itself.

If the composition was done correctly, the size of the whole data is a multiple of 32-bit. Both client and server check this *32-bit alignment* of the data, to detect possible memory corruptions. After composition and checking the data, the client sends the complete data block to the server. The server uses the same array format to decompose and read the contents of the data received. They obtained commands are then executed.

6.5.2 Data Format from Server to Client

The server prepares the answer to the received commands in similar manner to the scheme explained in the previous subsection. This data format is shown on the right side of fig. 6.6.

The data format consists of an array unsigned integer values with 32 bits width for each element. The first block (*ptss_header*) holds information about the data format itself, such as number of appending results, total data size and so on. The first result block follows directly the header and consists of the *ptss_result* and the associated result values. The *ptss_result* contains an identification of the command, which provoked the result, the number of appending result values and a value that tells, whether the command was successfully executed or not. This pattern continues for all results to be sent to the client.

After the last result block follows the *run_info* block, in case it was requested by the client. The *run_info* block is followed by the *configuration data* and contains all readable FPGA configuration of a certain front-end box or control box. It is desired to keep such information in a database. A special software framework performs this task and is described in the following section.

6.6 Configuration Database

After the run, it is desired to keep information about the configuration. The storage of the configuration parameters, the operation status and various run specific counters of each TRD module, including the pre-trigger system, is necessary for offline reconstruction and quality assurance of the configuration and is put into a database (OCDB). A software framework to acquire and store this information was implemented in the ALICE DCS and is shown in fig. 6.7. Upon the start and end of individual runs, the Experiment Control System (ECS) sends a signal to the fxsproxy to trigger the readout of the configuration. The fxsproxy runs permanently on one of the Linux worker-nodes, part of the ALICE DCS online network. It receives the data in XML format [58] from the individual modules, in case of the pre-trigger system, the pre-trigger finite-state machine daemon. The data is stored into a file and forwarded to the file exchange server. After each run, another software component (Shuttle) collects all files from the file exchange server and

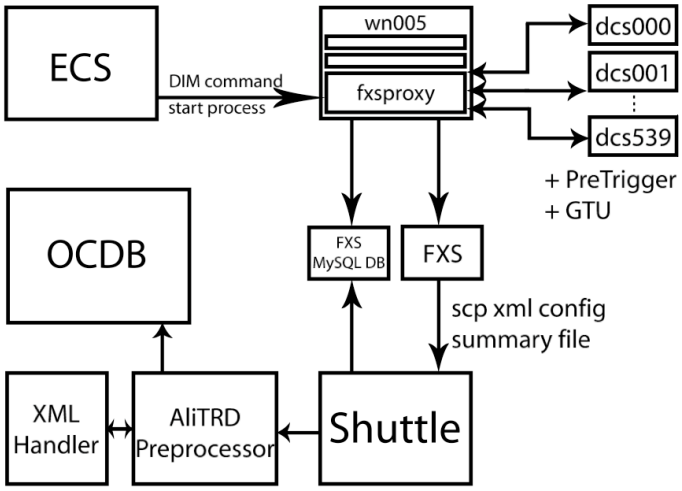


Figure 6.7: Diagram of the communication and data flow for the storage of the configuration data for the TRD, taken from [57]

stores them in a special format, compatible for offline analysis, in the ALICE offline calibration database [57].

6.7 The Pre-Trigger Injector

For debugging purposes, a special tool, called pre-trigger injector, has been developed. This tool does not comply with the finite-state machine paradigm and is used by experts only. It is a simple DIM client, that uses the *libptrg* to compose a single or a set of commands in the above explained data format and sends it directly to the PTSS. The pre-trigger injector provides the following features:

- Sends a single command to the specified server by invoking the programme with the '-c' option and followed by the desired command in the form:

  <command string> <argument 1> <argument 2> ...

  The list of command strings and possible arguments is given in sect. D. The arguments representing integers can be given in every numerical base by adding the corresponding commonly used prefix, like '0x' for hexadecimal numbers.

- Reads from a file, where every line represents a command in the above format, and sends them to the specified server. Here, the '-f' option followed by the file location must be added to the invocation.

- Prints a helping text, if it is invoked with the '-h' option.

7 Test Results of Pre-Trigger System with T0 detector

This chapter presents results from a test of the pre-trigger system with the T0 detector.

7.1 Scope of the Test

In June 2009, commissioning tests were performed with the pre-trigger system and the T0 detector on C-side. The scope of the test was to verify the proper operation of the interface between T0 detector and pre-trigger system of the TRD. This includes the proper discrimination of the T0 photomultiplier signals of known amplitude depending on a configured discriminator threshold and the processing of the digitized signal in the FPGA logic of the front-end box.

A focus of the investigation was the feasibility of the signals provided by the T0 detector for pre-trigger purposes. The effects of "extra pulses", such as after-pulses, noise and reflections, had to be quantified and evaluated, in order to characterize the purity and efficiency of the T0 pre-trigger.

After-pulses occur in each photomultiplier. For many applications they do not pose a problem, since a gated photomultiplier tube signal is used. However, in case of using a photmultiplier signal as a trigger, all after-pulses above the discriminator threshold will be interpreted as triggers. Therefore, the after-pulse rate of a photomultiplier tube, used in such applications, has to be as low as possible.

In 2007, the V0 group, who are using the same preamplifiers, observed signal reflections in the amplified output of the preamplifier (later referred to as "old preamplifier card") to the front-end electronics of the detector [59]. As a consequence, the preamplifier was redesigned and the new card (referred to as "new preamplifier card") is used in the V0 front-end boxes. However, the T0 group did not use the amplified output to their front-end electronics so far and therefore didn't observe reflections in their front-end electronics with the old card. But it was never tested, if the reflections appear in the amplified output of the pre-trigger system.

These effects were studied with three different test setups, explained in the next section.

7.2 Test Setup

For the test, the already installed equipment in the L3 magnet in C-side was used, namely T0-C (T0 detector C-side) and the front-end box FEB-T0-C (Front-End Box for T0 in C-side). Normally, this front-end box is equipped with 12 preamplifier cards. In the test, only three preamplifier cards were installed in the channels 1 to 3 in the mapping shown in tab. 7.1.

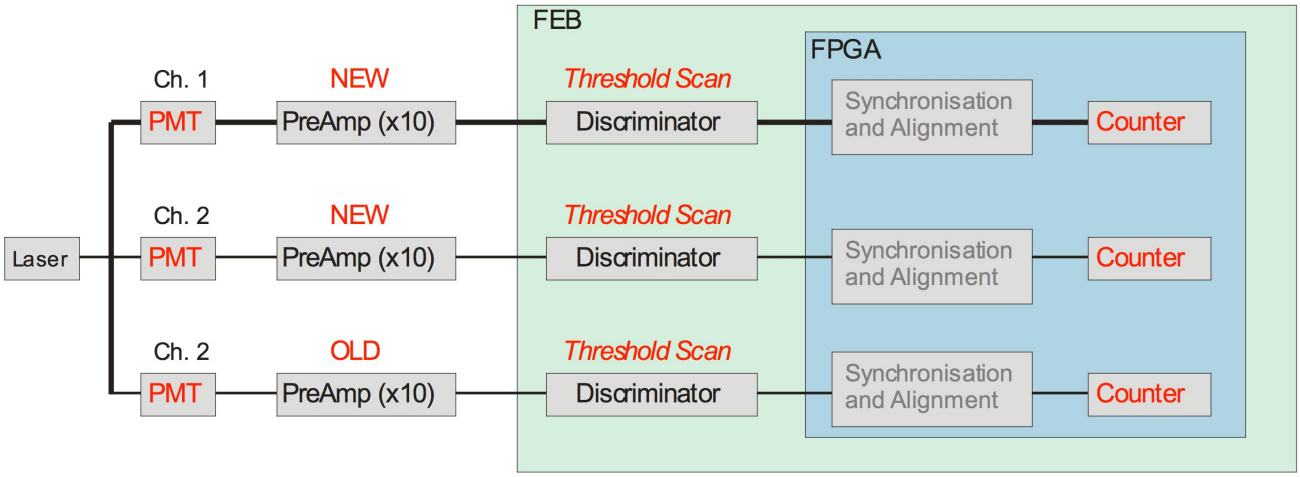


Figure 7.1: Threshold Scanning Setup. The laser provided signals of a set amplitude (in MIP) in a given frequency and they are counted for a set time intervall. For different amplitudes, the number of detected signals in each channel per time interval for a given discriminator threshold were compared to the set frequency of the laser. Any excesses to the number of signals expected from the laser frequency are "extra-pulses". The discriminator threshold for all channels was varied in a scale of 256 steps from 0 V to 1.2 V.

channel 1	channel 2	channel 3
new preamplifier card	**new** preamplifier card	**old** preamplifier card

Table 7.1:

In all measurements, a test signal of a fixed pulse height was generated with the help of a laser. The test signal was tuned to be equivalent in amplitude to the signal produced by a given number of minimum ionizing particles (MIPS) traversing the T0 detector. The T0 dector control system (DCS) was used to set up the signal pulse height in the range of 1MIP to 50MIP and signal rates from 100 Hz to 5 kHz.

The discriminator threshold is applied by setting a configuration register of the front-end box FPGA. The possible values are integer numbers in the range of 0 to 255 and correspond to voltages at the DAC in the range of 0 V to 1.2 V.

We took data with three different methods.

Threshold Scanning (fig. 7.1). The discriminator threshold was varied and the corresponding rates were counted for a constant amount of time. This provides the integrated count rate for all signals above the threshold. The expected graph of the counts versus the threshold has an initial fast drop when the threshold rises above the amplitude level of the noise. A plateau should follow, where the threshold is low enough to count the full signal distribution, but no more noise is present. Identifying this plateau region allows to define the threshold with the optimal efficiency for a given signal. When the theshold becomes comparable to the signal amplitude, the counts decrease and finally reach zero. The discriminators threshold

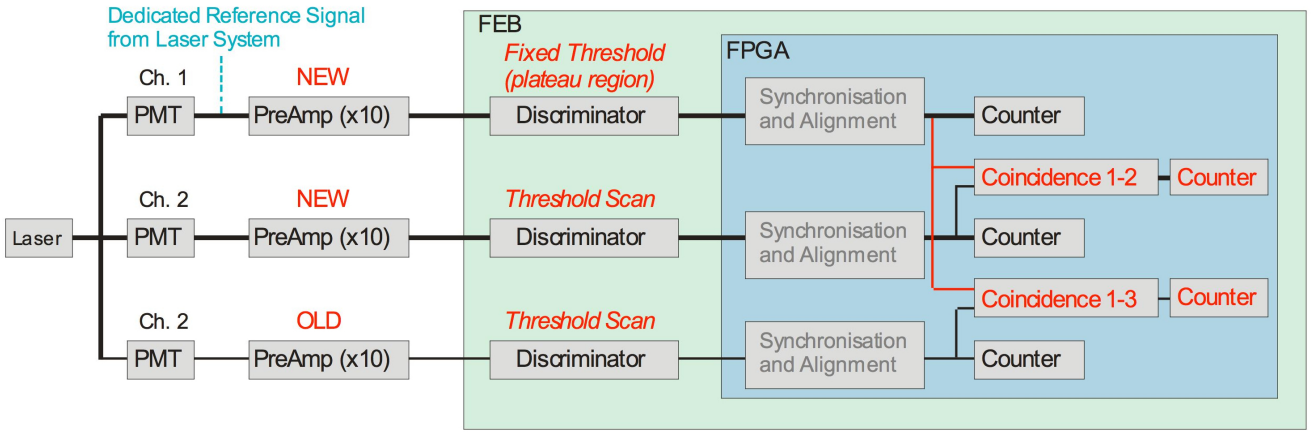


Figure 7.2: Test setup for the Coincidence Measurement. One channel is operated with a fixed threshold to provide a high efficiency signal reference. For the other channels, a threshold scan is performed and their coincidences with the reference channel are counted.

range is designed to remove noise, therefore it will reach the signal amplitude only for small signals of 1 or 2 MIP.

Coincidence Test (fig. 7.2) With a clear plateau region, the Threshold Scan would be sufficient to detemine the distribution of non-signal pulse. In case of a broader of the excess signal, as it is the case for after-pulses and reflections, additional information is needed for separation of the signal and the excess count. The Coincidence test uses a reference signal derived from a laser to tag true signals and to count coincidences of signals in each channel with the reference signal. The reference signal is fed to an unused channel of the front-end box and is counted in the same way as the others.The number of signals in the other channels in excess to that reference number is then not originating from laser-stimulated pulses, but from other sources such as after-pulses, noise and reflections. For this test, it was not possible to get an electronics pulse from the laser control system. Thus the signal in one of the channels, namely channel 1, was used as the reference signal. This reference channel can be set up in a way to provide basaically 100 % efficiency without contamination of the signal by applying lower high voltage settings to the photomultiplier tube. The lower voltage results in a smaller after-pulse contribution. A threshold scan for a channel with such settings (fig. 7.4 shows an extented region with a flat plateau, which allows to choose a safe threshold for that channel.

Timestamp Analyzer (fig. 7.3) allows to investigate the time structure of the "extra-pulses". For each discriminated pulse, the time (in cycles of a 40 MHz clock) after the last reference pulse is recorded. The spectrum shows a prompt peak from the true signal and a distribution of delayed pulses. It allows to quantify signal and non-signal counts and moreover the separation of different sources of extra-pulses.

Reflections exhibit a sharp peak at a time corresponding to the signal delay due to the cable length.

After-pulses appear as a broad signal distribution in time extending up to several μs.

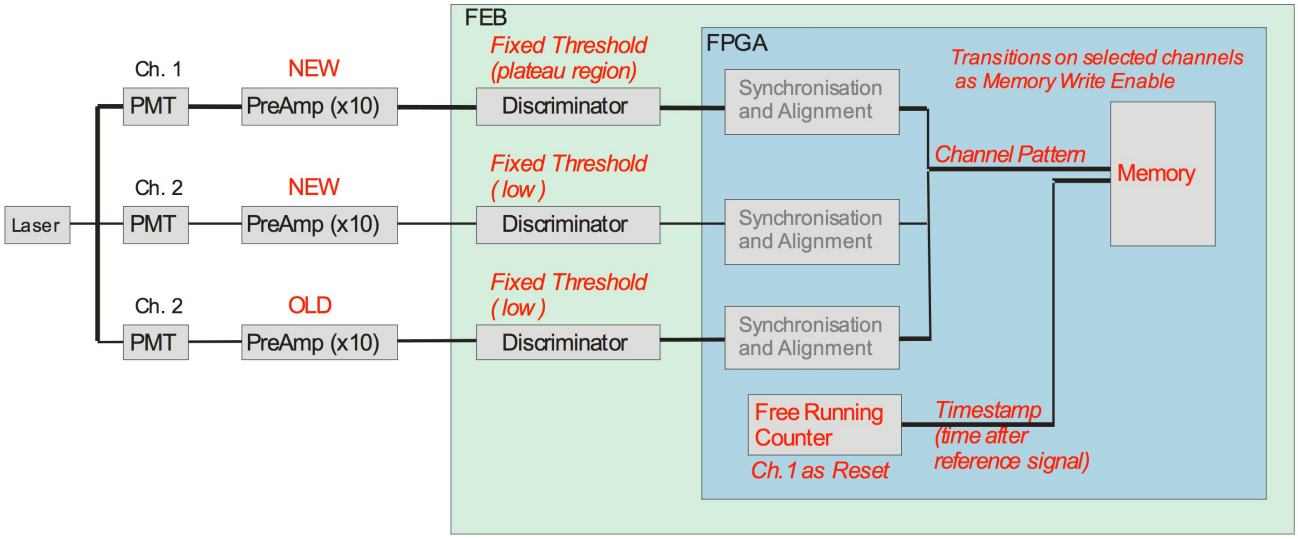


Figure 7.3: Schematic view of test setup for the time distribution of extra-pulses. The reference signal in channel 1 starts a timestamp counter. Signals discriminated in the other channels are stored to memory with their timestamp. This provides the time distribution of signals above the chosen threshold relative to the reference signal.

The timestamp analyzer method provides the most detailed information of all three used methods. However, readout of the timestamp data of all individual signals from the front-end box is slow, and thus the other two counter-based methods allow to collect significantly more statistics.

7.3 Test Results

Figure 7.4 shows data of the Threshold Scanning for channel 1 for different signal amplitudes (MIP). Channel 1 with a new preamplifier card shows the expected behaviour.

At a low discriminator threshold, low amplitude electronics noise dominates the counts. Going to higher thresholds, the number of counts decreases until it equals the laser rate. Above this threshold, all extra-pulses are suppressed and a flate plateu at the laser rate is visible. If the threshold exceeds the signal amplitude, induced by the laser, the count rate falls down very quickly. Only for the 1 MIP distribution (which was measured at a lower laser rate of 300 Hz) the threshold reaches the signal region, where the counts drop to zero over a threshold range that corresponds to the width of the signal distribution.A threshold of 40 was chosen for the measurements with channel 1 as reference channel. With this setting the efficiency of the channel for all signal amplitudes, from 1 MIP on, is 100%, and only at the highest amplitude (50 MIP) is a small contribution from extra-pulses present.

Figure 7.5 shows in direct comparison data from the Coincidence Test for channel 2 with new preamplifier and channel 3 with old preamplifier (coincidence means here, the coincidence of channel 2 and 3 with channel 1). The red curve in left plot and the green curve in the right plot are the coincidence counts, which are in good agreement with the set laser rate. The blue curves on the left and the magenta curves on the right are the total counts for different signal amplitudes. The difference between the total counts and the coincidence counts is the excess count for the

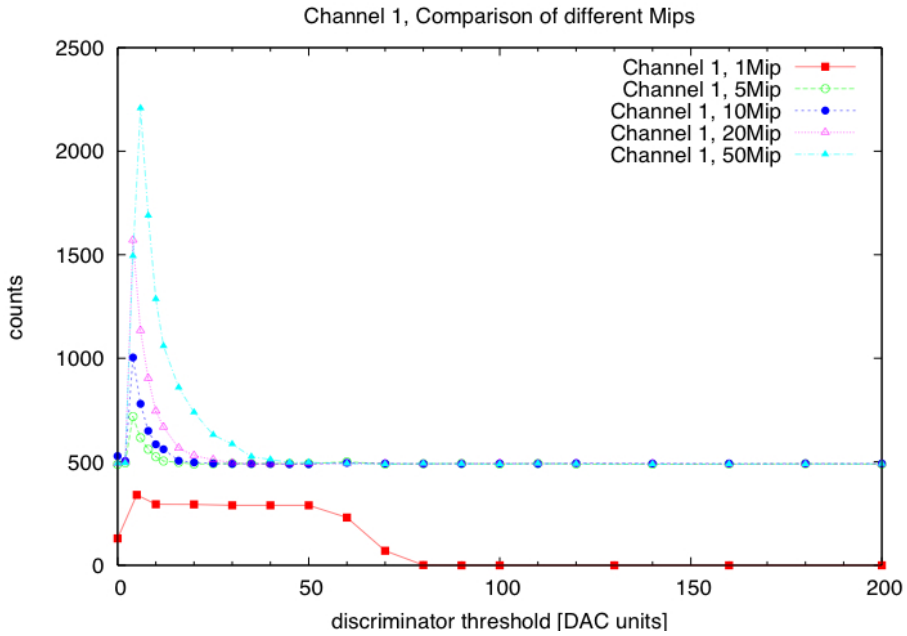


Figure 7.4: The overlap of the plateaus defines the proper threshold with almost 100% efficiency around 40 (in digital-to-analog units). This channel was later used as reference for the laser at the fixed threshold. The curve for 1 MIP was measured at a lower laser rate.

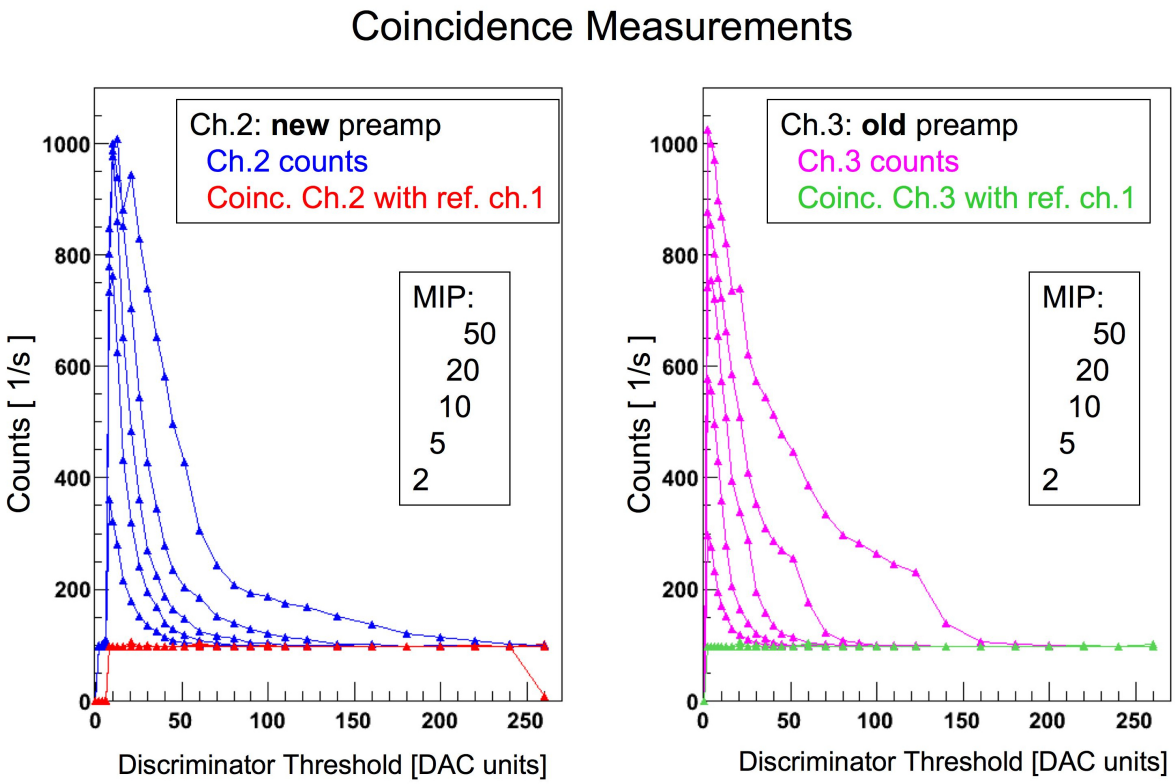


Figure 7.5: Coincidence Measurement for Channel 2 and Channel 3.

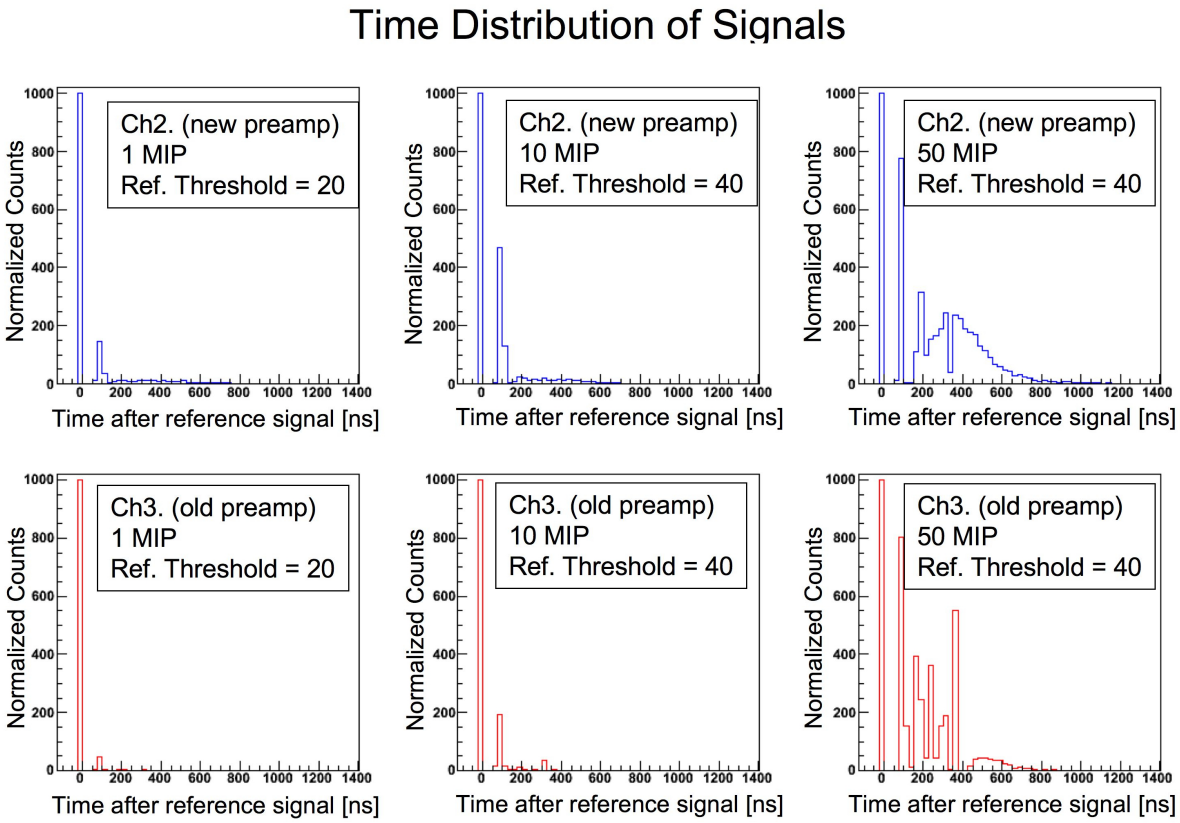


Figure 7.6: Time Distribution for Channel 2 and 3: both Channels show a strong signal at 100 ns and channel 3 in addition has some unexpected structure after the first two pulses.

corresponding channel. Both channels have an additional excess contribution with a rate that increases with signal amplitude, which extends for 50 MIP to above the discriminator threshold of 200. Channel 3 with an old preamplifier shows an additional structure (the "shoulder"), that probably comes from reflections. The amplitude of a reflection would be larger than other excess signals, because it depends on the amplitude of the true signal with some attenuation. That seems to fit here.

The data of the Timestamp Analyzer is shown in fig. 7.6, displaying the number of signals versus their timestamp relative to the reference signal. For the timestamp measurements, the thresholds for channel 2 and 3 were set low in order to record as much of the excess sources as possible. The gap after the main pulse in all plots, comes from a configurable dead time.

Additional signals are best viewed in the 50 MIP data (third column), due to the low statistics in the Timestamp Analyzer measurements. Both channels show a strong signal at around 100 ns. According to the T0 group, this signal comes from ringing.

In channel 2 (upper right) equipped with a new preamplifier, the smooth distribution following the 100 ns-signal is most likely produced by after-pulses. Afterpulses typically come from excited residual gas in the photomultiplier tubes and their number decreases with increasing time, what is visible here.

Channel 3, with old preamplifier, has less overall excess signal compared to channel 2 (prob-

ably due to the variation of individual photomultiplier tubes), but a strong structures with a pronounced peak at around 400 ns. Assuming a cable length of about 50 m from the preamplifier to the front-end electronics of T0, a signal, which is reflected, travels 100 m until it arrives again the preamplifier. At a speed of about 25 cm per nanosecond it would travel for about 400 ns. This means, the signal at 400 ns is a reflection.

7.4 Test Summary

The **Threshold Scanning** shows strong differences for the distribution of extra pulses, which makes it difficult to select a suitable threshold for the pre-trigger operation. Channel 2 and 3 show distributions of extra pulses with large tails, which makes it impossible to find any threshold with 100 % efficiency for a 1 MIP signal and negligible rate of extra pulses. The individual thresholds for each channel must be carefully selected to minimize the resulting fake trigger rate. To minimize the overall fake trigger rate for the front-end box of T0 even in case of fake triggers from individual channels, coincidences of more than one T0 channel could help. However the effect on overall pre-trigger efficiency has to be carefully studied.

The shape of the excess counts versus threshold, which can be unambiguously determined from the **Coincidence Counting**, shows structures for channel 3, that can be attributed to signal reflections.

The **Timestamp Analyzing** shows, that Channel 2 and 3 have a signal at around 100 ns, which comes, according to the T0 group, from ringing of the photomultiplier tube. The T0 group did measurements of the signal, that arrives at the front-end electronics, with an oscilloscope. With the high resolution they could identify the ringing, where the pre-trigger system only sees a single spike.

Channel 2 has a broad distribution of the number of signals after the main signal, which decreases with time. This can be explained by after-pulses, resulting form excited residual gas in photomultiplier tube.

Channel 3 exhibits a strong signal at around 400 ns, which can be identified with a reflection in the cable from the front-end box to the front-end electronics of the T0 detector. Since channel 2 uses a new and channel 3 an old preamplifier, it is suggested to use the new preamplifiers not only in the front-end boxes of V0, but also in the front-end boxes of T0. It would decrease the number of fake pulses in the pre-trigger system and would increase the trigger purity.

As a consequence of these measurements, it was decided to use the new preamplifier for T0.

8 Summary and Outlook

Within this thesis, the software to control and monitor the pre-trigger system of the ALICE TRD was developed. The functions and subroutines to program, configure and retrieve information about the status of the FPGAs in the pre-trigger system are collected in a single software library (*libptrg*), which is used by six servers (PTSS) in three control boxes inside the ALICE L3 magnet.

The programming design of the FPGAs was modified to enable the retrieval of the hardware configuration. The servers developed within this thesis use the DIM network to receive commands and send back information about the initiated actions to one single client (PTFSMD) outside the L3 magnet. For that purpose, the client and the servers exchange data in a dedicated format and the subroutines to prepare and readout these data streams are also collected in the library.

A finite-state machine was implemented on the client level to embed the pre-trigger system in the overall Detector Control System (DCS) of ALICE. In addition, the client provides information about the status and the configuration of the pre-trigger system in XML format. This kind of information is collected for all components of the TRD and is put into a configuration database. The functions to retrieve the configuration and format it into XML are also provided by the *libptrg*. Furthermore, a debugging tool was developed for easy-to-use and fast tracking of potential problems.

The control and monitor system developed during this thesis ensures a reliable operation of the pre-trigger system and provides access to information about the status and the configuration during run-time and for offline-analysis. All information on the status, including the finite-state machine, is transparent and it should be straightforward to implemented into a graphical user interface at the top software level in PVSS [63].

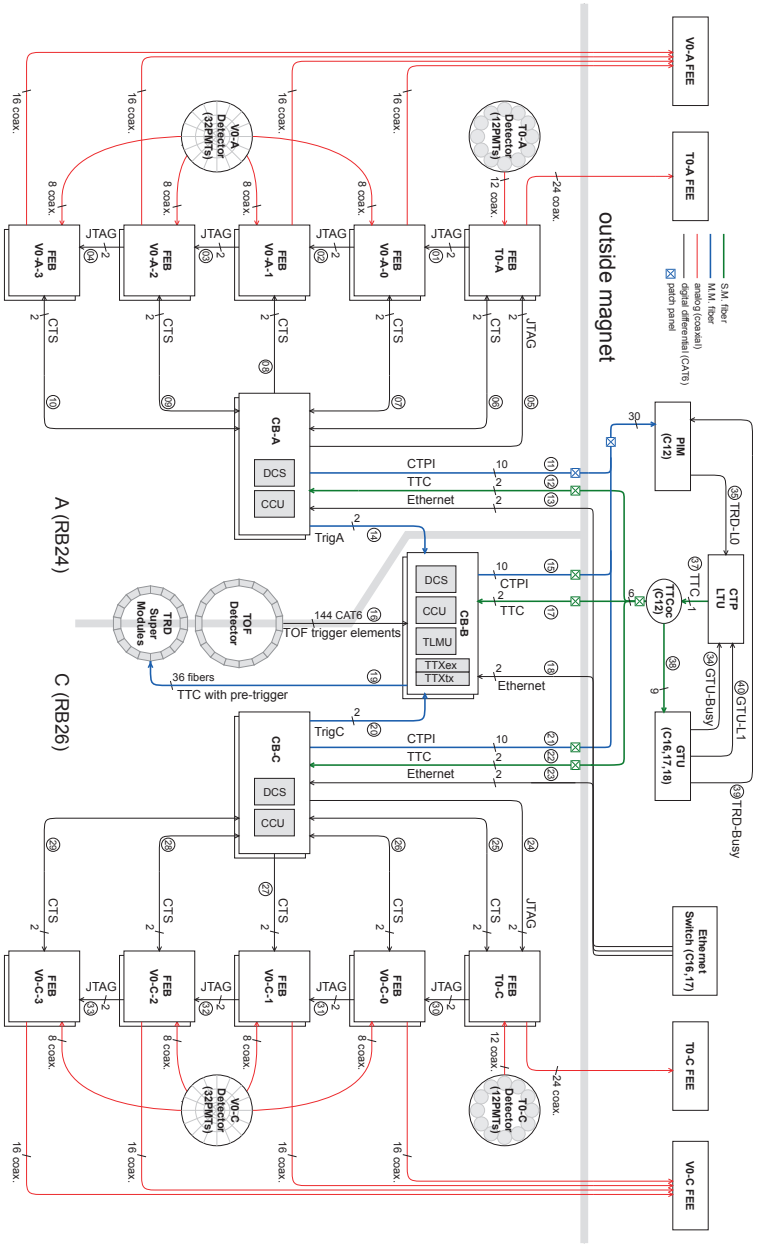
The hardware of the pre-trigger system was significantly extended and completed. The scheme for the power supply of the pre-trigger system on A-side was modified, which simplifies wiring and maintenance. Two new patch panels were designed and installed inside the L3 magnet. During this work, the control box A was moved closer to the patch panels to improve its accessibility. Also, a protective box was designed and installed around the control box. Furthermore, the hardware for the backup system was produced and installed during this thesis.

To ensure the proper operation of the interface between the T0 detector and the pre-trigger system, commissioning tests were carried in June 2009 and their results are presented in this thesis.

In the near future, the LHC will provide the first p+p collisions. The highly flexible configuration of the pre-trigger system allows for providing physics trigger, e.g. on diffractive scattering. This requires detailed knowledge on the underlying background levels. Optimization of trigger efficiencies and background can now be performed with the first proton-proton collisions.

Appendix

A Pre-Trigger System Overview



Schematic overview of the pre-trigger system.

B Lookup Table

Three different lookup tables corresponding to three decision levels are used within the pretrigger system. The table is ordered in ascending decision level from left to right. The input pattern of a lookup table is given as a binary number. The origin of a bit determines its place in the number. The lookup table in five front-end boxes (FEB) contribute each 2 bit to the 10 bit input pattern for the control box lookup table of A, respectively C side. The control boxes themselves contribute four and the TLMU five bit to the input of the lookup table of control box bottom.

Bit of LUT	FEB	CB-A/C	CB-B
0	DET(0)	FEB T0(0)	CBA(0)
1	DET(1)	FEB T0(1)	CBA(1)
2	DET(2)	FEB V0S0(0)	CBA(2)
3	DET(3)	FEB V0S0(1)	CBA(3)
4	DET(4)	FEB V0S1(0)	CBC(0)
5	DET(5)	FEB V0S1(1)	CBC(1)
6	DET(6)	FEB V0S2(0)	CBC(2)
7	DET(7)	FEB V0S2(1)	CBC(3)
8	DET(8)	FEB V0S3(0)	TLMU(0)
9	DET(9)	FEB V0S3(1)	TLMU(1)
10	DET(10)		TLMU(2)
11	DET(11)		TLMU(3)
12			TLMU(4)

Mapping of the input channels to the input bits of the lookup table.

C Power Supply

C.1 Power Supply Units

The following table shows the power supplies in use for the pretrigger system. Each channel of the power supplies is able to deliver 15V with a maximum of 20A. The even numbered power supplies support the control box bottom, the TOF Logic Multiplicity Unit and the front-end boxes in C side, while the uneven numbered the A side. The even power supplies have four channels, the others two.

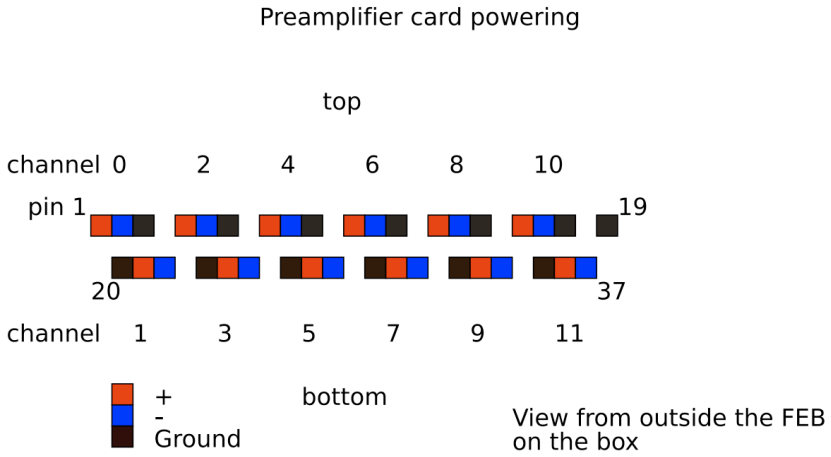
Name	Rack	Voltages	Usage
alidcswie093	O-06	±5V	prim. + back.(FEB-V0-A)
alidcswie094	O-26	±5V,±12V	prim. (CB−B + CB−C + FEB-T0/V0-C) + back.(FEB-V0-C) + TLMU)
alidcswie095	I-06	±5V	prim. + back.(CB−A + FEB-T0)
alidcswie096	I-26	±5V,±12V	back. (CB−B + CB−C + T0-FEB-C)

Power supplies used for the pretrigger system.

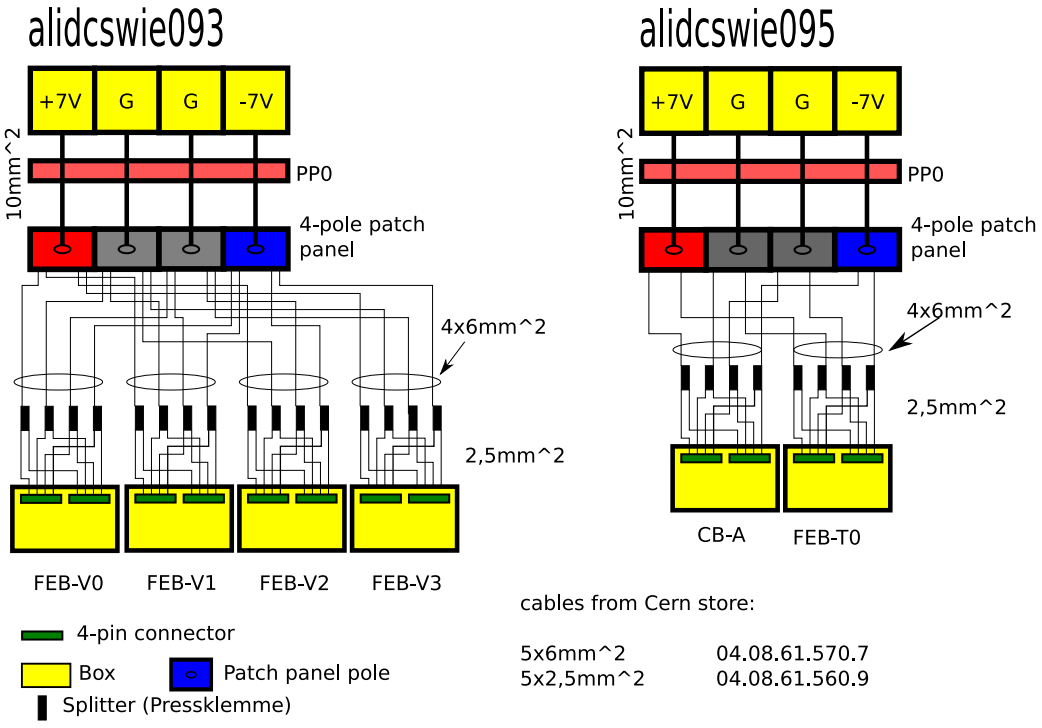
C.2 Power Scheme

More detailed diagrams for the powering scheme of the pre-trigger system. The following three figures show in the following order:

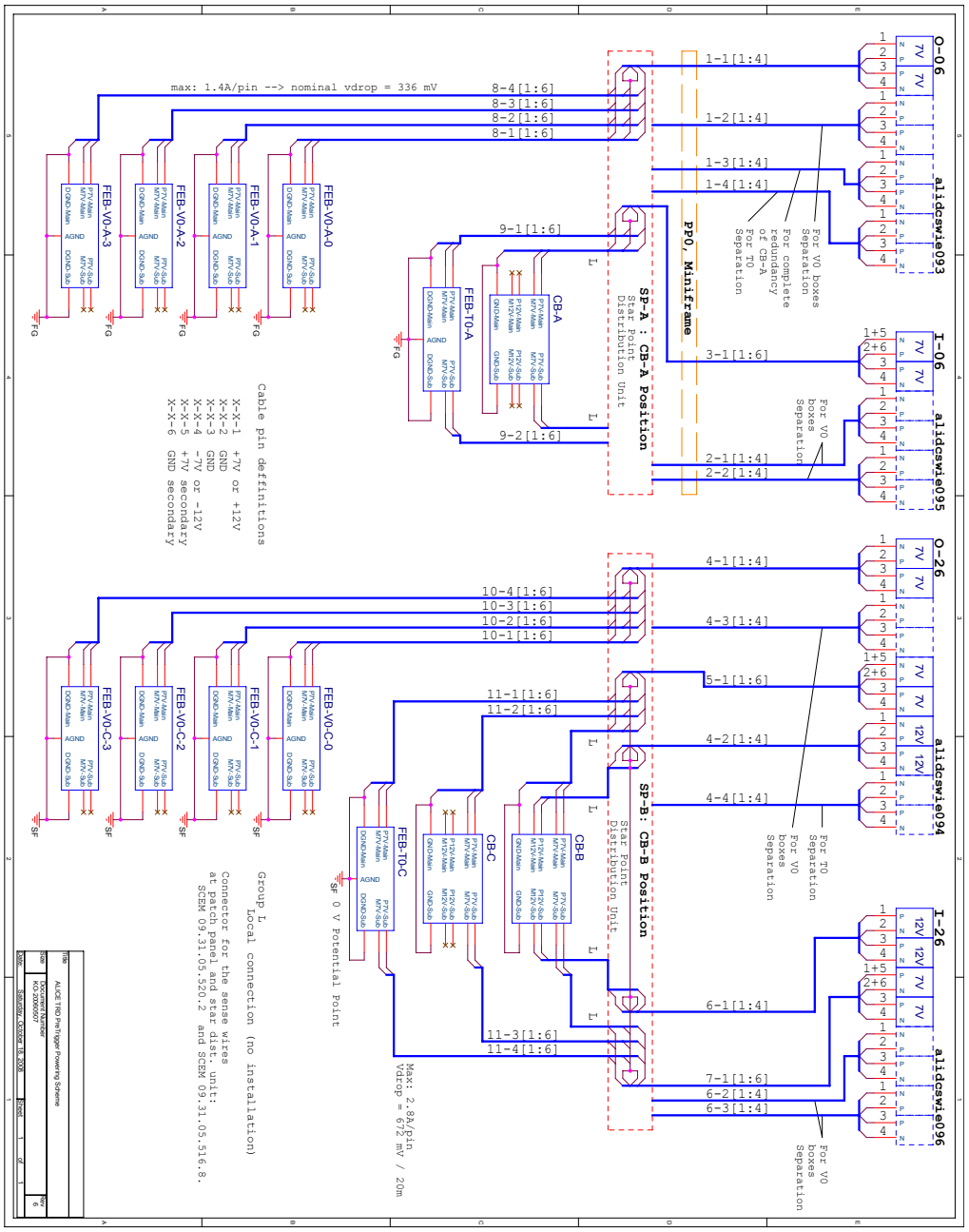
- The pin mapping of the power connector for the preamplifier cards.
- The new low voltage distribution scheme for A-side.
- The low voltage distribution power scheme, which was valid until June 2009. The wiring for the C-side as sketched here, remains untouched.



Pin Mapping for the preamplifier cards.



New power scheme for pretrigger system on A-side.



Former Power scheme until June 2009.

D Pre-Trigger Library

In this section the main definitions of the *libptrg* are listed. More information can be obtained from the code, downloadable from the svn repository of the TRD [53].

D.1 The defined boxes

The boxes in the pre-trigger system are identified with an integer number, which is used for some commands (and of course inside the code).

Pre-Trigger Box	integer number
CB_A_PRIM	10
CB_A_BACK	11
CB_B_PRIM	20
CB_B_BACK	21
CB_C_PRIM	30
CB_C_BACK	31
FEB_T0_A_PRIM	40
FEB_T0_A_BACK	41
FEB_V0_0_A_PRIM	42
FEB_V0_0_A_BACK	43
FEB_V0_1_A_PRIM	44
FEB_V0_1_A_BACK	45
FEB_V0_2_A_PRIM	46
FEB_V0_2_A_BACK	47
FEB_V0_3_A_PRIM	48
FEB_V0_3_A_BACK	49
FEB_T0_C_PRIM	50
FEB_T0_C_BACK	51
FEB_V0_0_C_PRIM	52
FEB_V0_0_C_BACK	53
FEB_V0_1_C_PRIM	54
FEB_V0_1_C_BACK	55
FEB_V0_2_C_PRIM	56
FEB_V0_2_C_BACK	57
FEB_V0_3_C_PRIM	58
FEB_V0_3_C_BACK	59
TLMU	60
CB_INVALID	100

D.2 The command data format between client and server

The client prepares the following C-structs to be sent to the server. The unit words equals 4 bytes.

struct raw_header This header contains information about the data format itself.

- char `hd_marker[8]` is fixed to `PTDAT\0\0\0`.
- signed `short hd_size` is the size in words of this header itself.
- unsigned short `ptdat_ver` contains the Version number (defined in PTDAT_VERSION).
- unsigned short `ptdat_size` holds the total size of the data format including the header.
- unsigned short `reserved3` is not used.
- unsigned short `reserved2` is not used.
- unsigned char `reserved1` is not used.
- unsigned char `target_dcs` holds the targeted box, defined in enum target_box.
- unsigned int `n_commands` holds the number of commands.
- unsigned int `offset_commands` defines the offset to the first command in words.
- unsigned int `n_files` contains the number of files.
- unsigned int `offset_files` defines the offset to the first file in words.
- unsigned int `terminator` should be NULL. Concludes the header.

struct raw_command holds command information.

- `unsigned short cmd` identifies command with an integer number.
- `unsigned short n_arg` holds the number of arguments following directly this struct.

struct raw_file holds binary data information

- `unsigned short type` should be '0' for the moment. Later compressed files are possible.
- `unsigned short tag` is a number that identifies the file. Four files are so far defined in ptssdat.cpp.
- `unsigned int length` is the length of the file in bytes. The data follows directly after this struct.

D.3 The result data format between server and client

The server prepares the results of the received commands with following C-structs.

struct ptss_header is the overall header, containing information about the result data format itself.

- char `ptss_marker[8]` is fixed to `PTSSDAT\0`.
- signed short `header_size` is the size in bytes of this header itself.
- unsigned short `sending_dcs` as defined in enum cb_type.
- unsigned short `n_results` is the number of processed commands.
- unsigned short `sn_success` is the number of successfully executed commands.

- unsigned short `totalsize` is the total size of the result data format.
- unsigned short `offset_to_results` is the offset to the results in words.
- unsigned short `n_rinfo` is number of appending run info structs.
- unsigned short `offset_rinfo` defines the offset to rinfo structs, defined in rinfo.hh.

struct ptss_raw_result holds information about individual results.

- unsigned `short sp_id` contains the process id, or the order in which the commands were received.
- unsigned short `sf_id` associates the result to the command identification number (see table below)
- unsigned short `ssuccess` tell whether the execution was successful or not, 1 means yes and 0 means no.
- unsigned short sn_val is the number of following result values. The associated results follow directly after this struct.

run_info contains only one integer number, which equals the box number defined above. The structs which follow directly after this struct and hold the configuration information of the different boxes, are too large to be shown here. Please refer to rinfo.hh, if more information is needed.

D.4 Command Table for the Pre-Trigger Slim Server

The following table shows the currently defined commands and their arguments as used internally in the code and for the pre-trigger interface class. If you use the pre-trigger injector tool, the syntax is as following:

```
Command Argument1 Argument2 ...
```

Examples:

```
CCWR 33666 1
PXSV /home/trd/dcsnfs/cbb.xsvf 1 0
```

ID	COMMAND	Command Description	# of Args	Arguments	Format	Return Format
1	SCSWR	Write to register via scsn bus	5	devicename deviceport slave register address	string uint16 uint16 uint16	int

				value to write	uint16	
2	SCSRD	Read from register via scsn bus	5	devicename deviceport slave register address returned data	string uint16 uint16 uint16 uint16	int
3	SCSRST	Reset scsn device	3	devicename deviceport slave	string uint16 uint16	int
4	CCWR	Write to register of FPGA	2	register address value	uint16 uint16	int
5	CCRD	Read from FPGA	1	register address	uint16	uint32
6	CCRST	Reset scsn of FPGA	0			int
7	FEBWR	Write to register of selected FEB	2	register address value	uint16 uint16	int
8	FEBRD	Read from FEB	1	register address	uint16	uint32
9	FEBRST	Reset scsn of FEB	0			int
10	CCRM	Read many registers from FPGA	2	start address end address	uint16 uint16	list of uint32
11	FEBRM	Read many registers of FEB	2	start address end address	uint16 uint16	list of uint32
12	FEBS	select FEB	1	FEB #	int16	int

13	PXSV	program FPGA via JTAG	1	filename filetag fileposition	string int int	int
16	JTAS	select JTAG line	1	jtag line	int16	int
17	COUR	Read counters of CC/FEB	2	device(FEB/CC) wished counter	uint16 uint16	uint32

E Acronyms and Technical Terms

ALICE **A** **L**arge **I**on **C**ollider **E**xperiment

ADC Analog-to-Digital Converter

CB Control Box

CB—A Control Box A

CB—B Control Box B

CB—C Control Box C

CTP Central Trigger Processor

CTS Control, Trigger and SCSN

PTM Pretrigger Mainboard

DAQ Data Aquisition

DCS Detector Control System

DCSB Detector Control System Board

DIM Distributed Information Management

ECL Emitter Coupled Logic

ECS Experiment Control System

FEB Front-End Box

FEE Front-End Electronics

FPGA Field-Programmable Gate Array

FSM Finite-State Machine

GTU Global Tracking Unit

HLT High Level Trigger

HMPID High Momentum Particle Identification

ITS Inner Tracking System

JTAG Joint Test Action Group (Protocol to program, debug and test integrated circuits)

LHC Large Hadron Collider

LVDS Low Voltage Differential Signal

MCM Multi Chip Module

PCB Printed Circuit Board

PIM Pretrigger Interface Module

PINJ Pretrigger Injector

PMT Photomultiplier Tube

PTFSMD Pretrigger Finite-State Machine Daemon

PTSS Pretrigger Slim Server

PVSS Prozessvisualisierungs- und Steuerungssystem

QGP Quark Gluon Plasma

RAM Random-Access Memory

ROB Readout-Board

RPC Remote Procedure Call

SCADA Supervisory Control and Data Acquisition

SCSN Slow Control Serial Network

SM Supermodule

SPD Silicon Pixel Detector

SSH Secure Shell

TLMU TOF Logic Multiplicity Unit

TOF Time of Flight

TPC Time Projection Chamber

TRAP Tracklet Processor

TRG Trigger System

TRD Transition Radiation Detector

TTC Timing, Trigger and Control

TTCoc Optical Tree Coupler

VHDL Very High Speed Integrated Circuit Hardware Description Language

XML Extensible Markup Language

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Erklärung

Ich versichere, dass ich diese Arbeit selbständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 01.10.2009 .....

Stefan Schmiederer