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High Resolution Time Measurement

in Pixel Detectors

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Hochauflösende Zeitmessung in Pixeldetektoren

In dieser Arbeit untersuche ich die hochauflösende TDC-Schaltung der Pixeldetektor-Prototypen der im 180nm CMHV7SF-Prozess produzierten Run2021-Serie. Die Schaltung wird erfolgreich in Betrieb genommen. Ein Algorithmus zur Kalibrierung der Schaltung wird präsentiert. Die TDC-Schaltung selbst erreicht eine Zeitauflösung von 100ps. Diese Auflösung kann aufgrund des langsamen Verstärkers im Pixel nicht realisiert werden. Die Zeitauflösung variiert bis zu $\pm 30\%$ zwischen den Pixeln, vermutlich aufgrund von Widerstand in den Versorgungsleitungen. Ein einfaches mathematisches Modell für die TDC-Schaltung wird entwickelt und durch Labormessungen mit Sr90 bestätigt. Die TDC-Schaltung nimmt permanent 10µW auf. Um die Leistungsaufnahme zu verringern wird eine verbesserte Version der TDC entwickelt und in Simulation verifiziert.

Zum Vergleich wird das verbreitete Konzept der Zeitmessung durch Verzögerungskette in Simulation und Literaturanalyse untersucht. Verzögerungsketten sind in den Prozessgrößen 180nm und 130nm nicht konkurrenzfähig aufgrund der hohen Leistungsaufnahme. Es wird erwartet, dass Verzögerungsketten in kleineren Prozessgrößen eine bessere Zeitauflösung bei vergleichbarer Leistungsaufnahme liefern.

High Resolution Time Measurement in Pixel Detectors

In this thesis, I investigate the high resolution TDC circuit implemented in the Run2021 pixel detector prototypes produced in the 180nm CMHV7SF process. The TDC is successfully commissioned. A calibration procedure is presented. The TDC in isolation can achieve a time resolution of 100ps. This resolution can not be realised due to the slow amplifier circuit in the pixel. Observations show pixel-to-pixel variation in time resolution of $\pm 30\%$ around the mean, likely due to supply line resistance. A simple mathematical model for the TDC is created and confirmed by simulation and Sr90 laboratory measurements. The TDC draws 10µW of power permanently. To reduce power consumption, improved versions of the TDC circuit are suggested and verified in simulation.

For comparison, the viability of the commonly used delay chain TDC is investigated in simulation and literature study. The delay chain approach is uncompetitive at 180nm and 130nm due to high power consumption but may yield better time resolution in smaller technologies.

Contents

Chapter 1

Introduction

1.1 Motivation

The quantum state of a particle consists of multiple quantum numbers that are mostly invisible to direct observation. Even state of the art particle detectors can directly measure only spacetime coordinates, energy and charge of a particle.

Given this context, there are two paths towards advancements in particle physics. On one hand, improved accelerators increase the envelope of input states for particle interactions, most famously in terms of energy. On the other hand, improved detectors increase precision, among other things allowing the observation of rare particle interactions.

The Mu3e experiment [1] [2] [3] is a detector experiment following the latter path, using very thin layers of highly integrated silicon pixel detector chips. This way, scattering is reduced, allowing for highly precise resolution of momentum and spacetime position. The first phase of the Mu3e experiment uses the MuPix11 pixel detector [4].

In the course of this thesis, I contribute to a future upgrade of the Mu3e experiment by investigating multiple options of time measuring circuits. I compare laboratory measurements of existing circuits and simulation studies for potential alternatives.

1.2 Goals and Performance Metrics

The *time to digital converter* (TDC) of MuPix11 described in section 1.7.2 allows for a time resolution of half a clock cycle (4ns). The set goal for Mu3e phase 2 is an improved resolution of 100ps [1]. This thesis investigates two different approaches to high precision TDC circuits in multiple variants. The performance of a TDC is evaluated in terms of the following metrics:

- time resolution
- ease and accuracy of calibration
- pixel to pixel (and sensor to sensor) variation
- average power consumption
- peak current draw

The performance of the TDC is measured in isolation. The rest of the readout chain introduces additional sources of imprecision, such as the timewalk effect described in section 1.6.5. These other sources of imprecision are not investigated in this thesis.

1.3 Structure of this Thesis

Chapter 1 introduces the terminology and fundamental relations required for this thesis.

In the Stretched TDC approach a short time interval is stretched proportionally to a longer one. In chapter 2 I evaluate this circuit, comparing laboratory measurements with simulation and a simple algebraic model of the circuit.

In chapter 3 I suggest improved versions of the Stretched TDC circuit underpinned by simulation studies. The suggested variations are compared in their measurement accuracy.

Using a chain of equal delay elements, a time interval can measured by the distance of propagation in the chain. Chapter 4 investigates multiple variants of this approach in simulation studies.

Finally, chapter 5 offers a summary of the findings, giving recommendations for calibration of the existing circuit and estimates for its overall performance. The viability of the alternative circuits investigated in comparison with the existing circuit.

1.4 Particles and Detectors

1.4.1 The Standard Model of Particle Physics

The Standard Model of modern particle physics describes particles as the discrete excitations of fields in spacetime. The internal structure of the quantum fields corresponds to the discrete properties of the particles, such as charge, weak isospin, flavour and colour charge.

A fundamental particle can only have specific discrete values for each of those quantum numbers. In contrast, the possible values for spacetime position and momentum can assume any continuous value.

1.4.2 Detectors

In a detector, typically the following quantities of a detected particle can and should be measured: Position and momentum in three dimensions, time of arrival, energy and charge. The goal of a detector is to measure one or more of these quantities as precisely as possible.

Detector Design Goals

Time and position of a particle are straightforward to measure. The directionality of momentum can be obtained by combining multiple measured positions in the flight path in a process called tracking. Most complicated is measuring energy, as the relation between particle energy and detector signal is usually not straightforward.

Time measurements can in principle be used to calculate the velocity. However, in many cases the particles move close to the speed of light, yielding a time of flight below the measurable precision. In this case, the time measurement can still be used to aid tracking, distinguishing between particles. If the species of particle (and therefore its mass) is already identified, there is one redundant degree of freedom, which can be used to improve accuracy of the tracking processes.

Pixel Detectors

Pixel detectors consist of thin layers of silicon *application specific integrated circuit* (ASIC) chips. They yield excellent spatial resolution, corresponding to the size of the pixels. Time resolution can be very good as well, since small scale silicon electronics are quite fast. Electric charge separation from ionisation is a measure for energy, the precision however is typically worse than in designated calorimeters.

Whilst the TDC circuits investigated in this thesis can be used in various applications, the optimisations made are targeted specifically at highly integrated pixel detectors.

1.5 HVMAPS

High Voltage Monolithic Active Pixel Sensors (HVMAPS) [5] are a recent development in silicon detectors. They combine the precision, efficiency and convenience of integrated electronics with the ability to create high voltage (HV) diodes for the purpose of efficiently detecting ionising radiation.

1.5.1 The Mu3e Experiment

The Mu3e experiment searches for lepton flavour violating decay modes

$$\mu^+ \longrightarrow e^+e^-e^+.$$

Mu3e searches for this reaction down to a branching ratio of 10^{-16} [1]. A particle interaction in this range implies physics beyond the standard model, as the only currently known mechanism for such a decay is neutrino oscillation, at an unmeasurable branching ratio below 10^{-50} [6]. To measure a significant number of events at such a low branching ratio, a high luminosity beam is required.

Figure 1.1 shows neutrino oscillation and one candidate process using an additional neutral boson. The decay $\mu^+ \longrightarrow e^+e^-e^+$ needs to be distinguished from similar signals, caused by other decay modes and coincidental events due to the high beam rate.

The dominating background processes involve the weak interaction Michel decay [7] [8]. Figure 1.2 shows two such processes. Unlike a proper $\mu^+ \longrightarrow e^+e^-e^+$ reaction, background processes either produce additional neutrinos or do not actually originate from a common vertex.

Almost all coincidental events are filtered out by filtering for energy-momentum and a common vertex. As coincidental events are spread over the phase space, only a negligible amount of them has both a common vertex and the correct energy-momentum sum. This phase space volume is limited by each of the 8 components of energy-momentum and spacetime. Each component on its own filters out background events, proportional to the precision of its measurement.

This is an important motivation for high precision time measurement. Timing precision directly suppresses the experimental background.

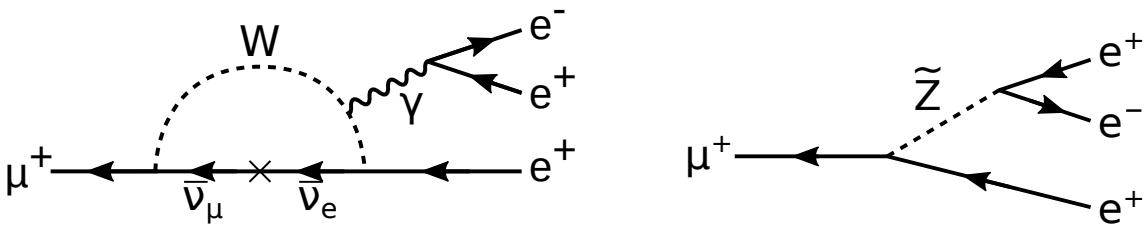


Figure 1.1: Feynman diagrams for $\mu^+ \longrightarrow e^+e^-e^+$ processes. *left*: neutrino oscillation. *right*: Flavour violating neutral boson as an example for a process beyond the standard model [9]

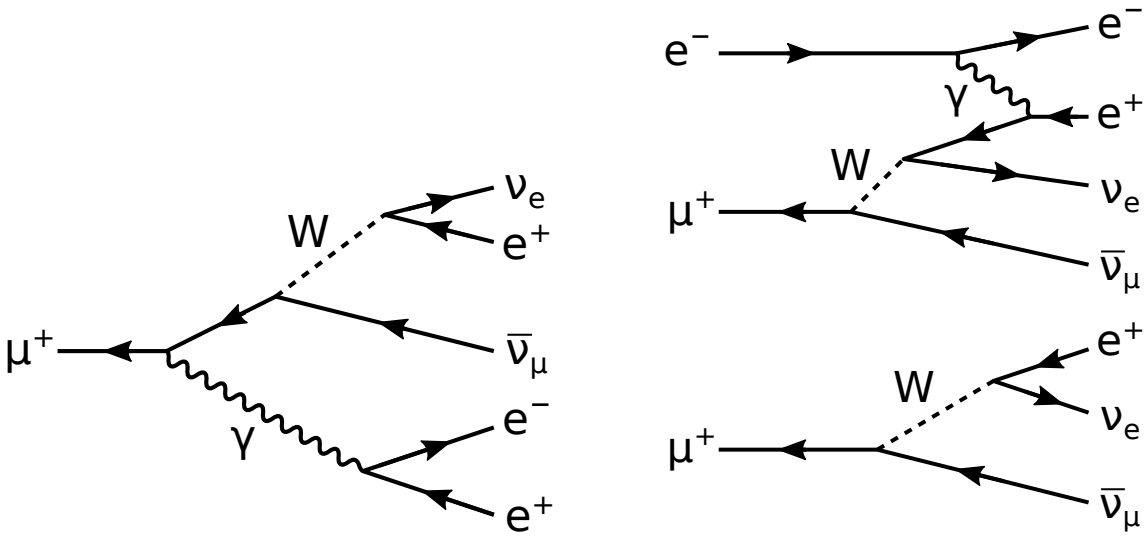


Figure 1.2: Feynman diagrams for background processes mimicking $\mu^+ \longrightarrow e^+e^-e^+$. *left*: Michel decay plus pair production. *right*: Two Michel decays plus ionisation via Bhabha scattering

1.5.2 MuPix

The MuPix [10] series of HVMAPS chips was developed for Mu3e, catering specifically to the needs of the experiment. The current iteration, MuPix11, will be used in the first stage of Mu3e.

Each electron and positron produced in a $\mu^+ \longrightarrow e^+e^-e^+$ reaction has a comparatively low energy $E < \frac{m_\mu}{2} \approx 53MeV$. At this energy, the momentum resolution is limited by scattering. To minimise scattering and maximise momentum resolution, the chips are thinned to 50µm.

To achieve a high efficiency, a reliably high sensor signal needs to be achieved. This conflicts with thin chips, as less charge is collected. To compensate, a high voltage above 100V is applied, enlarging the depletion zone (see chapter 1.6.1).

1.5.3 Run2021 Engineering Prototypes

Run2021 [11] is a set of engineering prototypes for further development of pixel sensors. They test improved circuits intended to be used in Mu3e stage 2 and other experiments. The laboratory measurements described in this thesis have been carried out on the Run2021V2 chip.

Run2021V2 features a matrix of 29×124 pixels, with long pixels of pitch $165\mu m \times 25\mu m$. The distinguishing feature of variant V2 is a CMOS amplifier.

1.6 Pixel Electronics

Modern particle detectors consist of a combination of analog sensor electronics and digital readout circuits. In this section I give a brief overview of design conventions and terminology used within this thesis.

For the purposes of this thesis, a single pixel cells consists of 5 modules processing the signal of an incoming particle. First, the particle generates free charge carriers in the sensor diode. Second, the signal given by the charge is amplified and shaped using analog electronics. Third, the analog signal is digitised using a comparator. Fourth, a signal above threshold for a sufficiently long time is detected as a hit. Last, the time of the signal is measured by synchronising with the detector's clock signal.

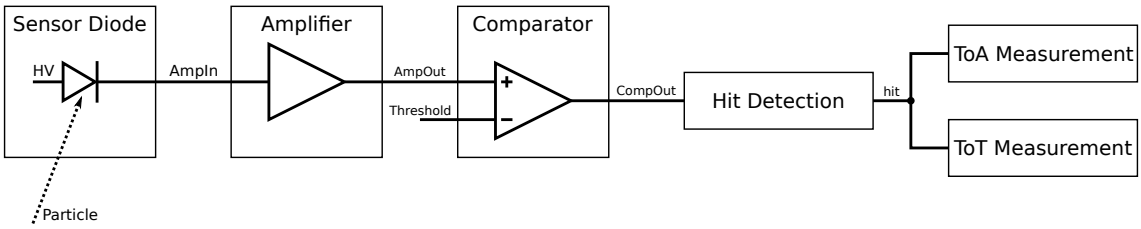


Figure 1.3: structure of a pixel: components relevant to this thesis.

1.6.1 Detector Diode

The core component of a silicon detector is the photodiode. On a junction between n-doped and p-doped substrate a depletion zone is formed, in which are no free charge carriers. Applying a high voltage in blocking direction of the diode increases the size of this zone significantly.

If an energetic particle passes through the depleted silicon, a large amount of electron-hole pairs are separated, on average one pair per 3.6eV deposited in the material [12, p. 24]. This results in free charge carriers which are following the *high voltage* (HV) electric field. The deposited energy therefore can be measured quite precisely by measuring the generated charge carriers.

1.6.2 Amplifier

The signal coming out of the sensor diode is rather small, typically consisting of a few thousand electrons. It therefore is amplified by an amplifier circuit. MuPix and Run2021 use a *charge sensitive amplifier* (CSA) [4].

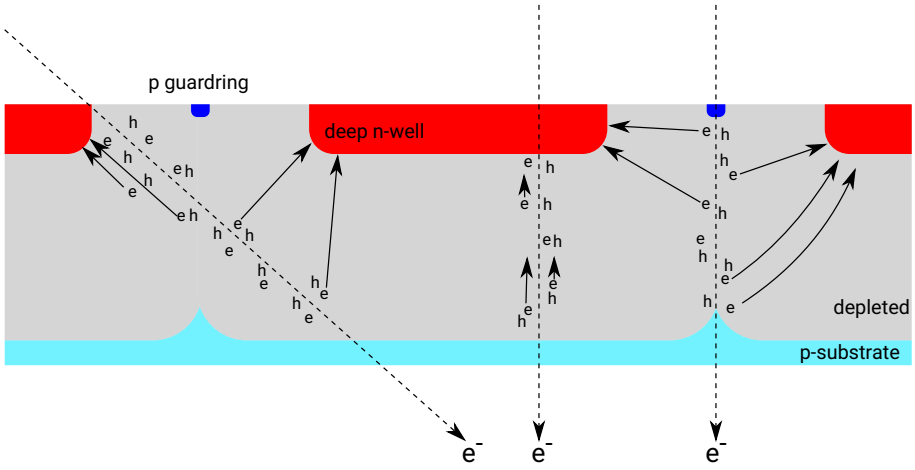


Figure 1.4: Pixel sensor cross section: Charge deposition in silicon by ionising particles and drift of charge carriers to the n-well encapsulating the pixel. Graphic used with permission of Heiko Augustin [9].

1.6.3 Comparator

Using a comparator (compare section 1.8.11), the amplifier output is compared with a fixed threshold in order to discriminate actual hits from random electronic noise. A higher threshold yields lower noise rate but also a reduction in detection efficiency.

1.6.4 Hit Detection

A positive flank at the output of the comparator is detected by a flank detection circuit. If a flank is detected, the *hit* signal is set.

1.6.5 Time Measurement

In the pixel, two time measurements are done: *Time of Arrival* (ToA) and *Time over Threshold* (ToT).

Time of Arrival

The ToA is the time of the ionising particle crossing the pixel layer. It is measured at the rising flank of the hit signal. As stated in section 1.5.1, vertex reconstruction requires a highly precise measurement for the ToA.

Time over Threshold

The ToT is the time interval between the positive and negative flank of the comparator output. It is a measure for the deposited charge, which relates to the energy of the particle via the energy dependent [13] ionisation rate $\frac{dE}{dx}$.

Timewalk Effect and Timewalk Correction

The ToA is measured as the comparator threshold is crossed. There is a delay between the signal at the amplifier input and the threshold being crossed. This delay is called timewalk. As seen in figure 1.5, timewalk is not constant. As the rising flank of the amplifier output is sharper if more charge is deposited, ToA correlates with deposited charge. This limits the accuracy of time measurements.

By using the measured ToT, the timewalk effect can be corrected for [14, p.37]. This requires the measured correlation of ToT and ToA obtained with an external time measurement.

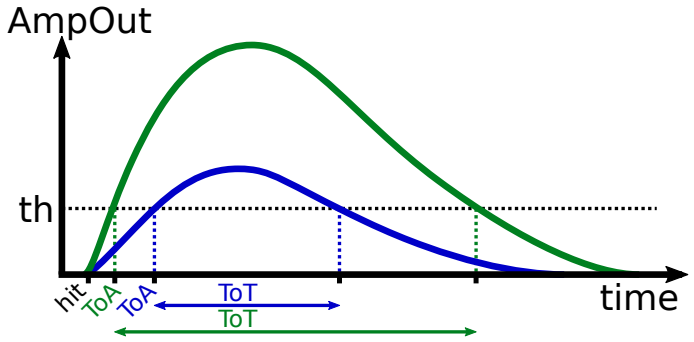


Figure 1.5: Sketch: Timewalk effect. Two hits at the same time but of different magnitude have a different measured ToA. The timewalk is the difference $\Delta = ToA - T_{hit}$. Both ToT and timewalk scale with signal magnitude.

1.7 Time to Digital Conversion

In this thesis, multiple variants of high resolution TDC circuits are compared. This section gives a brief overview of existing and newly developed TDC circuits.

1.7.1 Clock Sampling

The most trivial TDC is a digital counter counting up with each clock cycle. This yields a time resolution of one clock cycle. MuPix11 has an internal clock of 125GHz, corresponding to a clock cycle of 8ns. The clock is sampled in a Gray Counter [15]. The Gray Counter flips only a single bit on each clock edge, ensuring that the value sampled is never off by more than one.

1.7.2 Two Phase TDC

The time resolution can be improved by a factor of 2 using two Gray counters. One counter increments on the rising, the other on the falling clock edge. If the counters are equal, the ToA is in the first half of the clock cycle, otherwise in the second half.

This is the circuit used in MuPix11, achieving a resolution of 4ns. The TDCs investigated in this thesis offer an improvement in time resolution over this existing circuit.

1.7.3 Stretched TDC

When using a constant current I to charge a capacitance C, the voltage U behaves as described in equation 1.9. Starting at $U = 0$,

$$U(t) = \frac{Q(t)}{C} = \frac{1}{C} \int I dt = \frac{I}{C} t. \tag{1.1}$$

Therefore, U and t are proportional. This way, the time t can be measured with the same number of digits as the voltage using an ADC.

Instead of using a conventional ADC, the Stretched TDC [16] circuit introduced in chapter 2 uses this relation twice. First the time information is transformed into analog voltage using a constant $\frac{I_1}{C}$. Then the voltage is transformed back into a larger time interval using a smaller constant $\frac{I_2}{C}$. The result is a large time interval

$$t' = \frac{I_1}{I_2} t, \tag{1.2}$$

which can be measured by sampling the system clock.

The Stretched TDC circuit is implemented on the Run2021 engineering prototypes. It is investigated in chapter 2 of this thesis, comparing laboratory measurements and simulation.

1.7.4 Delay Chain TDC

A time interval can be transformed into a discrete spatial position using a chain of equal delay units. The beginning of the interval is marked by a flank at the input of the delay chain. At the end of the interval, the position of the signal in the chain is read out. This position is proportional to the initial time interval. The simplest feasible delay element is an inverter (see section 1.8.7). This circuit is referred to as delay chain TDC.

More realistically, instead of a long chain a circular structure is used in order to save space. This setup is called a Ring Oscillator. The number of revolutions is tracked using a counter. This ring oscillator TDC is quite common, as is quite simple to design and to calibrate. As literature suggests, the cost of this approach lies in high power consumption [17] or small structure size requirement [18] [19].

The delay chain TDC is investigated in chapter 4 of this thesis using simulation. The simulation studies focus on the linear circuit, as the only advantage of the ring oscillator is space preservation.

1.8 Electronic Components and Circuits

This section gives a brief overview of electronic components and related equations used in this thesis. A few simple circuits are presented, forming the building blocks for the TDC circuits investigated.

1.8.1 Analog and Digital Circuits

Digital electronic circuits are characterised by discrete voltage (sometimes current) levels a signal can obtain. Analog circuitry is characterised by a lack of such discretisation.

Analog electronics allow for a more detailed manipulation of physical signals. On the other hand, as there is some tolerance in the logic levels of a digital circuit, they do not deteriorate and are resilient to errors. This means, the best approach to readout electronics is to immediately use analog circuits for signal shaping and then digitise the signal as soon as feasible.

Digitisation must happen in a way that is resilient in regards to small changes in the analog signal. Two common digitisation methods are comparators and analog to digital converters (ADCs). For the rest of this thesis, the discrete binary states in the digital circuits are denoted as 0 and 1.

1.8.2 Synchronous and Asynchronous Digital Circuits

Synchronous electronic circuits are characterised by discrete time intervals, typically given by a clock signal. A synchronous signal changes only as the clock flank hits. Asynchronous circuits are characterised by a lack of such discretisation in time.

Similar to the difference between digital and analog circuits, asynchronous circuits allow for more detailed manipulation of signal timing whilst synchronous circuits are resilient to errors. Once again, the best approach is to immediately do asynchronous signal manipulation and then synchronise the signal as soon as feasible.

There is a potential for metastable states if the edge of the asynchronous signal hits just before the clock signal. A case of such a metastable state is observed in section 2.7.2.

1.8.3 Fundamental Relations

By the continuity equation

$$\dot{Q} = \boldsymbol{\nabla} \cdot j, \tag{1.3}$$

the net current flowing into a node is the derivative of the accumulated charge,

$$I = \dot{Q} \tag{1.4}$$

The voltage U between two points in space is the potential difference of the electric field. It relates to the potential energy W of a charge Q,

$$U = \frac{W}{Q} \tag{1.5}$$

In the context of electronic circuits, it is convenient to reformulate this as power consumption. Assuming constant supply voltage,

$$P = \dot{W} = U\dot{Q} = UI \tag{1.6}$$

1.8.4 Capacitance

The core components in both TDCs investigated are current drivers and capacitances. The precise nature of the Stretched TDC circuit requires a good understanding of the properties of non ideal capacitors.

The capacitance of an electronic component is typically defined as

$$C \coloneqq \frac{Q}{U}. \tag{1.7}$$

The resulting relation between current and voltage on a capacitor is a first order differential equation,

$$U(t) = \frac{Q(t)}{C} \tag{1.8}$$

$$\dot{U} = \frac{\dot{Q}}{C} = \frac{I}{C} \tag{1.9}$$

In many cases, the capacitance is constant. The transistors observed in this thesis however have a nonconstant capacitance $C = C(U)$ through some of their operational range. For example, the capacitor used in the Stretched TDC circuit is implemented as a PMOS transistor (see for example circuit diagram 2.2). The capacitance of a transistor depends on the channel geometry. It changes with applied voltage. The relation of U and I becomes nonlinear,

$$I = \frac{dQ}{dt} = \frac{d\left(CU\right)}{dt} = C\frac{dU}{dt} + U\frac{dC}{dU}\frac{dU}{dt} = \frac{dU}{dt}\left(C + U\frac{dC}{dU}\right) \tag{1.10}$$

$$\dot{U} = \frac{I}{\left(C + U\frac{dC}{dU}\right)} = \frac{1}{1 + \frac{U}{C}\frac{dC}{dU}}\frac{I}{C} \tag{1.11}$$

In case that $\frac{dC}{dU} = 0$, the correction term equals 1, yielding equation 1.8. Otherwise, depending on the sign of the term $\frac{dC}{dU}$, the charging rate may increase or decrease compared to the idealised case. Using the differential capacitance

$$C_d \coloneqq \frac{dQ}{dU}, \tag{1.12}$$

the differential equation simplifies directly to

$$I = \frac{dQ}{dt} = \frac{dQ}{dU}\frac{dU}{dt} = C_d\dot{U}. \tag{1.13}$$

As this mirrors the structure of equation 1.8, the differential capacitance is the more convenient generalisation in most cases. A more thorough discussion of the two definitions can be seen in [20].

The capacitance between two circuit nodes depends on geometry and isolating material permittivity ε. Between two ideal parallel flat conductor surfaces of area A with spacing d,

$$C = \varepsilon\frac{A}{d} \tag{1.14}$$

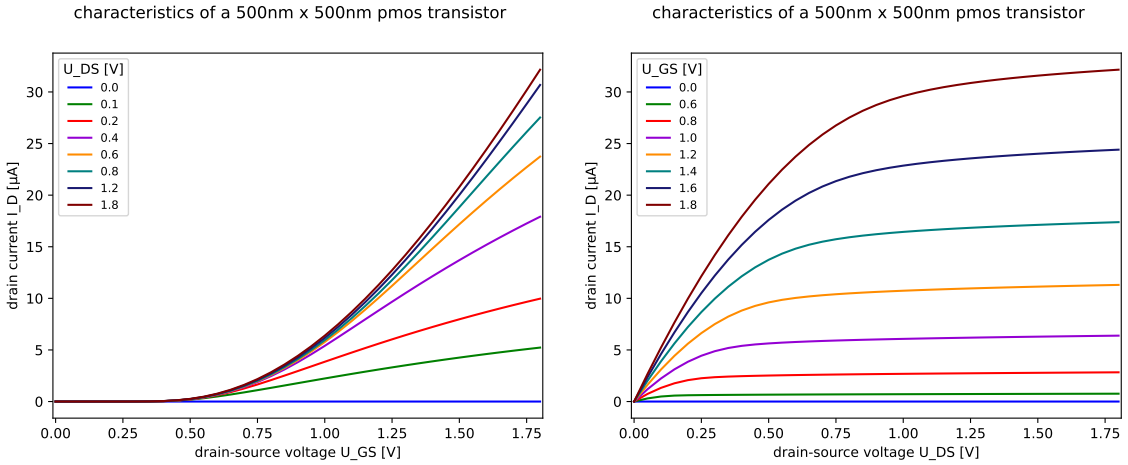
1.8.5 Transistor Characteristics

In this thesis, *Metal Oxide Semiconductor* (MOS) transistors make up the majority of electronic components. According to [21, section 4.2] at sufficiently high gate voltage $U_{GS} > U_{th}$, the drain current is

$$I_D = \kappa \frac{w}{l} \left[(U_{GS} - U_{th}) U_{DS} - \frac{1}{2} U_{DS}^2 \right] \qquad for \;\; U_{DS} < U_{GS} - U_{th} \tag{1.15}$$

$$I_D = \frac{\kappa}{2} \frac{w}{l} (U_{GS} - U_{th})^2 (1 + \lambda U_{DS}) \qquad for \;\; U_{DS} > U_{GS} - U_{th} \tag{1.16}$$

Here, w and l are the length and width of the transistor's active area and $\lambda \sim \frac{1}{l}$. The parameters κ and U_{th} are technology dependent constants.



(a) drain current dependence on U_{GS}

(b) drain current dependence on U_{DS}

Figure 1.6: DC simulation: current of a 500nm × 500nm PMOS transistor in CMHV7SF

Notably, κ is smaller by a factor of approximately 3 for PMOS transistors compared to NMOS transistors [21, p. 23]. This disbalance means that there is always a tradeoff between maximum speed and symmetry of rising and falling flanks.

At sufficiently high U_{DS} the transistor is in saturatuion (case 1.16). The current levels off, allowing the transistor to function as a voltage independent current source. The slight U_{DS} dependence is called *Early Effect* [21, p. 116]. Longer transistors are better current sources, as the Early effect is weaker.

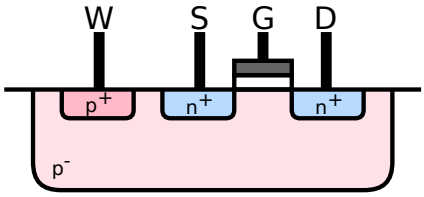


Figure 1.7: Sketch: Cross section of NMOS transistor with pwell contact

Figure 1.8: symbol for NMOS (*left*) and PMOS (*right*). Well contacts are omitted as they are connected to GND / VDD.

1.8.6 Current Mirror

This function of a MOS transistor as a current source can be used to create current mirrors. A current mirror is a circuit that copies, multiplies and divides a current.

Figure 1.9 shows the circuit diagram of a current mirror. By construction both transistors have the same gate-source voltage. This means, at sufficiently high drain-source voltage on the output side the output current is equal to the input current.

The Stretched TDC circuit uses current mirrors as current sources. Many of the nonlinearities observed in chapter 2 are caused by the imperfect nature of the current mirror circuits.

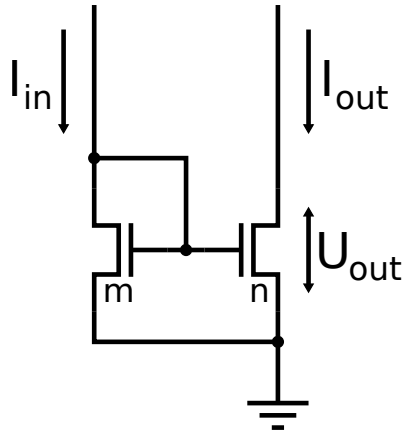
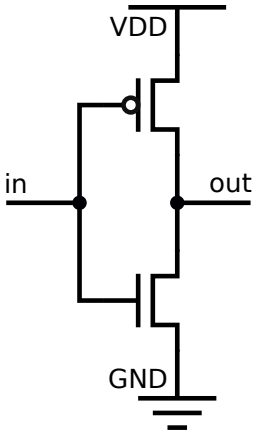


Figure 1.9: NMOS current mirror. Using m transistors on input side and n transistors on output side yields $I_{out} = \frac{n}{m} I_{in}$



in	out
0	1
1	0

Figure 1.10: Inverter circuit. *left*: circuit diagram. *right*: logic table

1.8.7 Inverter

An inverter is a circuit setting its output to a logical 0 if the input is 1 and to 1 if the input is 0. It can be constructed using an NMOS and a PMOS transistor (figure 1.10). If the input is low, the PMOS conducts, pulling the output to VDD. If the input is high, the NMOS conducts, pulling the output to GND. A real inverter has a delay caused by parasitic capacitance.

1.8.8 Transmission Gate

A transmission gate is an electronically controlled switch built from an NMOS and a PMOS transistor. If the transmit signal is set to 1, current can flow through the transmission gate in either direction, otherwise current cannot flow.

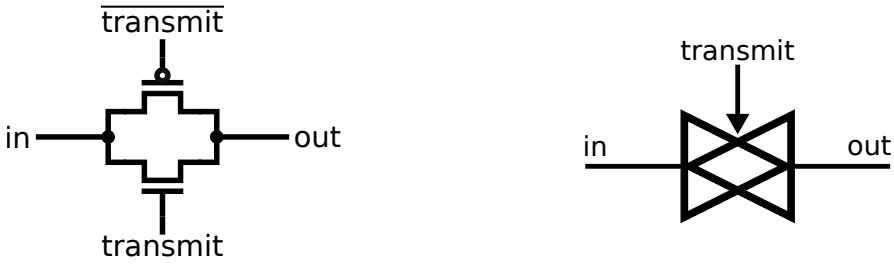


Figure 1.11: Transmission gate. *left*: circuit diagram. *right*: component symbol

1.8.9 Latch

A latch is a circuit which stores a digital signal. If the load signal is 1, the internal state is set to the input signal, otherwise the internal state is maintained. In the delay chain TDC, shown in figure, latches are used to control signal propagation. The latch circuit used in this application is shown in figure 4.3.

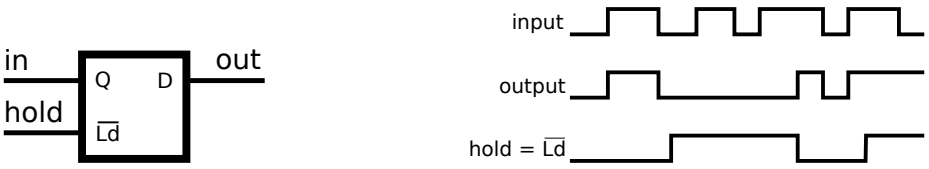


Figure 1.12: Latch circuit. *left*: component symbol. Q and D are commonly used to denote data input and output. The Ld (load) or equivalently hold signal decides whether the signal is stored or not. *right*: input response time diagram.

1.8.10 Flipflop

A flipflop is a circuit which stores the state of its digital input signal on the edge of a clock signal, sampling its state at this specific point in time.

A simple flipflop circuit can be constructed from two Latches (figure 1.13). The load signal of the first latch is active before the clock edge, so that it retains its input after the clock has switched. At this point, the load signal of the second flipflop is active, so that it propagates the stored signal.

The Stretched TDC circuit uses a flipflop in this configuration to synchronise the hit signal with the clock.

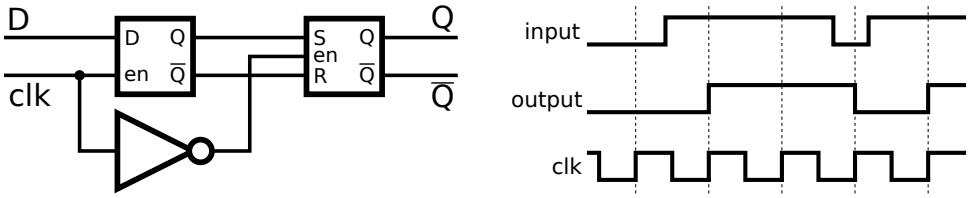


Figure 1.13: D-flipflop triggered on rising clock edge. *left*: implementation in master-slave configuration using two latches. *right*: input response time diagram

1.8.11 Comparator

A comparator is a circuit which compares two analog input signals giving a digital output signal. If the first signal is higher, the output is set to a digital 1, otherwise to 0. The circuit diagram for the comparator used in the Stretched TDC circuit is shown in figure 2.36.

A comparator is used in the Stretched TDC circuit. The time of crossing a predefined threshold is used as the measure for precise timing.

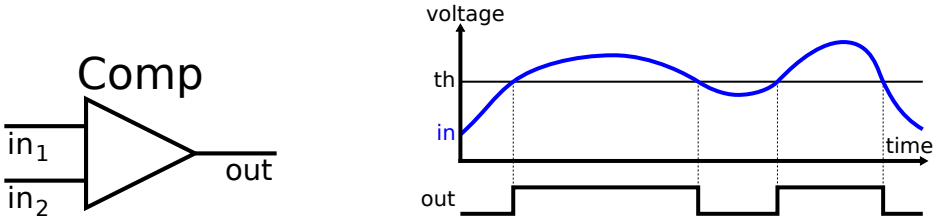


Figure 1.14: Comparator circuit. *left*: component symbol. *right*: comparator output for a constant threshold $in_2 = U_{th}$

1.9 Manufacturing Processes

The integrated circuits measured and simulated in this thesis are designed in the processes CMHV7SF and SG13G2. The produced specimen of MuPix11 [4] and Run2021 [11] are manufactured in CMHV7SF, whilst some new research prototypes like BeBiPix [22] are produced in SG13G2.

1.9.1 CMHV7SF Process

Both MuPix and Run2021 chips are produced in the 180nm IBM CMHV7SF process [23] by TSI foundry [24]. The process features deep n-wells, allowing for high voltage application in areas isolated from sensitive low voltage electronics. The transistors support a supply voltage of 1.8V.

The focus of this thesis is on CMHV7SF, encompassing simulations done in chapters 2, 3 and 4 as well as the laboratory measurements on the Run2021V2 chip.

1.9.2 SG13G2 Process

The SG13G2 process by IHP [25] is a 130nm BiCMOS process with a SiGe substrate. The standard transistors support 1.2V supply voltage with IO-transistors up to 3.3V. The BeBiPix prototype has been produced in SG13G2, using a bipolar transistor for the signal amplifier in the pixel.

As stated in section 1.6.5, the resolution of the TDC is not always the limiting factor for the resolution of the whole pixel. In MuPix11 and the Run2021 chips, the time resolution is in fact limited by the amplifier. A fast amplifier enabled by SG13G2 could harness the full resolution of the TDC. Section 4.5 shows a simulation study on delay chains in SG13G2.

1.10 Measurement Setup and Tools

This section gives a short overview of the software and hardware used to obtain the data discussed in this thesis.

1.10.1 Laboratory Setup

Statistical measurements are obtained using an Sr90 β-radiation source. The Run2021V2 chip is read out using the common MuPix readout chain [14, p. 30]. Figure 1.15 gives an overview of the components involved.

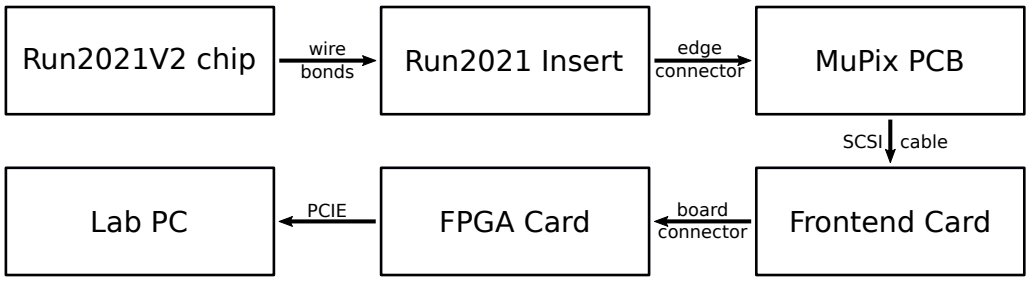


Figure 1.15: Readout chain for Sr90 laboratory measurements on Run2021V2

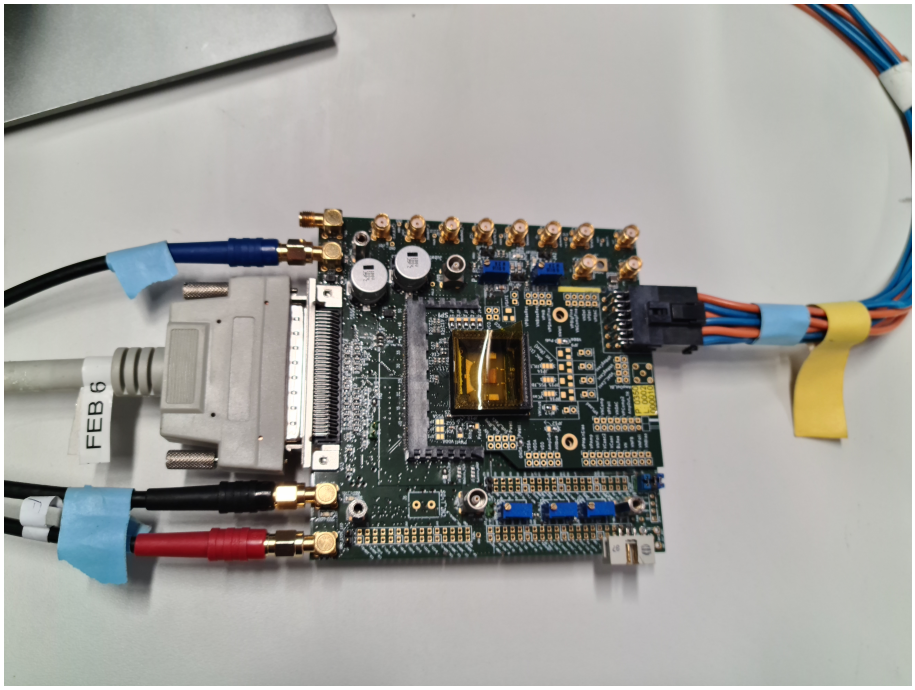


Figure 1.16: Photo of lab setup: MuPix motherboard, Run2021 Insert and Run2021V2 chip. The chip is protected with a black plastic frame. Power is externally supplied on the right. Data is read out using the white SCSI cable on the left.

1.10.2 Simulation Environment

The simulation studies done in this thesis are performed in Cadence Virtuoso [26] using the Spectre simulator and the OCEAN script language. For both CMHV7SF and SG13G2 detailed transistor models are available. Three simulation modes are used:

1. DC simulation: The equations of the components are solved for a stationary solution.
2. AC simulation: The response of the components to an infinitesimal sinusoidal stimulus is calculated.
3. transient simulation: The time dependent dynamics of the circuit are simulated.

Simulation studies are used to investigate not yet manufactured circuit designs and to supplement laboratory data of produced circuits. This is done whenever the statistical data obtained in the laboratory are showing secondary effects that cannot be measured directly.

Chapter 2

Stretched TDC

This chapter is about the Stretched TDC circuit, a fully analog approach to precise time measurement. Three paths are taken in parallel, in order to understand the circuit: A simple algebraic model for the circuit, results from circuit simulation and statistical data taken with produced specimen of the Run2021V2 pixel detector.

Section 2.1 gives an overview of the Stretched TDC circuit, including a mathematical model of the circuit. In section 2.2, The TDC is commissioned, confirming correct functionality and presenting a calibration algorithm. Sections 2.3 and 2.4 measure the charging current and investigate the linearity of the circuit, yielding an upper limit to the usable voltage range. An upper limit for the current DAC settings is determined in section 2.5. Section 2.6 verifies the model developed in section 2.1 in a parametric study.

Each of these measurements shows deviations from the linear model. In section 2.7, these deviations are analysed by investigating the components of the Stretched TDC circuit in isolation. For each component, an improved model is developed, explaining the laboratory data. The simulations done in section 2.7 hint at a nonlinearity at high current DAC settings. This nonlinearity is investigated further in section 2.8.

2.1 Stretched TDC Circuit

This section presents the Stretched TDC circuit and simple algebraic models to describe it. In addition to the previously existing timestamp TS1 coming from sampling the clock (compare section 1.7.2), the Stretched TDC circuit introduces an additional timestamp TS3. The precise reconstruction of input time is introduced in section 2.1.5. It revolves around the difference

$$\delta \coloneqq \mathrm{TS3} - \mathrm{TS1} \tag{2.1}$$

and its distribution over many hits. The distribution is expected to be a rectangular block, parametrised by its edges δ_{min} and δ_{max}. These parameter directly relate to the circuit's physical characteristics.

2.1.1 Stretched TDC Working Principle

The Stretched TDC circuit uses the linear relation 1.1

$$U = \frac{I}{C}t \tag{2.2}$$

of time and voltage when charging a capacitor with a constant current. Instead of using a conventional ADC to measure the voltage, this relation can be used a second time. A different

current is used to project the voltage in equation 2.2 back into time domain and sample it using the system clock.

To do this, after the initial charging process is complete, a different current continues to charge the capacitance until a set threshold voltage is crossed, as seen in figure 2.1. The time of crossing the threshold is registered as the additional timestamp TS3. This approach is simple and efficient both in component and current requirement.

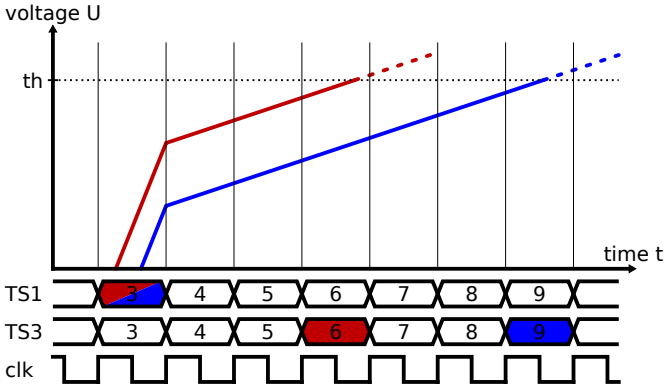


Figure 2.1: Sketch: TS3 resolving the time of arrival with sub clock cycle precision

2.1.2 Implementation of the Stretched TDC Circuit

Figure 2.2 shows the Stretched TDC circuit. It operates as follows:

1. in rest state, both pulldown NMOS and transmission gate conduct
2. once the hit signal switches to active, the pulldown is disabled
3. from this point, both PMOS current drivers charge the capacitor
4. on the rising clock edge, the flipflop propagates the hit signal, disabling the transmission gate
5. from this point, only the I_Small driver charges the capacitor
6. once the capacitor voltage crosses the threshold set in the comparator, the timestamp TS3 is registered

There are four parameters, which can be configured using the on-chip DACs. The current drivers are set using VP_Big and VP_Small. The comparator threshold is set using TH_Fine. The comparator operating point is defined by a current set by VN_Comp. The comparator circuit diagram is shown in figure 2.36.

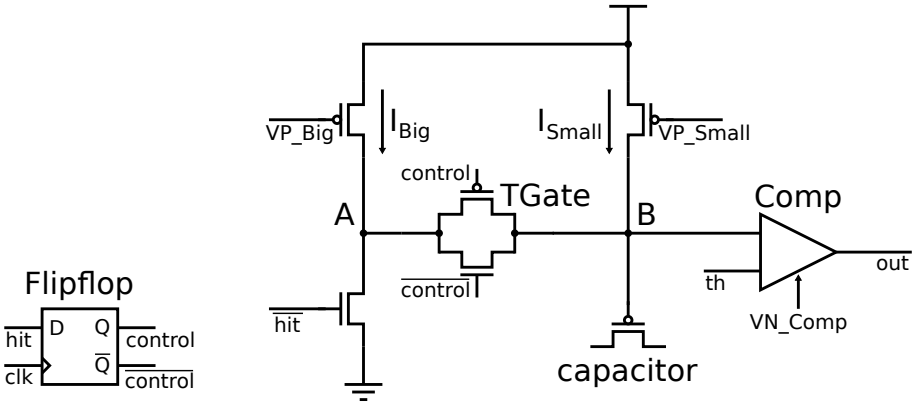


Figure 2.2: Stretched TDC circuit diagram

2.1.3 Stretched TDC Analysis

Figure 2.3 sketches the slopes of the charging curve in the Stretched TDC circuit. The charging rates before and after the clock edge relate to the time of hit and the threshold voltage.

$$s_A = \frac{U_C}{T_{clk} - T_{hit}} \tag{2.3}$$

$$s_B = \frac{U_{th} - U_C}{T_3 - T_{clk}} \tag{2.4}$$

$$\Rightarrow U_C = s_A \left(T_{clk} - T_{hit}\right) \tag{2.5}$$

The measure for determining precise timing is the difference δ between the timestamps $\mathrm{TS1}$ and $\mathrm{TS3}$.

$$\delta := \mathrm{TS3} - \mathrm{TS1} \equiv T_3 - T_{clk} = \frac{U_{th} - U_C}{s_B} \tag{2.6}$$

$$\boxed{\delta = \frac{U_{th}}{s_B} - \frac{s_A}{s_B}\left(T_{clk} - T_{hit}\right)} \tag{2.7}$$

This is a linear relation between δ and T_{hit}. For randomly distributed values of T_{hit}, the resulting distribution has the shape of a rectangular block, discussed further in section 2.1.5.

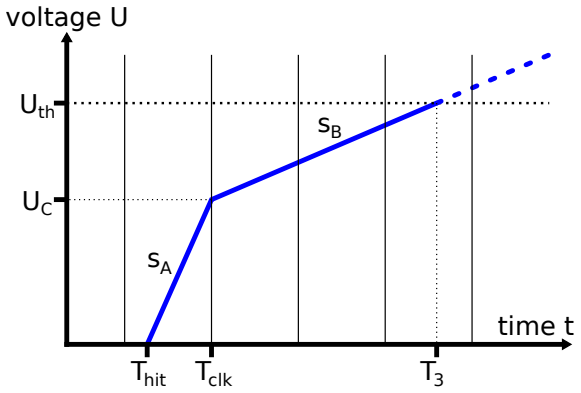


Figure 2.3: Sketch: charging curve and slope $s := \dot{U}$

Based on this equation for δ, the distribution parameters δ_{min} and δ_{max} can be calculated. The earliest hit in the clock period follows

$$T_{hit} = T_{clk} - T \tag{2.8}$$

$$\Rightarrow \boxed{\delta_{min} = \frac{U_{th}}{s_B} - \frac{s_A}{s_B} T} \tag{2.9}$$

For the latest hit,

$$T_{hit} = T_{clk} \tag{2.10}$$

$$\Rightarrow \boxed{\delta_{max} = \frac{U_{th}}{s_B}} \tag{2.11}$$

This yields for the width of the distribution:

$$\boxed{w = \frac{s_A}{s_B} T} \tag{2.12}$$

Next, express δ, δ_{max} and w in terms of the physical circuit parameters. The slopes correspond to a charging rate $\frac{dU}{dt}$:

$$s := \frac{dU}{dt} = \frac{d}{dt}\frac{Q}{C} = \frac{I}{C} \tag{2.13}$$

$$s_A = \frac{I_{Small} + I_{Big}}{C} \tag{2.14}$$

$$s_B = \frac{I_{Small}}{C} \tag{2.15}$$

For δ, δ_{max} and w, this yields

$$\delta = \frac{U_{th} C}{I_{Small}} - \left(1 + \frac{I_{Big}}{I_{Small}}\right)(T_{clk} - T_{hit}) \tag{2.16}$$

$$\boxed{\delta_{max} = \frac{U_{th}}{s_B} = \frac{U_{th} C}{I_{Small}}} \tag{2.17}$$

$$\frac{w}{T} = \frac{s_A}{s_B} = \frac{I_{Small} + I_{Big}}{I_{Small}} = 1 + \frac{I_{Big}}{I_{Small}} \tag{2.18}$$

$$\boxed{\frac{w}{T} = 1 + \frac{I_{Big}}{I_{Small}} \approx \frac{I_{Big}}{I_{Small}}} \tag{2.19}$$

This means, w can be set by only adjusting the two current drivers. The capacitance and the threshold voltage only influence the readout time δ_{max}.

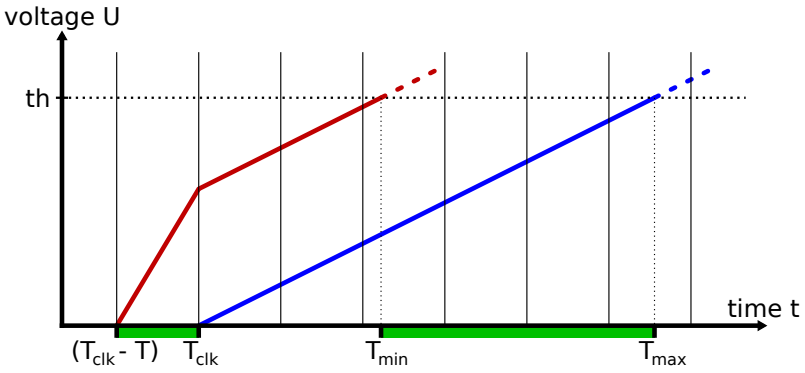


Figure 2.4: Sketch: projection of a clock cycle

2.1.4 Premature Threshold Case

If VP_Big is chosen too high for a given threshold, the threshold will be crossed before the clock edge. Figure 2.5 shows, how the values for TS3 will be distributed. Only part of the clock cycle is magnified whilst hits early in the clock cycle observe no magnification. This is highly undesirable, as it leads to silent miscalibration errors. To avoid this issue, TH_Fine needs to be chosen sufficiently high, or equivalently VP_Big sufficiently low.

The earliest possible hit in a clock cycle arrives at $T_{clk} - T$, crossing the threshold at T_x. The latest hit with the premature threshold issue arrives at $(T_{clk} - T) + (T_{clk} - T_x)$, crossing the threshold at T_{clk}. The unknown T_x can be eliminated using the slope equation:

$$s_A = \frac{U_{th}}{T_x - (T_{clk} - T)} \tag{2.20}$$

$$\Rightarrow T_x = (T_{clk} - T) + \frac{U_{th}}{s_A} \tag{2.21}$$

The ratio of hits with premature threshold issue is

$$\xi := \frac{(T_{clk} - T_x)}{T} \tag{2.22}$$

$$= \frac{T - \frac{U_{th}}{s_A}}{T} \tag{2.23}$$

$$= 1 - \frac{U_{th}C}{(I_{Big} + I_{Small})T} \tag{2.24}$$

The ratio reaches $\xi = 0$ as

$$\frac{U_{th}C}{(I_{Big} + I_{Small})T} = 1 \tag{2.25}$$

$$U_{th} = \frac{(I_{Big} + I_{Small})T}{C} \tag{2.26}$$

This poses two equivalent conditions to avoid the premature threshold issue:

$$U_{th} > \frac{(I_{Big} + I_{Small})T}{C} \tag{2.27}$$

$$I_{Big} < \frac{U_{th}C}{T} - I_{Small} \tag{2.28}$$

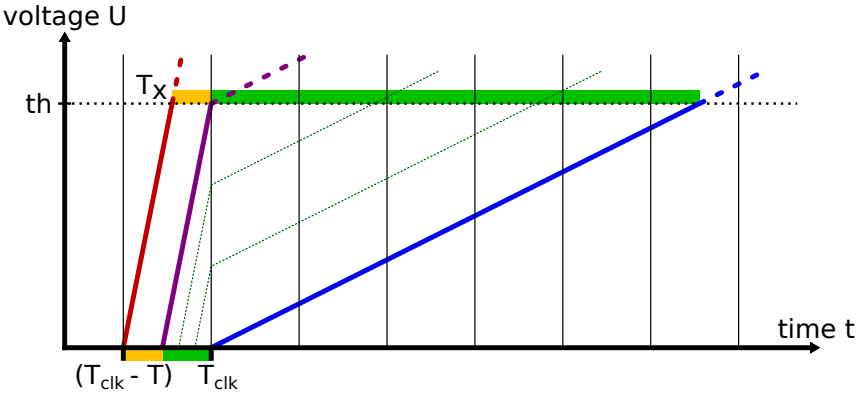


Figure 2.5: Sketch: premature threshold crossing

2.1.5 Time Reconstruction

As suggested by sketch 2.4, the Stretched TDC circuit stretches out a single clock cycle over multiple clock cycles. The probability density of δ can be calculated using equation 2.7,

$$\rho(\delta) = \rho(T_{hit}(\delta)) \left| \frac{dT_{hit}(\delta)}{d\delta} \right| \tag{2.29}$$

$$= \frac{1}{T} \cdot \frac{s_B}{s_A} = \frac{T}{w} = const. \tag{2.30}$$

$\mathrm{TS3}$ is sampled with the system clock and therefore has the same binning resolution as $\mathrm{TS1}$. This means, the resolution of t_{fine} is increased by the magnification factor

$$\boxed{\eta := \frac{d\delta}{dT_{hit}} = \frac{w}{T}}. \tag{2.31}$$

Since the magnification factor η is equal to the distribution width w in terms of bins of size T, the terms will be used interchangeably for the rest of this chapter.

As the density 2.29 is constant, the distribution of δ over many hits is a rectangular block distribution sketched in figure 2.6. This distribution can be obtained using a randomised source, such as radiation. As the relation of T_{hit} and δ is linear, the original time of hit within the clock cycle can be calculated by linear interpolation:

$$t_{fine} = \frac{\delta - \delta_{min}}{w} T \tag{2.32}$$

The reconstructed time then is

$$t = \mathrm{TS1} \cdot T + t_{fine} \tag{2.33}$$

$$\boxed{t = \left(\mathrm{TS1} + \frac{\delta - \delta_{min}}{w} \right) T}. \tag{2.34}$$

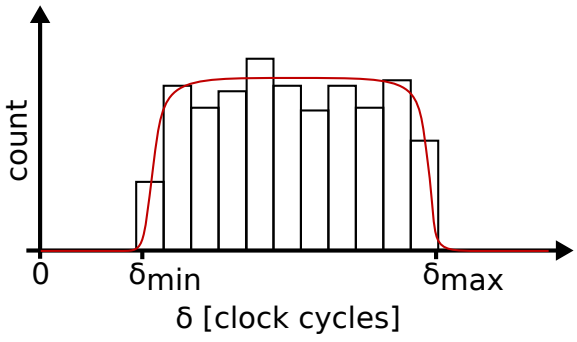


Figure 2.6: Sketch: Expected distribution of δ

2.1.6 Circuit Invariants

The only observable in produced specimen of the Stretched TDC circuit is the timestamp TS3 and thereby δ. Since equation 2.16 is invariant under the transformation

$$I_{Big} \mapsto \alpha I_{Big} \tag{2.35}$$

$$I_{Small} \mapsto \alpha I_{Small} \tag{2.36}$$

$$C \mapsto \alpha C, \tag{2.37}$$

the absolute value of neither quantity can be deduced from δ. Only the ratios of the quantities can be measured, for example by using the relations 2.17 and 2.19:

$$\frac{C}{I_{Small}} = \frac{\delta_{max}}{U_{th}} \tag{2.38}$$

$$\frac{I_{Big}}{I_{Small}} = \frac{w}{T} - 1 \tag{2.39}$$

2.1.7 Tradeoffs

The Stretched TDC approach achieves a good time resolution with a low amount of components and relatively low power consumption. In return, readout is slow, as reading out a single hit takes at least δ_{max}. Since $\eta = \frac{w}{T} < \frac{\delta_{max}}{T}$, the magnification is strictly bounded by readout time. The achievable time resolution of the TDC $\tau = \frac{T}{\eta}$ therefore is inversely proportional with readout time, as shown in figure 2.7. Since the calibration procedure requires fitting a distinct rectangular block, the realistic limit given the 7bit timestamp is a magnification of $\eta = 80$.

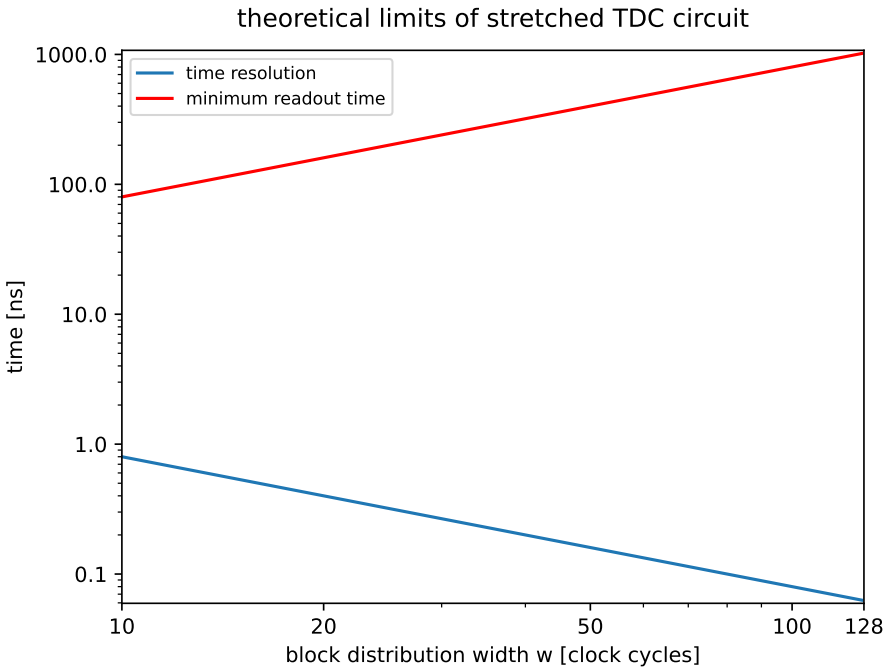


Figure 2.7: Theoretical limits for Stretched TDC performance. In practice, pixel-to-pixel variation demands some buffer in readout time to ensure correct operation in every pixel.

2.2 Functional Verification and Calibration

This section verifies the functionality of the Stretched TDC circuit and demonstrates the calibration procedure implied by equation 2.33. The key challenge is to reliably determine δ_{min} and δ_{max} from the observed distribution of δ.

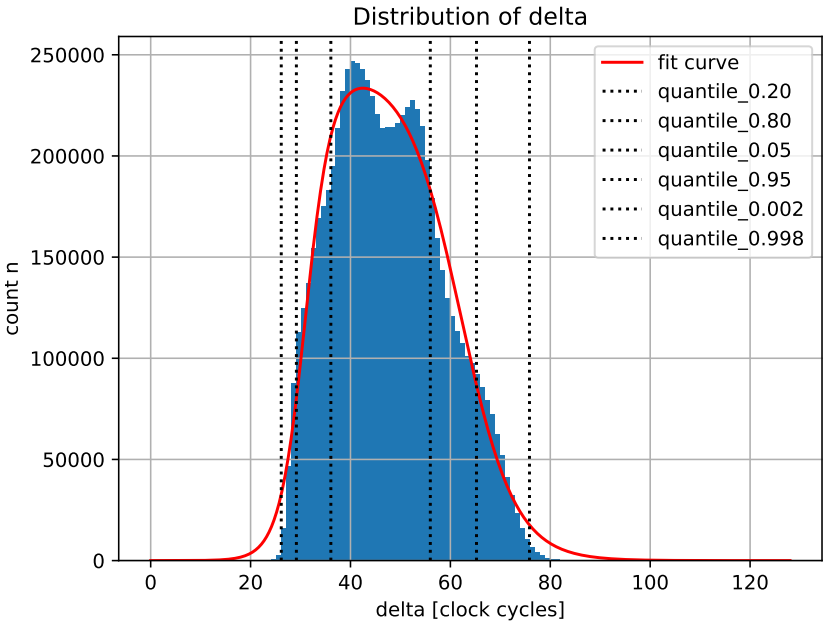


Figure 2.8: Sr90 measurement: Distribution of δ for all hits in all pixels

2.2.1 Functional Verification

If the Stretched TDC circuit works correctly, it produces a block shaped distribution of δ as calculated in section 2.1.3. Figure 2.8 shows the distribution of δ of all hits in all pixels, obtained in the laboratory using an Sr90 source. This distribution does not resemble a rectangular block. In contrast, figure 2.9 shows the distribution for a single pixel. This distribution very much looks like the expected rectangular block.

Therefore, using a shared calibration and reconstruction of the ToA for all pixels can be ruled out categorically. Instead, each pixel has to be calibrated individually. This entails a time resolution which varies between pixels.

The all-pixel distribution is the sum of the distributions of the individual pixels. Its shape reflects the distribution of the physical circuit parameters. The double peak structure reflects to the bimodal parameter distribution observed in section 2.4.3.

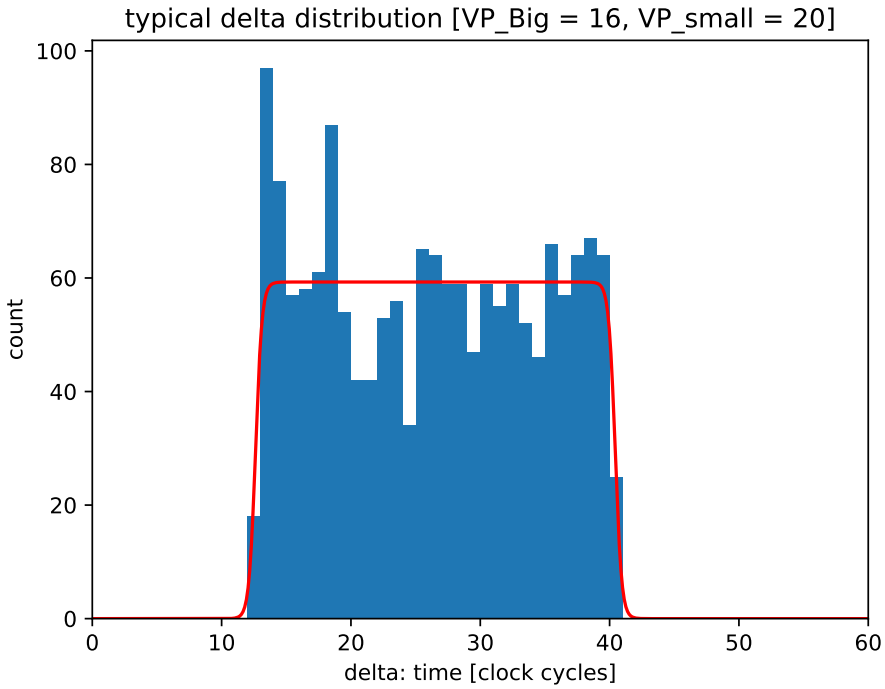


Figure 2.9: Sr90 measurement: Typical distribution of δ for a single pixel

2.2.2 Calibration Algorithm

The calibration of the time measurement is done using randomised hits. Sr90 is one such randomised source. In-place calibration in an assembled detector can be done with beam data.

The following calibration procedure has to be applied after every reconfiguration of the DACs. As temperature changes may shift the working point of the circuit, occasional recalibration is advised for long running experiments.

1. measure timestamps $\mathrm{TS1}$ and $tsthree$ for a lot of randomised hits
2. create a histogram of $\delta := \mathrm{TS3} - \mathrm{TS1}$ for each pixel
3. fit a block function to each histogram $n(\delta)$
4. obtain fit parameters δ_{min}, δ_{max} and $w = \delta_{max} - \delta_{min}$
5. for each hit reconstruct time as $t = \left(\mathrm{TS1} + \frac{\delta - \delta_{min}}{w}\right) T$
6. the time magnification is $\eta = \frac{w}{T}$, the resolution $\tau = \frac{T}{\eta}$

Since the timestamp TS3 has size 7bit, modular arithmetic is required for both fit function and time reconstruction. If, for example, $\delta_{max} < \delta_{min}$, the correct block width would be $w = 128 + \delta_{max} - \delta_{min}$ rather than the negative value.

Fitting the block distribution is not straightforward. The process is described in the following sections.

2.2.3 Block Function

For numerical reasons, it is more convenient to fit a smooth function rather than a discontinuous rectangular block. The block function is constructed from two sigmoid functions:

$$block(x; A, B, l, r, s_l, s_r) \coloneqq B + A \cdot sig\left(x; l, \frac{s_l}{A}\right) \cdot sig\left(x; r, -\frac{s_r}{A}\right), \tag{2.40}$$

$$sig(x; c, s) \coloneqq \frac{1}{1 + \exp\left(-4s(x - c)\right)} \tag{2.41}$$

There are 6 free parameters to fit the distribution of δ. Whilst in principle all can be obtained by fitting, there are physical relations between the parameters which can be used to constrain the equation or at least obtain an initial guess.

Leaving all 6 parameters free leads to overfitting issues. Figure 2.10 shows such an overfit in laboratory data. To avoid this issue, the slope parameters s_l and s_r are constrained. The edges of the distribution are expected to be sharp, such that the histogram steps from 0 hits per bin outside the block to A hits per bin in the block. This sharp step corresponds to an increment of A from one bin to the next. The resulting slopes are

$$s_l = s_r = A. \tag{2.42}$$

The block function therefore simplifies to

$$block_{simple}(x; A, B, l, r) \coloneqq B + A \cdot sig\left(x; l, 1\right) \cdot sig\left(x; r, -1\right). \tag{2.43}$$

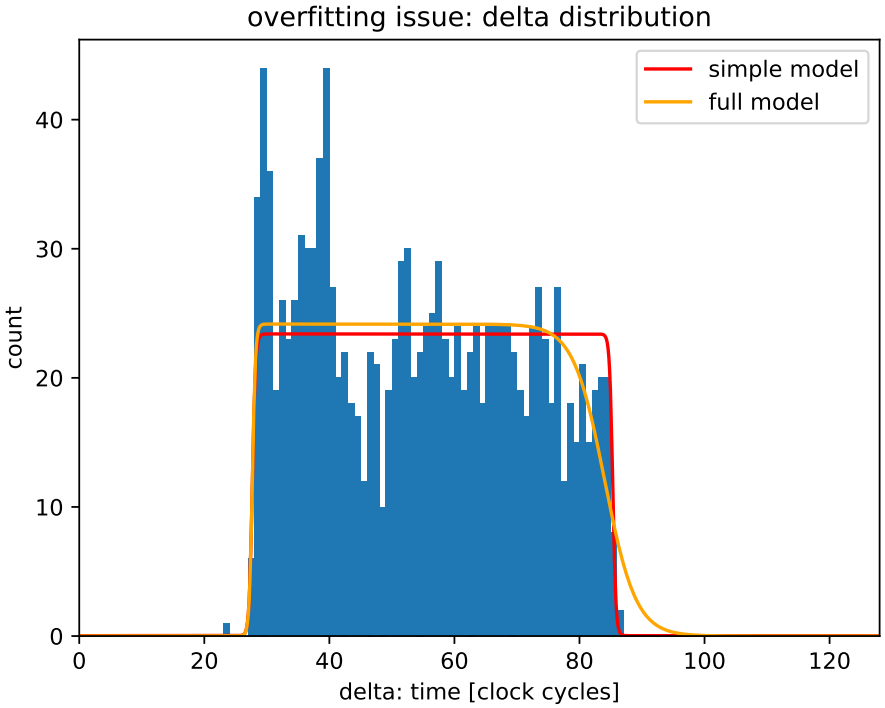


Figure 2.10: Sr90 measurement: Example of overfitting δ-distribution

Finally, the fit function needs to be compatible with the cyclical nature of the 7bit finite algebra. The block function must support blocks wrapping around and cannot have an unsteady point. This is ensured by centering the finite domain at the center m of the block distribution:

$$w \coloneqq mod_{128}(r - l) \tag{2.44}$$

$$m \coloneqq mod_{128}\left(l + \frac{w}{2}\right) \tag{2.45}$$

$$\tilde{x} \coloneqq mod_{128}(x - m + 64) \tag{2.46}$$

$$block_{wrap}(x; A, B, l, r) \coloneqq B + A \cdot sig\left(\tilde{x}; 64 - \frac{w}{2}, 1\right) \cdot sig\left(\tilde{x}; 64 + \frac{w}{2}, -1\right) \tag{2.47}$$

Figure 2.11 shows an example for this wraparound case.

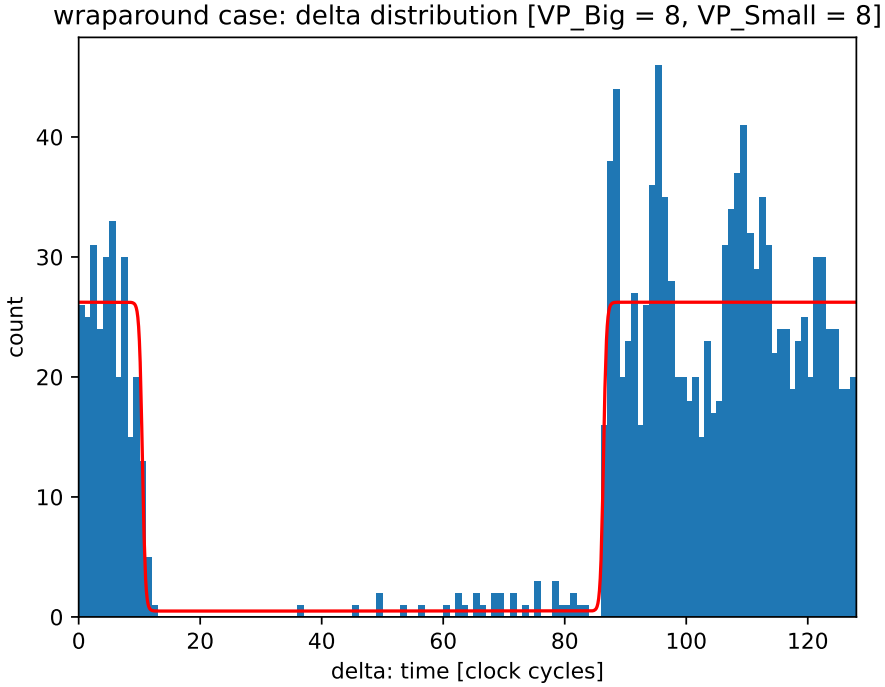


Figure 2.11: Sr90 measurement: Distribution of δ wrapping around.

2.2.4 Block Fit Result

The fit returns the optimal values for the four parameters A, B, l and r. The amplitude parameter corresponds to the probability density $A \equiv N\rho_\delta$. The baseline parameter B measures the amount of timestamps outside the rectangular block, ideally equalling 0. The edge positions are the parameters required for time reconstruction, $l \equiv \delta_{min}$ and $r \equiv \delta_{max}$.

As seen in figure 2.11, timestamps outside the block actually are observed. Investigations show that the cause for these faulty timestamps is most likely a faulty Gray counter readout circuit. Resolving this issue is a high priority for future iterations of the TDC.

2.2.5 Initial Parameter Guess

To ensure reliable calibration for millions of pixels without human oversight, the initial guess for the fit function must be chosen close to the expected result. This section discusses a strategy for choosing good initial value given an experimentally measured distribution $n(\delta), \delta \in 0...127$.

With N hits making up the histogram, the integral over the distribution needs to equal N:

$$N = (r - l) \cdot A + 128 \cdot B \tag{2.48}$$

If the circuit works correctly, all hits have $\delta \in [r, l]$ such that

$$B = 0, \tag{2.49}$$

$$N = (r - l) \cdot A. \tag{2.50}$$

If the block distribution wraps around, as seen for example in figure 2.11, the straightforward calculation of the mean using

$$\tilde{m} = \frac{1}{N} \sum_{\delta=0}^{127} \delta n(\delta) \tag{2.51}$$

does not match the actual center of the wrapping block. Instead, find the position $m \in 0...127$ minimising the symmetic variance σ^2:

$$m \coloneqq \underset{\mu \in 0...127}{\operatorname{argmin}} \ \sigma^2(m), \tag{2.52}$$

$$\sigma^2(\mu) \coloneqq \frac{1}{N} \sum_{\delta=-64}^{63} \delta^2 \cdot n(mod_{128}(\delta - \mu)) \tag{2.53}$$

The variance σ^2 of a block distribution relates to the block width w via

$$\sigma^2 = \int_{-\frac{w}{2}}^{\frac{w}{2}} \frac{1}{w} x^2 dx = \frac{1}{12} w^2 \tag{2.54}$$

$$\Rightarrow w = \sqrt{12\sigma^2}. \tag{2.55}$$

Using 2.44 and 2.45, the initial guess for the edges l and r of the block distribution can be determined from m and w.

To summarise, the initial guess for the fit parameters is

$$l = mod_{128}\left(m - \frac{w}{2}\right) \tag{2.56}$$

$$r = mod_{128}(l + w) \tag{2.57}$$

$$A = \frac{N}{w} \tag{2.58}$$

$$B = 0 \tag{2.59}$$

2.3 Current Draw Measurement

As observed in section 2.1.6, by measuring the output distribution of timestamps, the ratios $\frac{I_{Big}}{I_{Small}}$ and $\frac{C}{I_{Small}}$ can be obtained but no absolute values for I_{Big}, I_{Small} or C. By measuring the overall current draw of the chip and its relation with the DAC settings for VP_Big and VP_Small, such an absolute value can be obtained. The caveat is that this is only an average value and ignores pixel-to-pixel variation.

2.3.1 Expected Current Behaviour

When idle, the TDC circuit draws a constant current

$$I_{idle} = I_{Big} + I_{Small} + I_{Comp}. \tag{2.60}$$

When the hit signal is active, the pulldown NMOS transistor is deactivated, making I_{Big} and I_{Small} charge the capacitance C. This corresponds to a fixed amount of charge (or energy) over the readout time, resulting in a negligible power draw while active. The time average currents are therefore expected to be lower while the chip is irradiated. Assuming a constant readout time t_{ro} and hit rate r per pixel, the current is approximately

$$I_{irradiated} \approx (1 - rt_{ro})\,(I_{Big} + I_{Small}) + I_{Comp} < I_{idle}. \tag{2.61}$$

2.3.2 Measured Current Draw

Figure 2.13 shows the measured current draw for the three current drivers. Both VP_Small and VN_Comp drivers are highly linear. The current I_{Big} however is slightly nonlinear for low settings of VP_Big and asymptotically approaches a plateau at high values. This nonlinearity represents the current mirror leaving saturation, as is shown in simulation in section 2.7.4.

The current output curves are fitted with linear functions. For VP_Big this fit is limited to the linear area at low DAC settings. The resulting slope is the driver characteristic

$$k_{driver} \coloneqq \frac{dI}{dDAC}. \tag{2.62}$$

These characteristic are shown in table 2.12 for two different chips. As predicted, the current draw for VP_Big and VP_Small is slightly reduced when irradiated. In idle state, the ratio

$$k \coloneqq \frac{k_{Big}}{k_{Small}} \tag{2.63}$$

is 35.2 for chip1 and 42.3 for chip2. This ratio relates the fraction $\frac{I_{Big}}{I_{Small}}$ in equation 2.19 with the DAC settings of VP_Big and VP_Small. As investigated in section 2.7.4, the current mirrors generating VP_Big and VP_Small are designed to create a ratio 48:1. The deviation of the measured values is likely due to the observed nonlinearity in VP_Big.

At a typical working point of VP_Big = 14, VP_Small = 8 and VN_Comp = 10, chip1 would consume an average of 5.4µA per TDC, a total of 19.4mA for all TDCs. This is a significant contribution to the power consumption of the chip. As shown in chapter 3, the power consumption can be significantly reduced by using switched drivers. The value of 5.4µA corresponds to a power consumption of 9.7µW per TDC. This value is used as a reference when investigating the power consumption of the delay chain TDC in chapter 4.

chip	stimulated	$k_{Big}[\frac{nA}{DACstep}]$	$k_{Small}[\frac{nA}{DACstep}]$	$k_{Comp}[\frac{nA}{DACstep}]$
2	no	243	5.75	209
1	no	232	6.60	205
1	yes	228	5.27	204

Figure 2.12: driver current increase per DAC step (average, per pixel)

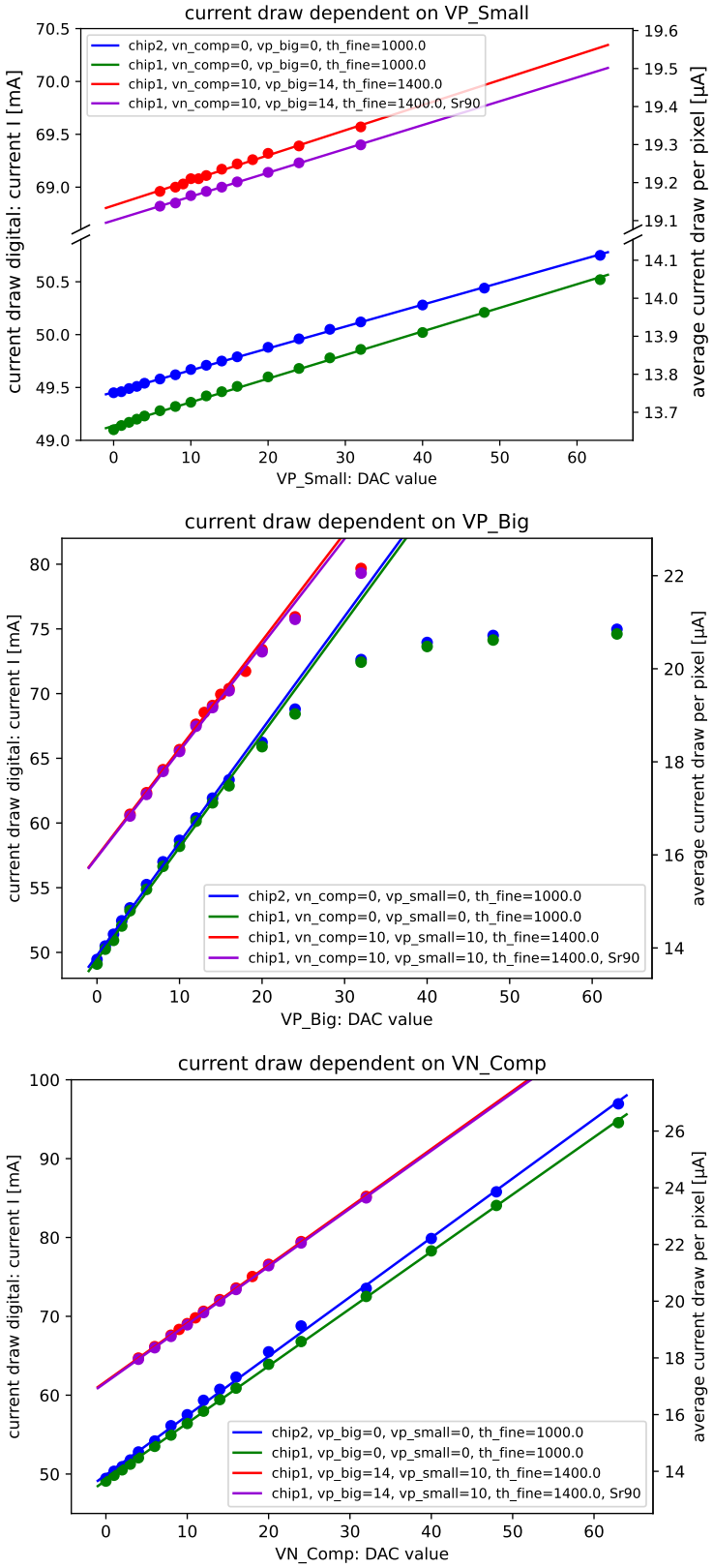


Figure 2.13: Laboratory measurement: whole chip current draw for chip1 (wafer 2 chip 10) and chip2 (wafer 1 chip 6) at different settings. *blue*: chip2, DACs at 0. *green*: chip1, DACs at 0. *red*: chip1, typical working point. *purple*: chip1, typical working point, stimulated with Sr90.

2.4 Charging Curve Reconstruction

In this section, the charging rate of the VP_Small driver transistor is reconstructed. This verifies the linearity of the charging process and shows any deviation from the simplifying assumptions made in section 2.1. Such deviations observed in laboratory measurements then are compared with simulation.

2.4.1 Reconstruction Method

In simulation, the voltage at the capacitor (node B) can be directly observed. In laboratory data however, only the timestamp of the threshold being crossed is available. Setting $I_{Big} = 0$ yields a magnification factor of 1, simplifying equation 2.16 to

$$\delta = \frac{U_{th}C}{I_{Small}} - (T_{clk} - T_{hit}). \tag{2.64}$$

Using a Sr90 radiation source creates random values for T_{hit}, yielding for the mean value

$$\overline{\delta} = \frac{U_{th}C}{I_{Small}} - \frac{1}{2}T. \tag{2.65}$$

δ by construction is the time required to cross U_{th}. Measuring $\overline{\delta}$ for different values of U_{th} allows recreating the charging curve

$$U(t) \equiv U_{th}(\overline{\delta}) = \frac{I_{Small}}{C} \cdot \overline{\delta} + const. \tag{2.66}$$

By fitting a linear function to the relation $U_{th}(\overline{\delta})$, the ratio $\frac{I_{Small}}{C}$ can be obtained.

2.4.2 Measured Charging Curve

Figure 2.14 shows the measured charging curve in a single pixel for different values of VP_Small. Comparison with the simulation results shown in figure 2.15 allows for interpreting the observed features more easily.

In the mid range, between 600mV and 1300mV, the charging curve is linear as desired, corresponding to a constant charging rate. In this range, linear functions are fitted to measure the charging rate (compare with 2.66).

In the low range, below 600mV, the charging curve appears to show a sudden rise which does not exist in simulation. This means, the comparator circuit is out of range in this regime, and responds with significant delay, after reaching a higher voltage.

In the high range, between 1300mV and 1650mV, the charging rate increases. This is a physical effect that can also be seen in simulation. This rise in charging rate can be explained by the drop of the gate capacitance of the PMOS, as shown in section 2.7.1. Operating the circuit in this range is undesirable, as it introduces nonlinearities. VP_Big should be chosen low enough to stay below 1300mV in the initial clock cycle.

Finally, the charging rate slows down again above 1650mV. This shows more clearly in simulation, as the measurements are restricted by the upper limit of the comparator. This slowdown corresponds to the driving transistor leaving saturation, as shown in simulation in figure 2.47.

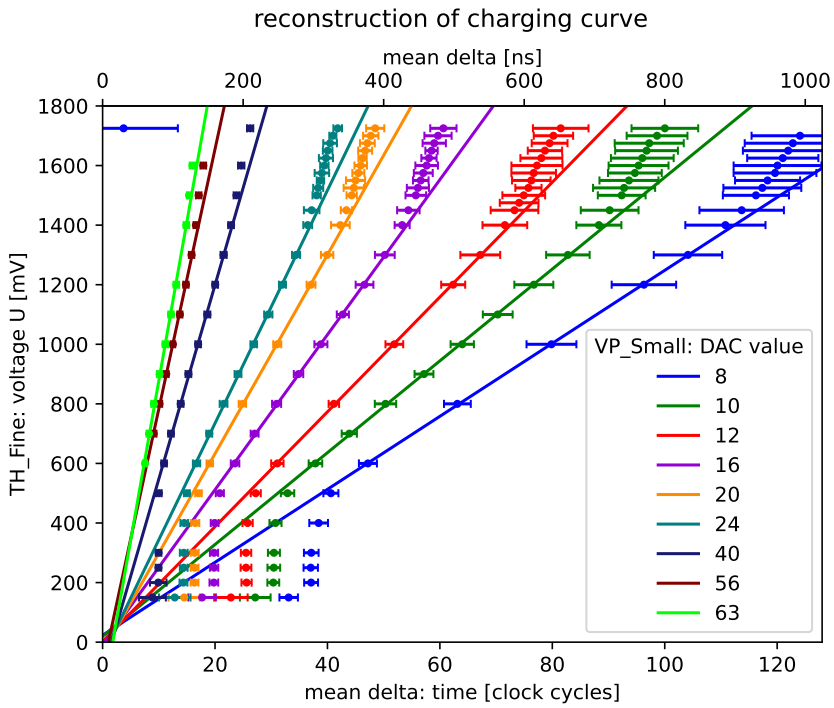


Figure 2.14: laboratory measurement: reconstructed charging curves of Stretched TDC circuit for a single pixel with VP_Big driver off for different values of VP_Small. Error bars correspond to standard deviation of $\overline{\delta}$. Note that the 7bit timestamp TS3 wraps from 127 to 0.

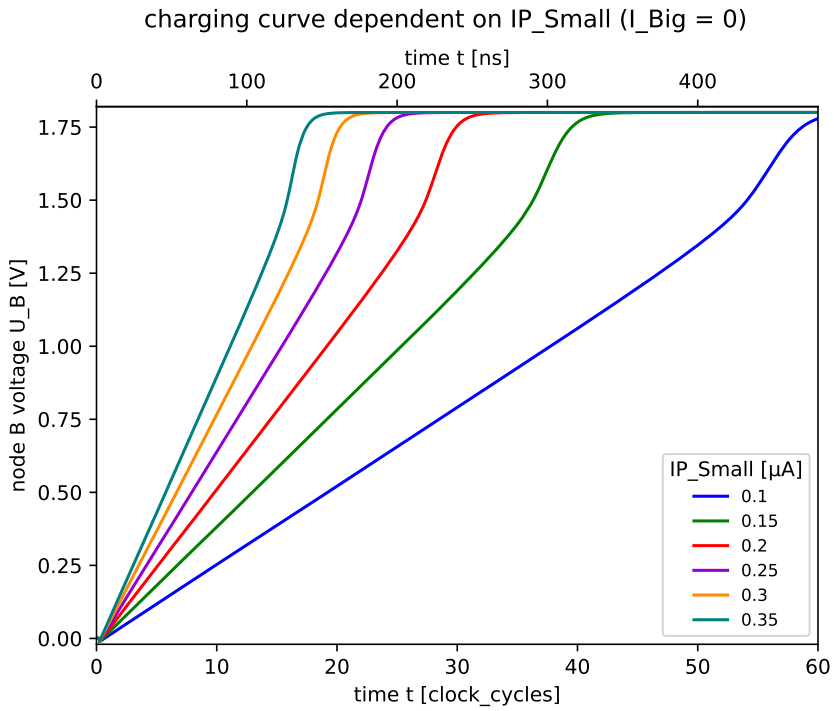


Figure 2.15: transient simulation: charging curve of the Stretched TDC circuit with VP_Big driver off

Figure 2.16 shows the relation between the DAC setting for VP_Small and the slope

$$\dot{U} = \frac{I_{Small}}{C} \tag{2.67}$$

obtained from the fits to the measured charging curves. This relation is highly linear, as shown also in simulation (figure 2.43) and current draw measurement (figure 2.13). The proportionality factor varies between pixels.

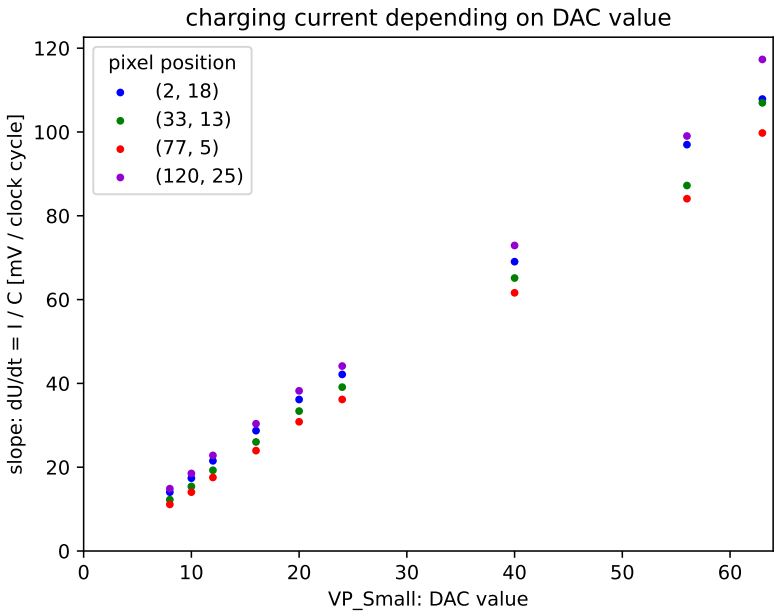


Figure 2.16: laboratory result: relation of charging rate obtained from fit and VP_Small DAC setting for different pixels

2.4.3 Pixel-to-Pixel Variation

The charging rate varies from pixel to pixel. The most likely explanations are manufacturing variation and power line resistance.

Im manufacturing, the most significant variations are in length and width of transistor gates, thickness of gate oxide and doping of the silicon. They can appear as stochastic variations, randomly distributed over the chip, or they can appear as systematic variations, with a specific pattern (e.g. chemical gradients).

Power line resistance induces voltage drops between the supply voltage on the bond pads and the different parts of the chip. Supply line resistance is visible as a gradient over the chip surface which is identical between chips.

Figure 2.17 shows the distribution of the charging rate as a histogram. The distribution is bimodal, which is atypical for purely stochastic variations. Figure 2.18 shows the relation between the charging rate and pixel position. There is a strong correlation between column address and charging rate. The correlation with the column is shown more explicitly in figure 2.19. This pattern turns out to be identical between chips, hinting at supply line resistance being the dominant cause.

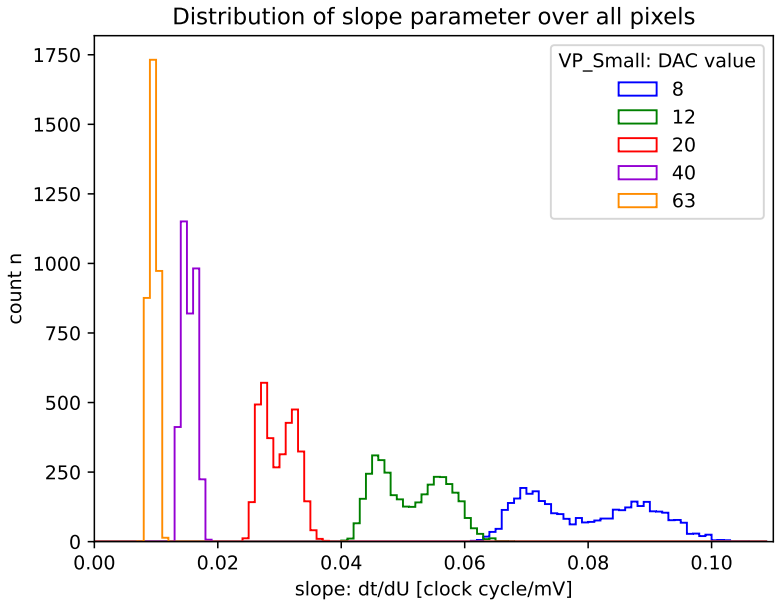


Figure 2.17: laboratory result: distribution of charging rate over all pixels for different values of VP_Small

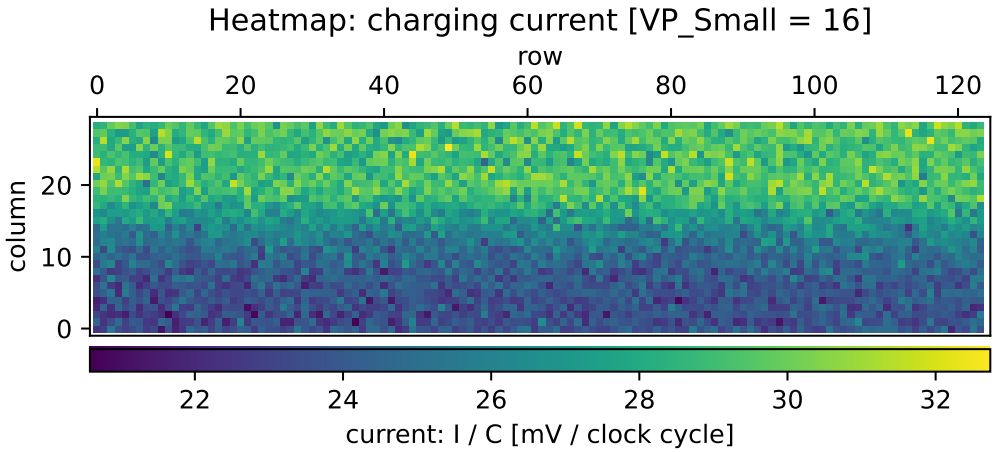


Figure 2.18: heatmap: relation of charging rate and pixel position

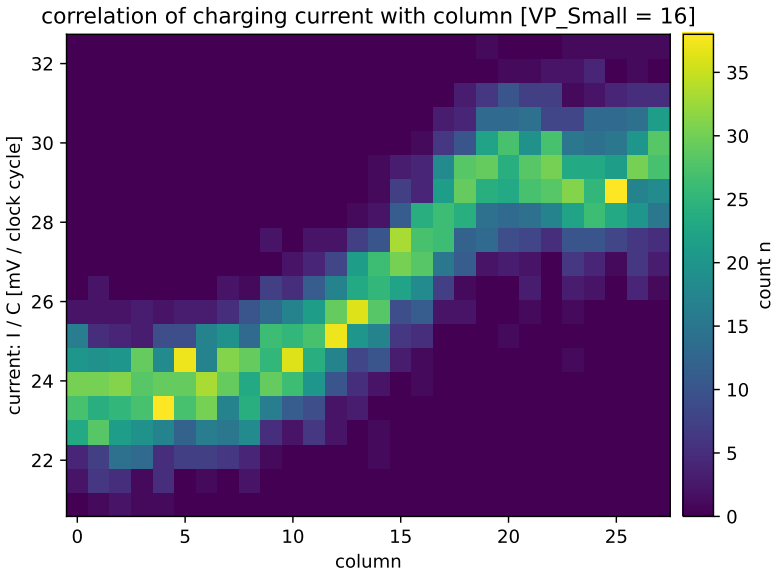


Figure 2.19: correlation plot: column dependence of charging rate

2.5 Premature Threshold Effect

This section investigates the premature threshold issue described in section 2.1.4 in order to get limits for the operating range of the Stretched TDC circuit. In the δ-distribution the premature threshold shows as a significant peak at the left edge of the distribution, as seen in figure 2.20.

Figure 2.21 shows the rise of the ratio ξ of timestamps with premature threshold condition. The ratio is 0 up to a value of VP_Big corresponding to equation 2.28. Above that value, the ratio rises, following equation 2.24. As described in section 2.3.2, the current levels off for high values of VP_Big, causing the visible plateau.

As postulated in equation 2.24, there is a light influence of VP_Small on the premature threshold effect. Higher VP_Small results in a lower limit for VP_Big. In the reasonable range 8 < VP_Small < 16, this effect is negligible.

The maximum safe value varies between pixels. TH_Fine = 1300mV is the upper limit of linearity determined in section 2.4. At this threshold, typical values are between VP_Big = 16 and VP_Big = 20. Generally, VP_Big ≤ 14 is considered safe. A threshold value of TH_Fine = 1500mV is recommended to ensure a safety margin.

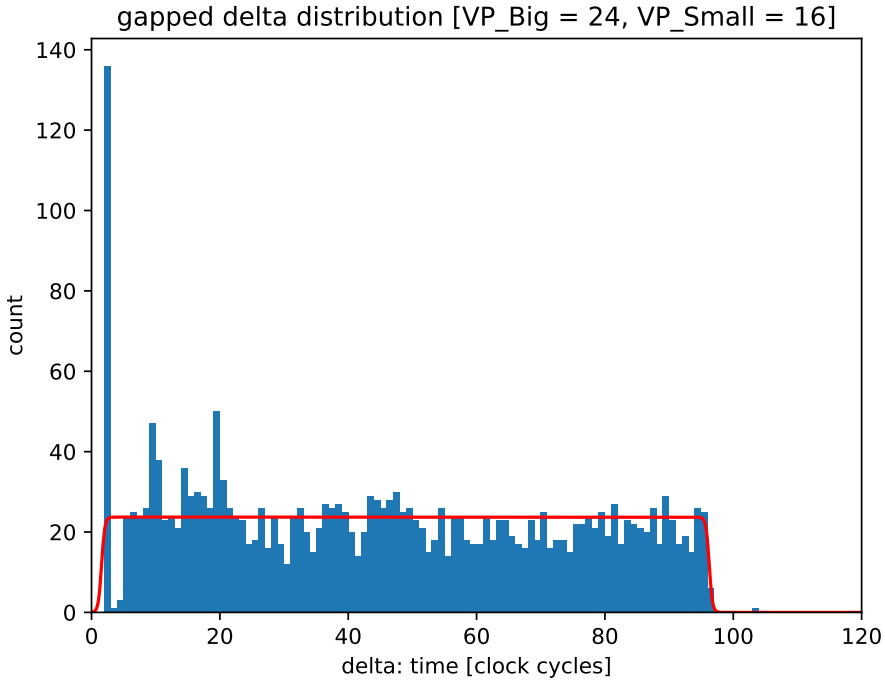


Figure 2.20: Sr90 measurement: δ-distribution for too high VP_Big: The premature crossing of the threshold causes an accumulation at low δ.

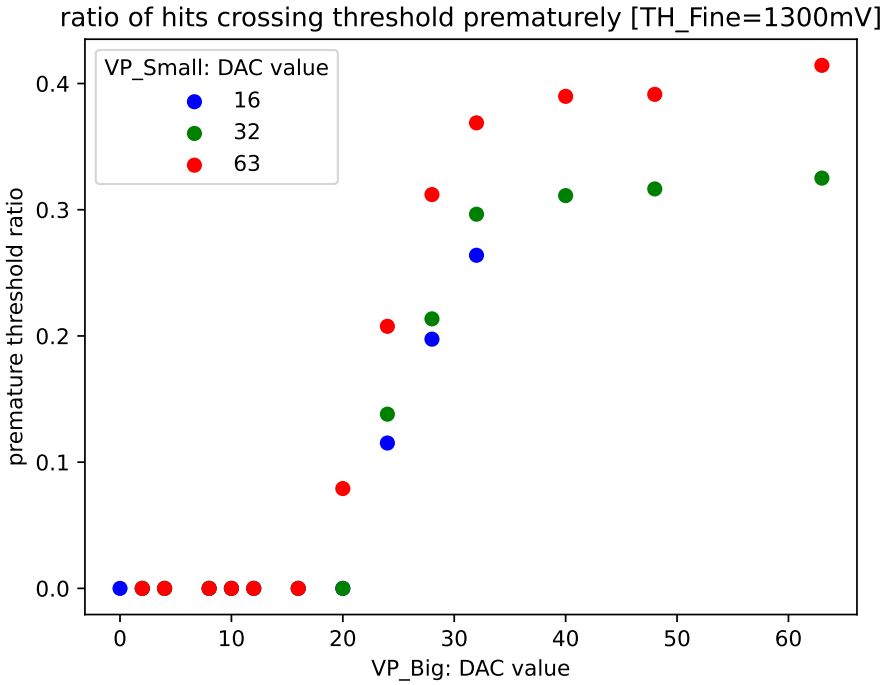


Figure 2.21: Sr90 measurement: Ratio ξ of timestamps in the initial peak (single pixel, typical)

2.6 Parametric Analysis

This section verifies the relation between the distribution parameters δ_{max} and w and the DAC settings for VP_Big, VP_Small and TH_Fine established in section 2.1.3. To do that, δ_{max} and w are obtained from Sr90 data for various settings of the DACs.

2.6.1 Distribution Width Fit

According to equation 2.19, w relates to VP_Big and VP_Small.

$$\frac{w}{T} = 1 + \frac{I_{Big}}{I_{Small}} \approx \frac{I_{Big}}{I_{Small}} \tag{2.68}$$

Fit Functions

This relation is fit individually for each pixel. The fit is done in three stages. First, an inversely proportional function is fit for each value of VP_Big and TH_Fine

$$w(\mathrm{VP\_Small}) = a + \frac{b}{\mathrm{VP\_Small}}. \tag{2.69}$$

The offset a should be 1. A slight deviation from that value can be explained by the capacitance correction discussed in section 2.7.1. The slope b should be proportional with VP_Big. In the second stage, this proportionality is fit for each value of TH_Fine,

$$b = kI_{Big}. \tag{2.70}$$

The relation of the DAC values set and the currents generated is given by the proportionality constants k_{Big} and k_{Small} investigated in section 2.3. The parameter k is the ratio of the current drivers' relative strength.

$$I_{Big} = k_{Big}\,\mathrm{VP\_Big} \tag{2.71}$$

$$I_{Small} = k_{Small}\,\mathrm{VP\_Small} \tag{2.72}$$

$$k := \frac{k_{Big}}{k_{Small}} \tag{2.73}$$

As stated in section 2.3.2, the value should be 48 by design but in current measurements turns out to be lower, around 40. A singular value for k is obtained by averaging over the values of TH_Fine.

VP_Small Dependence

Figure 2.22 shows the dependence of w on VP_Small. The inversely proportional fit matches the measurements well. For high VP_Big, w asymptotically approaches a plateau. VP_Big = 32 has values below VP_Big = 24, likely due to temperature differences between measuring sessions. The offset parameter a has a wide distribution around 0. This suggests that the capacitance correction is dominated by the random variations in Sr90 data and temperature differences between measurements and cannot be measured this way.

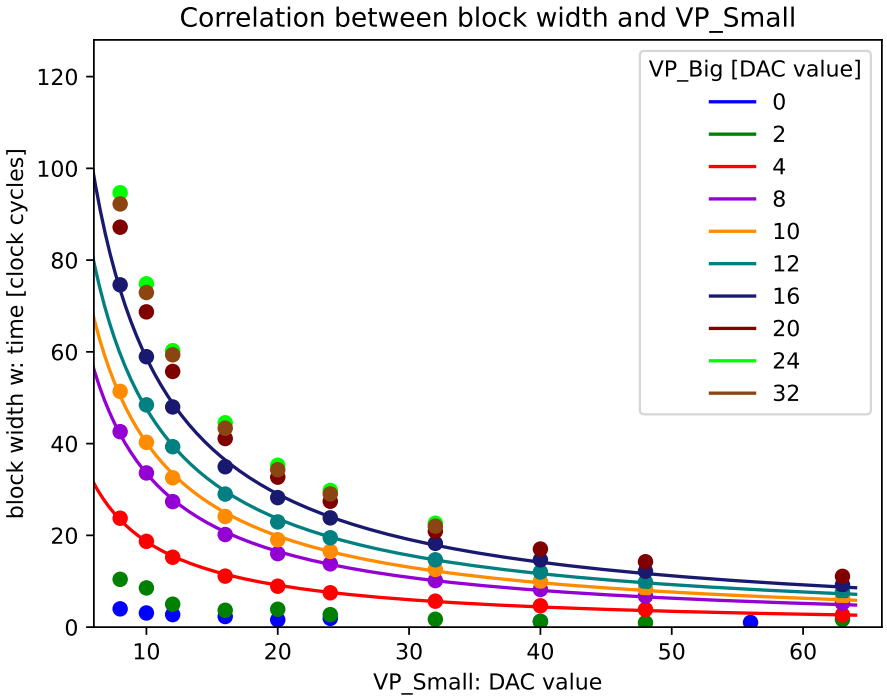


Figure 2.22: Sr90 measurement: Influence of VP_Small and VP_Big on δ-distribution at TH_Fine = 1300mV. Fits of $a + \frac{b}{\text{VP\_Small}}$ are shown for values of VP_Big in the operating range.

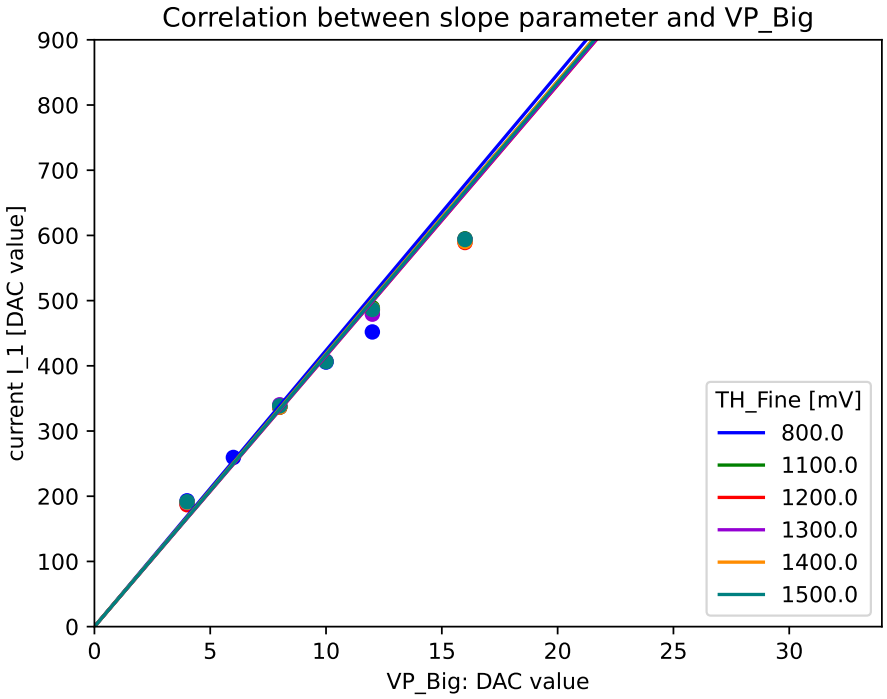


Figure 2.23: Sr90 measurement: Slope b of VP_Small fit to w according to equation 2.70, depending on VP_Big and TH_Fine.

VP_Big Dependence

Figure 2.23 shows the results for the fit slope b of the VP_Small fit. The proportionality factor k is fit to the curve. Due to the nonlinearity of the VP_Big driver, the values do not quite match the fit, showing the concave curve observed in figure 2.13. As predicted, there is no influence of TH_Fine on w and the derived fit parameter b.

Position Dependence

Figure 2.24 shows the heatmap of parameter k over the pixels. The fixed pattern seen for the charging rate in figure 2.18 can also be observed for k. The pattern is consistent between chips, supporting the hypothesis that supply line resistance is the main cause.

The variation between pixels is $\pm 30\%$ from the average value. This is a significant spread, which results in a variation in time resolution of the TDC of the same amount.

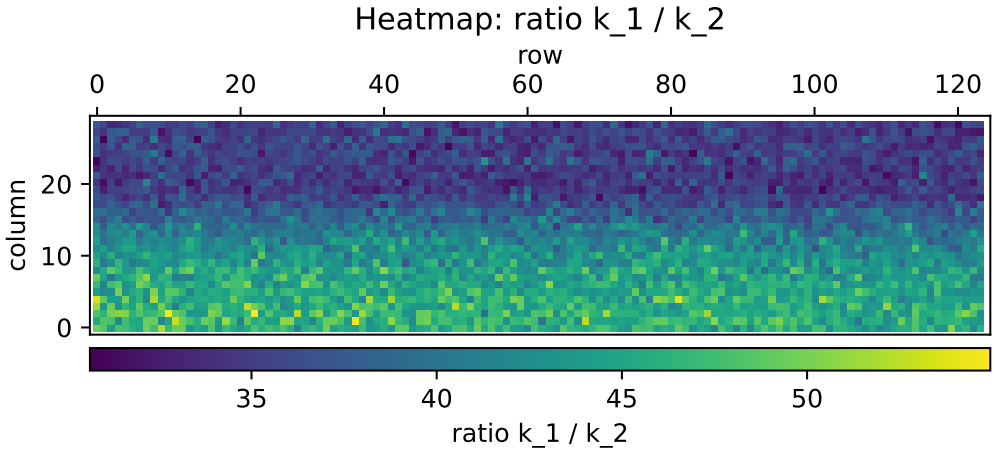


Figure 2.24: Sr90 measurement: Heatmap of current driver ratio $k = \frac{k_{Big}}{k_{Small}}$

2.6.2 δ_{max} Fit

According to equation 2.17, δ_{max} depends on VP_Small and TH_Fine but not on VP_Big,

$$\delta_{max} = \frac{U_{th}C}{I_{Small}} \tag{2.74}$$

Fit Functions

In addition, some secondary effects need to be considered. A constant delay K accounts for the comparator delay introduced in section 2.7.3 as well as potential delays in the readout chain. In addition, the flipflop delay D investigated in section 2.7.2 needs to be considered, as it introduces a slight dependence on VP_Big stated in equation 2.101.

$$\delta_{max} = \frac{U_{th}C}{I_{Small}} + \frac{I_{Big}}{I_{Small}}D + K \tag{2.75}$$

The fits are done in three stages. First, a linear function fits the VP_Big dependence,

$$\delta_{max}(\mathrm{VP\_Big}) = \alpha_s + \beta \cdot \mathrm{VP\_Big}\,. \tag{2.76}$$

The fit results are the offset $\alpha_s = \frac{U_{th}C}{I_{Small}} + K$ and the slope $\beta = \frac{1}{I_{Small} \cdot D}$. In the second stage, an inversely proportional function fits the VP_Small dependence of α_s,

$$\alpha_s(\mathrm{VP\_Small}) = \frac{\alpha_{th}}{\mathrm{VP\_Small}} + K. \tag{2.77}$$

The result of this fit is the delay K and the slope α_{th}. Finally, the proportional relation with TH_Fine is fitted, yielding the ratio $\alpha = \frac{C}{k_{Small}}$ of capacitance and VP_Small driver strength.

$$\alpha_{th} = \alpha \cdot \mathrm{TH\_Fine} \tag{2.78}$$

Dependence on VP_Small and VP_Big

Figure 2.25 shows the dependence of δ_{max} on VP_Small. It shows the expected inversely proportional relation. A slight dependence on VP_Big can observed. The dependence on VP_Big can be seen more clearly in figure 2.26. It is a linear relation, consistent with the flipflop delay in model equation 2.75.

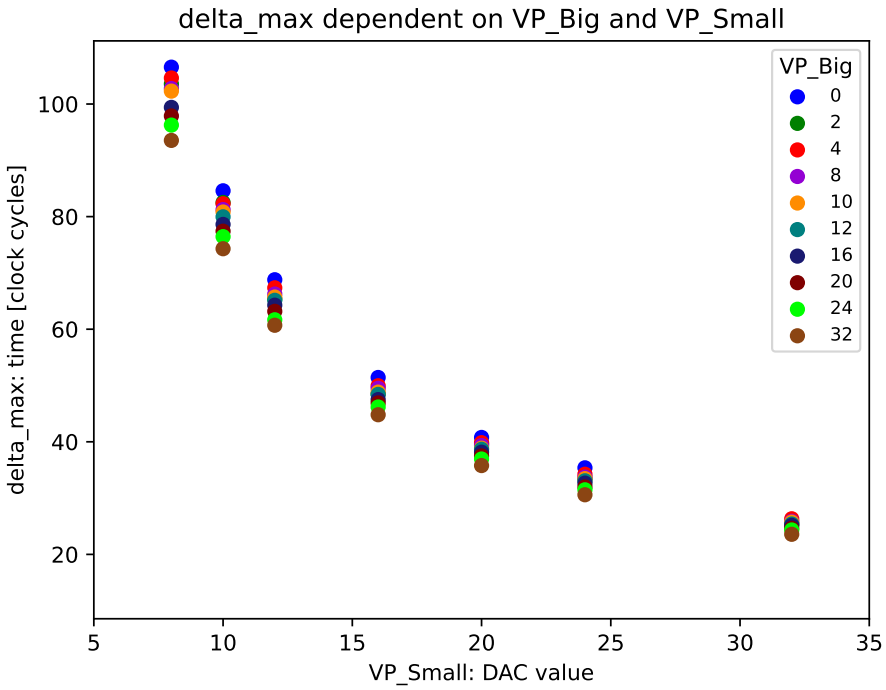


Figure 2.25: Sr90 measurement: Dependence of δ_{min} on VP_Small.

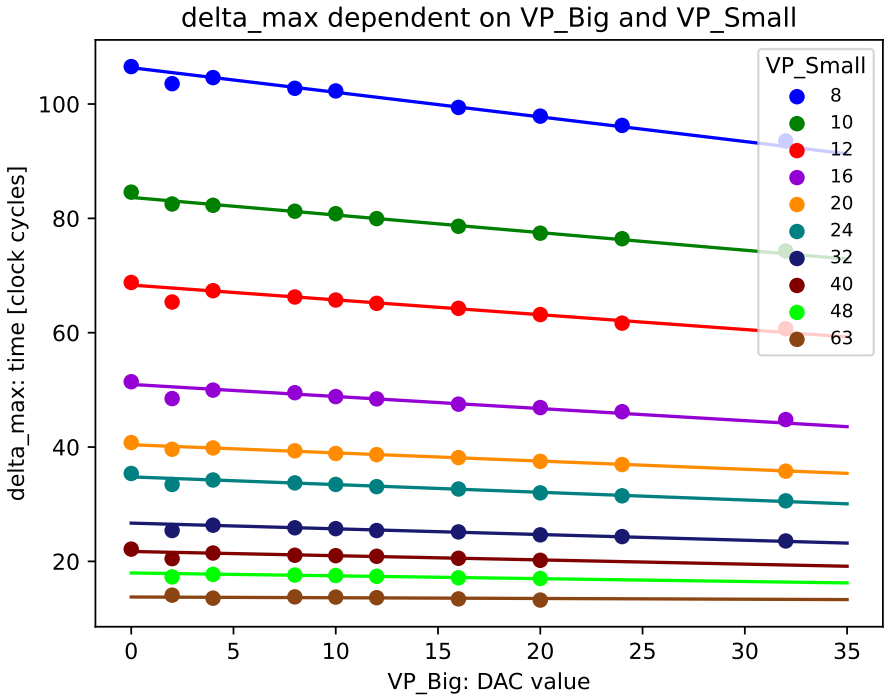


Figure 2.26: Sr90 measurement: Linear dependence of δ_{max} on VP_Big.

Threshold Dependence

Figure 2.27 shows the dependence of the intermediate fit parameter α_{th} on the threshold. According to the fit model 2.78, $\alpha_{th} = \frac{C}{k_{Small}} U_{th}$. The predicted proportionality can be observed.

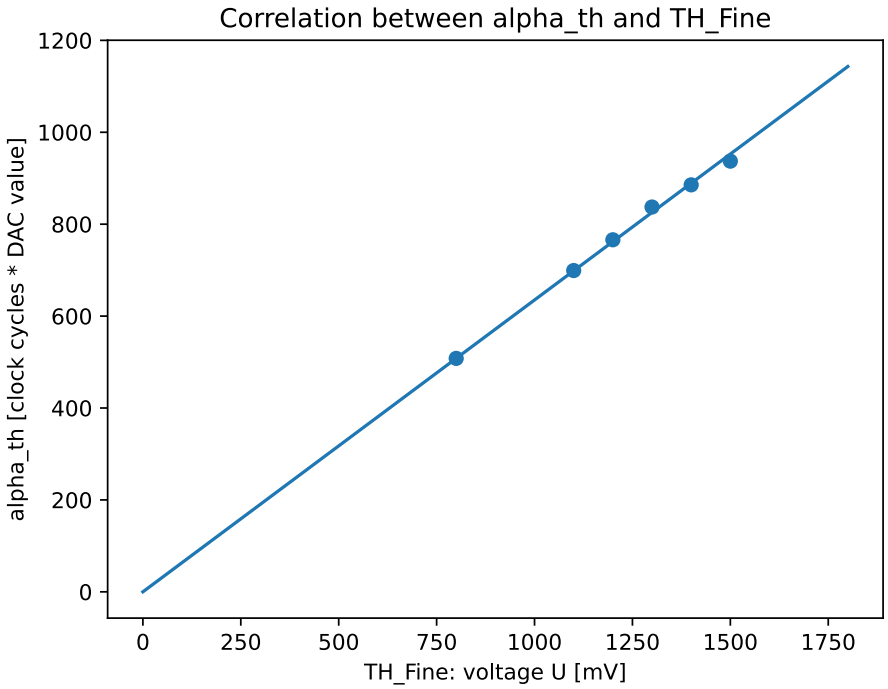


Figure 2.27: Sr90 measurement: Dependence of δ_{max} on TH_Fine, measured by fit parameter α_{th}.

Position Dependence

Figure 2.28 shows the heatmap of parameter α over the pixels. It shows the same fixed pattern as the values determined for k in the w-fits. Once more, the pattern is consistent between chips. Like for k, the variation between pixels is $\pm 30\%$ from the average value.

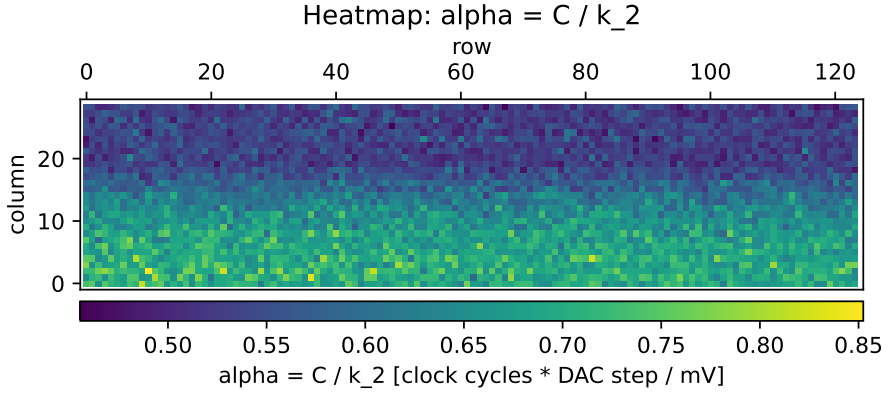


Figure 2.28: Sr90 measurement: Heatmap of ratio $\alpha = \frac{C}{k_{Small}}$ (capacitance over VP_Small current)

2.6.3 Cause of Pixel-to-Pixel Variation

According to the heatmaps 2.24 and 2.28, the ratios $k = \frac{k_{Big}}{k_{Small}}$ and $\alpha = \frac{C}{k_{Small}}$ have a pixel-to-pixel variation of $\pm 30\%$. The Fixed pattern dominates the stochastic variation in both cases.

Dividing the two ratios yields a third ratio $\zeta := \frac{C}{k_{Big}}$. The heatmap for this ratio can be seen in figure 2.29. The relative variation of ζ is $\pm 14\%$, far lower than the two other ratios. The variation of ζ still shows the same fixed pattern, corresponding to a gradient over the row index. However, the stochastic variation this time is of similar magnitude.

The ratios $\frac{k_{Big}}{k_{Small}}$ and $\frac{C}{k_{Small}}$ feature a similar, high level of variation and $\frac{C}{k_{Big}}$ a lower level. This suggests that the dominant cause in pixel-to-pixel variation is the VP_Small driver. As VP_Small drives small currents, a high relative error is unsurprising. The fixed pattern hints at a significant voltage drop in the supply lines as the likely cause.

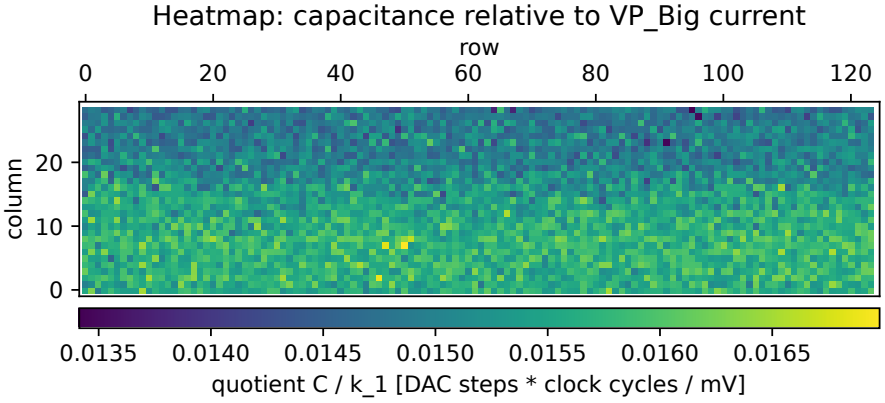


Figure 2.29: Sr90 measurement: Heatmap of ratio $\zeta = \frac{C}{k_{Big}} = \frac{\alpha}{k}$ (capacitance over VP_Big current)

2.7 Secondary Effects and Component Analysis

In the previous sections, a few cases have been found, in which observed laboratory data differs from the linear model suggested in section 2.1. The linear model simplifies the current sources and the capacitance as constant, the switches as instantaneous and the comparator as ideal. Deviations from this idealised picture will reduce the calibration accuracy by deviating from the linear reconstruction curve suggested by figure 2.3 and equation 2.7.

The following sections show algebraic approximations and simulation results for the observed effects. Each section isolates a specific component or subcircuit of the TDC, analysing the potential effects and assessing their significance.

2.7.1 Non Constant Capacitance

The capacitance in the Stretched TDC circuit has so far been considered to be constant. This is however not accurate. Firstly, as the transmission gate switches, the parasitic capacitance from the pulldown NMOS and the VP_Big driver is disconnected from the node at the comparator input (node B). Secondly, as MOS transistors make up most of the capacitance, it changes with the voltage dependent channel geometry.

This section first presents an algebraic model for the influence of the first effect on the δ-distribution. Then, the significance of both effects is investigated in simulation.

Algebraic Model

In section 2.1.3, the equations 2.14 and 2.15 for the charging slopes assume an equal capacitance in both phases of the charging process. However, in the first phase there is an additional parasitic capacitance C_{par} made up from the NMOS and PMOS transistor at node A.

Whilst the charging slope s_B remains

$$s_B = \frac{I_{Small}}{C} \tag{2.79}$$

as in equation 2.15, the slope s_A is

$$s_A = \frac{I_{Small} + I_{Big}}{C + C_{par}} \tag{2.80}$$

in this more accurate model. δ_{max} remains as before, but the distribution width is reduced by a factor κ:

$$\frac{w}{T} = \frac{s_A}{s_B} = \frac{C}{C + C_{par}} \frac{I_{Small} + I_{Big}}{I_{Small}} \tag{2.81}$$

$$= \frac{1}{1 + \frac{C_{par}}{C}} \left(1 + \frac{I_{Big}}{I_{Small}}\right) \tag{2.82}$$

$$\equiv \kappa \left(1 + \frac{I_{Big}}{I_{Small}}\right) \tag{2.83}$$

Notably, the time reconstruction is unaffected. This effect only changes the operating point in terms of the DAC values VP_Big and VP_Small.

Measurement Method

To get an idea, if and how much influence the non constant capacitance has on the TDC circuit, the circuit is simulated in the small signal model of the SPECTRE AC simulator. In order to determine the capacitance C at voltage U_0, bias the node with the constant voltage and stimulate the circuit with a sinusoidal voltage

$$U = \hat{U} \sin \omega t. \tag{2.84}$$

This measurement has to be done at a frequency high enough such that the capacitance dominates any resistive component of the impedance but not so high that inductive parasitics dominate.
At low frequency, resistive impedance dominates. The output current in this case is constant.

$$I = \frac{U}{R} = \frac{\hat{U}}{R} \cos \omega t \tag{2.85}$$

$$\equiv \hat{I} \cos \omega t \tag{2.86}$$

$$\hat{I} = \frac{\hat{U}}{R} \equiv const \tag{2.87}$$

At sufficiently high frequency, capacitive impedance dominates. The output current in this case rises linearly with the frequency. In small signal approximation,

$$I = \dot{Q} = C_d \dot{U} = \omega \hat{U} C_d \cos \omega t \tag{2.88}$$

$$\equiv \hat{I} \cos \omega t \tag{2.89}$$

$$\Rightarrow \ \hat{I} = \omega \hat{U} C_d \ \sim \ f \tag{2.90}$$

When measuring the current amplitude for a given input stimulus with amplitude $\hat{U}$ and frequency f, the corresponding differential capacitance is

$$C_d = \frac{\hat{I}}{2\pi f \hat{U}}. \tag{2.91}$$

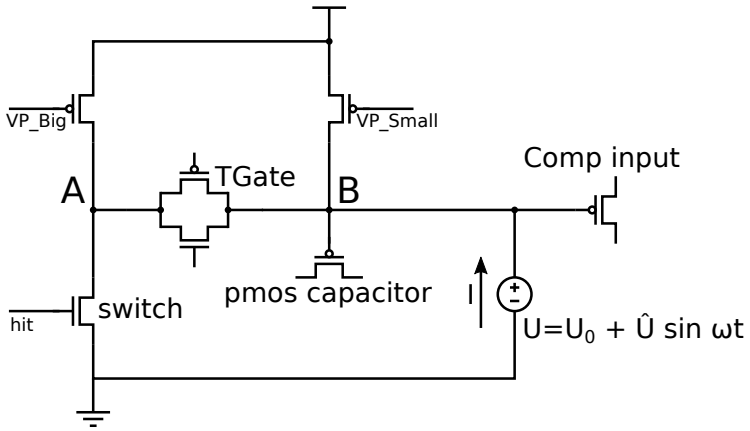


Figure 2.30: circuit setup for capacitance simulation

Simulation Results

A frequency scan yields that the circuit is dominated by capacitance in the region between 1GHz and 10GHz, since $\hat{I} \sim f$ (see figure 2.31). Therefore, set the frequency to 1GHz. The voltage amplitude is arbitrarily chosen to be 1mV.

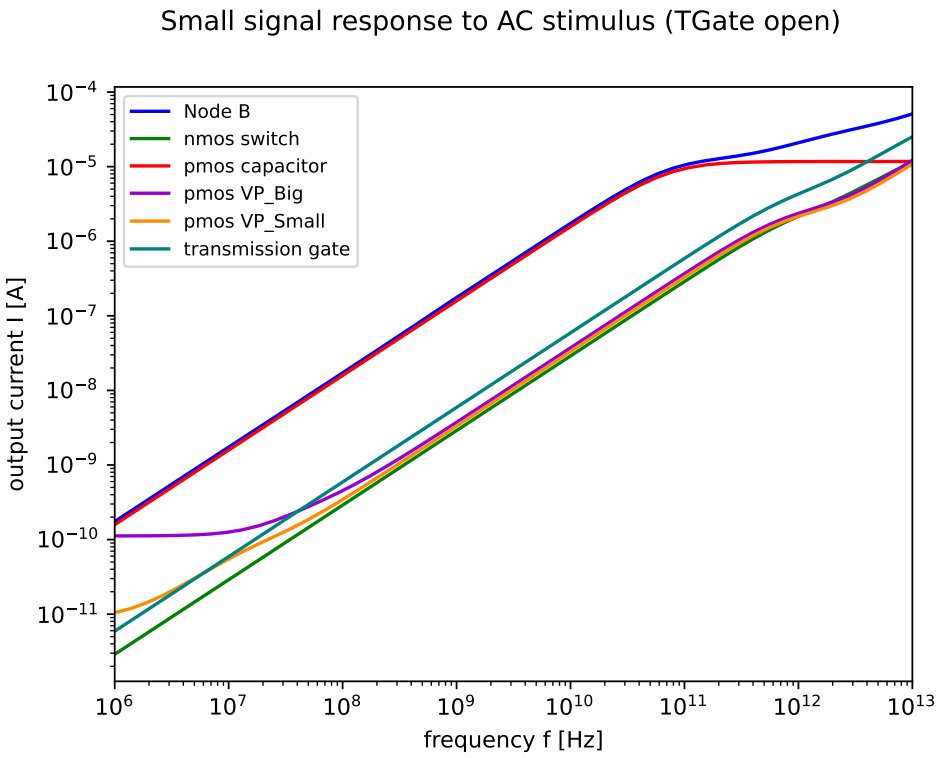


Figure 2.31: AC simulation: frequency scan of current amplitude

At these settings, a scan of the operating voltage U_0 at node B is performed. In figure 2.32, the full capacitance of node B is shown, for both conducting and blocking state of the transmission gate. In addition, the capacitances of the individual components are shown.

As expected, the capacitances of the individual components add up to the full node capacitance. The dominating contribution is the PMOS capacitor. The capacitance of node B is close to constant up to 1.0V. Beyond 1.4V, a significant dropoff in capacitance from 31fF to 13fF is observed. In addition, there is a difference (31fF vs. 28,5fF) in capacitance at node B between the conducting and blocking case.

The reduction in capacitance beyond 1.4V can be explained by the the pmos transistor used as a capacitor going below threshold. There is a similar but opposite effect, as the driver PMOS transistors go out of saturation. However, the contribution of the driver transistors is low in comparison as they are smaller.

The difference in node B capacitance between the cases of conducting and blocking transmisson gate is made up of two contributions. Firstly, as the transmission gate blocks connectivity to node A, both the pulldown NMOS and the driver PMOS for VP_Big are disconnected. Secondly, as the gate voltage of the transmission gate transistor goes below threshold, the channel capacitance no longer contributes. The correction factor for equation 2.81 obtained in this simulation is κ = 0.92.

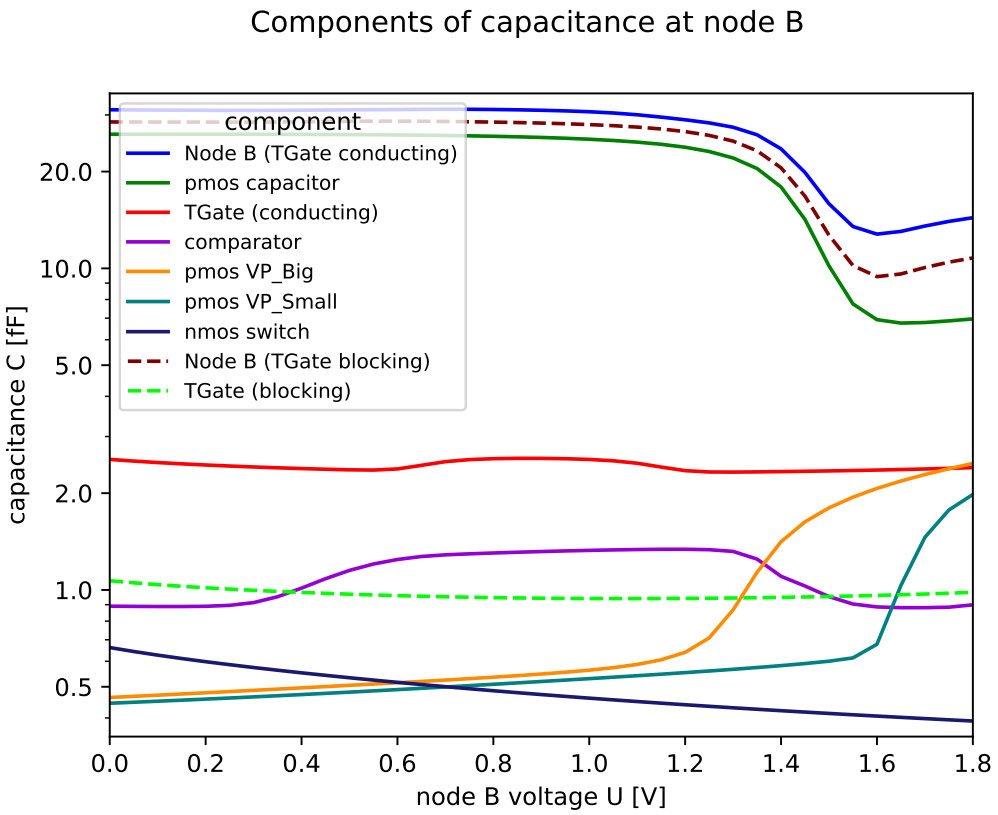


Figure 2.32: AC simulation: differential capacitance C_d at node B and for singular components. *blue*: total with TGate conducting. *brown dashed*: total with TGate blocking. *green*: PMOS capacitor

The contribution of the driver transistors rises from 0.5fF to 2fF when leaving saturation. This is as small but relevant contribution to the overall capacitance. The point of saturation shifts with the gate voltage set by the DAC. For VP_Small this turns out to be above 1.5V and therefore out of the operating range of the TDC. For VP_Big however, it can happen below 1.4V and therefore introduce a slight nonlinearity into the charging curve.

The dependence of the capacitance of the VP_Big driver on the driven current can be observed in figure 2.33. Above $I_{Big} = 1\mu A$, the nonlinearity occurs inside the operating range. This, together with the reduction in current seen in section 2.7.4, should be avoided in a future iteration of the TDC by using a wider transistor.

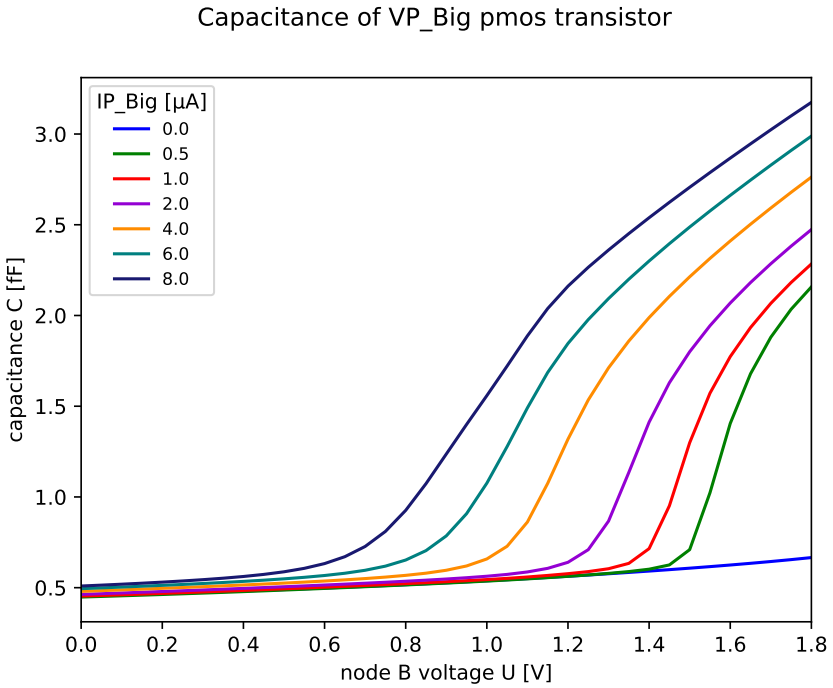


Figure 2.33: AC simulation: dependence of VP_Big driver drain capacitance on driven current

2.7.2 Flipflop

In the initial calculations, the flipflop was assumed to be ideal, that is to switch instantly and without any setup time. In reality, a fliflop always has a delay compared to the clock edge. Also, if the input switches just before the clock edge, the flipflop may be left in a metastable state. In that case, the flipflop delay may be arbitrarily long.

This section first gives an algebraic approximation of the effect of the flipflop delay on the distribution of δ. Then, the flipflop delay is investigated using the SPECTRE transient simulator.

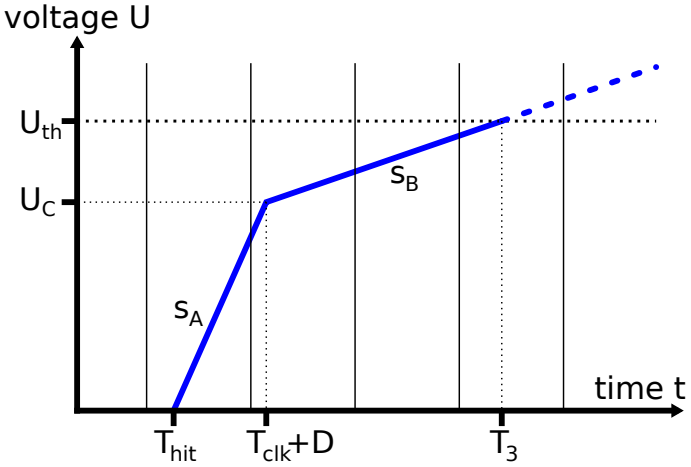


Figure 2.34: Sketch: charging curve including flipflop delay

Algebraic Model

A nonzero flipflop delay D modifies the charging rate equations 2.3 and 2.4. This yields for δ:

$$s_A = \frac{U_C}{(T_{clk} + D) - T_{hit}} \tag{2.92}$$

$$s_B = \frac{U_{th} - U_C}{T_3 - (T_{clk} + D)} \tag{2.93}$$

$$= \frac{U_{th} - s_A\,(T_{clk} + D - T_{hit})}{T_3 - (T_{clk} + D)} \tag{2.94}$$

$$\delta \equiv T_3 - T_{clk} \tag{2.95}$$

$$= \frac{U_{th} - (T_{clk} + D - T_{hit})\,s_A}{s_B} + D \tag{2.96}$$

$$= \frac{U_{th}}{s_B} - \frac{s_A}{s_B}\,(T_{clk} - T_{hit}) + \left(1 - \frac{s_A}{s_B}\right) D \tag{2.97}$$

This is equation 2.7 plus a correction term dependent on the flipflop delay. The resulting distribution parameters δ_{min}, δ_{max} and w are

$$\delta_{min} = \frac{U_{th}}{s_B} - \frac{s_A}{s_B} T + \left(1 - \frac{s_A}{s_B}\right) D \tag{2.98}$$

$$\delta_{max} = \frac{U_{th}}{s_B} + \left(1 - \frac{s_A}{s_B}\right) D \tag{2.99}$$

$$w = \frac{s_A}{s_B} T \tag{2.100}$$

The time magnification is the same as calculated before, in equation 2.12. For calibration, the flipflop delay therefore makes no difference. However, δ_{max} is modified to

$$\delta_{max} = \frac{U_{th}C}{I_{Small}} + \frac{I_{Big}}{I_{Small}}D. \tag{2.101}$$

This is a slight dependence of δ_{max} on I_{Big} that did not exist in the idealised calculation 2.17. It can be seen in the parametric study of δ_{max} in section 2.6.2.

Simulation Results

Figure 2.35 shows the delay of the flipflop depending on the time of the input signal edge. For most of the clock cycle, the delay is stable at 94ps. There is a critical time t_{crit} characterised by the following traits:

- If the hit input arrives after t_{crit}, the flipflop will switch at the next clock cycle, as intended.
- In the time frame just before t_{crit}, the flipflop delay rises exponentially with input time.

In the time window of around 1ps before t_{crit}, the error in measured time will be above 100ps. This corresponds to $\approx$ 0.01% of the hits. At most, the resulting measured time may be off by up to half a clock cycle. Such a large error will occur only at a negligible rate.

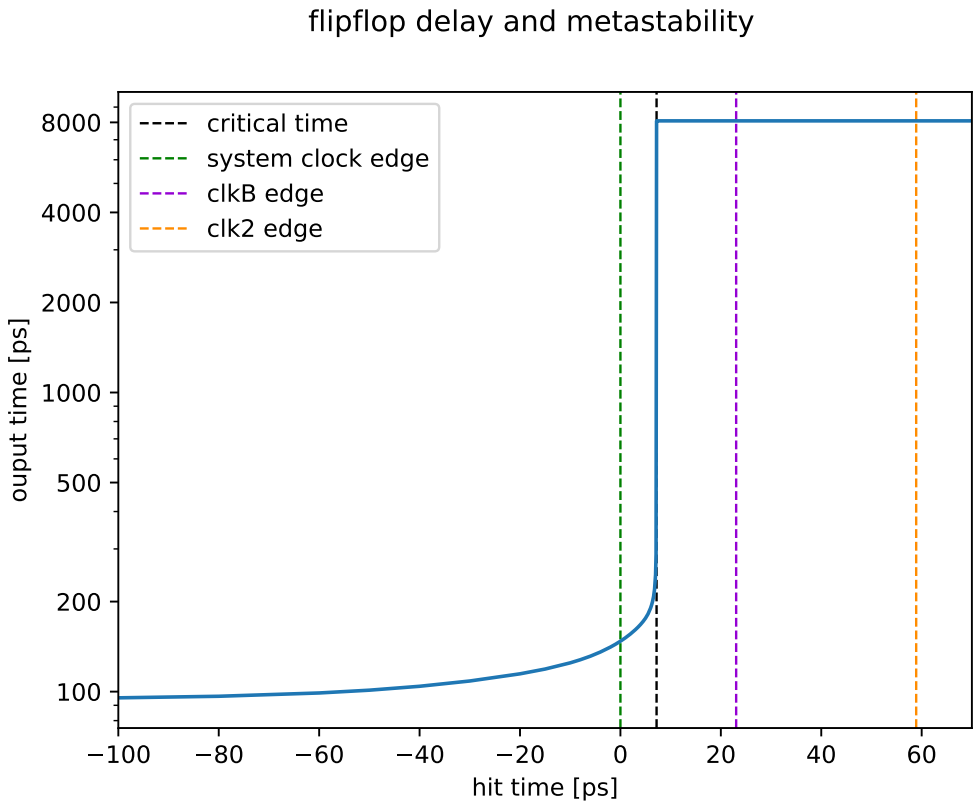


Figure 2.35: transient simulation: Time difference between clock edge and flipflop switching vs. time of input flank. At input hit time 0, the input switches at the same time as the system clock. The flipflop is triggered by repeated local copies of the system clock, clk2 and clkB.

2.7.3 Comparator

The comparator has so far been assumed to be ideal. That is, it switches instantaneously and exactly at the set threshold voltage. This section investigates, how significant deviations from this ideal case are, regarding the accuracy of the TDC.

Comparator Circuit

Figure 2.36 shows the comparator circuit. On the left, 5 transistors make up the core of the comparator, followed by a gain stage and an inverter. In addition to the threshold, there is a second DAC controlling the current driven by the NMOS transistor.

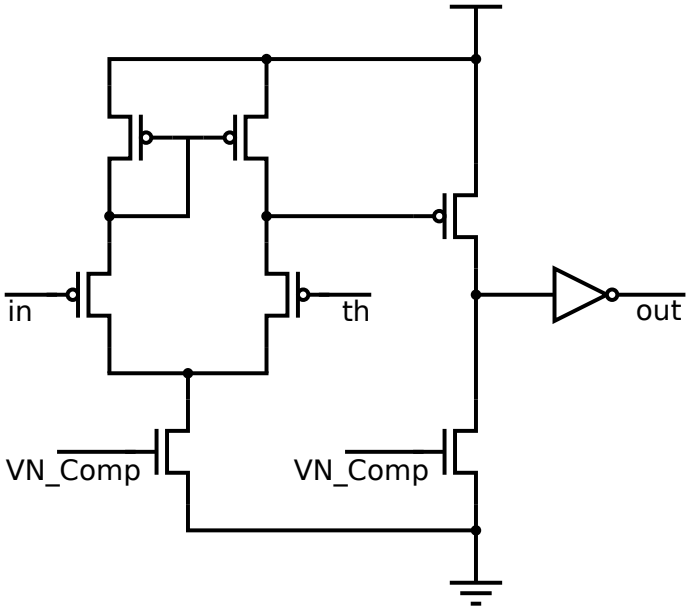


Figure 2.36: comparator circuit diagram

Switching Point and Accuracy

This section investigates the accuracy of the comparator, measured as the deviation of the switching point from the threshold voltage. Notably, even a large deviation of would not influence time magnification, as seen in equation 2.19. However, there is an influence on δ_{max}, as seen in equation 2.17.

Figure 2.37 displays the output voltage of the comparator around the switching point set by the threshold. Here, the switching point is inaccurate only by a few mV. There is no significant range of input voltage, in which the output voltage is in an intermediate state.

Figure 2.38 shows, how far the actual switching point differs from the set threshold for different DAC settings. Over the range of reasonable DAC values, the deviation is in the mV range, thereby inconsequential.

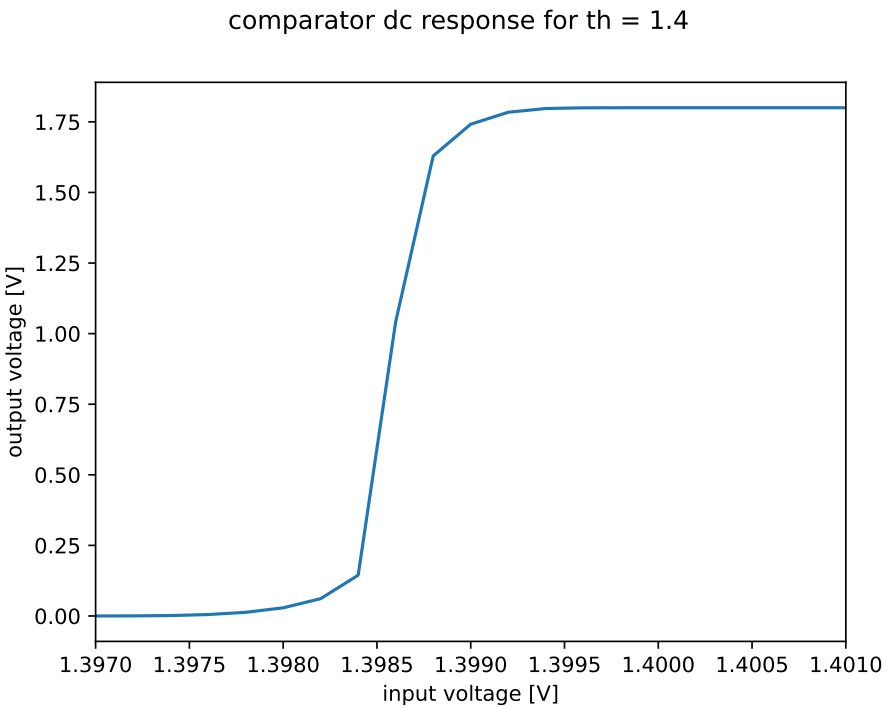


Figure 2.37: DC simulation: comparator input-output curve

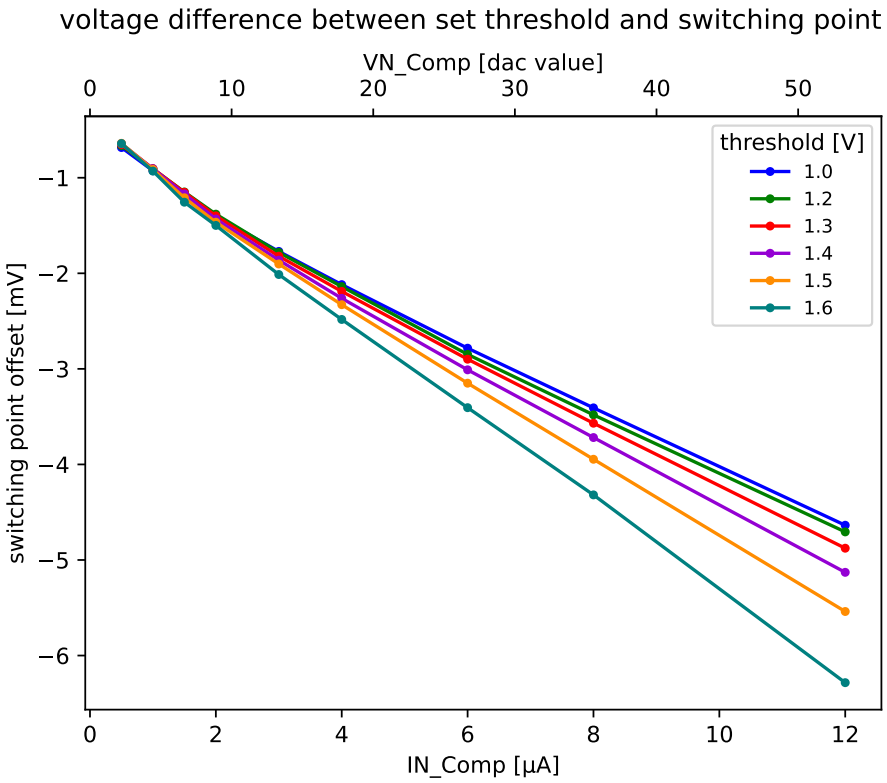


Figure 2.38: DC simulation: comparator accuracy

Comparator Delay

More important for the TDC is the the delay between input and output of the comparator. It is simulated using the SPECTRE transient simulator. Such a delay K_{cap} would appear as a constant added to equation 2.7:

$$\delta = \frac{U_{th}}{s_B} - \frac{s_A}{s_B}\left(T_{clk} - T_{hit}\right) + K_{cap} \tag{2.102}$$

However, this delay would be added to both δ_{min} and δ_{max}, resulting only in a shift of the δ-distribution:

$$\delta_{min} = \frac{U_{th}}{s_B} - \frac{s_A}{s_B}T + K_{cap} \tag{2.103}$$

$$\delta_{max} = \frac{U_{th}}{s_B} + K_{cap} \tag{2.104}$$

$$\frac{w}{T} = \frac{s_A}{s_B} \tag{2.105}$$

As the magnification is the same, the resulting time resolution does not change. For this delay to play a significant role, it would have to be both large and not constant between hits.

Figure 2.39 shows the simulated delay of the comparator. It is higher for higher values of VN_Comp and for lower values of TH_Fine. In the reasonable operating range of the circuit, the delay is between 2ns and 12ns. That corresponds to $K_{cap} < 1.5\ clock\ cycles$ of delay, which is barely significant.

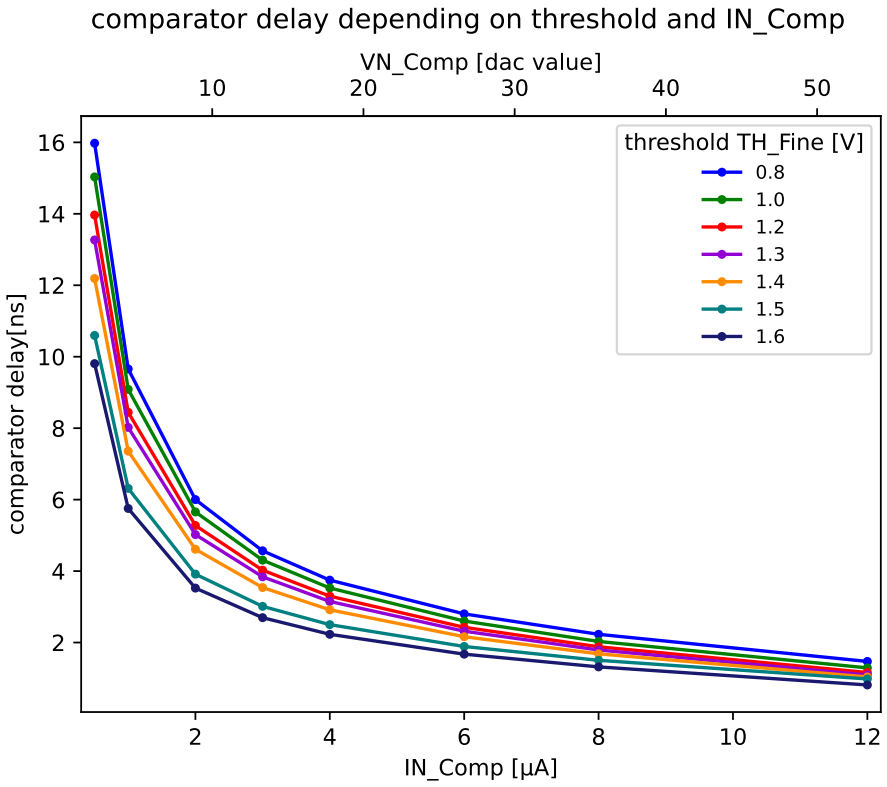


Figure 2.39: transient simulation: delay from comparator input to output

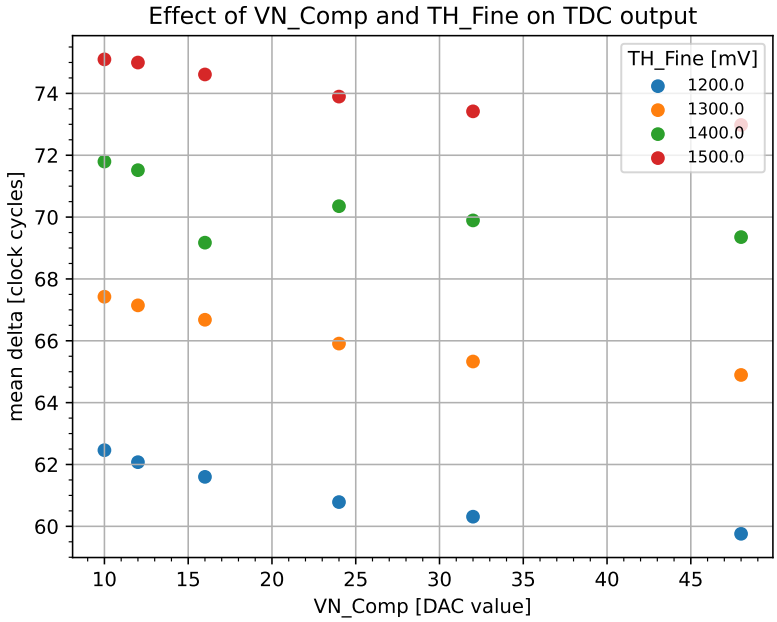


Figure 2.40: Sr90 data: influence of VN_Comp on δ. A difference in delay of 3 clock cycles is observed between low and high values.

Figure 2.40 shows the influence of VN_Comp on δ measured in SR90 data. VP_Big is set to 0, similar to the setup in section 2.4.1. Absolute values of the delay cannot be measured in this way, but the difference in delay between low and high values of VN_Comp can. This difference turns out on the order of 3 clock cycles. That is larger delay than the simulation suggests, likely due to the line capacitance not considered in simulation.

Influence of Charging Rate on Delay

Figure 2.41 shows the effect of the charging current on the delay. The comparator switches faster for higher currents. That makes sense, as higher currents move the comparator input farther from the threshold more quickly.

This effect can actually be observed in laboratory data. In the case of premature threshold crossing, the large difference between I_{Big} and I_{Small} will cause a gap in the distribution between the initial peak and the rest of the distribution, as seen in figure 2.20.

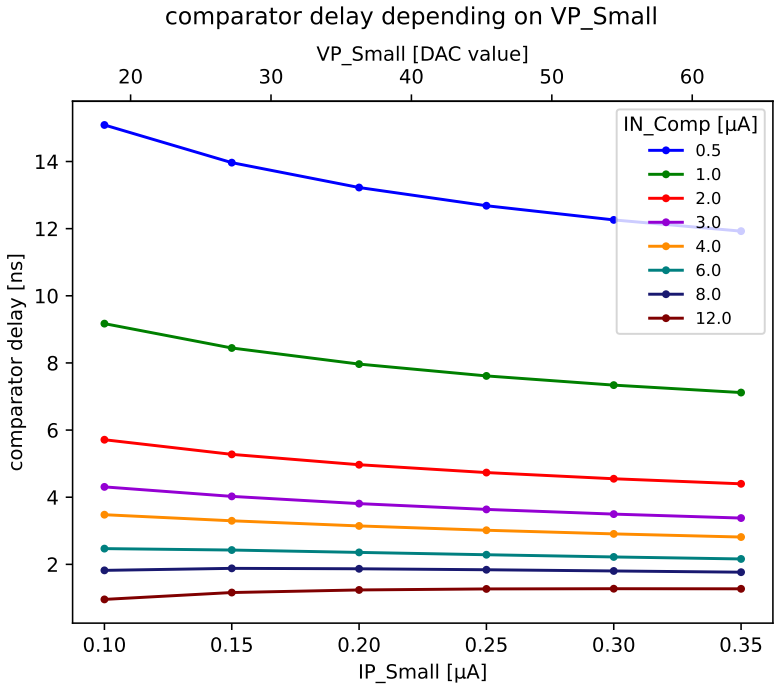


Figure 2.41: transient simulation: influence of charging current on comparator delay

2.7.4 Current Drivers

A further potential source of nonlinearity are the PMOS current drivers and the DAC circuits setting their gate voltages.

DAC Circuit

Each DAC circuit has a similar structure. A standardised current DAC produces a current linearly rising with the set digital value. This current is then fed into a series of current mirrors (see section 1.8.6), multiplying and dividing the current in the process. The multiplication factor is 1 for VP_Big and $\frac{1}{48}$ for VP_Small. Figure 2.42 shows this general structure for the example of the DAC generating the VP_Big voltage.

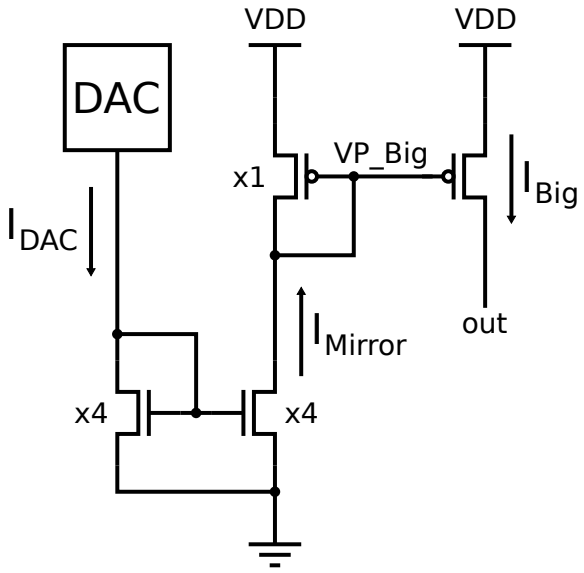


Figure 2.42: Circuit generating VP_Big voltage and I_Big current

Current Driver Linearity

The currents in equations 2.14 and 2.15 are assumed to be linearly related to the numerical DAC values set. As observed in section2.3, this assumption does not actually hold true for VP_Big.

Figures 2.43 and 2.44 show the current driver output versus the DAC input for VP_Big and VP_Small. The DAC is linear for VP_Small, though the multiplication factor does not quite match the expected $\frac{1}{48}$. The VP_Big DAC is slightly nonlinear in its low range and levels off around a setting of 40. As the kink in the voltage shows, this is due to the NMOS in the current mirror leaving saturation as U_{DS} approaches 0.

The nonlinear relation of the DAC setting and I_{Big} does not impede the linearity of TDC calibration. However, it does prevent the user from selecting VP_Big by straightforwardly using 2.19.

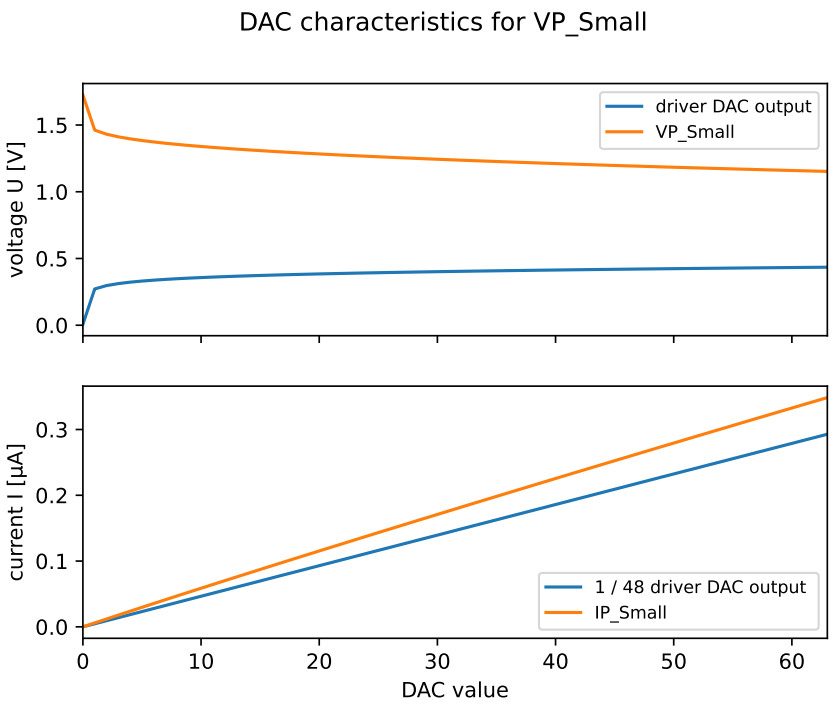


Figure 2.43: DC simulation: Generated voltage and output current for VP_Small. *top:* voltage generated by the standard DAC and resulting voltage after current mirrors. *bottom:* current output of the standard DAC and current driven in the TDC circuit

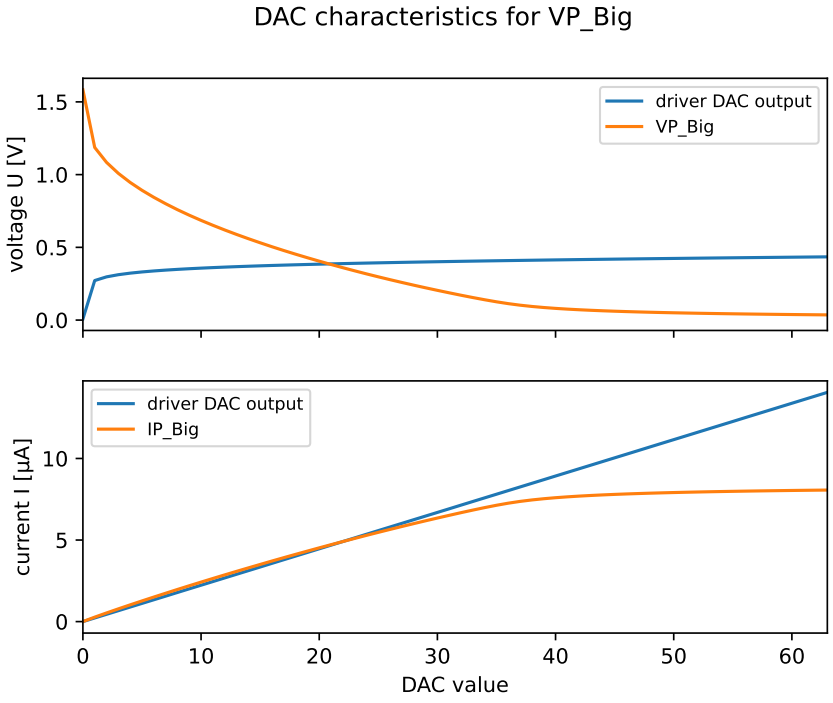


Figure 2.44: DC simulation: Generated voltage and output current for VP_Big. *top:* voltage generated by the standard DAC and resulting voltage after current mirrors. *bottom:* current output of the standard DAC and current driven in the TDC circuit

Resistance Effect

Since VP_Big and VP_Small are generated in the bias block but the TDCs are in the digital pixel cell, there is a voltage difference introduced by supply line resistance. This reduces the gate-source voltages at the current drivers, resulting in lower than expected current. This could cause a shift in operating point but no issues with linearity.

Figure 2.45 shows the effect of line resistance on current driver output. It is negligible. This result conflicts with the assessment that voltage drops across the supply lines cause the fixed pattern in pixel-to-pixel variation. Further research is needed.

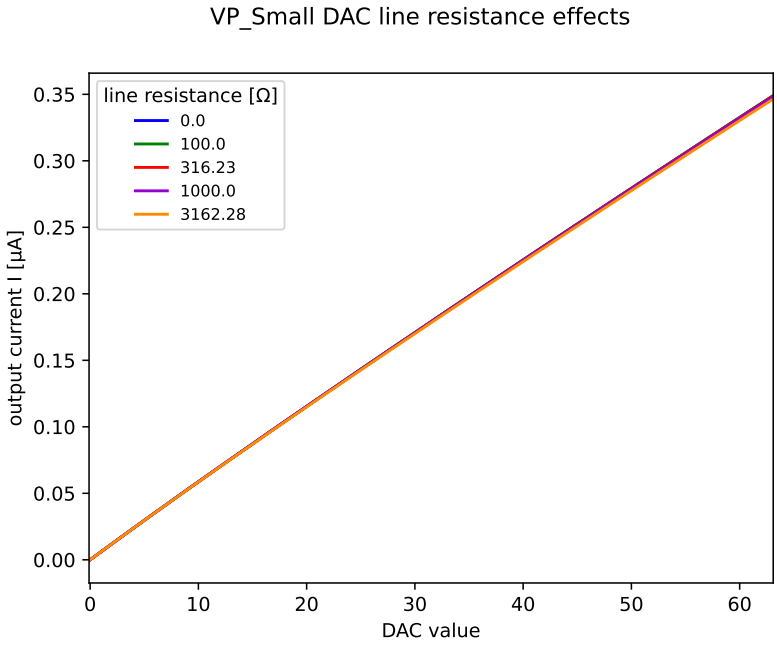


Figure 2.45: DC simulation: influence of line resistance on driver output for VP_Small

Temperature Effect

During the laboratory measurements, the temperature was neither controlled nor measured. The dominating temperature dependence in the TDC circuit is the conductivity of the current driving PMOS transistors. Simulation allows for an estimate of the scale of temperature effects.

Figure 2.46 displays the VP_Big current driver output curve for different values of temperature. For higher temperature, the driver PMOS reaches its maximum earlier but peak conductivity is reduced. The reduction in peak conductivity reflects the reduction in charge carrier mobility predicted by theory [27, p. 265]. The earlier point of levelling off reflects the increase in transistor threshold [27, p. 816].

As long as the DAC values for VP_Big stay below the point of levelling off, the variation in current is below 5% across a reasonable temperature range. If necessary, occasionally adapting the operating point will compensate temperature variation.

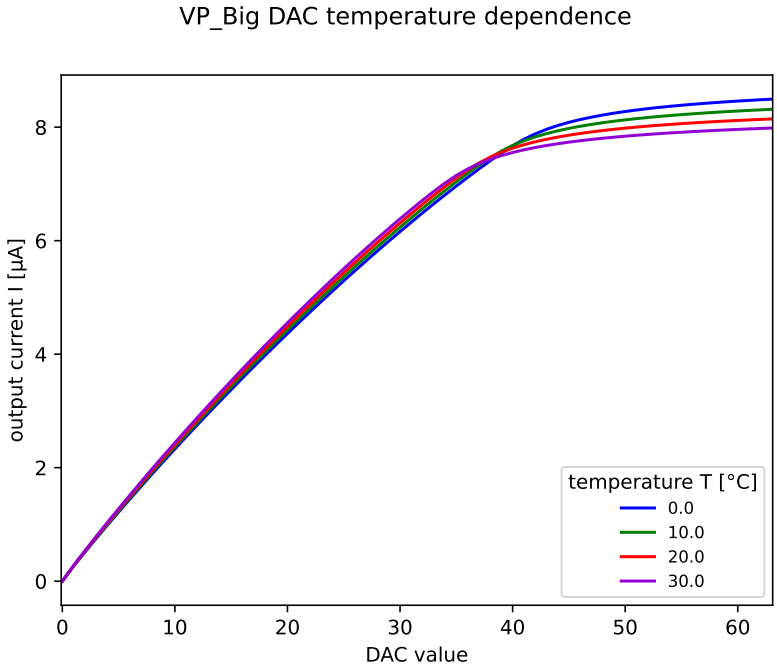


Figure 2.46: DC simulation: temperature dependence of current driver output

Voltage Dependence

The current driver outputs have so far been assumed to be independent of the voltage across the driving transistors. In reality, the current output is given by the drain-source curve of the transistor (see section 1.8.5).

Figures 2.47 and 2.48 show this relation. For low voltage at the driver output node (corresponding to high drain-source voltage), the transistor is in saturation. In this regime, the dependence of current on voltage is minimal, following equation 1.16. However, as $U_{DS} = U_{GS} - U_{th}$ the transistor leaves saturation. Beyond that point, the current rapidly falls as the voltage approaches U_{DD}, following equation 1.15.

This is highly undesirable, as the linearity between δ and T_{hit} stated in equation 2.29 requires that the charging rates 2.14 and 2.15 are constant. Therefore, the operating range needs to be set such that both current drivers stay firmly in saturation.

Whilst the VP_Small driver only leaves saturation for voltages beyond 1.6V, the VP_Big driver leaves saturation far earlier, especially for high DAC settings. In laboratory measurements, this manifests as a δ-distribution with significant accumulation at low δ.

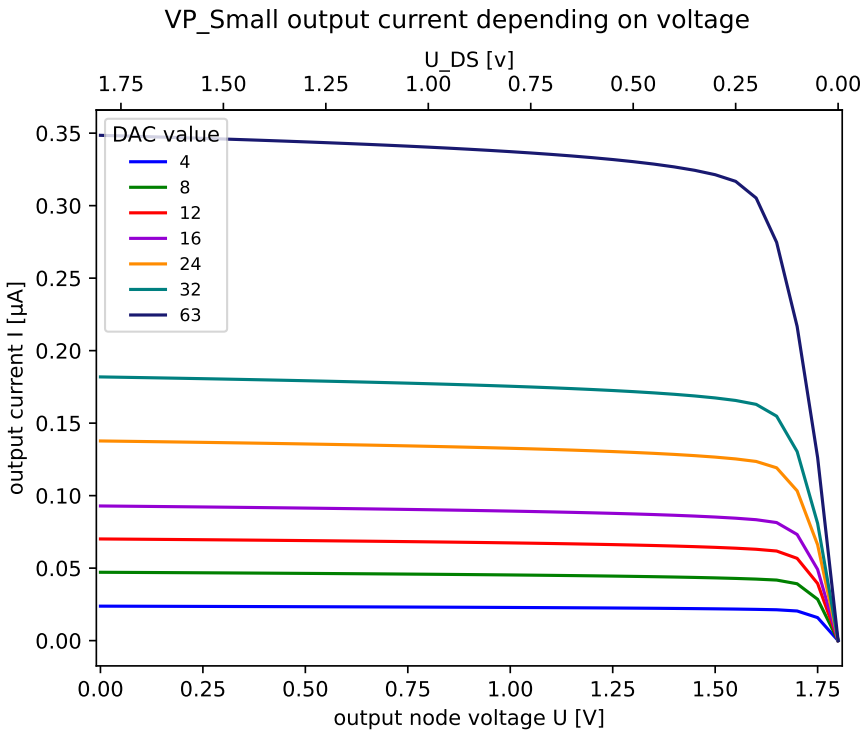


Figure 2.47: DC simulation: dependence of output current on voltage at driver output (drain side) for VP_Small

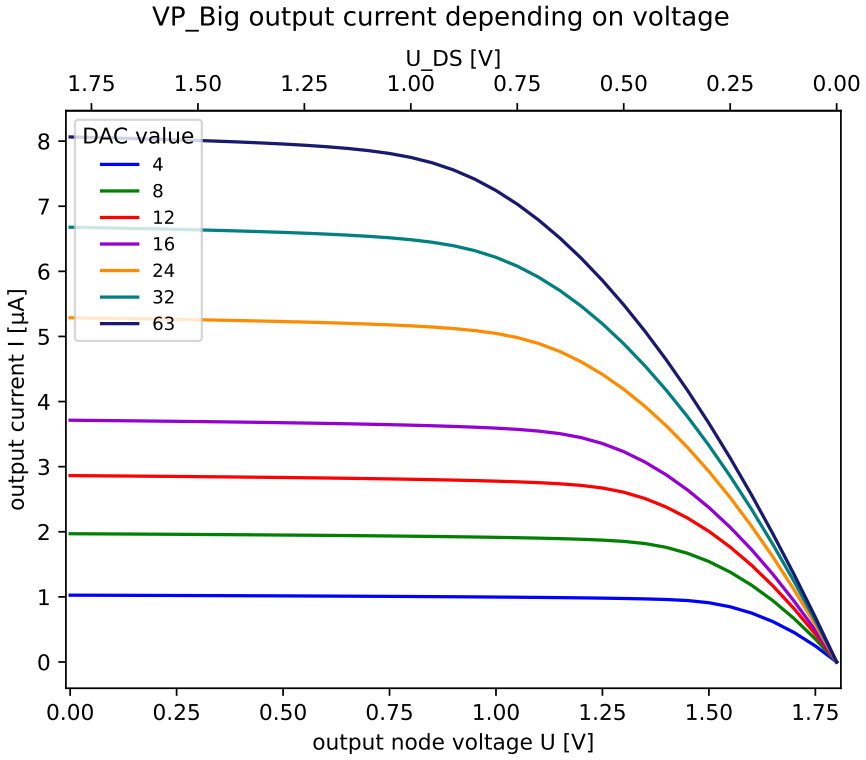


Figure 2.48: DC simulation: dependence of output current on voltage at driver output (drain side) for VP_Big

2.8 Bunching Effect

As seen in figure 2.48, at high VP_Big the current I_{Big} drops for voltages at the upper end of the operating range. At VP_Big = 16, this dropoff starts at 1.2V, inside the operating range of the circuit.

This current dropoff causes a nonlinearity, which can be seen in laboratory measurements. It bunches up the probability density, for example in the δ-distribution 2.49. It is hard to discern this nonlinearity from the random nature of the radiation. A simulation study is used to get a clearer picture of the magnitude of this effect.

Using transient simulation, a direct map $T_{hit} \mapsto TS3$ can be created. The probability density is reconstructed using

$$\rho(TS3) = \rho(hit) \left| \frac{dT_{hit}}{dTS3} \right| \tag{2.106}$$

$$= \frac{1}{T} \cdot \left| \frac{dT_{hit}}{dTS3} \right|. \tag{2.107}$$

The derivative is calculated using numerical differentiation.

Figure 2.50 shows the probability density of δ for different values of VP_Big. Each distribution has a slim peak at the end for the distribution, for high δ. This peak is a result of the exponential increase of the flipflop delay near the clock edge seen in figure 2.35. The distributions for $I_{Big} = 6\mu A$ and $I_{Big} = 8\mu A$ also show a peak at low δ. This peak corresponds to the premature threshold effect described in section 2.1.4 and observed in section 2.5.

The bunching effect can be seen for $I_{Big} = 8\mu A$, $I_{Big} = 6\mu A$ and $I_{Big} = 4\mu A$. Below $\delta = 15$ the probability density increases significantly towards the lower end of the distribution. At $I_{Big} = 8\mu A$, the density rises twofold, for the lower currents it is less pronounced.

This bunching effect is highly undesirable, as it ruins the linear relation 2.16 of T_{hit} and δ required for calibrating the TDC. A nonlinear calibration is infeasible, as the random nature of the measured δ-distributions restricts the ability to fit nonlinear functions with many parameters. Instead, high values of VP_Big need to be avoided, limiting the operating range further than the premature threshold effect.

The cause of the bunching effect is the reduction in current I_{Big}, as the PMOS transistor leaves saturation for $U_{DS} < U_{GS} - U_{th}$. By using a wider transistor, the same current can be achieved with a smaller U_{GS}, such that the transistor stays in saturation longer. This is a straightforward solution for future iterations of the circuit, investigated in section 3.1.

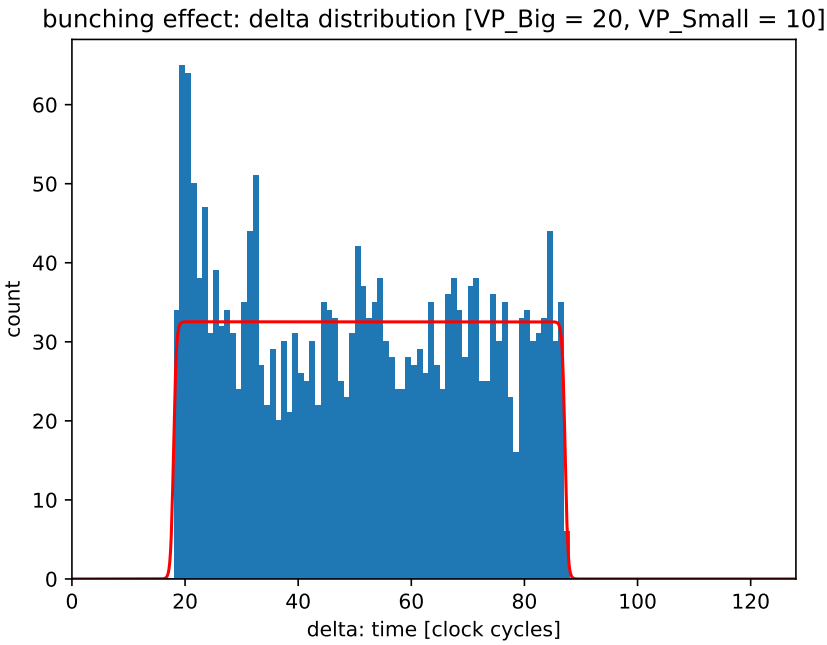


Figure 2.49: Sr90 data: Distribution of δ at high VP_Big. The distribution bunches up at low δ.

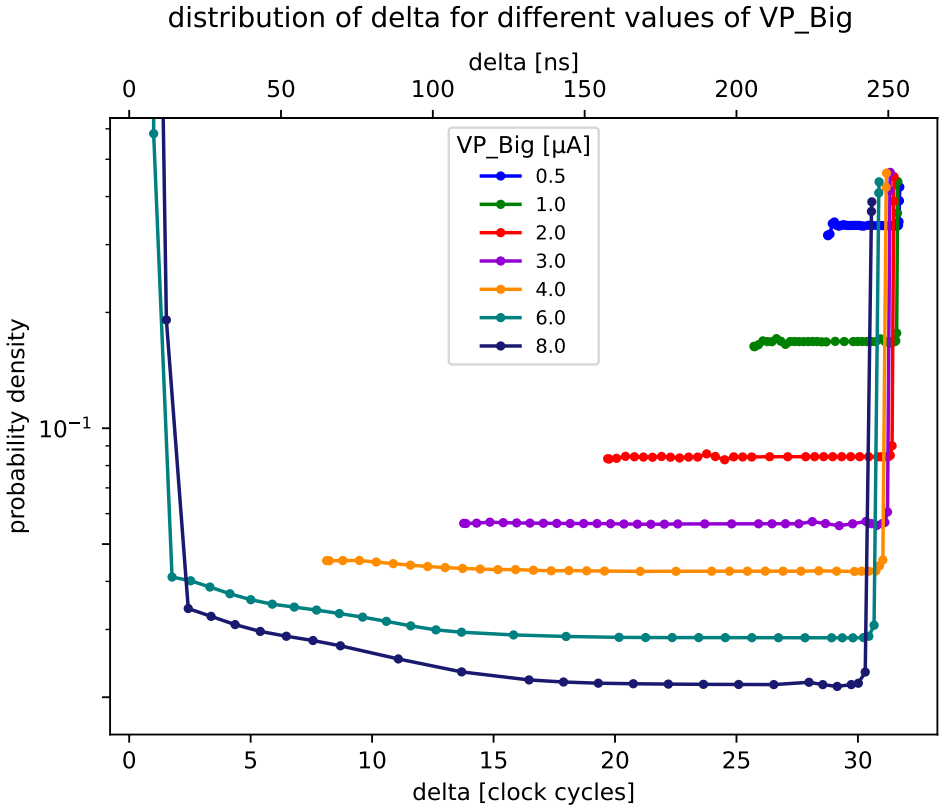


Figure 2.50: transient simulation: Simulated probability density of δ for different values of VP_Big

Chapter 3

Modified Stretched TDC

In the course of my research, I implemented several modified versions of the Stretched TDC circuit. In this section, I present these modifications and verify the circuits in simulation studies. Physical test structures will be produced in the CMHV7SF process.

The bunching effect observed in section 2.8 limits the usable operating range of the circuit. An increased range would likely enable a reduction in pixel-to-pixel variation. Section 3.1, evaluates whether larger current drivers for VP_Big improve this issue.

Apart from that, there are two obvious downsides of the existing Stretched TDC circuit. First, the achievable resolution is proportional to the dead time of the circuit, during which it cannot respond to another hit. Second, as the current drivers are on permanently, the current draw of the circuit is higher than necessary. To solve the latter issue, I created multiple variations of the Stretched TDC circuit using switched current drivers analysed in section 3.2.

3.1 Resized VP_Big driver

As discussed in section 2.8, the driver for VP_Big is too small to supply a constant current over the whole operating range. A wider transistor is expected to supply a constant current over a larger voltage range.

Modified Stretched TDC circuits using resized driver transistors for VP_Big are investigated using the SPECTRE transient simulator. Like in section 2.8, the simulated probability density is used to observe deviations from linearity.

Figure 3.1 compares the simulated probability density for the existing driver ($w_{pmos} = 500nm$) with drivers resized to $750nm$, $1000nm$ and $2000nm$. The larger drivers significantly improve the bunching, it is almost gone for $w = 2\mu m$. For more reasonable (lower) values of VP_Big, the effect is less pronounced and linearity is better overall. For the rest of this chapter, the VP_Big driver is always chosen at $w = 1\mu m$.

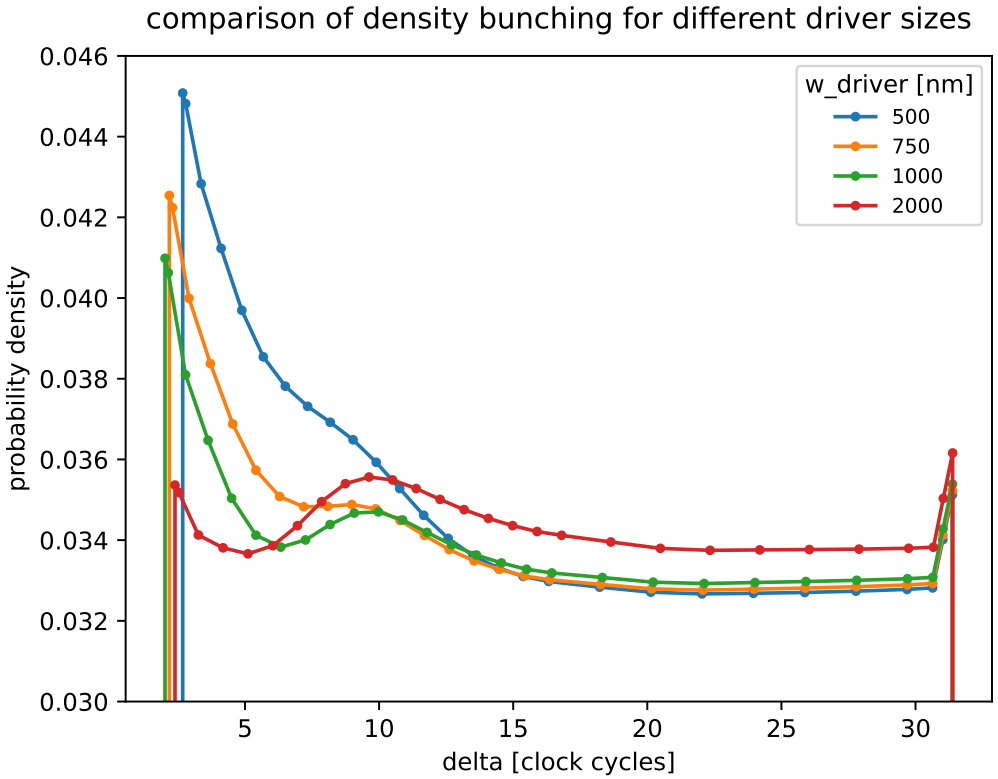


Figure 3.1: Transient simulation: Density of δ-distribution at $I_{Big} = 5.2\mu A$ for different driver sizes. Density bunching can be observed at low δ for the smaller transistors.

3.2 Switched Current Drivers

The Stretched TDC circuit draws a constant current, whether active or not. By disabling the current drivers in idle state, almost 100% of used power can be saved. I developed four variants for switched power supply circuits investigated in this section.

3.2.1 Switched Current Driver Circuits

The switch enabling the power supply is implemented as a PMOS transistor. In a digital circuit, the order of switch and driver would not matter. In an analog circuit however, it is crucial for the dynamic behaviour of the charging process.

V1: Switch First

If the switch is directly at the power supply (*switch first*), the supply node between the two transistors is quickly charged from $U = 0$ to $U \approx U_{DD}$ when the switch is activated.

For the simulation studies done in this chapter, the driver has dimensions $w \times l = 1\mu m \times 2\mu m$ and the switch has minimum length $l = 180nm$, its width to be studied. An optional capacitance is added to suppress the voltage spikes in VP_Big observed in section 3.2.3.

V2: Driver First

If the driver is directly at the power supply (*driver first*), the supply node between the two transistors is at $U = U_{DD}$ in idle state. As the switch is activated, the supply node voltage quickly drops to a value $U > U_{node}$, at which $I_{driver} = I_{switch}$.

Like for V1, the driver has dimensions $w \times l = 1\mu m \times 2\mu m$ and the switch has minimum length $l = 180nm$. An optional capacitance is added for VP_Big.

V3: Parallel V1 and V2

As observed in section 3.2.3, the voltage spike in VP_Big makes the charging process nonlinear. The spike is positive for V1 and negative for V2. This allows for the compensation of the two spikes by connecting V1 and V2 in parallel. By selecting the correct ratio of w_{V1} and w_{V2}, the voltage spike can be eliminated.

The sum of the drivers is chosen as $w_{total} = w_{V1} + w_{V2} = 1\mu m$ with the ration between them to be investigated:

$$r := \frac{w_{V1}}{w_{total}} \tag{3.1}$$

$$w_{V1} = r \cdot w_{total} \tag{3.2}$$

$$w_{V2} = (1 - r) \cdot w_{total} \tag{3.3}$$

The length for both drivers is $l = 2\mu m$. Both switches are at minimum length.

V4: Compensated V1

The remaining issue in V3 is the reduction of the operating rate cased by the V2 supply seen in figure 3.4. By using V1 as the supply and compensating with a V2 supply feeding a dummy capacitance, a highly linear charging rate can be achieved over the full operating range.

The driver of the V1 supply circuit is fixed at $w \times l = 1\mu m \times 2\mu m$. The driver of the compensatory V2 circuit is chosen at $l = 2\mu m$ and width

$$w_{V2} = \frac{1 - r}{r} w_{V1} \tag{3.4}$$

such that the ratio is again

$$r = \frac{w_{V1}}{w_{total}}. \tag{3.5}$$

The overall transistor width w_{total} in V4 is larger by a factor $\frac{1}{r}$ compared with the other circuits. This means, the power consumption is also larger by the same factor.

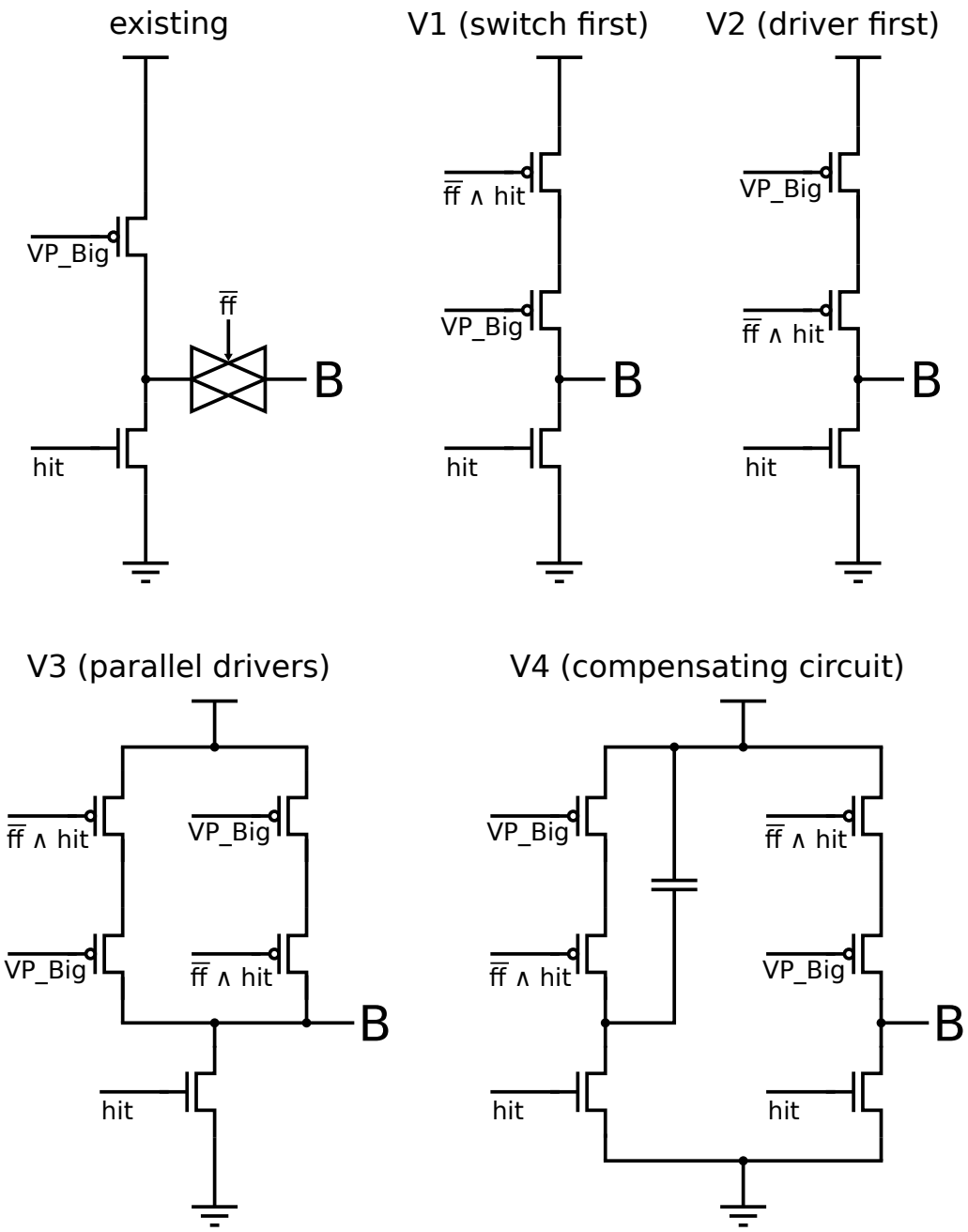


Figure 3.2: Existing switchless circuit and variants of switched current drivers. The capacitor node is designated node B, like in figure 2.2.

3.2.2 Evaluation Metric

The linearity of the charging curve stated in equation 2.7 is essential for the calibration equation 2.33 to yield accurate results. Any deviation leads to a systematic inaccuracy in time reconstruction. The quality of the supply circuits presented in section 3.2 is measured in terms of this accuracy. To do this, a linear equation $f(t) = a + bt$ is fitted to the charging curve $U(t)$. The residual

$$\Delta(t) \coloneqq U(t) - f(t) \tag{3.6}$$

can be used to measure the local miscalibration. The maximum residual

$$R = \max_{0<U(t)<U_{th}} |\Delta(t)| \tag{3.7}$$

is used as the metric measuring the quality of the circuit.

As stated in section 2.1.7, the highest realistic time magnification is $\eta = 80$. At an operating range of $U_{th} = 1.4V$, any inaccuracy above $R > \frac{U_{th}}{\eta} = \frac{1.4V}{80} = 17.5mV$ can be observed, whilst inaccuracies below that value cannot.

3.2.3 Comparing Switched Supplies V1 and V2

This section compares the switched driver variants V1 and V2. The shortcomings observed in this section inform the construction of variants V3 and V4.

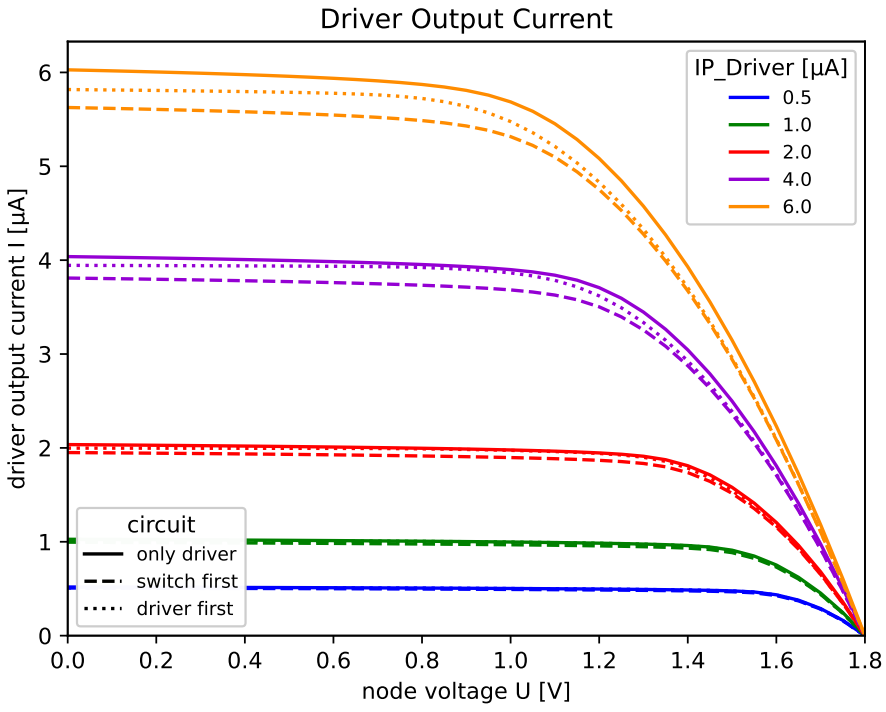


Figure 3.3: DC simulation: Dependence of current supply output on voltage and current set by the DAC. Comparison of V1 and V2 with switchless supply.

Driver Output Current

Figure 3.3 shows the steady state current output for the switched supply variants V1 and V2. The voltage drop across the switch transistor reduces the voltage across the driver transistor. In V2, the switch effectively functions as a cascode, reducing the slight drain-source dependence caused by the Early effect (see section 1.8.5). However, it also causes an earlier and sharper current dropoff for V2.

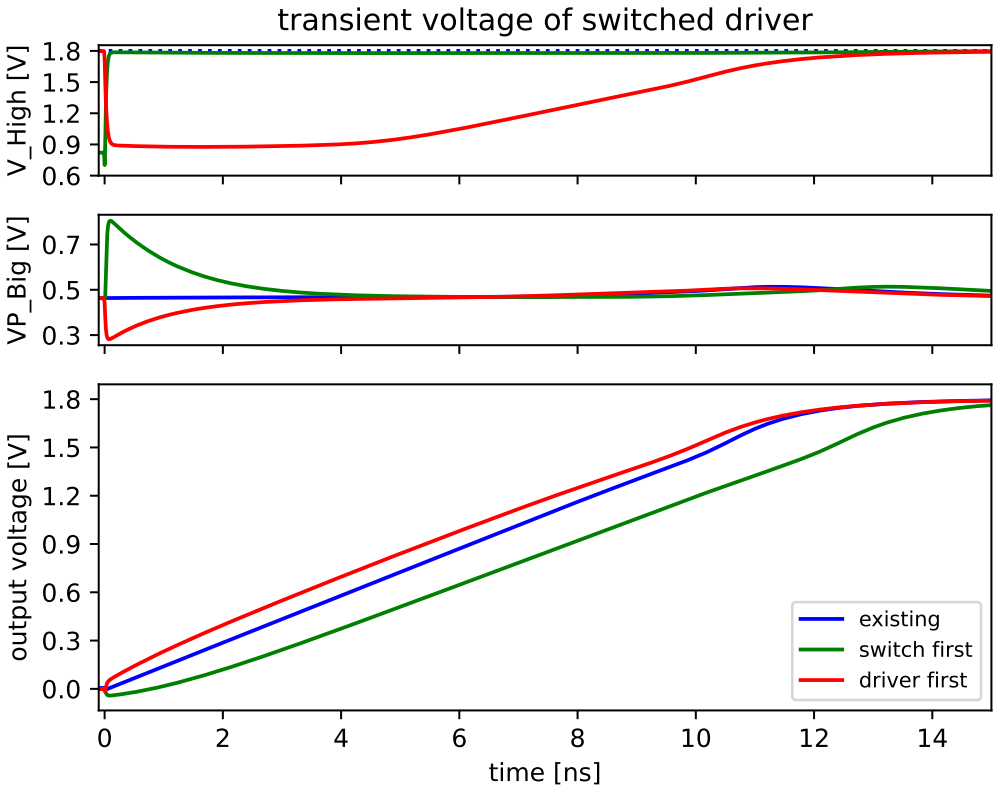


Figure 3.4: Transient simulation: Charging dynamics of switched supplies V1 and V2 compared with switchless supply at typical working point. *bottom*: voltage at the capacitor node (node B). *middle*: VP_Big DAC voltage. *top*: Voltage at the supply node between driver and switch.

Transient Behaviour

Figure 3.4 shows an example of the charging curve for V1 and V2 driver circuits. There are three main differences to the switchless circuit.

First, there is a peak in the VP_Big DAC voltage. This peak corresponds to the charge released by the changing capacitance of the driving transistor. As the switch is enabled in the V1 circuit, the source voltage at the driver transistor increases. In the V2 circuit, it instead drops. This opposite behaviour of V1 and V2 yields the opposite direction spikes observed. The spikes in VP_Big take half a clock cycle to settle back to normal, which corresponds to the nonlinearity in the charging curve observed for the switched supplies in the first 3ns.

Second, the voltage at the capacitor node itself experiences a step. V1 experiences a negative step, whilst V2 experiences a positive one. The effect of this step on performance is negligible, as the step is almost instantaneous. The positive step is for V2 reduces the operating range by approximately 50mV.

Third, supply V2 experiences a reduced charging rate above 1V, causing a nonlinearity that effectively reduces the usable operating range. This is a more pronounced version of the density bunching investigated in section 2.8. Unlike in V1, the current through the switch is limited by the driver. As seen in the supply node voltage (figure 3.4, top), the switch leaves saturation at 900mV. Beyond this point, the voltage across the driver is reduced, lowering the current and causing the nonlinearity.

Voltage Spike

Figure 3.5 shows the measured absolute amplitude of the voltage spike observed in VP_Big. The spike is about twice as large for the V1 circuit, compared to V2. An artificially added capacitance can suppress the voltage spike. The capacitance needed to significantly reduce the spike is at the scale of the PMOS capacitor being charged at node B (compare figure 2.32).

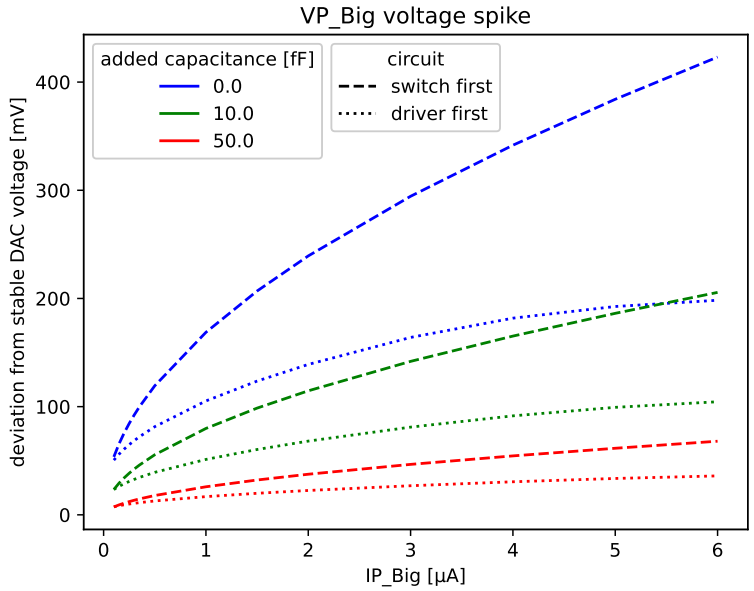


Figure 3.5: Transient simulation: Dependence of voltage spike absolute amplitude on driven current and added stabilising capacitance

Linearity

Figure 3.6 shows the residuals of a linear fit made to the charging curves. The residuals of V1 and V2 circuits are significantly higher than for the switchless circuit, around 50mV. As stated in section 3.2.2, an inaccuracy of this size is significant. The fact that the residuals for V1 and V2 are opposite but similar in magnitude is used in variants V3 and V4 to recover accuracy.

Figure 3.7 shows the linearity, measured in terms of maximum fit residual (see equation 3.7). High capacitance at VP_Big is generally favourable to suppress the nonlinearity induced by the peak in VP_Big. Whilst for V1 there is no clear relation between switch size and residuals, V2 favours a small switch.

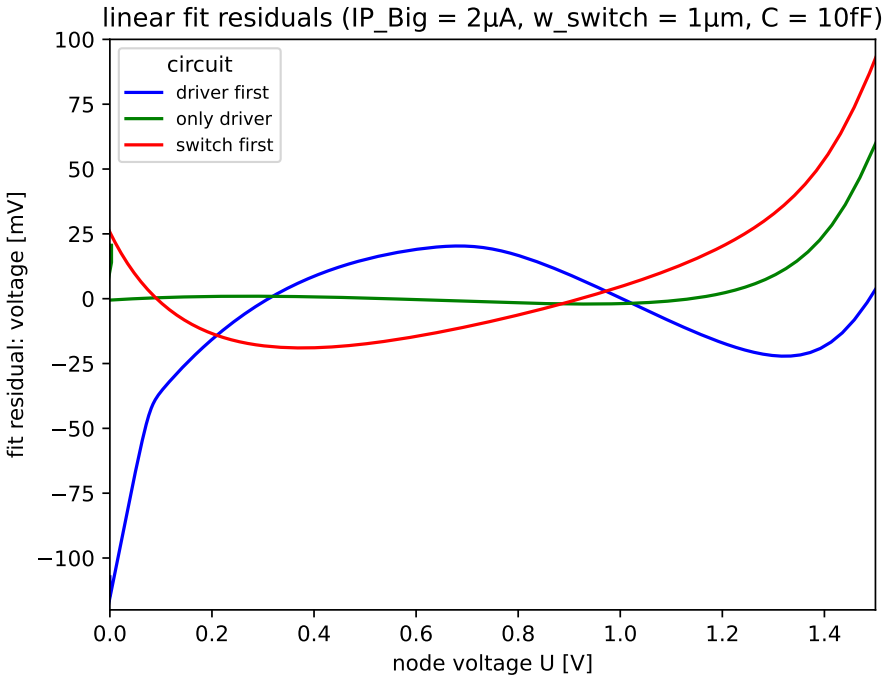


Figure 3.6: Transient simulation: Residuals $\Delta(t)$ of the charging curve fits for variants V1 and V2 compared with the switchless circuit

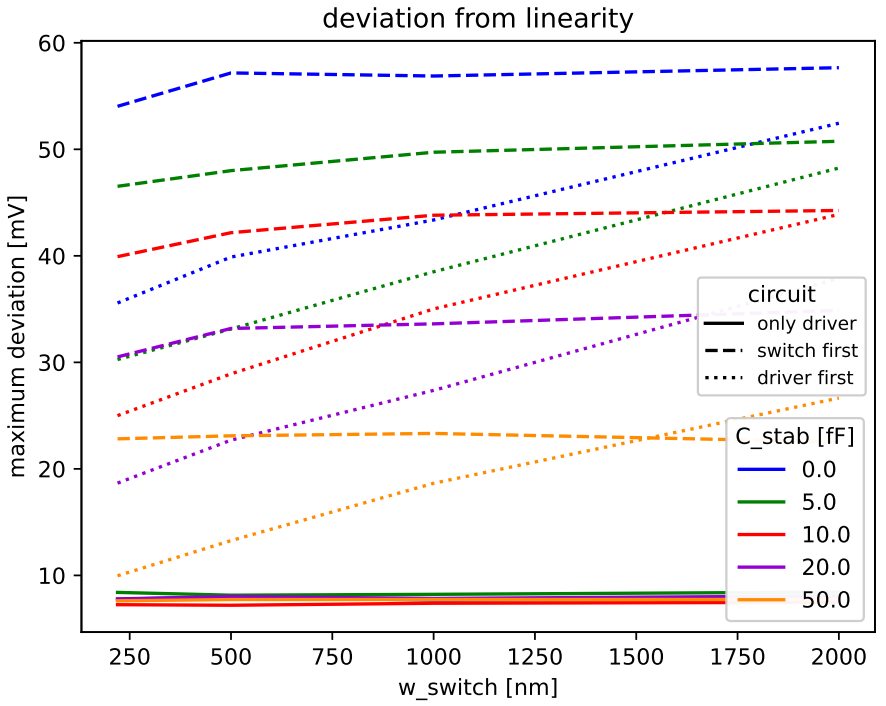


Figure 3.7: Transient simulation: Influence of capacitance and switch size on linearity, measured as maximum fit residual R

3.2.4 Investigation of V3 and V4

Figure 3.8 shows the charging curve for variants V3 and V4 compared to the switchless circuit for the ratio $r = 0.4$ (compare equations 3.1 and 3.4). The linearity looks significantly improved over V1 and V2. The main difference between V3, V4 and the switchless circuit is in the voltage step at $t = 0$. The negative voltage step of V4 is favoured over the positive step of V3. As can be seen in the top graph, this choice of r mostly eliminates the peak in VP_Big observed in figure 3.4.

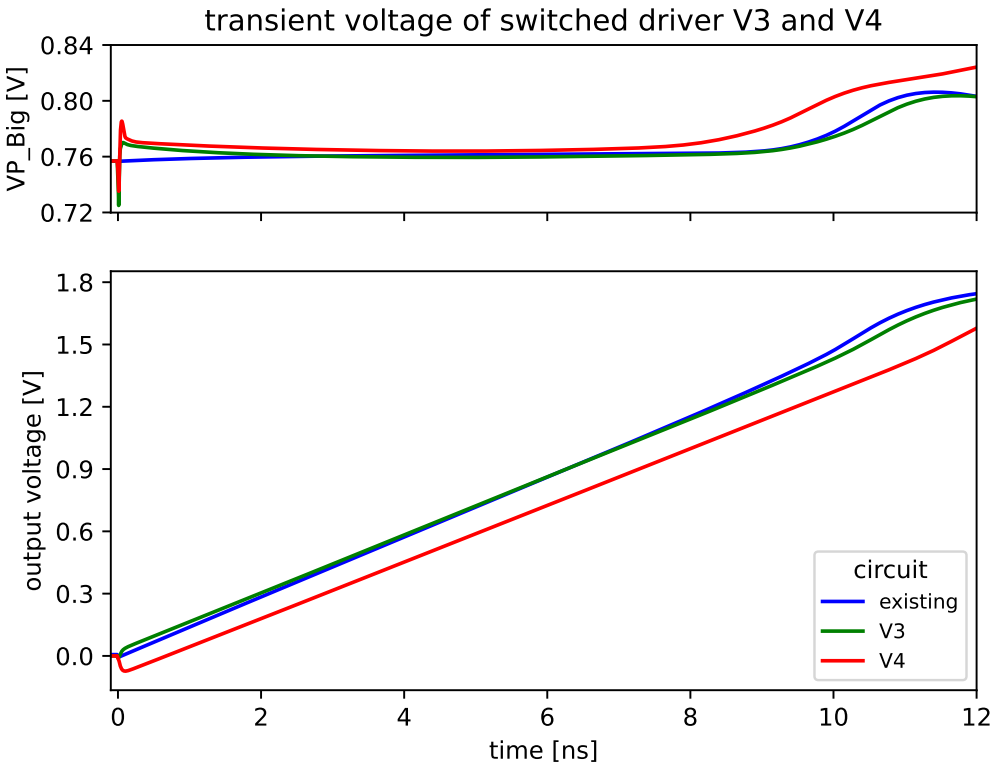


Figure 3.8: Transient simulation: Charging dynamics of switched supplies V3 and V4 compared with switchless driver at typical working point. *bottom*: voltage at the capacitor node. *top*: VP_Big DAC voltage.

Figure 3.9 shows the fit residuals for V3 and V4. Both circuits perform significantly better than V1 and V2, with residuals below 2mV corresponding to an inaccuracy below the sampling threshold stated in section 3.2.2. Notably, circuit both V3 and V4 even increases the usable operating range over the switchless circuit.

Figure 3.10 shows the influence of the ratio r on the residual R. A value of $r \approx 0.4$ delivers the best results. This optimum ratio has a slight dependence on VP_Big. The graph shown is at $I_{Big} = 4\mu A$, corresponding to a typical operating point. Even at a slightly different operating point the linearity is still quite good.

A similar residual plot determines optimal sizes for the switch transistors at w_switch_V1 = 1µm and w_switch_V1 = 220nm, matching the observations in figure 3.7.

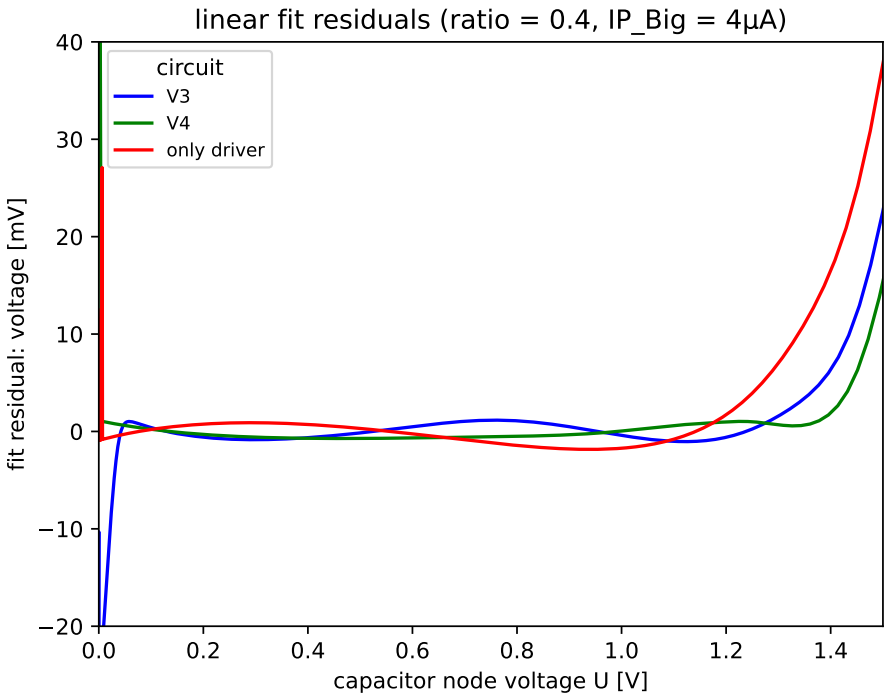


Figure 3.9: Transient simulation: Residuals of charging curve fits for the variants V3 and V4 compared with switchless circuit.

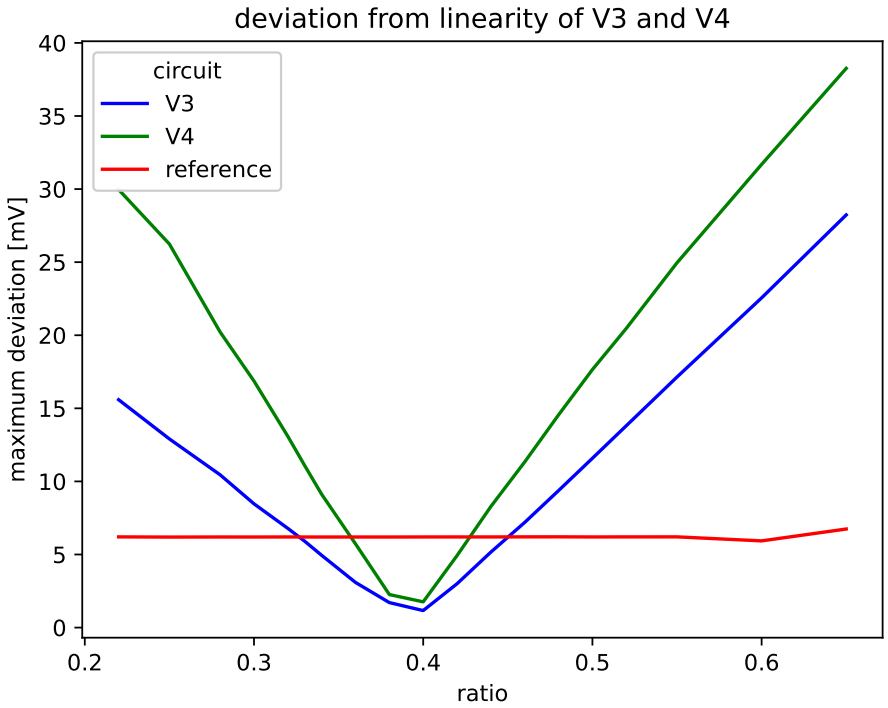


Figure 3.10: Transient simulation: Influence of driver size ratio on linearity, measured as maximum fit residual. Taken at $I_{Big} = 4.0\mu A$.

Chapter 4

Delay Chain TDC

The second class of TDC circuits investigated in this thesis uses a chain of delay elements. Such a chain transforms time information into a discrete position. This chapter compares various variants of delay elements. In simulation studies time resolution and current draw are evaluated for each variant. The 180nm CMHV7SF and 130nm SG13G2 technologies are compared in performance. Finally, the overall feasibility of this approach in comparison with the Stretched TDC circuit is discussed.

4.1 Delay Chain Operation

The delay chain TDCs investigated are all operated in the same way. The *hit* signal marks the start of the time interval to be measured and the *clk* signal its end. The *hit* signal is fed into the first delay element, starting the measurement at the signal flank. The signal propagates though the delay cells, sequentially flipping them. At the clock flank, the current position of the signal is read out.

The readout process can take two shapes. Either the signal propagation is halted after the clock flank, locking the signal position in place. Or the readout branch circuit is disconnected from the chain after the flank, effectively functioning as a flipflop arrangement.

The position x of the signal is given by the two neighbouring delay cells with equal digital state. The ToA is reconstructed from the output distribution of x measured for random hits by linear interpolation. The procedure is similar to the algorithm described in section 2.1.5 for the Stretched TDC,

$$w \coloneqq x_{max} - x_{min} \tag{4.1}$$

$$t = \left(TS1 + \frac{x_{max} - x}{w} \right) T \tag{4.2}$$

4.2 Delay Chain Architecture

A delay chain is made out of identical *unit cells* linked output to input. The time resolution is the delay from input to output in a single unit cell. As shown in figure 4.1, a unit cell consists of two components: A delay element connecting input and output and a branch circuit featuring readout and secondary functionality. In the rest of this section, various options for delay- and branch circuit are discussed.

The core tradeoff in delay chain TDCs is between time resolution and power consumption. The time resolution reflects the ratio of the current driven by the delay element and the parasitic capacitance being charged. By using large components in the delay element and small

components elsewhere, time resolution can be optimised. On the other hand, a large delay element drives a larger current, using more power. A detailed mathematical model is developed in section 4.3.

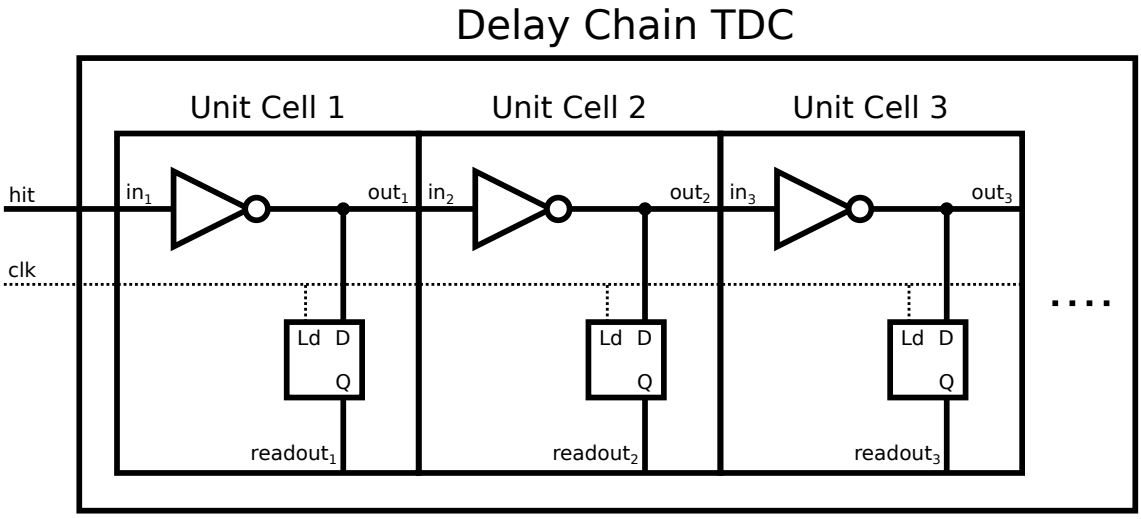


Figure 4.1: Structure of a delay chain TDC. This unit cell uses an inverter as delay element and a latch as readout element.

4.2.1 Delay Element

The delay element defines the unit cell delay by driving a current against the parasitic capacitance. Three delay are investigated:

1. Inverter
2. Switched Inverter
3. Latch

The differences are in their ability to drive current, the parasitic capacitance and the complexity of the readout circuit.

Inverter

A simple inverter (see section 1.8.7) has low parasitic capacitance and drives a high current, since it uses the minimum number of transistors.

Switched Inverter

A switched inverter (see figure 4.2) features two transistors to enable or disable the inverter. If enabled, it functions like an inverter. If disabled, the output is preserved in a high impedance state. This is convenient as it halts propagation, locking the signal in place.

The switched inverter has the same parasitic capacitance as the normal inverter. The current driven by a switched inverter is smaller compared to the inverter, as the current has to pass two transistors rather than just one.

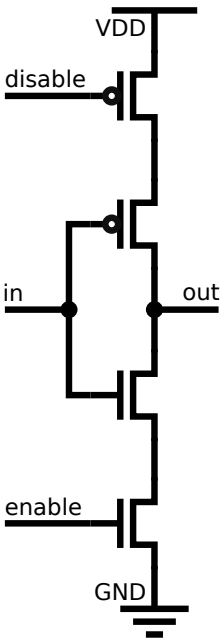


Figure 4.2: Switched inverter

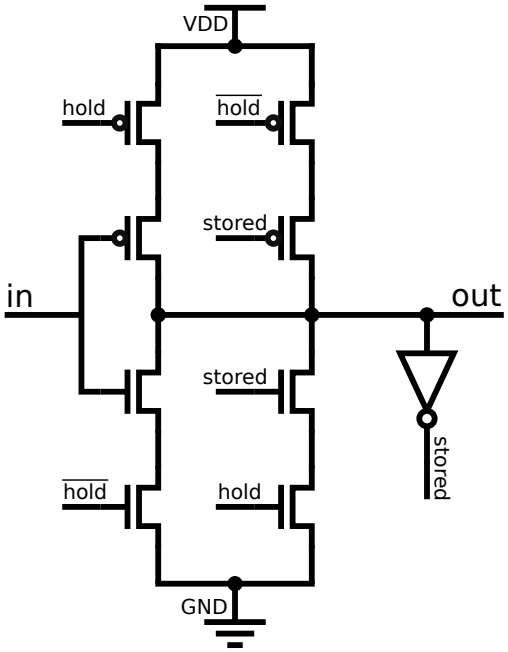


Figure 4.3: 10 transistor latch circuit

Latch

With active *load* signal (=inactive *hold*), a latch propagates its input signal to the output (compare section 1.8.9). By using a latch as delay element, a separate readout branch can be omitted, as it is integrated in the latch. This allows for a very simple readout architecture.

On the downside, the latch has more transistors than the other delay elements, resulting in higher parasitic capacitance. The latch circuit used (see figure 4.3) is made up of an inverter and two switched inverters. This means, the current is the same as for a switched inverter in isolation.

4.2.2 Branch Circuit

The branch circuit serves two functions. Firstly, it contains any supplementary functionality, such as counters and feedforward circuits. Secondly, it provides the readout circuit, effectively working as a flipflop (compare section 1.8.10).

For good time resolution, the branch circuit needs to minimise the capacitive load on the delay chain. Therefore, no more than two transistors are used to tap into the chain for each branch circuits.

Circuits within the branch contribute to the overall power budget. For this reason, the number of transistors switching with every pass of the signal in the chain needs to be minimised. To do that, any readout logic has to be isolated from the state of the chain using a latch circuit.

Transmission Gate

A transmission gate can be used as the first stage of a flipflop arrangement. It requires the least number of transistors, however it directly diverts current from the delay element to the readout branch, slowing down the signal propagation.

Switched Inverter

By tapping the chain with a switched inverter, the chain is loaded only capacitively. This is an improvement over the transmission gate, whilst otherwise working equivalently.

Latch

The delay chain can directly be tapped using a latch. This yield the arrangement of figure 1.13. The downside is an increase in power consumption, as the latch contains a higher internal parasitic capacitance.

4.2.3 Common Design Parameters

The investigated unit cells have four parameters to be investigated.

The pmos to nmos ratio mentioned in section 1.8.5

$$\alpha := \frac{w_{PMOS}}{w_{NMOS}}, \tag{4.3}$$

needs to be chosen correctly, so that the positive and negative flank of the delay element have the same delay.

The chain to readout ratio

$$\beta := \frac{w_{chain}}{w_{readout}} = \frac{w_{chain}}{w_{min}}, \tag{4.4}$$

corresponds to the balance between resolution and power consumption.

The switched inverter has a pair of transistors for enable and disable. These transistors cause a voltage drop, reducing the driven current. The larger these transistors are, the closer the current output will be to the simple inverter. The ratio

$$\gamma := \frac{w_{enable}}{w_{chain}} \tag{4.5}$$

measures this size. This parameter exists for switched inverter and latch.

Lastly, the supply voltage U_{DD} strongly influences the driven current and thereby both delay and power consumption.

4.2.4 Investigated Unit Cells

In the course of my research I investigated 5 unit cell circuits. Table 4.4 compares the designs. Since

$$C = \varepsilon \frac{wl}{d} \sim w, \tag{4.6}$$

the sum width of all gates being charged is an estimate for the relative performance of the circuits. The best performance is expected for UC2, as it minimises both capacitance in chain and overall capacitance.

circuit	delay cell	branch cell	parasitic gates in chain $[(1+\alpha)w_{min}]$	parasitic gates in branch $[(1+\alpha)w_{min}]$
UC1	inverter	latch	$\beta+1$	3
UC2	inverter	switched inverter	$\beta+1$	1
UC3	inverter	transmission gate	$\beta+2$	0
UC4	switched inverter	switched inverter	$\beta+1$	1
UC5	latch	–	$\beta+1$	2

Figure 4.4: List of unit cells investigated and approximate parasitic capacitance in terms of gate size w. The capacitance is stated in terms of the scale parameters α and β.

4.2.5 Ring Oscillator

In a linear delay chain, the space required by the components is antiproportional to the time resolution achieved. To achieve a resolution of 25ps with the 8ns clock signal requires a minimum of

$$n = \frac{T}{\tau} = \frac{8ns}{25ps} = 320 \tag{4.7}$$

identical delay elements.

By arranging the delay elements in a ring shape, this number can be significantly reduced. Instead, the number of laps is counted using a counter circuit. For example, 15 delay elements and a 4bit counter are sufficient in this scenario.

A ring oscillator has been simulated in SG13G2, using these numbers. The concept has been verified successfully but is not investigated quantitatively beyond that.

4.2.6 Precharged Delay Chain

The delay element can be sped up by using a feedforward circuit, precharging the output side of an inverter ahead of the arrival of the signal. The output of unit cell n-3 can be used to precharge cell n.

A precharge circuit requires a significant increase in current supplied to the TDC. As observed in section 4.4, the delay chain TDC already has a significantly higher power consumption than the Stretched TDC circuit. A feedforward-precharge solution would increase that value by a factor of 3 or more.

Preliminary simulations of a precharged delay chain have shown time resolutions down to 17ps in SG13G2. Because of the power consumption concerns (seen for example in [17]), it is not investigated further.

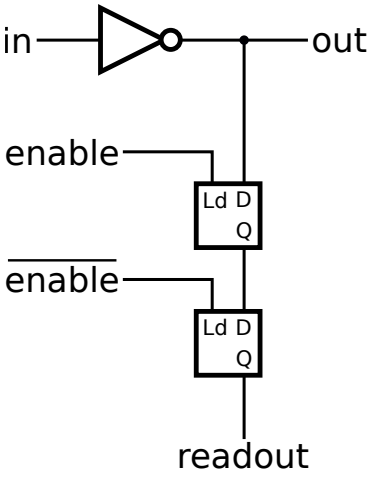


Figure 4.5: UC1 (inv / latch)

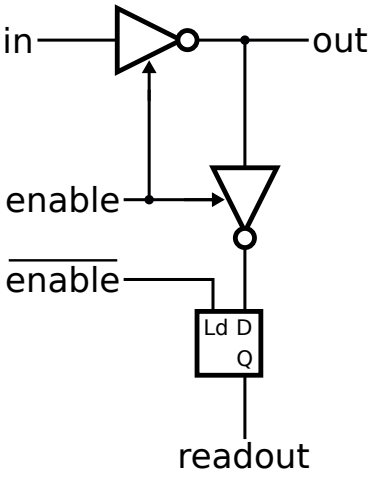


Figure 4.6: UC4 (sinv / sinv)

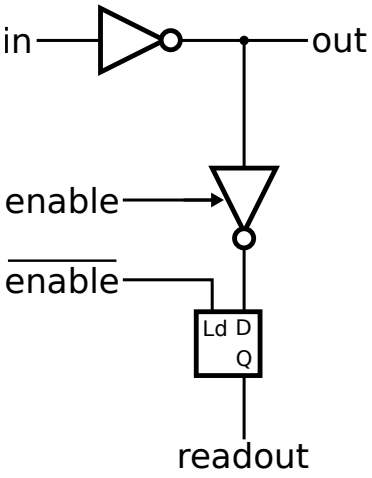


Figure 4.7: UC2 (inv / sinv)

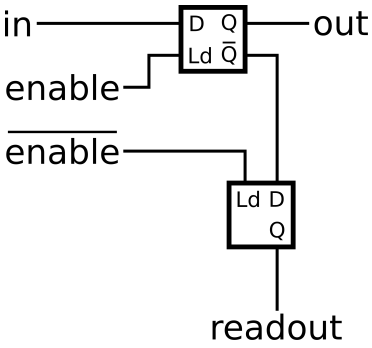


Figure 4.8: UC5 (latch)

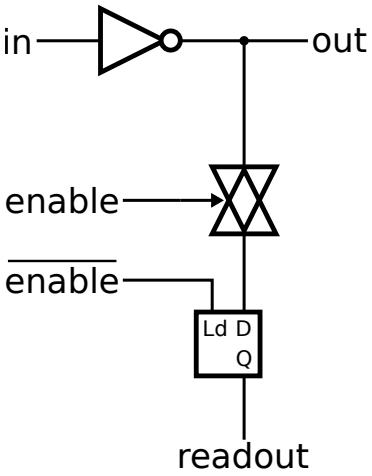


Figure 4.9: UC3 (inv / tgate)

4.3 Mathematical Model

This section presents a simplified mathematical model relating the delay τ and the power consumption P of a unit cell with the physical parameters of the circuit.

4.3.1 Model Simplifications

The switching process of an inverter involves charging the parasitic capacitance on its output. The exact relation between time and voltage is a nonlinear differential equation, defined by the transistor equations 1.15 and 1.16 and the differential capacitance equation 1.13. Since the inverter output is also the input of the next inverter in the chain, this yields a set of coupled equations,

$$\dot{U}^{(n)} = \frac{I_D\left(U^{(n-1)}, U^{(n)}\right)}{C_d\left(U^{(n-1)}, U^{(n)}, U^{(n+1)}\right)} \tag{4.8}$$

This set of equations has a highly nonlinear solution. The exact solution however is not required to understand the delay chain.

After the inverter input is fully charged, a charge Q is accumulated on the parasitic capacitances. Assuming constant capacitance,

$$Q \coloneqq CU_{DD}. \tag{4.9}$$

To simplify the charging rate, define an effective value

$$I_{eff} \coloneqq \frac{Q}{\tau} = \frac{CU_{DD}}{\tau}. \tag{4.10}$$

The time resolution then simply is

$$\tau = \frac{CU_{DD}}{I_{eff}}. \tag{4.11}$$

4.3.2 Parasitic Capacitance

The capacitance charged by the driving current is made up from many parasitic capacitances. The dominating capacitances are the gate capacitances of the transistors. The gate size of the next delay element in line scales with the driving transistor, whilst the tap for the readout branch does not.

The gate capacitance can be approximated by the plate-to-plate capacitance (equation 1.14).

$$C_G \approx \varepsilon\frac{A}{d} = \varepsilon\frac{wl}{d} \tag{4.12}$$

The driven capacitance can therefore be written as

$$C_{chain} = C_{driver} + C_{rest} \equiv k_C \cdot w_{driver} \cdot l_{driver} + C_{rest} \tag{4.13}$$

4.3.3 Transistor Current

The transistor for a significant part of the switching process is in strong inversion ($U_{GS} > U_{th}$) and in saturation ($U_{DS} > U_{GS} - U_{th}$). In that case, the drain current charging the parasitic capacitances follows equation 1.16. For sufficiently high supply voltage, the scaling can be approximated as

$$I_D \approx \frac{\kappa}{2} \cdot \frac{w_{driver}}{l_{driver}} \left(U_{GS} - U_{th}\right)^2 . \tag{4.14}$$

The effective current can be written as

$$I_{eff} \equiv k_I \frac{w_{driver}}{l_{driver}} \left(U_{DD} - U_{th}\right)^2 . \tag{4.15}$$

4.3.4 Time Resolution

Combining the equations for capacitance and current yields

$$\tau = \frac{C_{chain} U_{DD}}{I_{eff}} \tag{4.16}$$

$$= \frac{(k_C \cdot w_{driver} \cdot l_{driver} + C_{rest}) \cdot l_{driver}}{k_I w_{driver}} \cdot \frac{U_{DD}}{\left(U_{DD} - U_{th}\right)^2} \tag{4.17}$$

$$= \frac{k_C}{k_I} l_{driver} \cdot \left(l_{driver} + \frac{C_{rest}}{w_{driver} \cdot k_I} \right) \cdot \frac{U_{DD}}{\left(U_{DD} - U_{th}\right)^2} \tag{4.18}$$

The lesson are the ones mentioned in section 4.2. For better time resolution,

- use minimum length transistor
- use wide driver transistors
- minimise parasitic capacitance C_{rest} using minimum size transistors for the readout branch

The threshold voltage and maximum supply voltage are given by the process node. However, it is possible to reduce the supply voltage for reduced power consumption.

4.3.5 Current and Power Consumption

The energy required to flip the state of a single unit cell is constant. It corresponds to accumulating a charge Q on the sum parasitic capacitance C_{tot} of the components. In addition to the in-chain capacitance C_{chain} driven by the delay cell, this includes the parasitic capacitance C_{branch} of all transistors in the readout branch not isolated by a latch.

$$W = \frac{1}{2} C_{tot} U_{DD}^2 \tag{4.19}$$

$$P = \frac{W}{\tau} = \frac{1}{2} \frac{C_{tot}}{C_{chain}} U_{DD} I_{driver} \tag{4.20}$$

$$= \frac{1}{2} \left(1 + \frac{C_{branch}}{C_{chain}} \right) U_{DD} I_{driver} \tag{4.21}$$

To minimise power consumption, the readout capacitance needs to be as small as possible. This involves two optimisations.

Firstly, choose transistors in the readout branch at minimum size. Secondly, avoid unnecessary elements in the branch being flipped. The readout logic is isolated behind a latch for this reason. Any necessary functionality that needs to monitor the live state of the chain, like counters or feedforward, contributes to the power budget.

4.3.6 Scaling Laws

Further simplification yields general scaling laws. Whilst these are not exact equations, the approximate scaling behaviour is observable in simulation.

Capacitance Scaling

Assuming the driving transistor dominates the capacitance,

$$C \approx \varepsilon \frac{wl}{d} \tag{4.22}$$

$$\sim wl \tag{4.23}$$

This approximation assumes that other parasitics are negligible, so it is more accurate for larger transistors. When comparing different process nodes, the layer thickness needs to be taken into account.

Transistor Current Scaling

Assuming low threshold voltage, the transistor current scales as

$$I_D \approx \frac{\kappa}{2} \cdot \frac{w}{l} \left(U_{GS} - U_{th}\right)^2 \tag{4.24}$$

$$\approx \frac{\kappa}{2} \cdot \frac{w}{l} U_{DD}^2 \tag{4.25}$$

$$\sim \frac{w}{l} U_{DD}^2. \tag{4.26}$$

This approximation inevitably fails as the supply voltage goes near or below U_{th}. When comparing different process nodes, the difference in transconductance parameter κ and threshold U_{th} needs to be considered.

Time Resolution

Using equation 4.11 for the delay, the scaling of the inverter delay can be calculated.

$$\tau = U \frac{C}{I} \tag{4.27}$$

$$\sim U \frac{wl}{\frac{w}{l} U^2} \tag{4.28}$$

$$= \frac{l^2}{U} \tag{4.29}$$

Power Consumption

The current draw and power consumption scale as

$$I \sim \frac{w}{l} U^2 \tag{4.30}$$

$$P = UI \tag{4.31}$$

$$\sim U \cdot \frac{w}{l} U^2 \tag{4.32}$$

$$= \frac{w}{l} U^3. \tag{4.33}$$

Using equation 4.27, current draw and power consumption can be expressed in terms of the desired time resolution.

$$I = \frac{Q}{\tau} = \frac{CU}{\tau} \tag{4.34}$$

$$\sim \frac{wlU}{\tau} \tag{4.35}$$

$$P = UI \tag{4.36}$$

$$\sim \frac{wlU^2}{\tau} \tag{4.37}$$

This means, lowering the supply voltage is an efficient way of saving power without sacrificing too much time resolution. On the other hand, improving time resolution using higher voltage is very costly.

Using smaller transistors is favourable for both time resolution and power consumption. As the transistor size is limited by technology, the delay chain based TDC approach favours smaller process nodes in general. On the other hand, manufacturing has the highest relative error at minimum transistor size. This means, the inaccuracy induced by variation between individual transistors partly counteracts the raw performance gains.

4.4 CMHV7SF Simulation

This section presents the simulation results for the delay chain TDC in the CMHV7SF process node. Using the same technology gives a direct comparison with the observed performance of the Stretched TDC. The simulations are perfomed in the SPECTRE transient simulator.

4.4.1 Unit Cell Comparison

Figure 4.10 compares the unit cells in terms of the time resolution achieved, measured as the flank-to-flank delay observed in simulation. The circuits UC1 to UC3 using inverters as delay elements are faster than UC4 and UC5, as the inverter provides a higher current.

The circuit using the transmission gate for readout is slower, as it has a higher capacitive load on the current driver. The latch based delay cell is the slowest, as it has the highest parasitic capacitance.

As discussed in section 4.3.4, the expected relation of time resolution and driver width is

$$\tau \sim 1 + \frac{k}{w_{chain}} \sim 1 + \frac{k}{\beta} \tag{4.38}$$

The observed curves match this relation. The higher observed slopes for UC3 and UC5 match the higher parasitic capacitance in these circuits.

Figure 4.11 shows the current consumption of the circuits. The order of the circuits reflects the antiproportional relation of I and τ (equation 4.11). In addition, the difference in off-chain capacitance stated in table 4.4 can be observed as significant difference in current draw between UC1 and UC2.

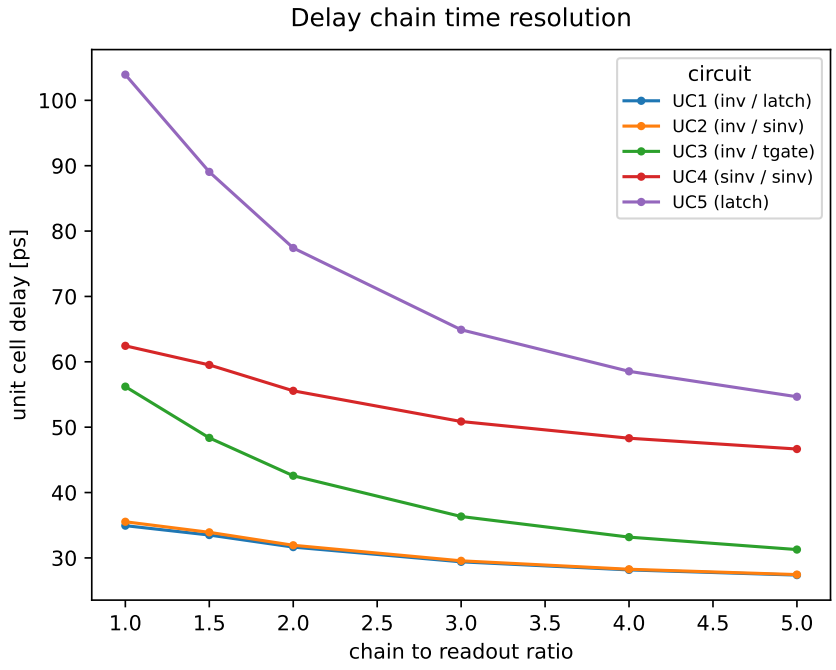


Figure 4.10: Transient simulation: Comparison between different unit cells. Time resolution, measured by time difference between flanks vs. chain to readout size ratio $\beta = \frac{w_{chain}}{w_{readout}}$

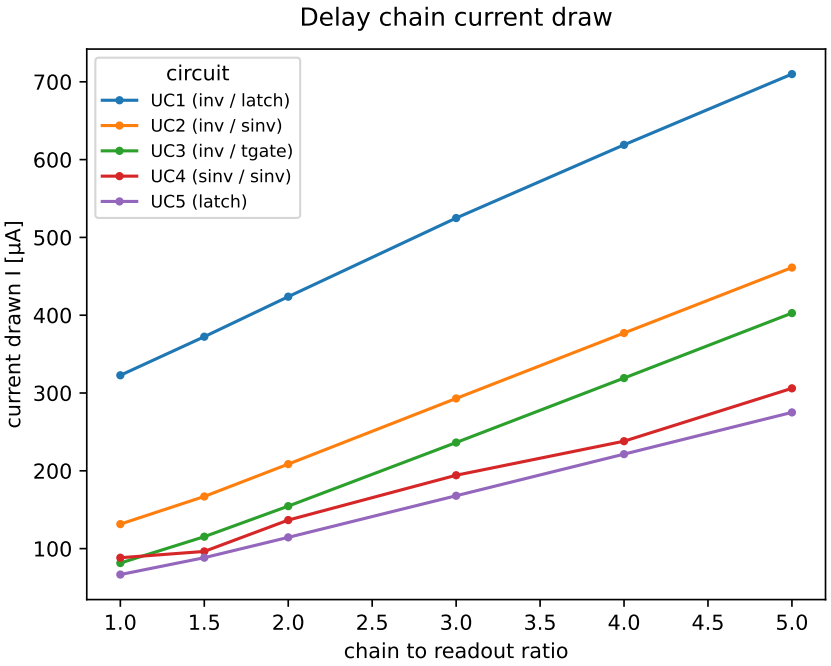


Figure 4.11: Transient simulation: Comparison between different unit cells. Active state current draw vs. chain to readout size ratio $\beta = \frac{w_{chain}}{w_{readout}}$

4.4.2 Size of Supply Transistor in Switched Inverter

UC4 and UC5 have a pair of transistors enabling or disabling the current. They cause a voltage drop, reducing the current.

Figure 4.12 shows the impact of the width of this supply transistor on the time resolution. The time resolution approaches the limit set by the simple inverter with an inversely proportional curve. A ratio of γ below 1 causes a significant slowdown. A ratio above 2 yields diminishing returns.

Note that the values in figure 4.12 are taken for a chain-to-readout ratio $\beta = 3$. At $\gamma = 3$, this results in a supply transistor of size $w_{supply} = \gamma w_{chain} = \gamma\beta w_{min} = 1980nm$. The space usage is significant.

4.4.3 PMOS to NMOS ratio

To achieve a consistent time resolution between rising and falling flanks, the ratio between PMOS and NMOS size needs to be chosen correctly. As figure 4.13 shows, a value of $\alpha = 2.3$ corresponds to minimised asymmetry.

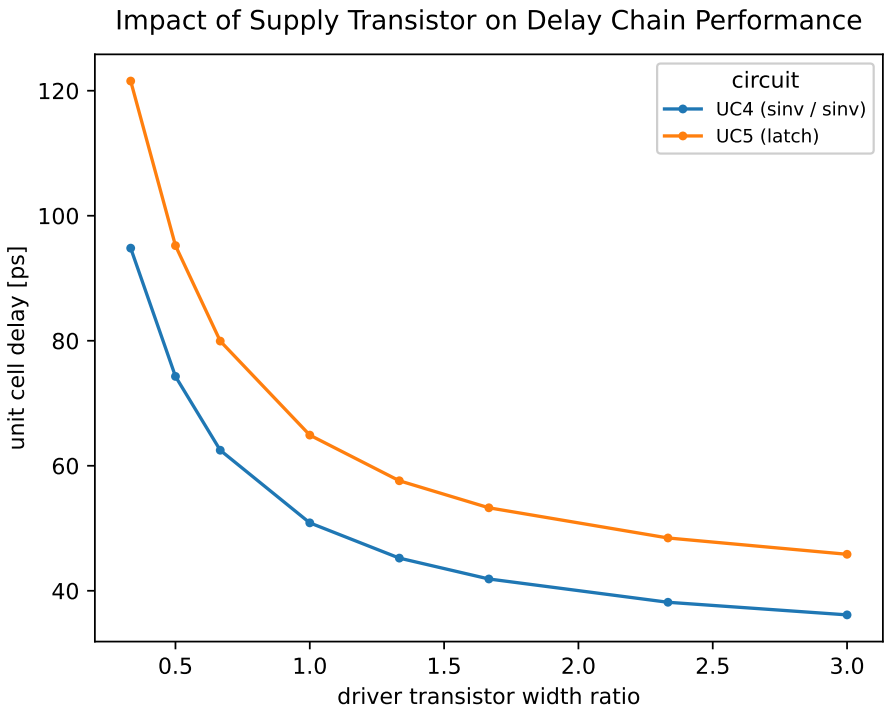


Figure 4.12: Transient simulation: Influence of ratio $\gamma = \frac{w_{supply}}{w_{chain}}$ of supply transistor and inverting transistor on time resolution.

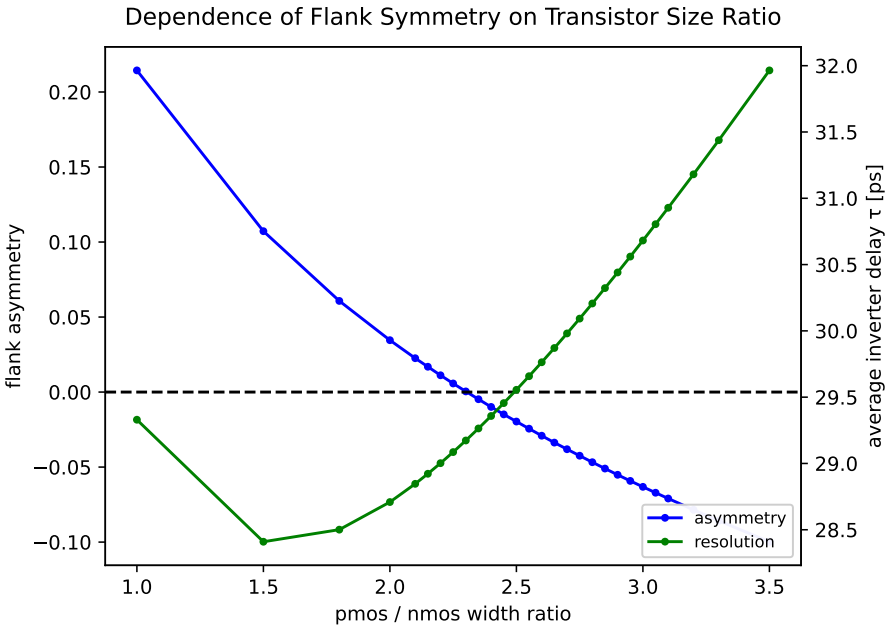


Figure 4.13: Transient simulation: Influence of ratio $\alpha = \frac{w_{PMOS}}{w_{NMOS}}$ on symmetry between flanks and average time resolution for UC2. The asymmetry is measured as relative deviation $\delta = \frac{\tau_+ - \overline{\tau}}{\overline{\tau}}$.

4.4.4 Voltage Dependence

As postulated in section 4.3.6, power consumption P can be reduced disproportionally compared to time resolution τ by reducing the supply voltage. This can be seen in figure 4.14. At $1.8V$, $\tau = 29.6ps$ at $P = 527\mu W$. At $1.2V$, $\tau = 67.3ps$ at $P = 99\mu W$. This is an increase in time resolution of a factor 2.2 for a power reduction factor of 5.3. This power reduction is even stronger than the square relation in equation 4.36. The difference is likely due to the threshold voltage being neglected in this approximation.

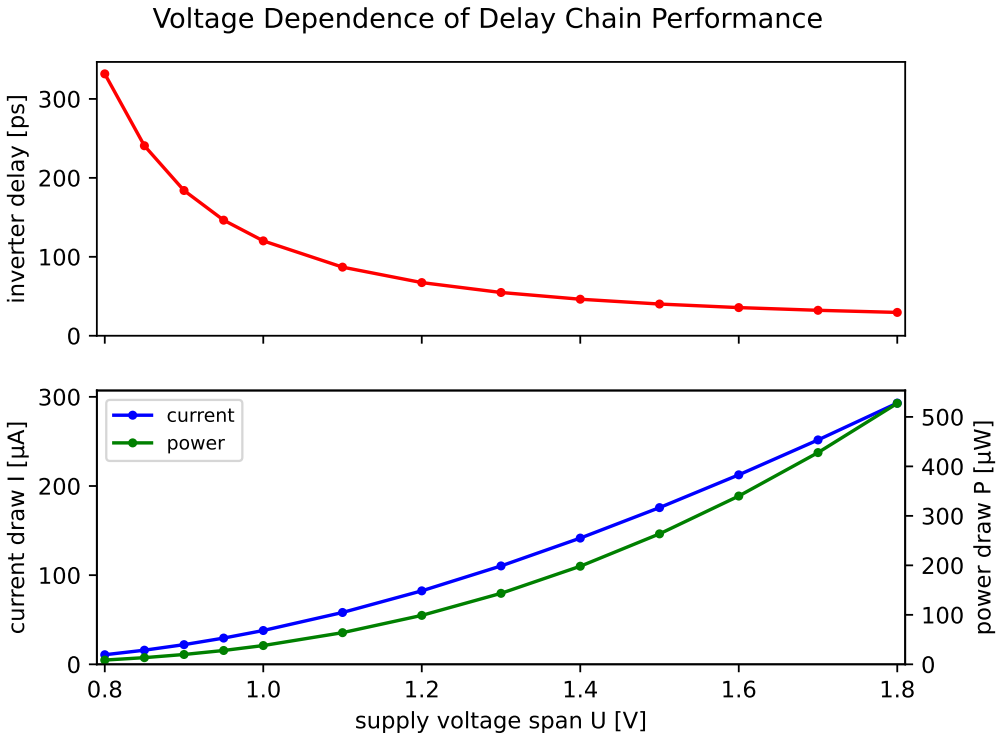


Figure 4.14: Transient simulation: Scaling of time resolution and power consumption with supply voltage for UC2 at $\beta = 3$

4.5 SG13G2 Simulation

This section presents the simulation results for the delay chain TDC in the SG13G2 process node. The comparison with CMHV7SF is used to verify the scaling relation postulated in section 4.3.6. In this section, only UC2 is analysed, as it showed the best performance for CMHV7SF.

4.5.1 Transistor Size

Figures 4.15 and 4.16 show the dependence of inverter delay and current draw on the transistor size. As expected, the current rises linearly with transistor width and the delay falls antilinearly. There are two significant differences compared with CMHV7SF.

First, for transistors just above minimum size there is a kink in the curves, giving smaller delay for $\beta = 1$ compared with $\beta = 2$. This is due to a sublinear increase of drain current with NMOS width near minimum size. It is not known whether this effect is physical.

Second, the slope of τ is stronger than for CMHV7SF. This means, the gate capacitance is less dominant than in CSMHV7SF.

4.5.2 PMOS to NMOS ratio

As the SG13G2 process features a SiGe substrate, the mobility of electrons and holes likely differs. As seen in figure 4.17, this is indeed the case. The observed point of symmetry is at $\alpha = 1.45$. Unlike in CMHV7SF, the point of symmetry coincides with the best average unit cell delay.

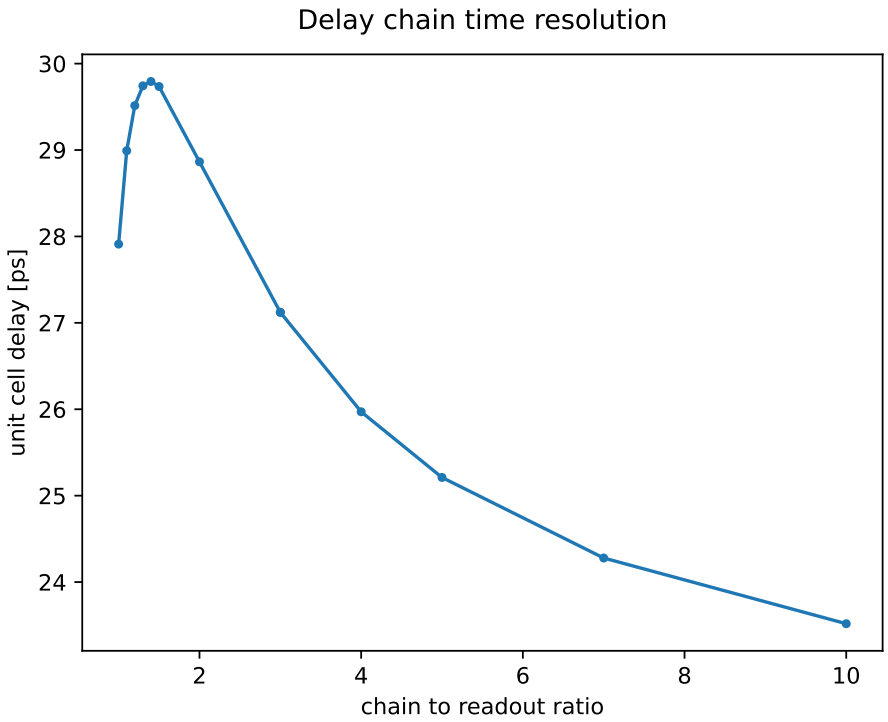


Figure 4.15: Transient simulation: time resolution of UC2 in SG13G2 vs. size ratio $\beta = \frac{w_{chain}}{w_{readout}}$

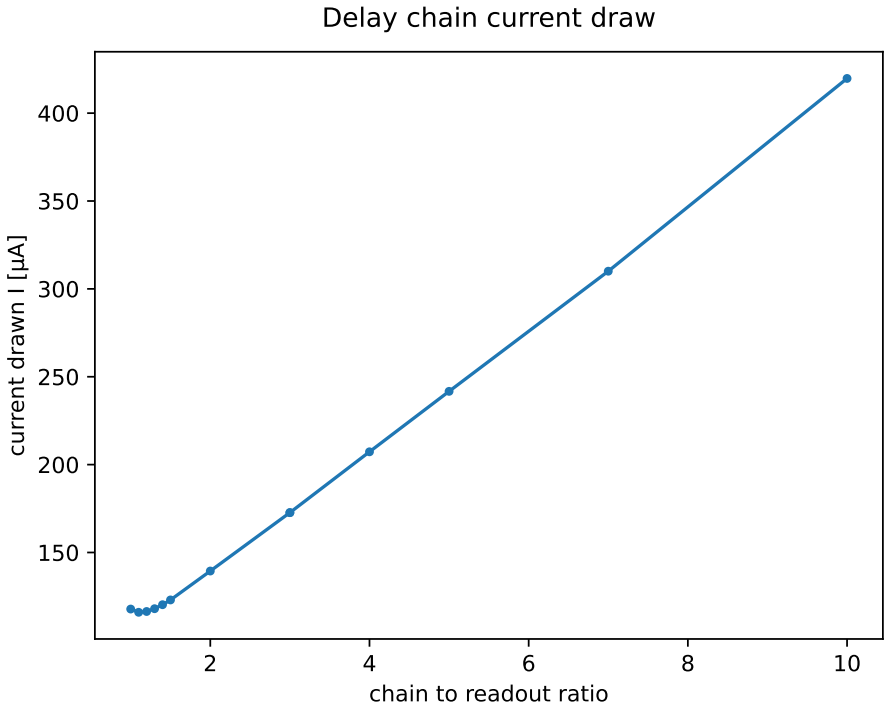


Figure 4.16: Transient simulation: Active state current draw of UC2 in SG13G2 vs. size ratio $\beta = \frac{w_{chain}}{w_{readout}}$

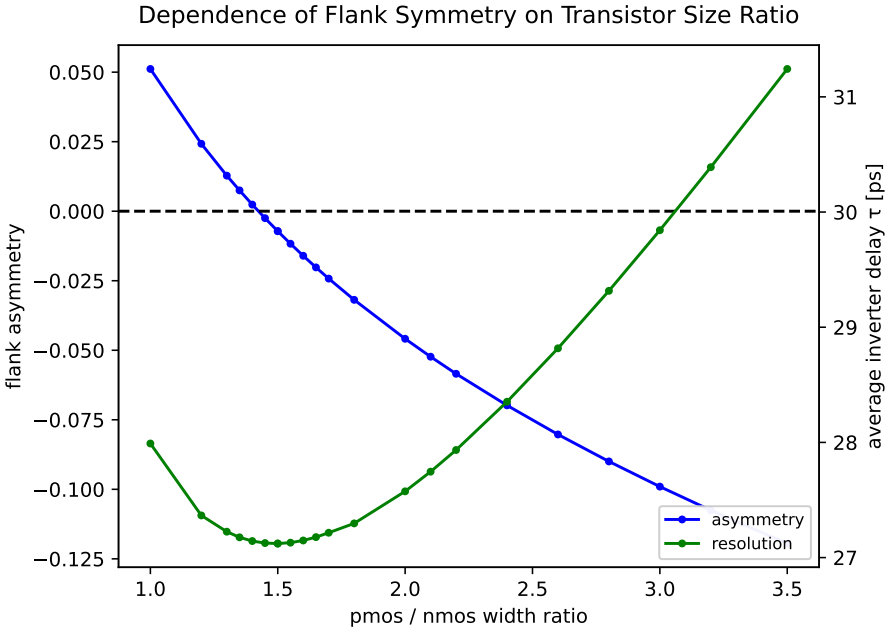


Figure 4.17: Transient simulation: Influence of ratio $\alpha = \frac{w_{PMOS}}{w_{NMOS}}$ on symmetry between flanks and average time resolution

4.5.3 Voltage Dependence

Figure 4.18 shows the scaling of time resolution with the supply voltage. The scaling is similar to CMHV7SF. An unexpected kink is observed in the curve, around 0.7V. This corresponds to a sudden drop in the capacitance of the NMOS transistor around 0.7V. It is unknown, whether this effect is physical.

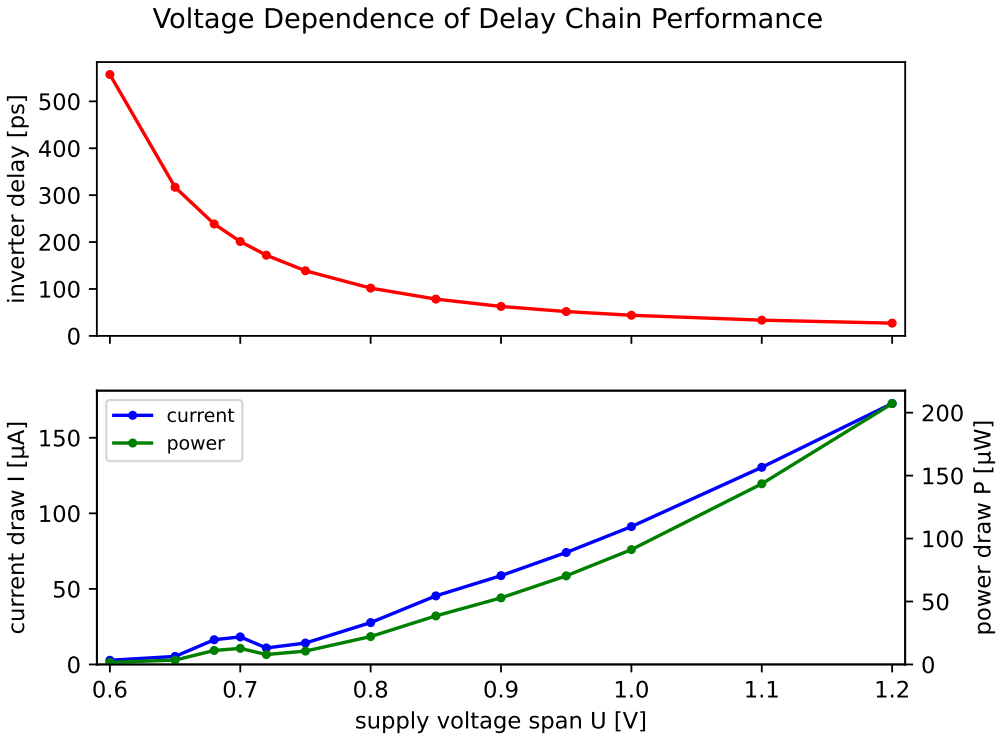


Figure 4.18: Transient simulation: Scaling of time resolution and power consumption with supply voltage

4.6 Comparison of CMHV7SF and SG13G2

The two processes differ in more than just size and supply voltage. Further differences are in substrate, doping and layer thickness, influencing threshold, transconductance and capacitance. Despite all that, a comparison at similar working points is in order. The following comparison uses UC2 at transistor size ratio $\beta = 3$.

The 130nm process SG13G2 is smaller by a factor of 0.72 compared to the 180nm CMHV7SF process. According to equation 4.27, the time resolution scales with l^2. The ratio here would be $l^2 = 0.52$, corresponding to approximately half the resolution at equal supply voltage.

As seen in table 4.19, CMHV7SF at 1.8V and SG13G2 at 1.2V have a similar time resolution. The CMHV7SF3G2 process draw more power by a factor of 3.6. CMHV7SF at 1.3V and SG13G2 at 1.2V have a similar power consumption. This time, the time resolution is smaller in SG13G2 by a factor of 0.54. At equal supply voltage of 1.2V, the factor instead is 0.44, deviating slightly from the value $l^2 = 0.52$ mentioned above. Given that the somewhat crude scaling calculations ignored layer thickness and the significantly different substrate material, this is quite a close match.

Using both a smaller process scale and a lower supply voltage yields a significant improvement in power draw. The comparison with projects like TimePix [19] and PicoPix [18] suggests that the delay chain TDC is competitive in smaller process technology.

process	supply voltage U [V]	time resolution τ [ps]	current draw $I[\mu A]$	power consumption $P[\mu W]$
CMHV7SF	1.8	29.6	293	527
CMHV7SF	1.3	54.8	111	144
CMHV7SF	1.2	67.3	84	99
SG13G2	1.2	29.7	123	147
SG13G2	0.8	102	27.6	22.1

Figure 4.19: Comparison of CMHV7SF and SG13G2 at different supply voltages.

Chapter 5

Conclusion

5.1 Summary

Verification of the Stretched TDC Circuit

In this thesis, I commissioned the Stretched TDC circuit. In section 2.2.1 the functionality of the Stretched TDC was confirmed on the Run2021V2 engineering prototype using Sr90 measurements. The calibration procedure introduced in section 2.2.2 works with high reliability. Due to significant pixel-to-pixel variation, it has to be applied individually for each pixel. The abridged algorithm is

1. measure timestamps and $\delta \coloneqq \mathrm{TS3} - \mathrm{TS1}$ for randomised hits
2. create a histogram $n(\delta)$ for each pixel
3. fit a rectangular block, obtaining fit parameters δ_{min}, δ_{max} and $w \coloneqq \delta_{max} - \delta_{min}$
4. for each hit reconstruct time as $t = \left(\mathrm{TS1} + \frac{\delta - \delta_{min}}{w}\right) T$

Parametric Model

The working point of the Stretched TDC circuit is configured using four DACs: VP_Big, VP_Small, TH_Fine and VN_Comp. In section 2.1.3, a simple parametric was developed to express the distribution of δ in terms of physical parameters of the circuit. It allows expressing the distribution parameters w and δ_{max} in terms of the capacitance C, the currents I_{Big} and I_{Small} and the threshold U_{th},

$$\delta_{max} = \frac{U_{th} C}{I_{Small}}$$
$$\frac{w}{T} = 1 + \frac{I_{Big}}{I_{Small}}$$

The parametric model was confirmed in section 2.6 using simulation and Sr90 measurements.

In section 2.7, the deviations from this simplified model are explained by isolating circuit components in simulation. The most significant effects are the non constant capacitance and the reduction of I_{Big} as the PMOS transistor leaves saturation.

Suggested Parameter Choice

Based on the limits to the operating range seen in sections 2.4.2, 2.5 and 2.8, I recommend the following settings for the DACs (values in decimal):

1. VN_Comp = 10
2. TH_Fine = 1500mV
3. VP_Big = 14

The suggested values ensure some safety margin to avoid the premature threshold issue encountered for small TH_Fine and the driver nonlinearity for large VP_Big. Based on the desired time resolution, select VP_Small:

desired time resolution	required w [clock cycles]	VP_Small [dec]	minimum readout time [ns]
1ns	8	60	64
500ps	16	30	128
200ps	40	12	320
100ps	80	6	640

Figure 5.1: Suggested values of VP_Small to achieve different time resolutions

Pixel-to-Pixel Variation

The Stretched TDC circuit is subject to high pixel-to-pixel variation. As analysed in section 2.6.3, the main cause is the VP_Small current driver. A variation of $\pm 30\%$ has to be expected when setting the working point using the DACs. The variation is dominated by a systematic gradient between low and high column address, potentially due to supply line resistance.

The impact of this pixel-to-pixel variation at a typical working point can be seen in figure 5.2. The magnification ranges from 55 to 100, resulting in a time resolution between 80ps and 145ps.

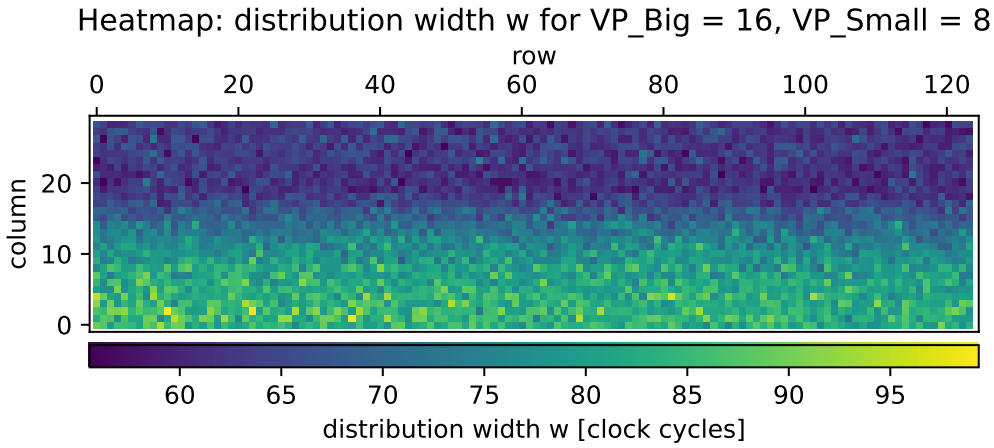


Figure 5.2: Sr90 measurement: Heatmap of time magnification $\eta = \frac{w}{T}$ over pixels at a typical working point.

Power Consumption

The power consumed by the Stretched TDC circuit depends on the DAC settings. At a typical operating point, a single TDC circuit consumes around 10µW. As the current drivers are active even in idle state, this power draw is constant.

Improved Stretched TDC

The existing Stretched TDC circuit draws a permanent current. With switched driver circuits, the current is only drawn when active. This yields a reduction in power consumption of nearly 100%. Of the circuits developed in this thesis, versions V3 and V4 (see section 3.2.1) are promising due to good linearity. Circuit V4 allows for the greatest operating range at the cost of higher power consumption and space usage due to larger components compared to V3.

Delay Chain TDC

As an alternative to the Stretched TDC circuit, delay chains were investigated. Delay chain TDC circuits are limited by technology, most significantly by process scale. In the 180nm CMHV7SF process, all investigated circuits draw current in the range of 100µA to 500µA (see section 4.4) when active. This is more than 20 times the typical consumption of the Stretched TDC circuit, making the delay chain TDC uncompetitive. In CMHV7SF, the delay chain TDC can achieve a time resolution of 30ps, lower than the one achieved by the Stretched TDC circuit.

In the 130nm SG13G2 process, both time resolution and power consumption are improved over CMHV7SF. 25ps resolution can be achieved at a power consumption of 150µW. By using a lower supply voltage of 0.8V, a resolution of 100ps can be achieved using 22µW of power.

Comparison between TDC Circuits

For the CMHV7SF process, the investigated TDC circuits compare as follows:

performance goal	Stretched TDC	Improved STDC	Delay Chain
time resolution [ps]	100	100	30
power consumption	high	low	moderate
peak current draw	low	low	high
readout time [clock cycles]	≈ 150	≈ 150	1

The improved Stretched TDC is strictly better than the existing circuit. Both circuits achieve the target of 100ps. The delay chain TDC is uncompetitive in CMHV7SF due to the high peak current draw. However, in SG13G2 the same time resolution can be achieved at only 22µW power consumption, which is close to competitive already.

Around a process scale of 100nm, the delay chain TDC is expected to overtake the Stretched TDC in performance. Whilst the power consumption of the Stretched TDC circuit can be reduced at smaller process nodes, it cannot match the resolution due to the inherent nonlinearities.

5.2 Outlook

Test Structures in CMHV7SF

A chip containing test structures for the TDC circuits discussed in this thesis has been submitted for production. The test chip contains modified versions of the Stretched TDC circuit using the switched current driver versions V1, V2 and V3. The test structures contain only the TDC circuits with direct readout, so that the distribution $n(\delta)$ is not required to confirm functionality and accuracy. In addition, a delay chain circuit is on the chip to compare the simulated time resolution and power consumption with produced specimen.

Limits to Time Precision

After integrating the TDC in the pixel, the time precision of the whole readout chain is expected to be far worse than the resolution of the TDC suggests. This is mainly due to the slow amplifier circuit and the timewalk effect. Even after timewalk correction, the TDC is not the limiting factor in time measurement precision [14, p.38]. Measurements with a telescope could be used to investigate the precision achieved by the whole chain. Improved, faster amplifier circuits are currently under development, for example in BeBiPix [22].

Bibliography

[1] F. Wauters on behalf of the Mu3e collaboration. The Mu3e experiment. *SciPost Phys. Proc.*, page 20, 2021.

[2] M. Pohl et al. A. Blondel, A. Bravar. Research Proposal for an Experiment to Search for the Decay μ -> eee, 2013.

[3] P. Baesso et al. K. Arndt, H. Augustin. Technical design of the phase I Mu3e experiment. Technical report, 2021.

[4] Sebastian Dittmeier et al. Heiko Augustin, Niklaus Berger. MuPix10: First Results from the Final Design. In *Proceedings of the 29th International Workshop on Vertex Detectors (VERTEX2020)*, 2020.

[5] Ivan Peric. A novel monolithic pixel detector implemented in high-voltage CMOS technology. In *2007 IEEE Nuclear Science Symposium Conference Record*, volume 2, pages 1033–1039, 2007.

[6] G. Hernández-Tomé, G. Castro, and P. Roig. Flavor violating leptonic decays of τ and μ leptons in the Standard Model with massive neutrinos. *The European Physical Journal C*, 79, January 2019.

[7] Andrzej Czarnecki, Matthew Dowling, Xavier Garcia i Tormo, William J. Marciano, and Robert Szafron. Michel decay spectrum for a muon bound to a nucleus. *Physical Review D*, 90(9), November 2014.

[8] L. Michel. Interaction between Four Half-Spin Particles and the Decay of the μ-Meson. *Proceedings of the Physical Society. Section A*, 63(5):514, May 1950.

[9] Heiko Augustin. *Development of a novel slow control interface and suppression of signal line crosstalk enabling HV-MAPS as sensor technology for Mu3e*. PhD thesis, Uni Heidelberg, 2021.

[10] Christian Kreidl et al. Ivan Perić, Peter Fischer. High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 731:131–136, 2013. PIXEL 2012.

[11] Ruben Kolb for the HD-HVMAPS collaboration. Charge Deposition and Charge Collection in HV-MAPS. DPG- Frühjahrstagung 2023, March 2023.

[12] Gerhard Lutz. *Semiconductor Radiation Detectors*. Springer Verlag, Heidelberger Platz 3, 14197 Berlin, 2007.

[13] J F Bak, A N Burenkov, J B B Petersen, Erik Uggerhøj, S P Møller, and P Siffert. Large departures from Landau distributions for high-energy particles traversing thin Si and Ge targets. *Nucl. Phys. B*, 288:681–716, 1987.

[14] Florian Frauen. *Characterisation of the time resolution of the MuPix10 pixel sensor*. PhD thesis, Uni Heidelberg, 2021.

[15] Frank Gray. Pulse Code Communication, November 1947.

[16] Hui Zhang. *Development of integrated detectors for charged particles and photons*. PhD thesis, Karlsruher Institut für Technologie (KIT), 2022. 54.12.01; LK 01.

[17] F. Martinelli, P. Valerio, R. Cardarelli, E. Charbon, G. Iacobucci, M. Nessi, and L. Paolozzi. A massively scalable Time-to-Digital Converter with a PLL-free calibration system in a commercial 130 nm process. *Journal of Instrumentation*, 16(11):P11023, November 2021.

[18] Xavier Llopard. The PicoPix Project. MONOLITH Workshop on silicon sensors for timing and their applications, September 2022.

[19] K. Heijhoff, K. Akiba, R. Ballabriga, M. van Beuzekom, M. Campbell, A.P. Colijn, M. Fransen, R. Geertsema, V. Gromov, and X. Llopart Cudie. Timing performance of the Timepix4 front-end. *Journal of Instrumentation*, 17(07):P07006, July 2022.

[20] Shmuel Ben-Yaakov Ilya Zeltser. On SPICE Simulation of Voltage-Dependent Capacitors. *IEEE Transactions on Power Electronics*, 33(5), May 2018.

[21] Holger Göbel. *Einführung in die Halbleiter-Schaltungstechnik*. Springer Verlag, Heidelberger Platz 3, 14197 Berlin, 6th edition, 2019.

[22] Benjamin Weinläder. Development of a Pixel Sensor with sub-nanosecond Time Resolution in BiCMOS. DPG-Frühjahrstagung, March 2021.

[23] IBM Corporation. IBM CMHV7SF. 2012.

[24] TSI Semiconductors. 7501 Foothills Boulevard, Roseville, CA 95747. *https://www.tsisemi.com/*.

[25] IHP GmbH. Im Technologiepark 25, 15236 Frankfurt (Oder). *https:/www.ihp-microelectronics.com/*.

[26] Inc Cadence Design Systems. 2655 Seely Avenue, San Jose, CA. *https://www.cadence.com/*.

[27] Marius Grundmann. *The Physics of Semiconductors*. Springer Cham, 3 edition, March 2018.

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for good times and intense debates, for a relaxed and collegial atmosphere whilst each of us confronts serious challenges

Erklärung:

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 21.06.2023 .....