Front-End Electronics for a TPC-Detector

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Abstract

The CERES/NA45-Collaboration upgrades the existing lepton-pair spectrometer at the CERN SPS with a TPC detector which improves the momentum resolution. We present the development of new front-end electronics to read out the nearly 20000 channels of the chamber. It is comprised of two circuits: (i) A continuously sensitive preamplifier with semi-Gaussian shaper and tail-cancellation, which offers selectable time constants to cope with various detector gases. The design is based on a low noise charge sensitive amplifier with P-channel input device matched to 12 pF input capacitance with an equivalent noise charge ENC=120 e rms at 27 μs peaking time. The CSA-Shaper features ENC=180 e rms at 580 ns peaking time. (ii) A 16$\times$256 cell analog-memory stores the input waveform at 10 MHz during the drift-time of the chamber. Both circuits are developed in a 0.8 μm CMOS technology and we will focus on the result of prototype measurements. Although the complete system is geared towards the CERES-TPC, its necessary flexibility make it feasible for the ALICE experiment.

1 INTRODUCTION

A novel radial TPC-detector is presently under construction [1] and will be installed in 1998 behind the existing NA45 spectrometer. The huge multiplicity of produced charged particles in 158 GeV/u Pb-Pb collisions requires high granularity to resolve the individual tracks. The chamber consists of (i) a cylindrical drift volume (2m length, 1m/2.6m inner/outer diameter) filled with 90% Ne + 10% CO_2 and (ii) 16 read-out modules equipped with MWPCs and a two-dimensional pad-plane. The signal on each individual pad is read out with a charge sensitive preamplifier. During the drift-time of the chamber (30 - 70 μs) the preamplifier output waveform is recorded at up to 10 MHz and stored in 256 individual time samples to allow a three dimensional reconstruction of the tracks. The requirements of the front-end electronics are largely dictated by the parameters of the TPC (drift-time, diffusion, gas mixture). The front-end electronics needs to have some flexibility in order to cope with different operating conditions. The front-end boards will be mounted directly on the pad-plane. To meet the luminosity requirements of the experiment a total read-out time below 300 μs has to be achieved, which is not possible with existing designs for other TPC-detectors. In this paper we report on the development of the new front-end electronics, which has been carried out in the past months. We concentrate on the performance of the preamplifier and the SCA prototypes.

2 CMOS PREAMP-SHAPER WITH TAIL CANCELLATION

The charge pulse produced by an ionizing track across the TPC is processed by a low noise Preamp-Shaper with tail suppression. We aimed to develop a flexible CSA-Shaper which can be adapted to various working conditions for the TPC: selectable peaking time in the range 140ns–580ns and selectable tail suppression in the range between 0.1μs-1μs. We aim to achieve an equivalent noise charge ENC$<$600 e rms at Ts=400ns peaking time with the circuit connected to a pad with Cpad=12pF.

Among the different technologies, the CMOS one offers the advantage of being inexpensive and readily available for full custom design. The quadratic dependence of the transconductance on the drain current is compensated by the small channel length of the MOS transistor. Consequently, at the expense of higher power consumption, it's possible to achieve transconductances (i.e. thermal noise) equal to the ones of BJT's transistors [2]. As far as the bipolar technology is concerned, the effect of the BJT's base current on the noise performance at long shaping time [3][4] makes the noise performance weakly dependent on the power consumption. For these reasons, the BJT technology is preferable to the CMOS one for ultra-low power Preamp-Shapers at the expense of a worse noise performance. As far as the bipolar technology is concerned, we mention the gateable Preamp-Shaper based on a current-mode integration scheme developed in a bipolar rad-hard technology [5]. For our application the power consumption constraint is not critical, thus we have chosen the CMOS technology.

Recently a CMOS Preamp-Shaper with tail cancellation has been developed for the STAR experiment at RHIC [6]. This circuit is based on a charge sensitive amplifier (CSA) with pulsed reset [7]: the signal charge integrated onto the feedback capacitance CF is discharged with a reset to prevent the CSA from being saturated by tracks from subsequent events. The drawbacks of the pulsed reset scheme are: (i) dead time, (ii) the system is blind until the next reset cycle if a large undesired signal is collected, (iii) digital signals are running on an analog low noise circuit. To address these issues we used a MOS transistor RF which establishes the DC path and continously discharges CF with a decay time Tdecay=CF·Rdrain-source(MF) (Fig. 1). The value of

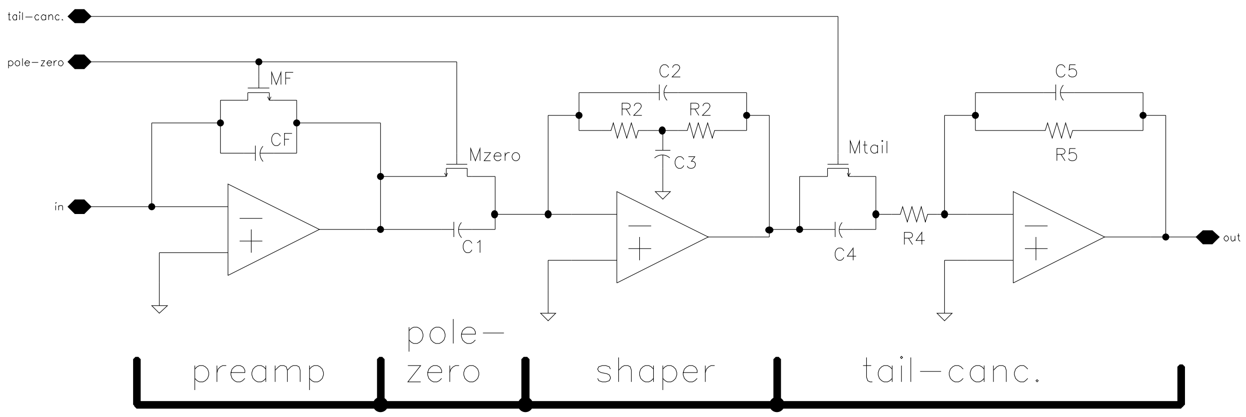

Figure 1: Schematic of the preamplifier chain with shaper and tail-cancellation

RF is a trade-off between noise performance and capability to process events with high occupancy. For a peaking time Ts=400ns, noise considerations dictate a feedback resistance RF $> 4\text{M}\Omega$. The only practical way to realize such a high resistance in CMOS technology is by using the associated drain- source resistance Rds(MF) of a MOSFET transistor. Rds(MF) depends on the biasing condition of MF, in particular decreases at Vgs(MF) increasing. This dependence is an advantage in our case as signal charges increase Vgs(MF): the integration of small charges results in small Vgs(MF) swings, thus Rds(MF) $\simeq$ Rds,DC(MF), its value being high enough not to worsen the noise performance. Conversely, large charges are discharged with a faster decay time and the CSA-Shaper's baseline is quickly restored. What is more important, undesired large signals (as delta electrons) collected on the TPC pad are transferred onto CF and quickly discharged minimizing the dead time.

In order to use a MOSFET transistor as feedback resistance, two issues must be addressed: (i) how to bias MF in the MΩ region while tracking process, temperature, supply voltage variations (in particular the threshold voltage can change by +-100mV from chip-to-chip); (ii) how to prevent the gain linearity from being worsened by a non-linear resistance in the feedback loop. The voltage- charge conversion gain, which in an ideal CSA is 1/CF, is reduced if the ratio Tdecay/Trise is not high enough. In this condition, a variation of Tdecay affects the gain, and the dependence of Rds(MF) on the input charge worsen the gain linearity.

The two issues have been addressed by using general purpose circuit techniques developed for continuously sensitive CMOS Preamp-Shapers. Two different CSAs, matched to 12pF and 20pF pad capacitance have been designed and fabricated with the 0.8 μm AMS CMOS process. Noise considerations dictated the choice of a P-channel input device.

2.1 Design Techniques

The feedback transistor MF is biased in the triode region by using a Self-Adaptive Bias technique proposed and implemented in a CSA for a Silicon Drift Detector to be used for particle tracking [8][9] and in a CSA-Shaper for X-Ray Spectroscopy [10][11]. In our case we introduced a feedback transistor MF with W/L=2μm/40μm to achieve 50 MΩ and 5.5 MΩ for respectively the 12pF and the 20pF version. The Self Bias circuit keeps Vg(MF)–Vin(M1)=const, making Rds(MF) independent on process, temperature and supply voltage variations.

As already pointed out, the integration of a large signal charge causes a reduction of Rds(MF), desirable as it speeds up the return to the baseline of the CSA. In Fig. 2 the 12pF-CSA responses to negative charge pulses with Qin=(5.2, 52, 520)fC are reported on the same scale showing the reduction of the decay time in the self-biased condition.

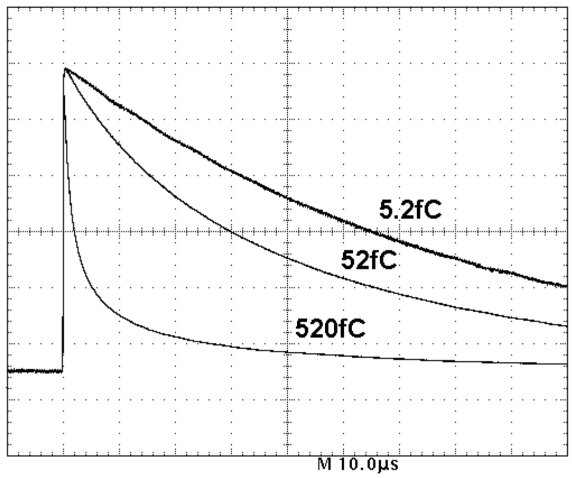

Figure 2: CSA's response to charge pulses Qin=(5.2, 52, 520)fC (the vertical scale is 100mV/div for Qin=520fC).

The gain linearity of the CSA has been measured by using an on-chip injection capacitance and the result is shown in Fig. 3: the non-linearity of the CSA's gain (within 5% up to Qin=500fC, and within 2% up to 350fC) is mostly due to the second order effect of the dependence of Rds(MF) on Qin. The absolute value of the gain (G=1.16 mV/fC) is known within 20%, its calibration is now in progress.

If a conventional Pole-Zero cancellation would be used [12], the dependence of Rds(MF) on Qin would worsen the linearity of the Preamp-Shaper. To solve this issue, we use an Adaptive Pole-Zero cancellation scheme [8][9][11] to suppress the Pole associated with Rds(MF) and CF.

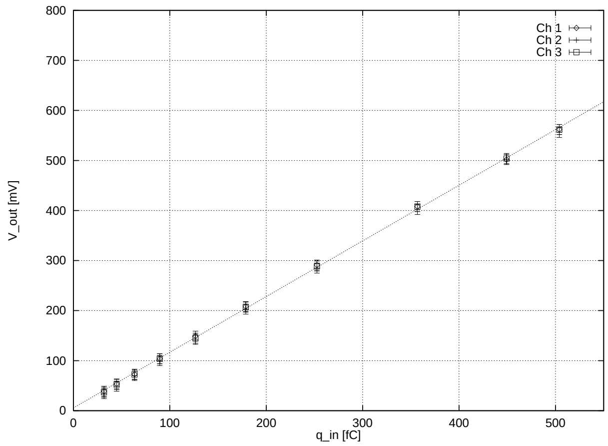

Figure 3: CSA's gain vs input charge Qin for three channels.

With reference to Fig. 1, the MOS transistor Mzero is biased in the same way as MF during the discharge of CF. The Zero associated to the network Mzero-C1, adapts itself dynamically to accurately cancel the Pole associated to the network CF-MF. In other words, the second order effects of Rds(MF) on the CSA's gain is accurately suppressed in the CSA-Shaper.

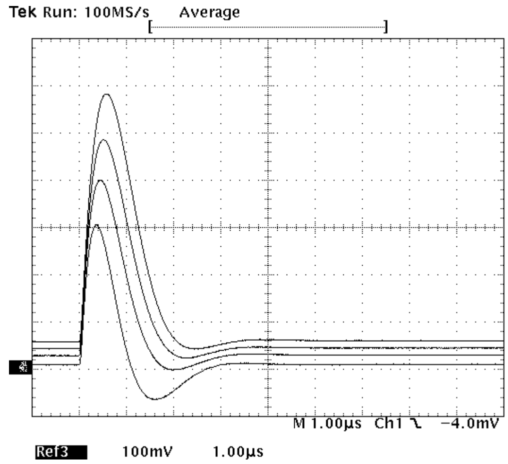

Figure 4: Response to Delta-like input signal for different tail-cancellation time-constants

We have implemented two different circuits based on the classical tail cancellation scheme to suppress the tail of the charge pulse. One is a variation of the scheme implemented in [6], the other scheme (as depicted in Fig. 1) uses a third stage to introduce a Pole-Zero: the Pole provides additional shaping and the Zero can be adjusted to accurately cancel the tail of the charge signal. Both schemes suppress the signal-tail over a range of 0.1 μs - 1 μs. The gain and the peaking time of the CSA-Shaper with tail suppression can be adjusted by changing the setting of the RC network of the Shaper. A fine tuning is also possible by changing the bias condition of Rds(Mtail).

In the final version the second scheme has been implemented, the response to a delta-like input signal with various cancellation time-constants applied is shown in Fig. 4.

The fabricated CMOS CSA's use a P-channel feedback transistor, thus the reported Adaptive Pole-Zero cancellation scheme works for negative charge pulses. To use the same scheme while processing a positive charge pulse, the final CSA-Shaper will use a N-channel feedback transistor and a N-channel cancellation device, biased using the same Self-Adaptive cancellation technique.

2.2 *Noise Performance of the CSA and CSA-Shaper*

The CSAs have been connected to an external shaper with selectable shaping time and the equivalent noise charge (ENC) vs. peaking time Ts has been measured. The CSA matched to 12pF has been measured in two bias conditions for MF, the self-biased and the pinched one (with Rds(MF)=2.5GΩ) achieved by forcing a proper voltage on the gate of MF.

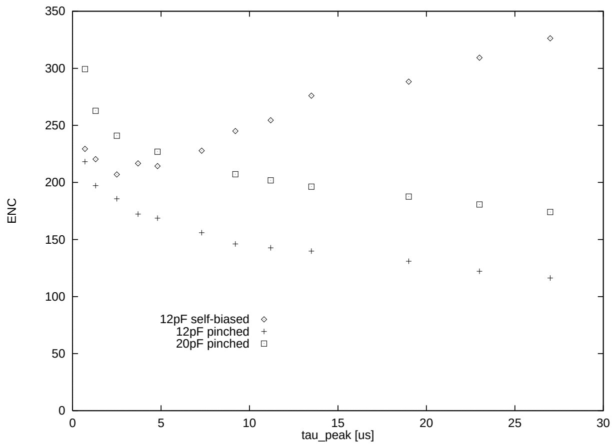

Figure 5: ENC vs. peaking time Ts for the CSA connected to an external shaper (12pF and 20pF version)

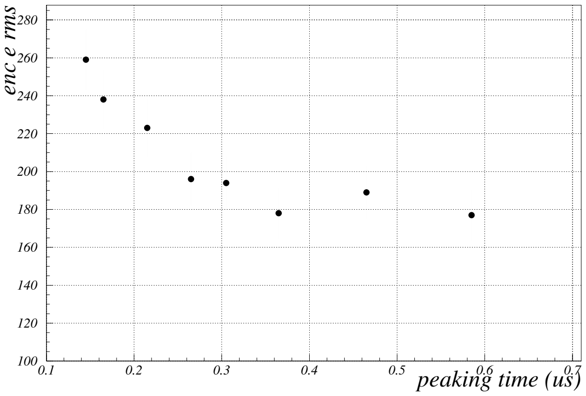

Figure 6: ENC vs. peaking time for the CSA-Shaper with Tail suppression (12 pF version)

The CSA matched to 20pF has been measured in the pinched condition. The results are shown in Fig. 5. With MF pinched there is no parallel noise contribution and we measure ENC=120 e rms at Ts=27 μs for the 12pF version. The noise performance of the CSA-Shaper is reported in Fig. 6. At 580ns peaking time we measure ENC=180 e rms. The better noise performance (we measure a higher noise with the external shaper at lower peaking times) is due to a cleaner set-up in this last measurement.

3 ANALOG-STORAGE AND DIGITIZATION

There are two different options for the architecture of the front-end electronics: (i) digitization with an FADC at 10 MHz and digital storage [13] or (ii) analog storage [14] and slow digitization to meet the dead-time specifications. We have chosen the last concept because the large ratio of sampling- to readout-frequency offers a much lower power consumption as compared to a digital storage. During the drift-time of the detector the waveform of the preamplifier is sampled and stored in an analog-memory (SCA) at 10 MHz. The data are read out and digitized with 1 MHz which results in a readout time of less than 300 μs. A configuration which allows simultaneous read- and write-operation brings only a small benefit and was therefore not considered.

3.1 SCA

The overall scheme is shown in Fig. 7. We have started our development with two test versions of the SCA-chip. The first chip consists of a small 48$\times$8 cell array and has been produced in the 1.2 μm AMS CMOS-technology. The main goal was to assess the performance of different switches and layout strategies to select the final configuration. The second version is a 64$\times$16 cells memory (0.8 μm AMS CMOS), equipped with an 16-1 analog output multiplexer and a high bandwidth output buffer to drive external capacitances up to 30 pF. In this way the SCA can drive an external 16 MHz ADC. We use a voltage-read–voltage-write configuration [14], which has the benefit that the output is independent on the exact value of the storage capacitor. Each memory cell consists of a 1.4 pF double poly capacitor which is connected by two transmission-gates to the common lines. This scheme reduces parasitic capacitances during readout, when the storage cells are switched in the feedback loop of an operational amplifier. Without this second switch the read amplifier would charge the total capacitance of all bottom plates to the substrate. This capacitance has been estimated equal to 25 pF. In addition the two transmission-gates, inherently less sensitive than single transistor switches, further reduce clock-feed-through and charge injection: only the difference of the capacitor voltages between the top- and bottom-plates are relevant and over a small range of input voltages the noise influence is the same on both plates. Symmetrical layout and only complementary signals running near analog cells ensure low switching noise caused by digital signals. The n-tub layer of the PMOS-switches is extended to cover also the capacitors in order to minimize coupling to the substrate, which in this technology is common to the digital and analog parts. The read-amplifier consists of a one stage voltage amplifier with source-follower output-stage and uses small sized input transistors. This is necessary as during readout charge sharing between the storage capacitor and the input capacitance of the amplifier would result in a distortion of the signal.

The digital part includes two shift registers to sequentially address two columns of 8 cells each. A programmable clock window allows non overlapping addressing signals so that no charge-sharing between adjacent cycles is possible. During sampling the two shift registers are driven by the same clock, while during the readout one block is delayed by half a clock cycle. This ensures that the analog values presented to the output multiplexer have properly settled for all the 16 channels.

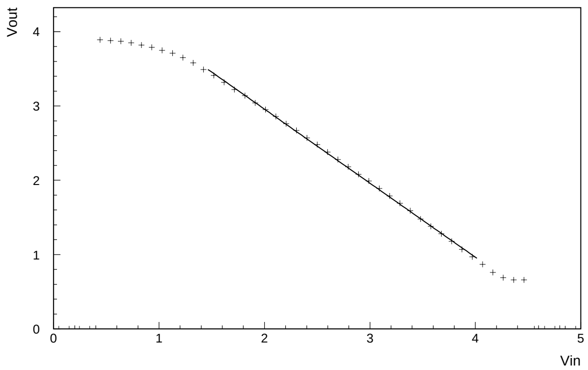

Figure 8: Linearity measurement of SCA

The active area of the TPC varies for different positions along the beam axis. Two registers in the control section of the chip can be used to store a delay value for the start of the sampling and the maximum number of read out channels. This allows to suppress tracks outside the conical area of the TPC enclosing the tracks to be matched to the other detectors. This results in a reduction of storage cells and therefore chip area by 30%. Furthermore the control logic provides all the necessary signals for the external components (ADC, drivers) and once initialized requires only a trigger signal and external reference clocks. The digital blocks have been assembled from standard cells and take only a small part of the total chip size.

The prototypes have been measured and the results are within the design specifications. The baseline uniformity for all channels connected to the same read-out amplifier is below 500 μV, while different read-amplifiers show offsets up to 50 mV.

The response is linear up to an input range of 2.5 V (see Fig. 8). In the present setup the precision is limited by external noise interference, but exceeds already the required 8 bit resolution for 1 V input range. The measured fluctuation of individual channels is around 4 mV (peak-to-peak value),

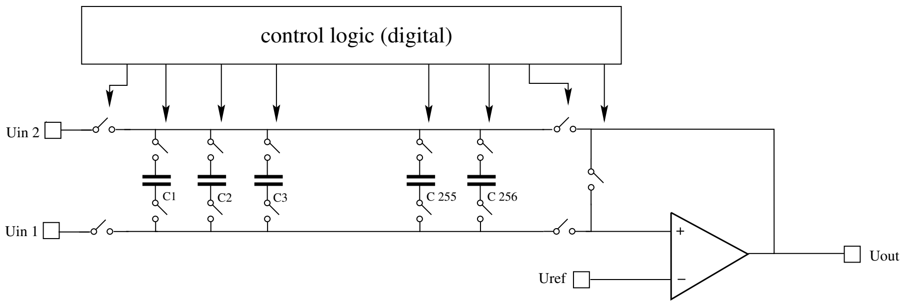

Figure 7: Double switch scheme implemented in the SCA

which corresponds to 10 - 11 bit resolution. The total power consumption is 2.1 mW/channel, plus a significant contribution of the output buffer (60 mW), which in low power applications would favour to use an on-chip ADC instead. The final chip with 256×16 cells has been submitted to production.

4 CONCLUSIONS

A new front-end electronics for the read-out of a TPC has been designed and fabricated with the AMS 0.8μm process. Although the complete system is geared towards the CERES-TPC, its necessary flexibility to accommodate different operating conditions make it feasible for the ALICE experiment.

The CSA-Shaper uses a PMOS transistor MF to discharge continuously the charge signal integrated onto CF. Novel circuit techniques have been implemented to cope with the biasing of MF and its non-linear resistance. The advantages of the chosen scheme are: (i) no dead-time, (ii) no digital signals are running on a low noise analog chip, (iii) no external components or adjustments are needed to operate the CSA-Shaper, (iv) fast baseline restoring in presence of highly ionizing tracks.

The gain of the CSA-Shaper with tail suppression can be adjusted between 17 and 30 mV/fC and its peaking time between 140ns and 580ns. The noise performance of the CSA is 120 e rms at Ts=27μs if MF is pinched. For the CSA-Shaper we measure 180 e rms at Ts=580ns. The noise performance and the gain are accurate within 20%, the gain calibration is in progress. The CSA uses a PMOS feedback transistor; to process the positive charge pulse collected on the TPC pad while using the Adaptive Pole-Zero cancellation scheme, an NMOS feedback device will be used in the final CSA-Shaper.

An analog memory-slow digitization scheme has been used to fully exploit the large write-to- readout frequency ratio of the application. A double-switch scheme has been successfully implemented: a second switch connects every capacitor of the array to the bottom plate. Consequently, the total capacitance substrate-bottom plate, estimated to be equal to 25pF, is not charged by the read amplifier and the readout frequency can be increased keeping constant the power consumption even for large arrays. Two prototypes have been fabricated and characterized to asses the best strategy for the layout of capacitors and switches. The sampling frequency ranges up to 40 MHz. The two-switch scheme increases the read frequency up to 8 MHz at a power consumption of 2.1 mW/channel, making our read-out scheme feasible for other applications, as the Silicon Drift Detectors on the ALICE inner tracking system. The dynamic range of the SCA extends up to 2.5V. The characterization of the SCA showed a resolution of 10 - 11 bit, which exceeds the required 8 bit precision for this application.

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