CMOS Detectors
Ingeniously Simple!

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B-Workshop
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Detector System on Chip?
ATLAS Pixel Module
ATLAS Insertable B-Layer
ATLAS Pixel Module

Front-end electronics

~250 $\mu$m

n-type bulk

deprecated

~5000-7000 e

FE chip

Bump-bond pad

8-bit time stamp

Address & time stamps

Analogue part

Digital part

1. readout cell

2. readout cell

Hit buffer cell

D/A converter

Column-level readout controller

Hit address

Hit amplitude

Chip-level readout controller

Delayed BC clock

L1

Time stamp

Control

Chip address

Slow control

Clock

Sync

Data output

L1

Power supplies

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Silicon Hybrid Detectors

Features
- high signal and high noise
- complex compound
- bump bonding
- wire wrapping
- custom-made sensor
- lots of material (radiation lengths!)

- expensive (e.g. ATLAS II pixel HW: 16 mill.CHF for ~5m²)
- scalability problem (e.g. Future experiments at FCC)
- miniaturization problem >10⁸/m² bump bonds?
- quality assurance problem
Silicon Detector

- HV hole
- HV guard ring
- Type0 connector
- barrel pigtail
- flex
- NTC
- sensor
- sensor (silicon)
- CMOS (intelligence)
- cables
- MCC
- decoupling capacitors
- TMT (cooling)
- glue
- FEs
- bump bonds
Silicon Detector → CMOS chip

- no composite
- no interconnects
- simplified design (ASIC design)
- profits from miniaturisation

→ System on a chip
CMOS Features

- minimum pixel size 10-20 feature size → 5μm possible!!!
- low power (CMOS)
- low noise compared to hybrids
- compact VLSI design
- standard process
- cheap
Dopings

p-type

holes are majority charge carriers

n-type

electrons are majority charge carriers
What is CMOS?

Complementary Metal Oxide Semiconductors
- n-channel MOSFET (NMOS)
- p-channel MOSFET (PMOS)

MOSFET = metal oxide semiconductor field effect transistor
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MOSFET = metal oxide semiconductor field effect transistor

n-channel (NMOS)
Advantages of CMOS

- fast switching characteristics → used for CPUs
- no ohmic resistors needed → low power
- easy to implement capacitors

CMOS Inverter
Monolithic Active Pixel Sensors (MAPS)

How to design a CMOS particle detector?

**Problem:** low resistivity
→ fast recombination
→ small charge collection

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Monolithic = single process
The MAPS Principle

- diffusion
- random walk
- recombination!

MIMOSA = Minimum Ionizing MOS Active pixel sensor

time scale: $\tau \sim 100$ ns

voltage $\sim 3V$
Challenge: separation of analog and control signals
e.g. readout control should not affect signal
MIMOSA Pixel Layout

1-diode pixel

4-diode pixel

transistors (intelligence) on sensor!
Rolling Shutter MAPS Readout

Turchetta et al. NIMA 458 (2000) 677

analogue output

64 x 64 array

20 x 20 μm²
MIMOSA: Energy Distribution

Berst et al., LEPSI 99-15

Charge in 9 pixels

3 x 3 pixel á 20 x 20 μm²

Landau approximation
The charge collection efficiency

ENC = equivalent noise charge

charge is spread over many pixels!
MAPS Charge Collection Time

Berst et al. (2001)

Substrate layer thickness [m]

substrate thickness = 20 \mu m

collection time \( t_c \)

90% of charge

in 3-by-3 pixels cluster

Epitaxial layer thickness [m]

5 \mu m

20 \mu m

5 \times 10^{-6} \quad 10 \times 10^{-5} \quad 1.5 \times 10^{-5} \quad 2.0 \times 10^{-5}

central pixel
4 pixels cluster
3-by-3 pixels cluster
Noise in CMOS Sensors

usually dominant source is the so called **Reset** or **Capacitive Noise**:

\[ V_{RMS} = \sqrt{\frac{kT}{C}} \]

\[ Q = C V_{RMS} \]

\[ n_{RMS} = \sqrt{\frac{kTC}{e}} \]

**typical signal over noise: S/N=20-50**

**Other sources:**
- **thermal noise** \( S_v(w) = 4kTR \)
- **shot noise**
- **flickering noise (1/f)**
MAPS Applications

- MIMOSA originally proposed for ILD vertex detector
- used in DESY Aconite telescope (EUDET)
- STAR vertex detector (350 mill. pixel)
- new ALICE vertex detector (~ 10 m²)

applications where time resolution is not a serious issue

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Neckarzimmern Workshop, 18.February 2015
High Voltage MAPS

Floating structure
MOSFETS in well
100% fill factor
high depletion at 50 V

Ivan Perić, NIMA 582 (2007) 876
HV-MAPS Pixel Design

Fast circuit and thin sensor!

DAC = digital to analog converter → adjustment of threshold

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HV-MAPS and Multiple Scattering

HV-MAPS:
- allow for small pixel sizes
- can measure very low momentum tracks (thin sensor)

→ multiple scattering regime
Mu3e Experiment

Search for $\mu^+ \rightarrow e^+ e^+ e^-$ (signal)

Background: $\mu^+ \rightarrow e^+ \nu \nu$

$\sim 1$ muon decay / ns

Fast and very thin detector required $\rightarrow$ MuPix sensor

$p(e^+) < 53$ MeV
Mupix Chip

Pixel

- Sensor
- Injection
- CSA
- Source follower
- Amplification
- Integrate charge
- Drive high C of signal line

Periphery

- BL
- Comparator
- Tune DAC
- Threshold
- AC coupling via CR filter
- Set individual threshold
- Digital output (ToT)
- Readout
Mupix Chip

Mupix7 prototype:
- ~ 3 x 3 mm²
- ~1200 pixels
- pixel size ~ 80 x 100 µm²

Mupix7 features:
- Tune DACS for every pixel
- double stage amplifier (every pixel)
- zero suppression
- timestamp generation up to ~100 MHz → 10 ns
- 1.2 GHz PLL
- integrated 1.2 (2.4) Gbit/s link
- about 40 pads needed (wire bond)

System on Chip!
Mupix Readout Design

Mupix7 prototype:
- ~3 x 3 mm²
- ~1200 pixels
- pixel size ~ 80 x 100 µm²

Readout periphery

- DAC and SRAM
- Coupling capacitor
- CMOS digital part
- Comparator
- Address ROM
- TS DRAM
MuPix Time Resolution

Timestamp frequency 100 MHz
DESY Testbeam with 5 GeV electrons

\[ \sigma = 16.6 \text{ ns} \]

includes time resolution of setup and sampling

fastest monolithic pixel sensor!
MuPix Time Resolution

Latency vs ToT

PSI Testbeam with 500 MeV protons

→ timewalk correction possible
MuPix Pixel Efficiency

Efficiency > 99.5%

0° incidence angle
70 V high voltage
823 mV threshold
**MuPix Requirements**

- 50μm thickness
- <100μm resolution
- S/N >20
- Efficiency >99%
- 20ns resolution
- <250-400 mW/cm²

+ Full digital readout
+ 2x2 cm² size
MuPix Tracker Construction

Ultra-thin detector mock-up:
- sandwich of 25 µm Kapton®
- 50/100 µm glass (instead of Si)

50 µm silicon wafer

X/X₀ ~ 0.1% per layer
Summary

- CMOS detectors = System on Chip
- provides very thin sensors and small pixels
- used and/or considered for many upgrade projects
- HV-CMOS (HV-MAPS) solves timing and rate issues

→ clearly the way to go in future!
Outlook

HV-MAPS for LHC or FCC experiments?

ATLAS II tracker (ITK)
- costs ~130 MCHF
- 14 tracking layers (10 strip + 4 pixel)
- $X/X_0 \sim 1\text{-}2\%$ per layer

ATLAS stereo strip module

HV-MAPS Pixel only tracker?
- only 6-9 pixel layers required
- 0.1-1% per radiation length
- reduced material costs
- reduced assembly costs
- 3D tracking $\rightarrow$ performance
Pulse Shape Measurement with ToT

ToT = time over threshold

Signal

Threshold

Latency

ToT

Time
Noise Measurement with Threshold Scan

(a) HV: -1 V

(b) HV: -70 V
Silicon on Insulator (SOI) Concept

- CMOS
- buried oxide layer (insulator)
- depletion zone

- depletion ~50 um
- signal ~ 3000e
- noise ~ 30e

higher radiation tolerance with n-well and p-well

T. Hemperek et al. (Bonn)
Austria Microsystems™ (AMS)

- High-Voltage CMOS technology
- H18 process 0.18 µm available since March 2012
- 1.8V, 5V, 20V and 50V devices on a single chip without any process modifications
Mu3e Baseline Design

Long cylinder!

~180 cm

~15 cm

Recur pixel layers

Scintillator tiles

μ Beam

Target

Scintillating fibres

Inner pixel layers

Outer pixel layers

B = 1 Tesla

not to scale