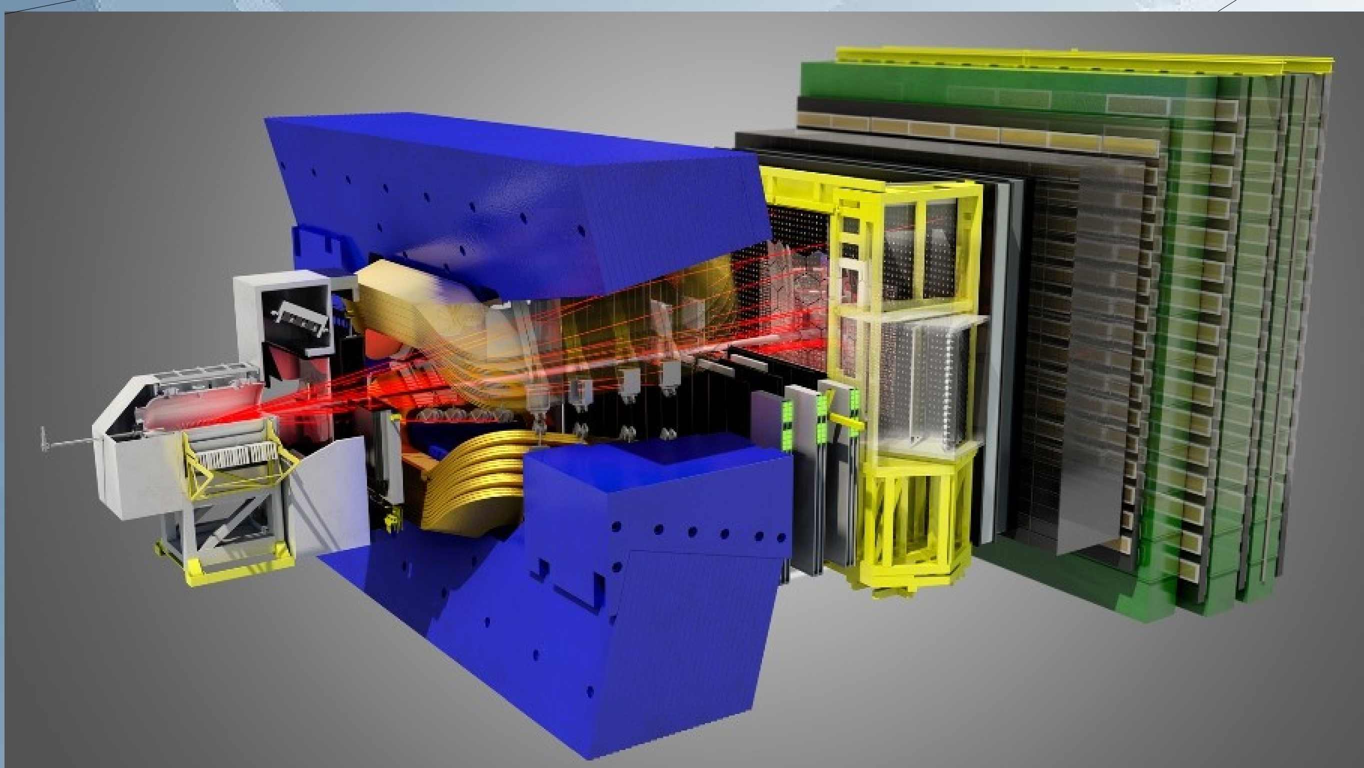
CMOS Detectors
Ingeniously Simple!

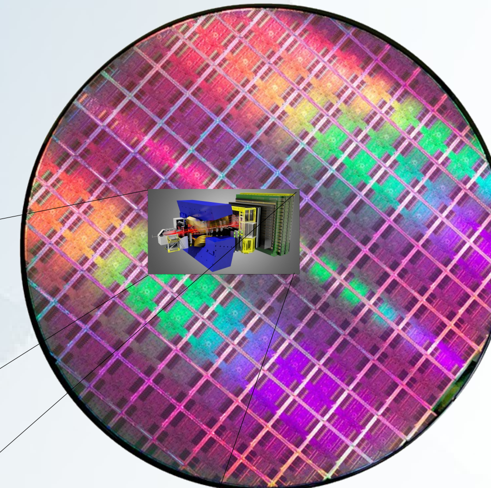
A.Schöning
University Heidelberg

B-Workshop

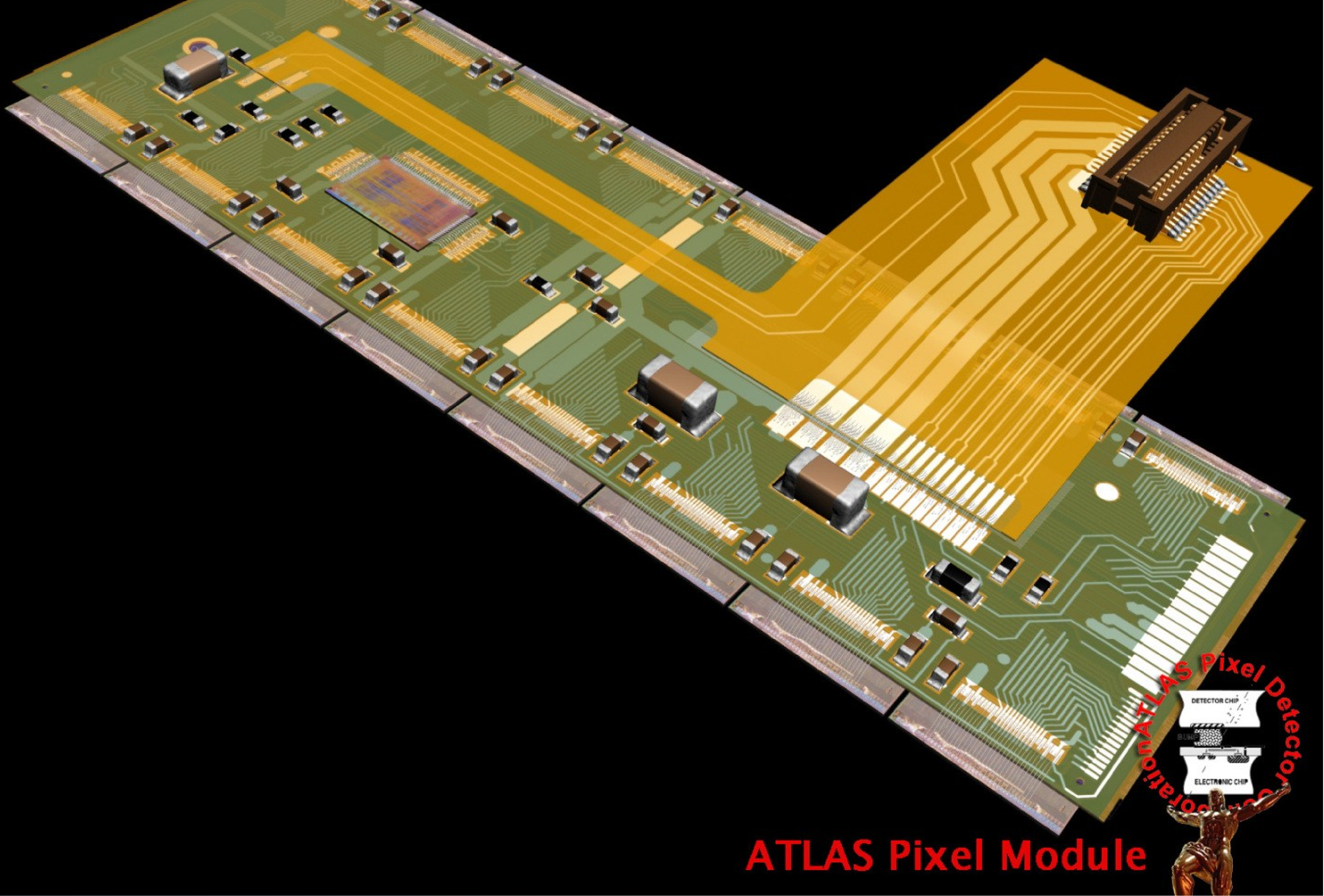
Neckarzimmern 18.-20.2.2015

Detector System on Chip?





ATLAS Pixel Module



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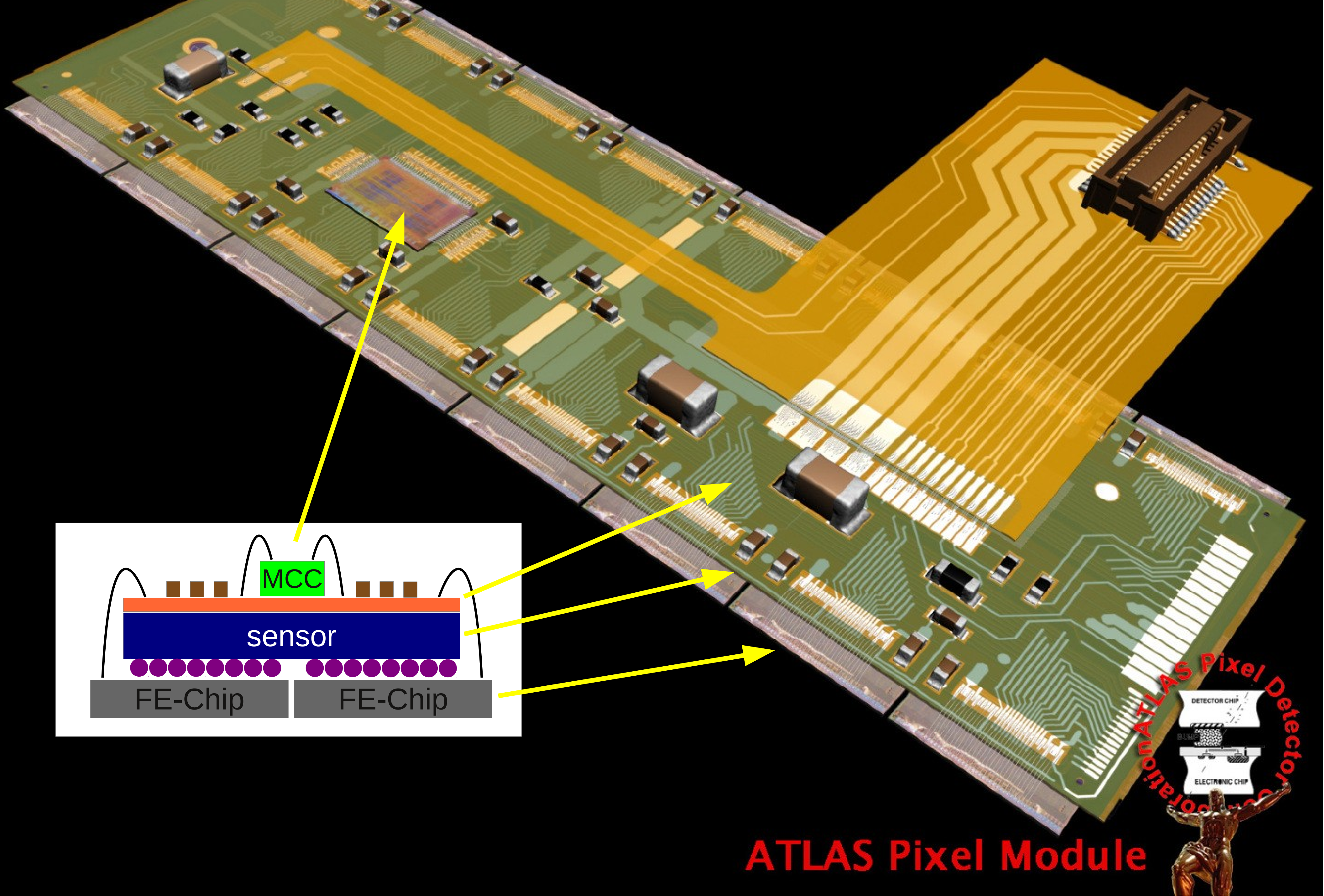
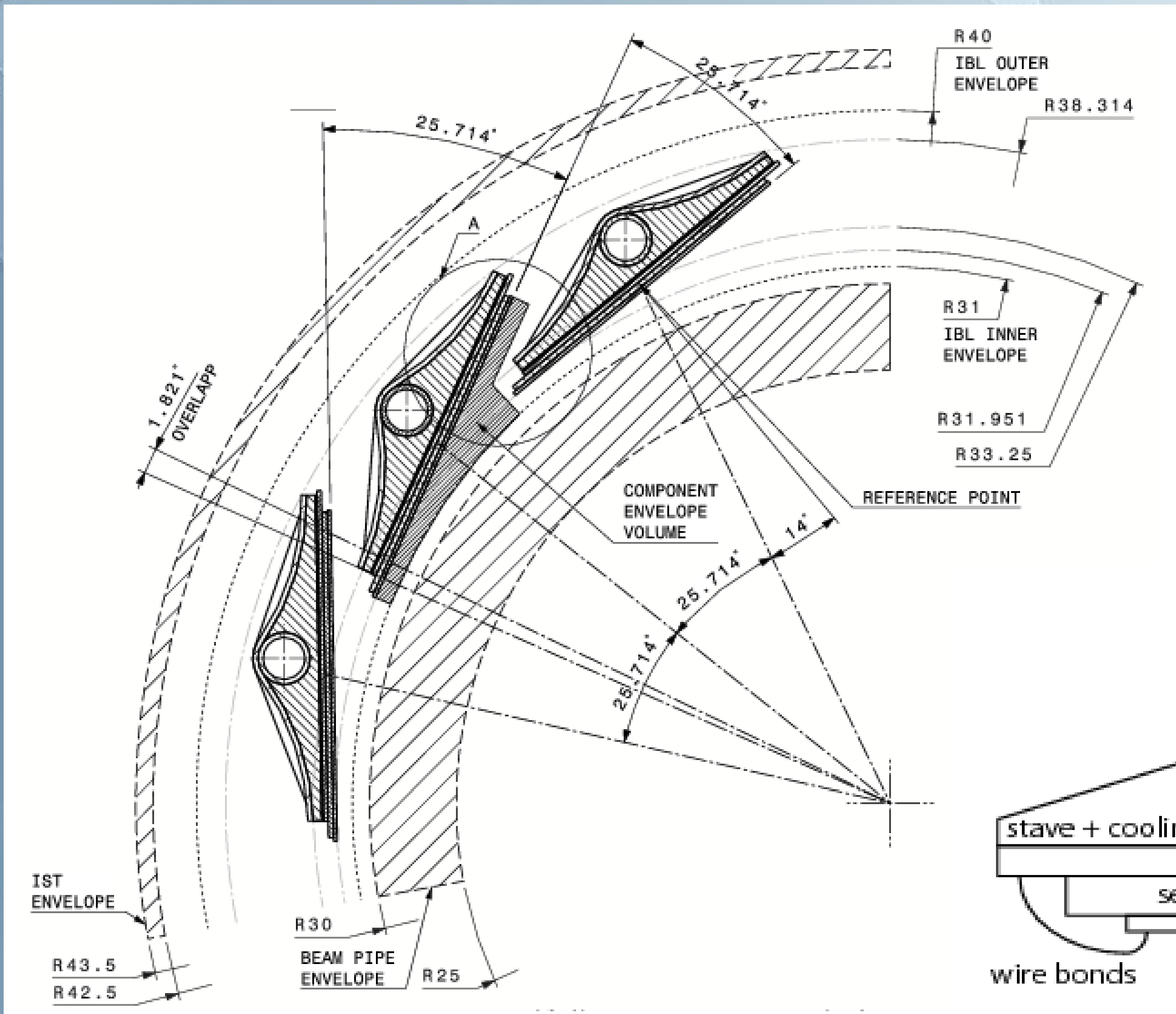
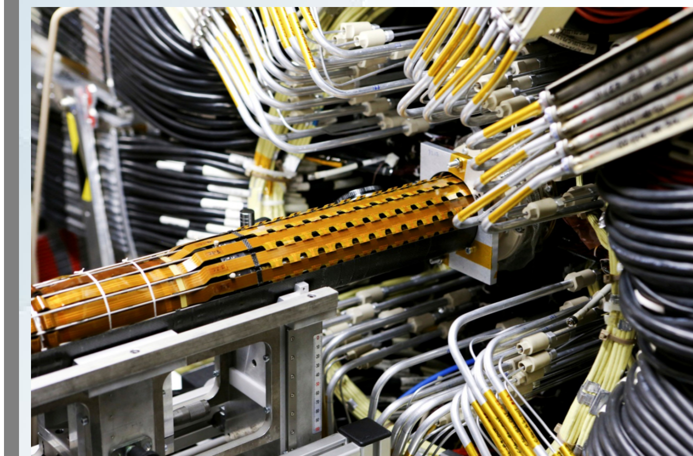
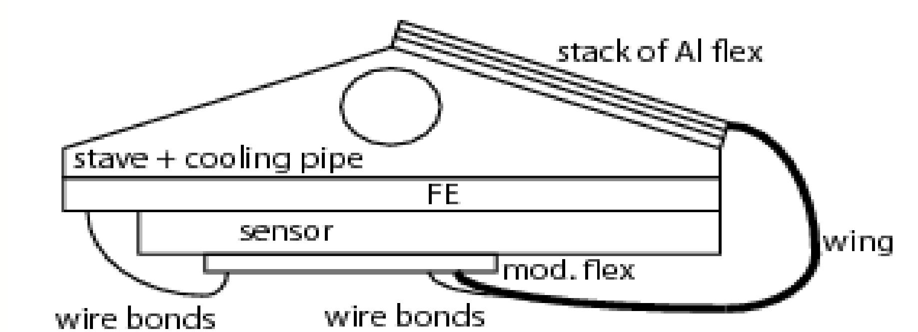


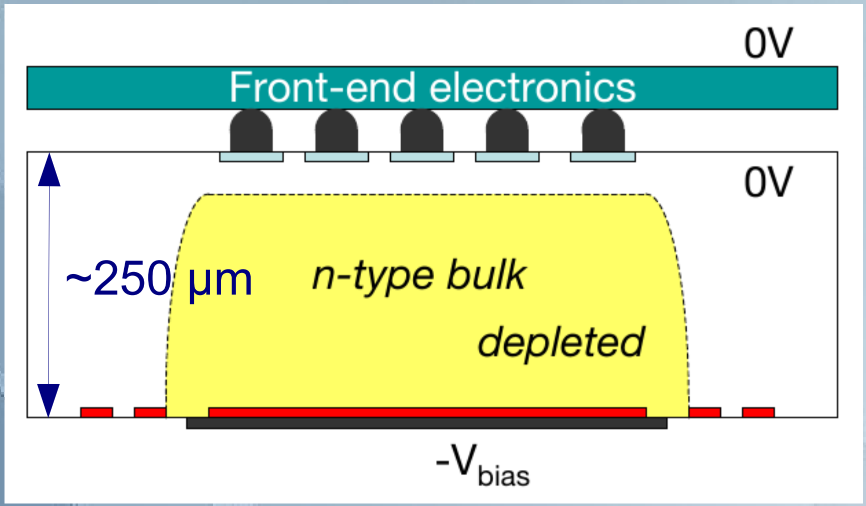
ATLAS Insertable B-Layer

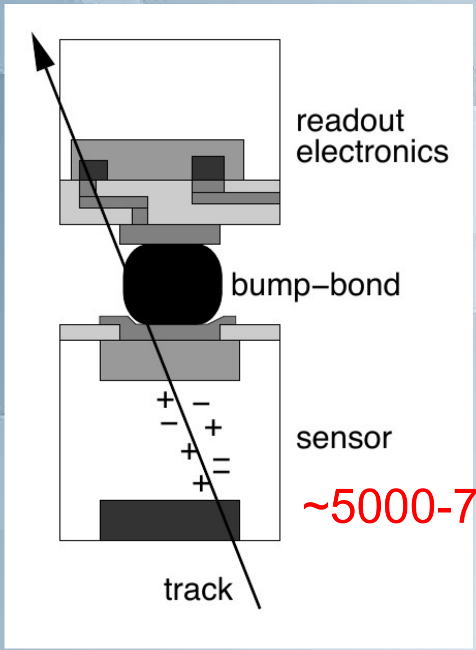






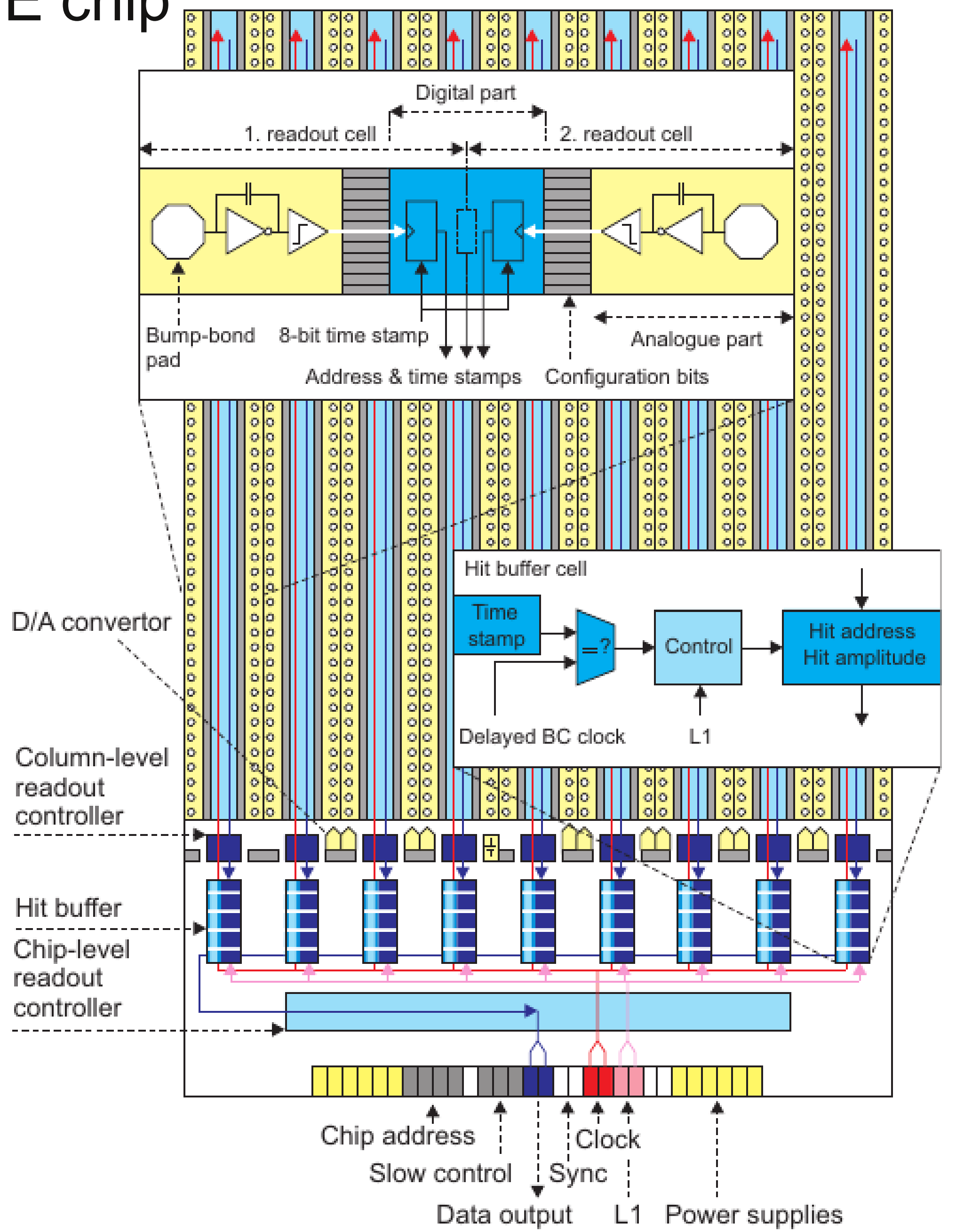
ATLAS Pixel Module



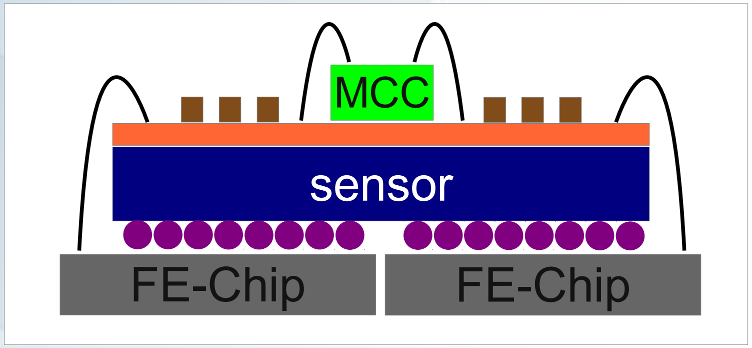


~5000-7000 e

FE chip



Silicon Hybrid Detectors

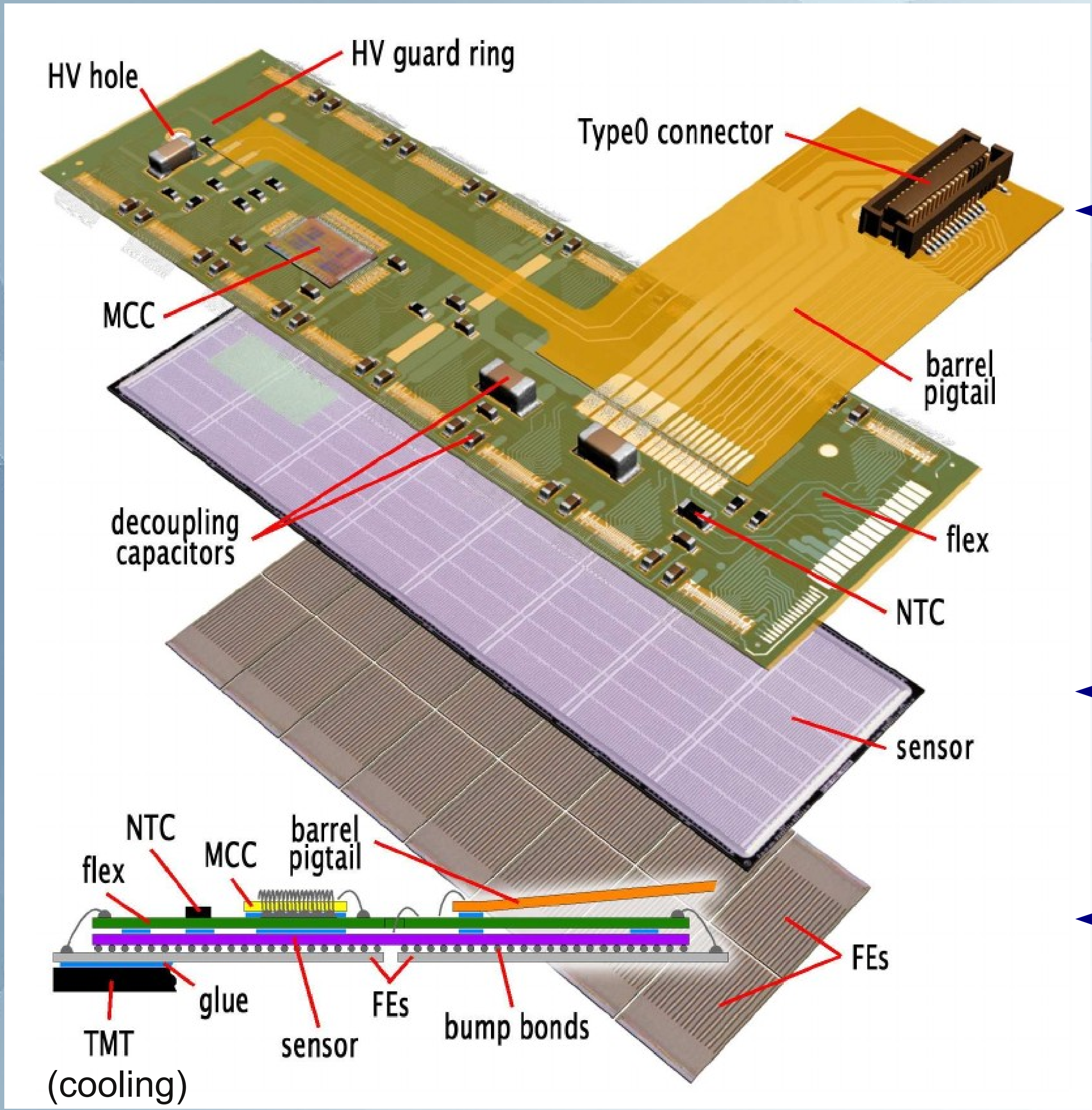


Features

- high signal and high noise
- complex compound
- bump bonding
- wire wrapping
- custom-made sensor
- lots of material (radiation lengths!)

- expensive (e.g. ATLAS II pixel HW: 16 mill.CHF for ~5m^2)
- scalability problem (e.g. Future experiments at FCC)
- miniaturization problem $>10^8/m^2$ bump bonds?
- quality assurance problem

Silicon Detector

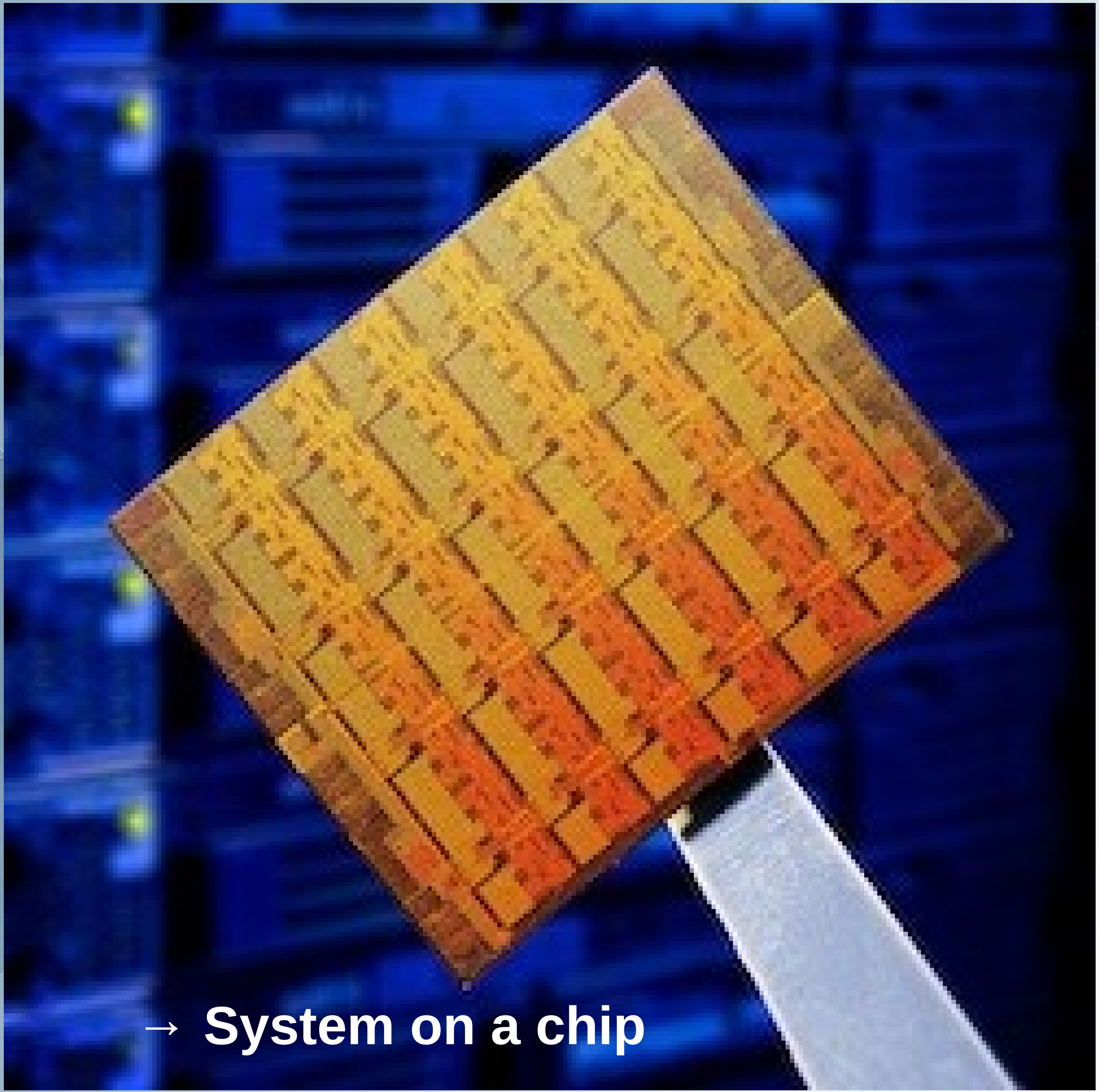


cables

sensor
(silicon)

CMOS
(intelligence)

Silicon Detector → CMOS chip

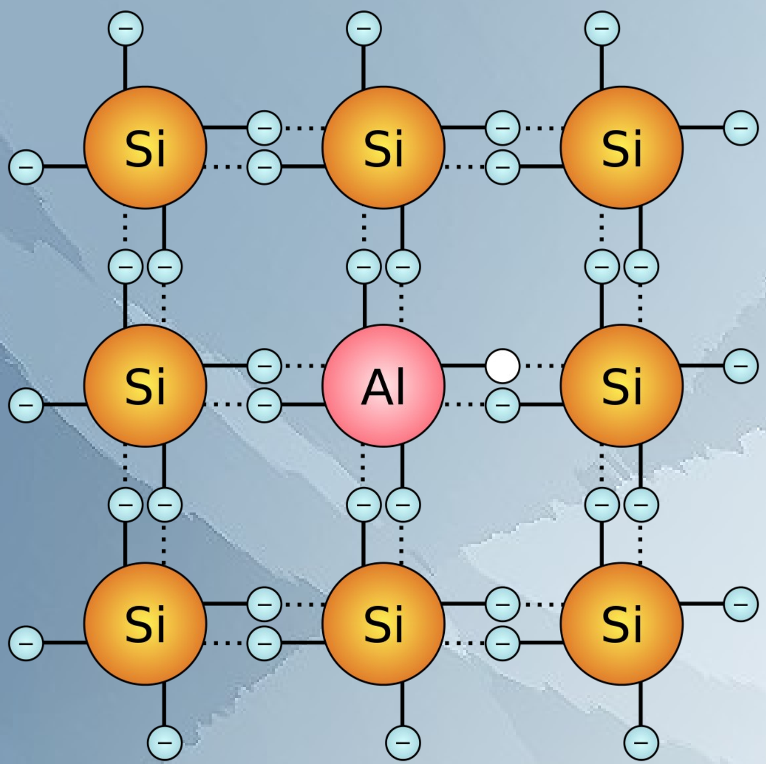


- no composite
- no interconnects
- simplified design (ASIC design)
- profits from miniaturisation

CMOS Features

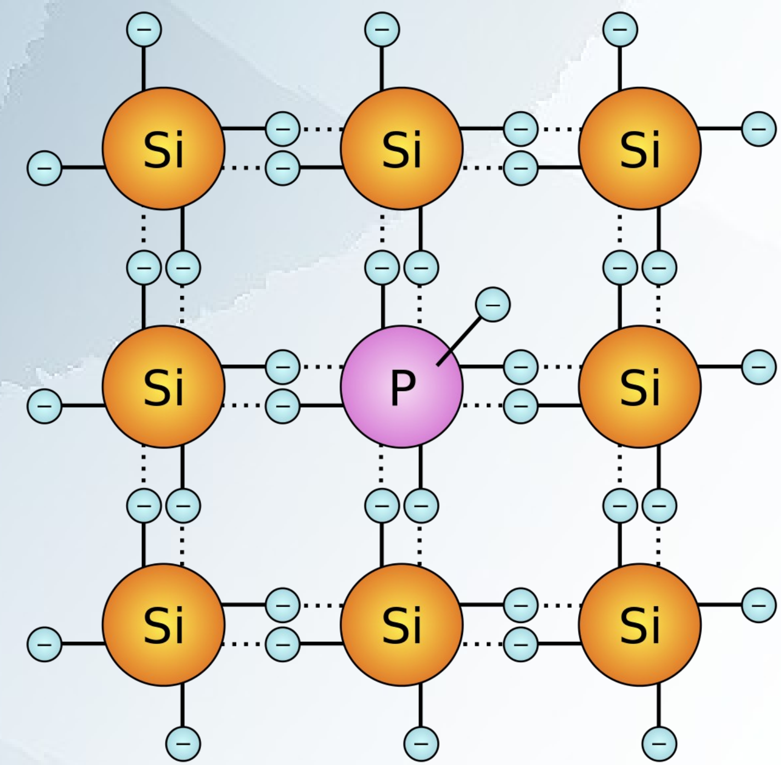
- minimum pixel size 10-20 feature size
  → **5µm possible!!!**
- low power (CMOS)
- low noise compared to hybrids
- compact VLSI design
- standard process
- cheap

Dopings



p-type

holes are majority charge carriers



n-type

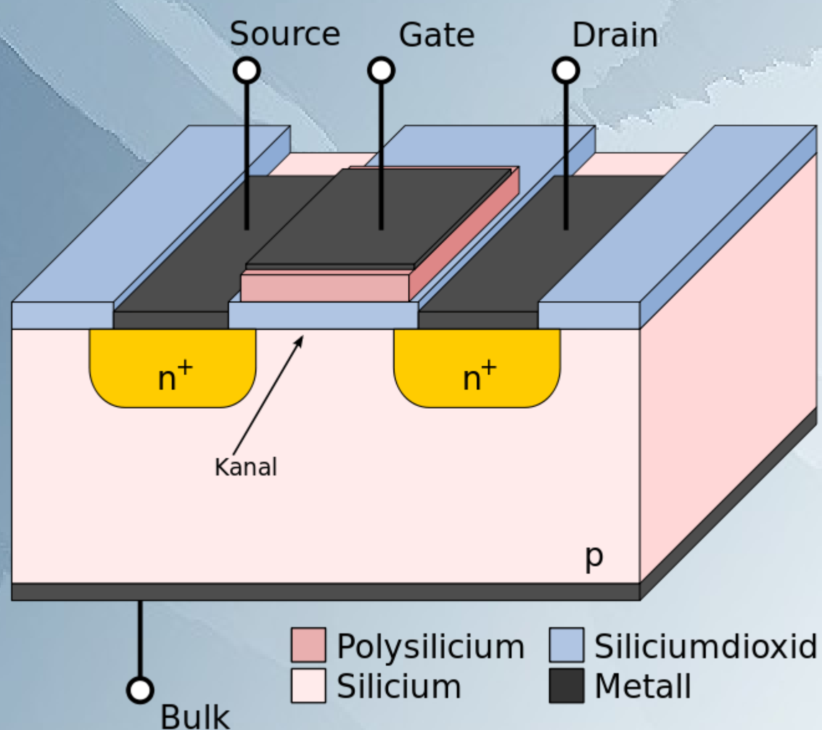
electrons are majority charge carriers

What is CMOS?

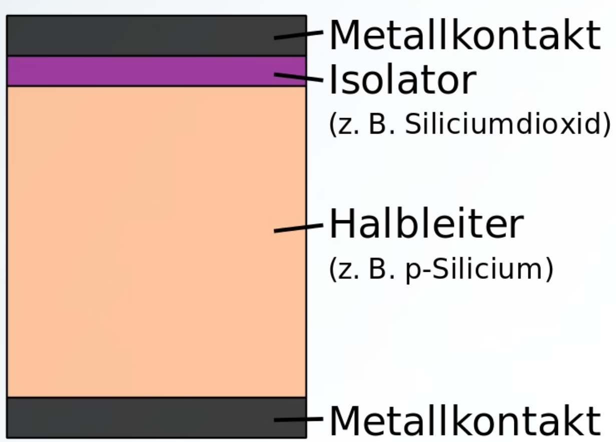
Complementary Metal Oxide Semiconductors

- **n-channel MOSFET (NMOS)**
- **p-channel MOSFET (PMOS)**

MOSFET= metal oxide semiconductor field effect transistor



Metal-Isolator-Semiconductor (MISFIT)- structure



What is CMOS?

Complementary Metal Oxide Semiconductors

- **n-channel MOSFET (NMOS)**
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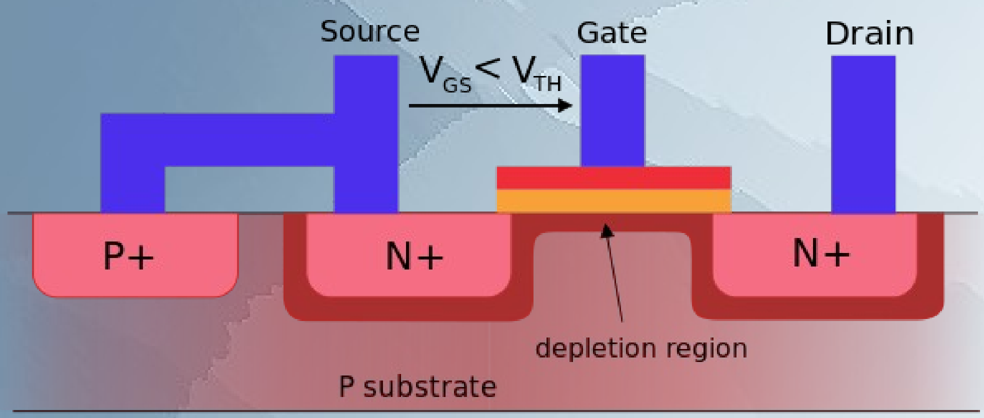
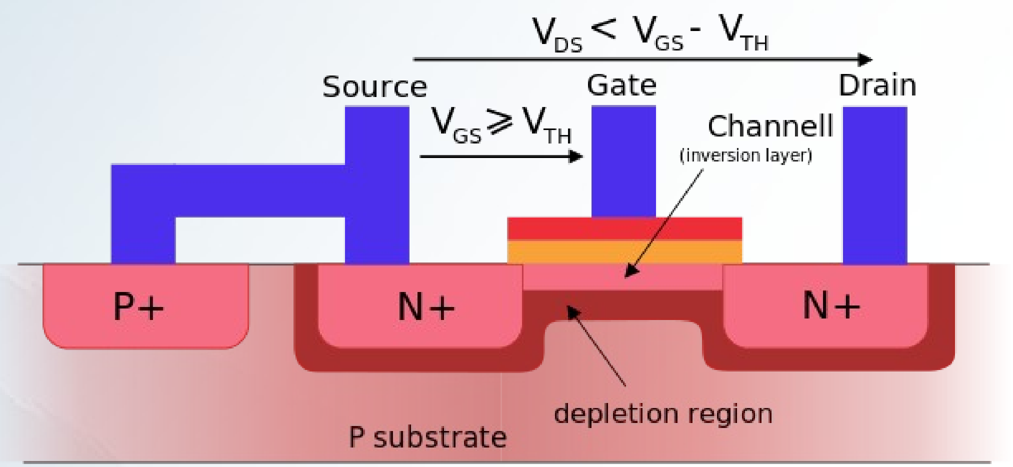
MOSFET=metal oxide semiconductor field effect transistor

n-channel (NMOS)

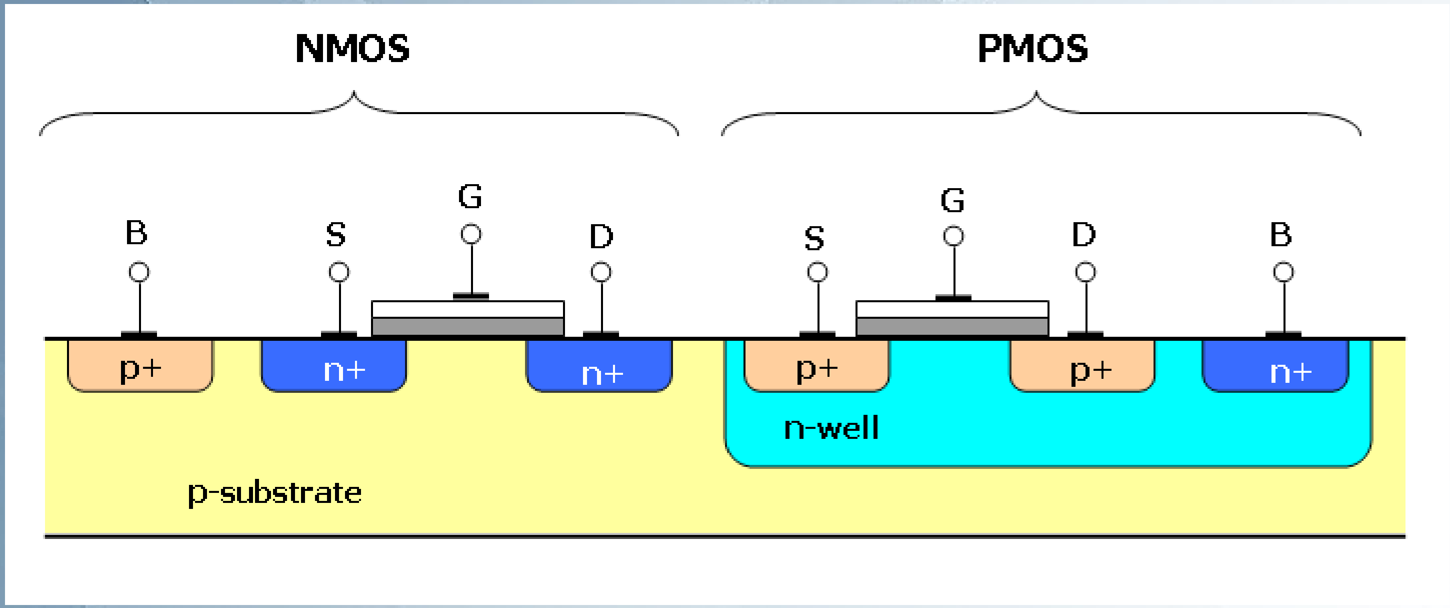


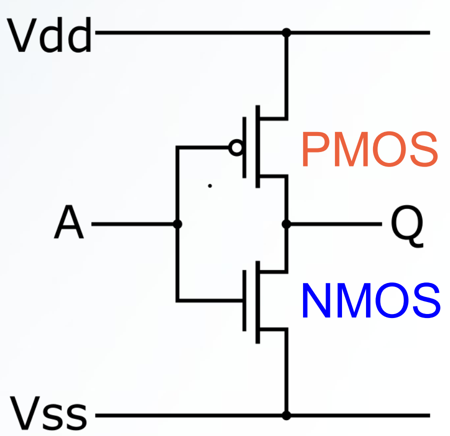


Linear operating region (ohmic mode)

Advantages of CMOS

- fast switching characteristics
  → used for CPUs
- no ohmic resistors needed
  → low power
- easy to implement capacitors

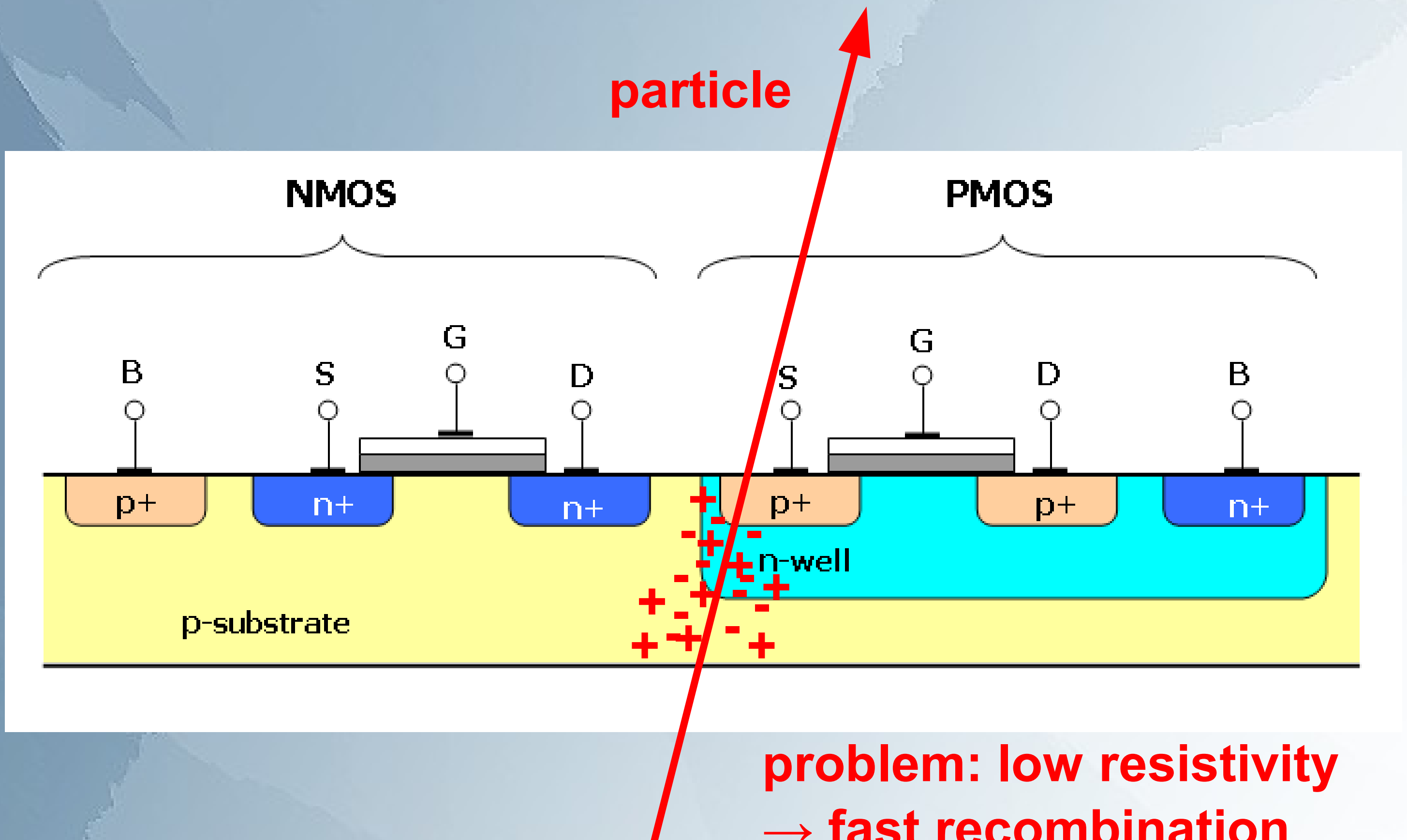




CMOS Inverter

Monolithic Active Pixel Sensors (MAPS)

How to design a CMOS particle detector?

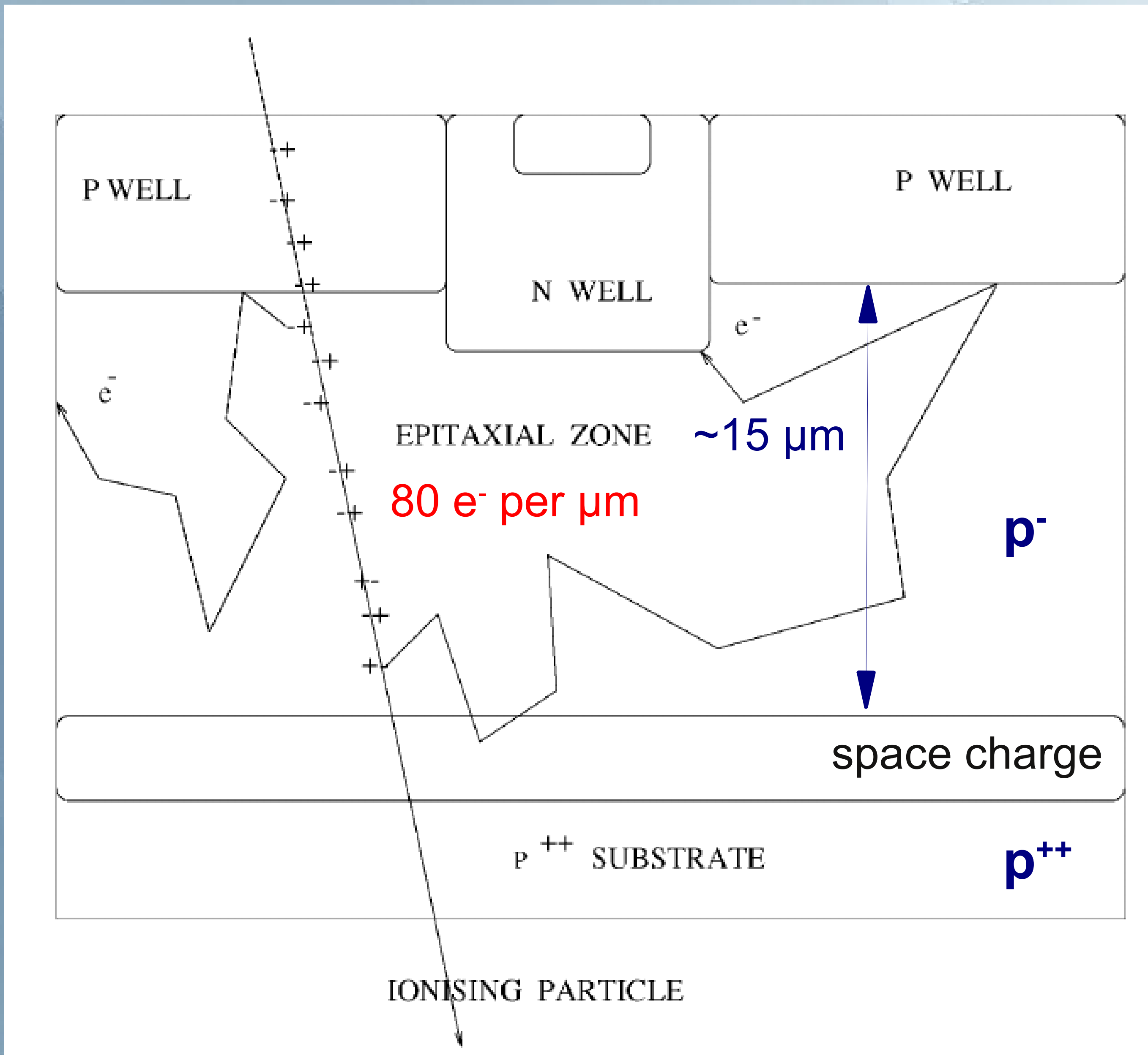


monolithic = single process

problem: low resistivity
→ fast recombination
→ small charge collection

The MAPS Principle

D.Husson, NIMA 461 (2001) 511-513



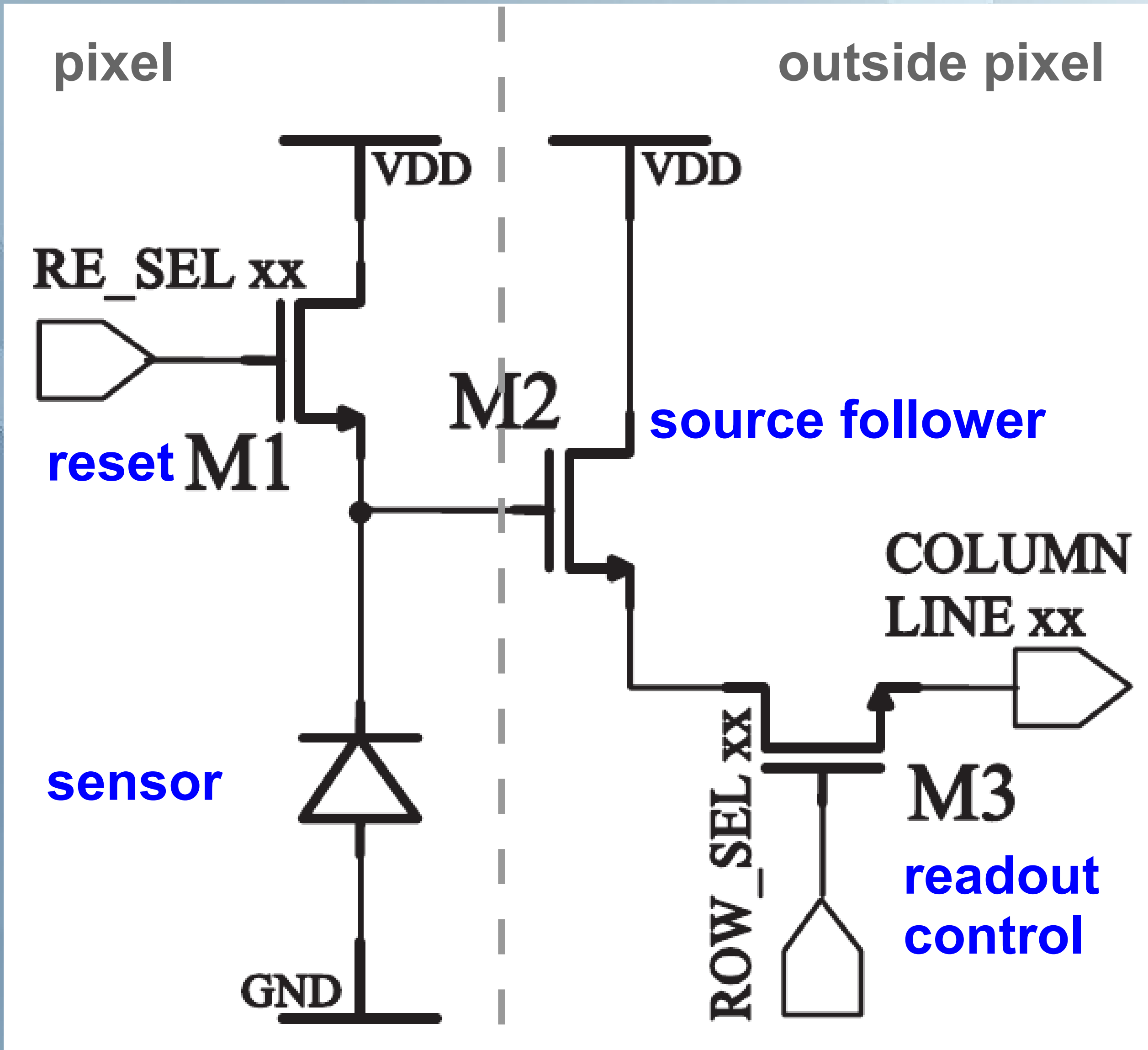
MIMOSA =
Minimum **I**onizing **MOS**
Active pixel sensor

- **diffusion**
- **random walk**
- **recombination!**

time scale: τ ~ 100 ns

voltage ~3V

MIMOSA Schema



Berst et al. (1999)

Idea dates back to the 1980ies → SSC

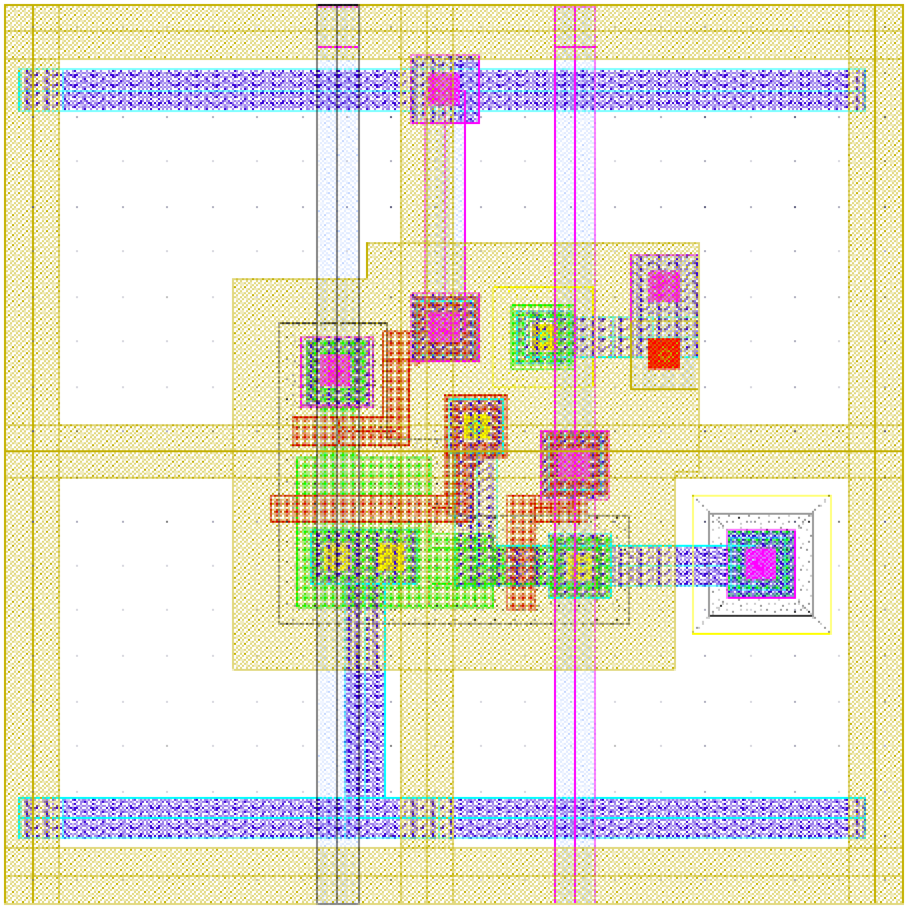
Sh. Parker, NIMA 275 (1989) 494

<u>Challenge:</u>
separation of analog and control signals

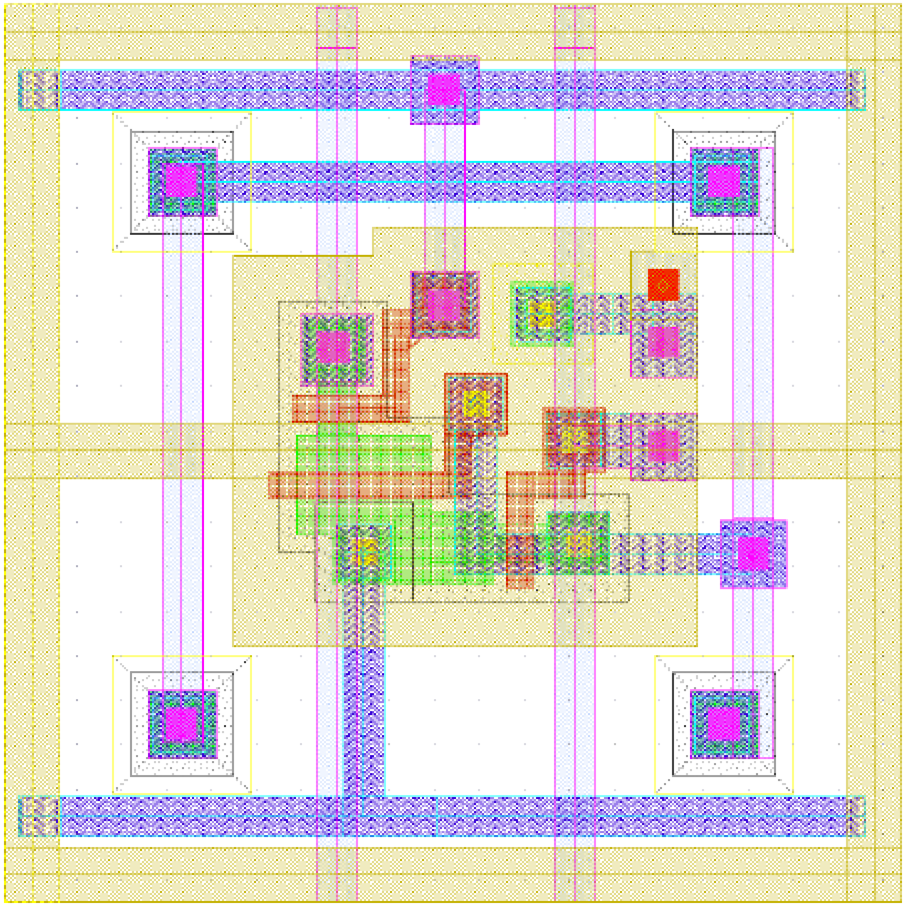
e.g. readout control should not affect signal

MIMOSA Pixel Layout

1-diode pixel



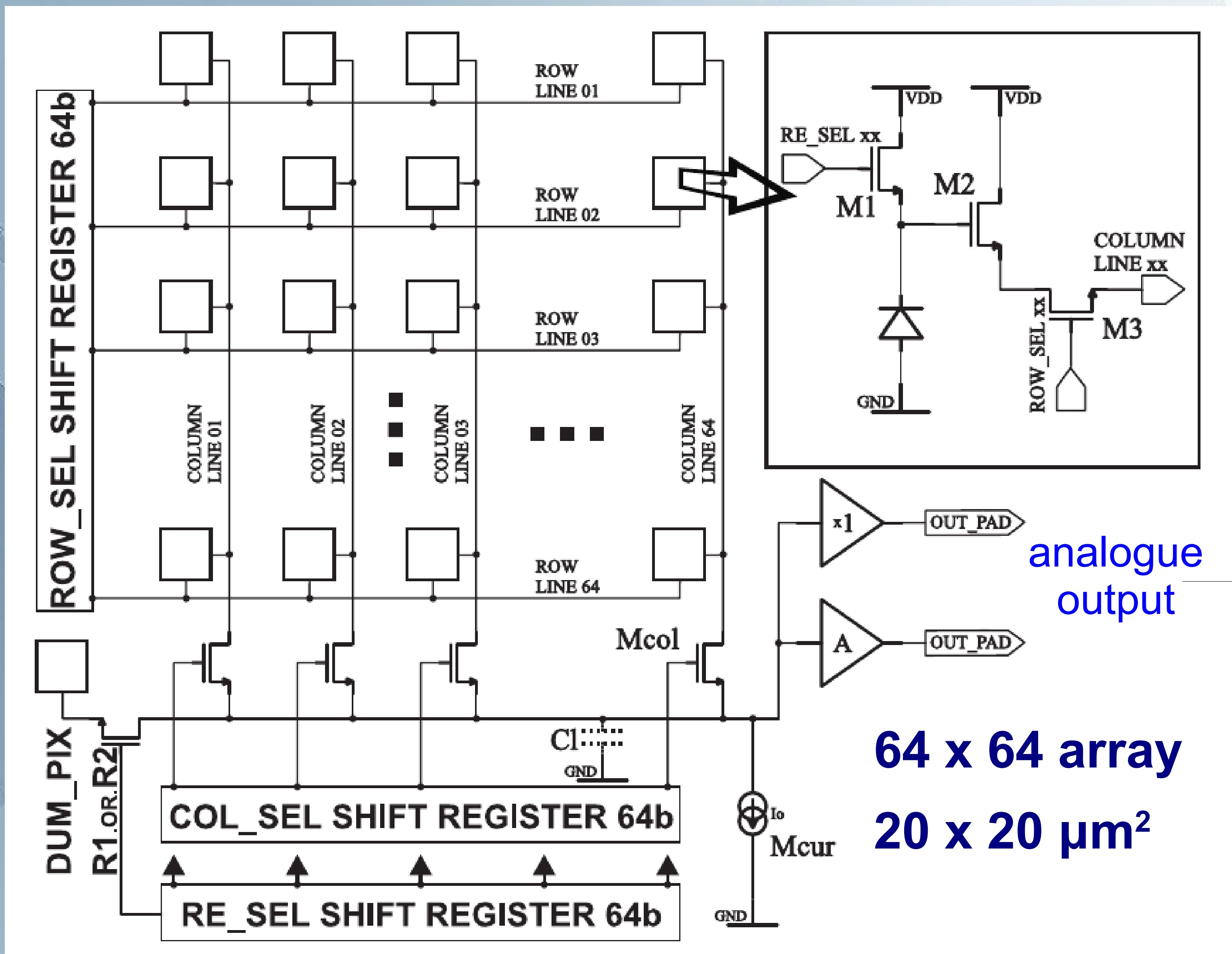
4-diode pixel



transistors (intelligence) on sensor!

Rolling Shutter MAPS Readout

Turchetta et al. NIMA 458 (2000) 677



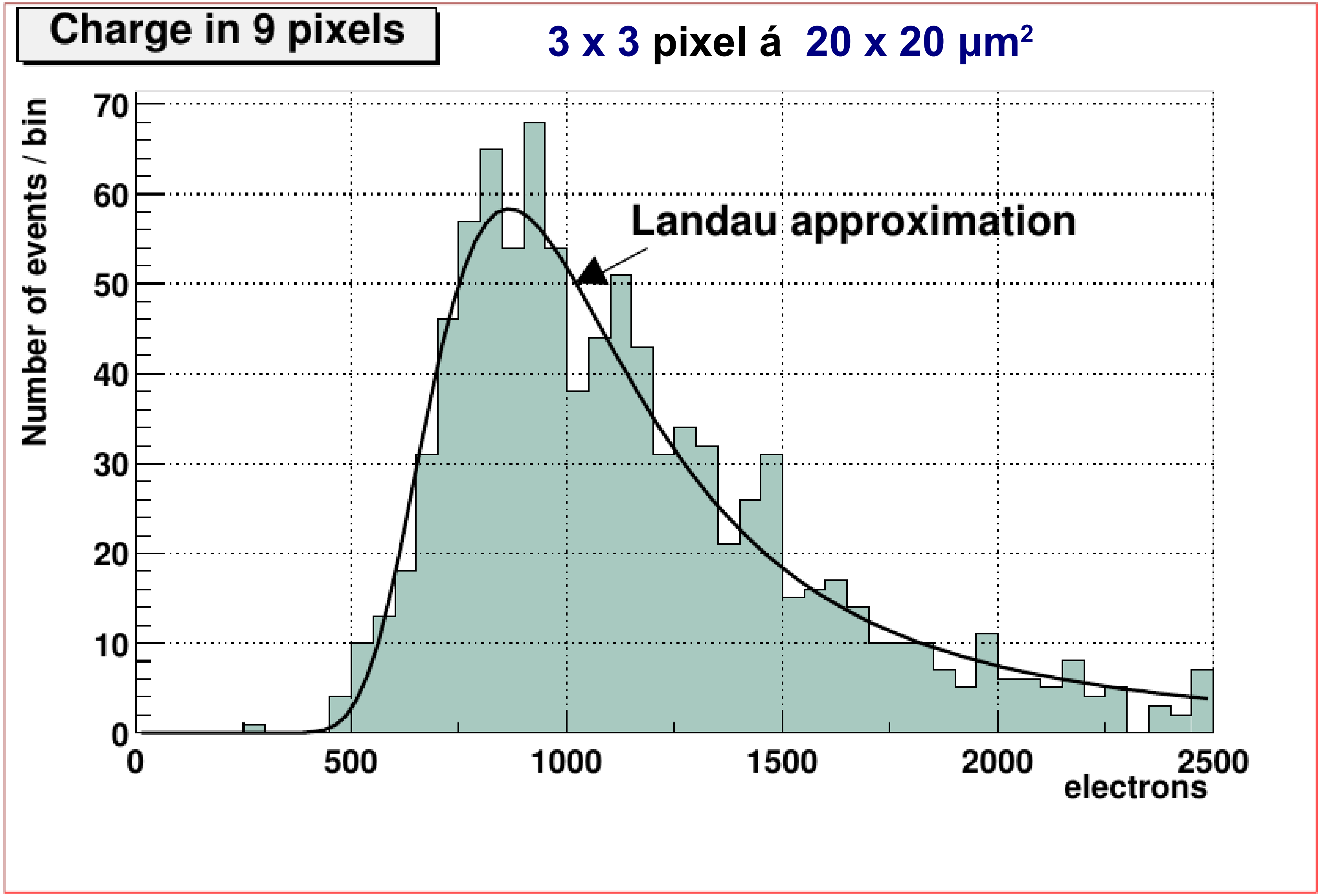
analogue output → discriminator

64 x 64 array

20 x 20 μm²

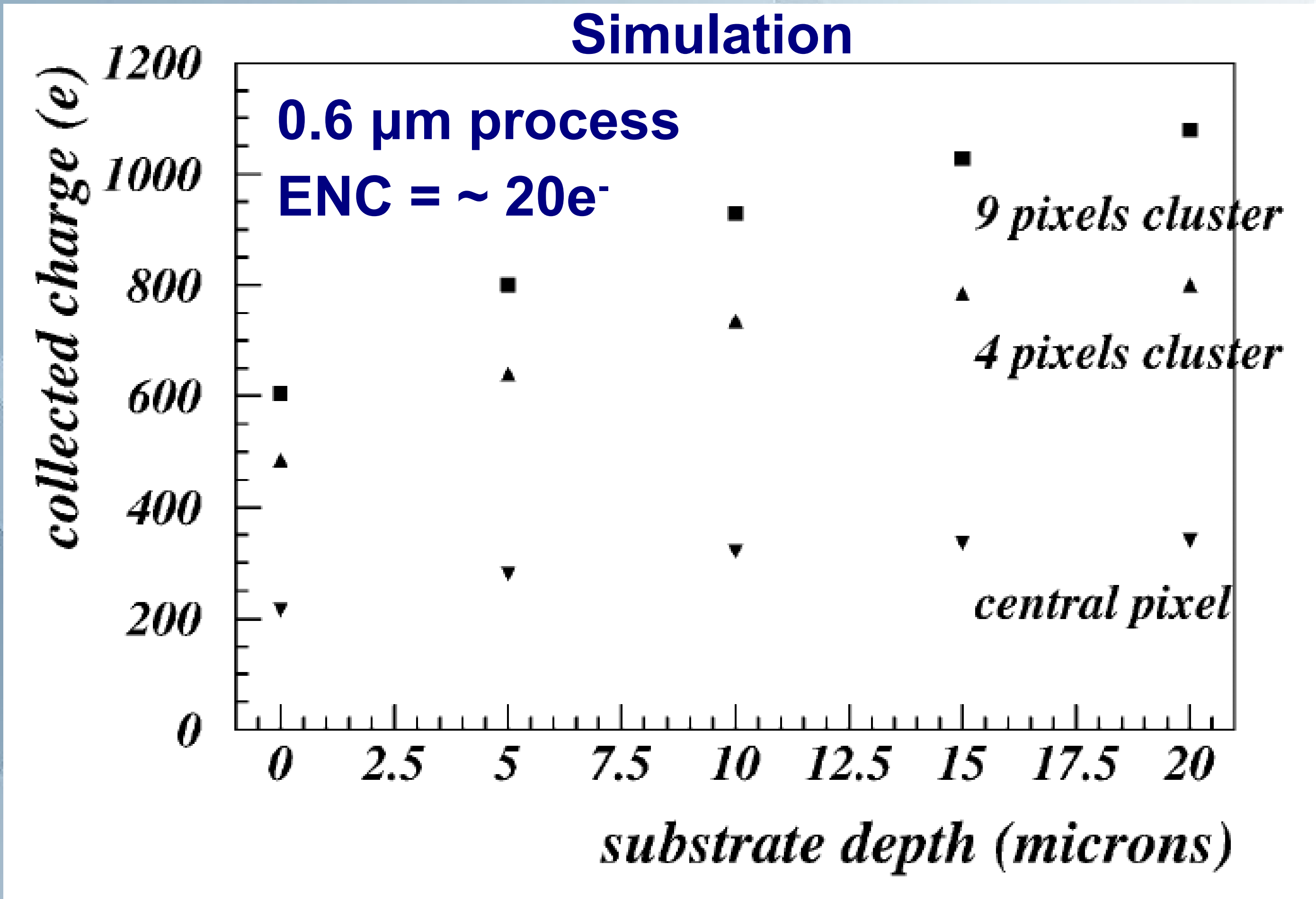
MIMOSA: Energy Distribution

Berst et al., LEPSI 99-15



The charge collection efficiency

D. Husson, NIMA 461 (2001) 511

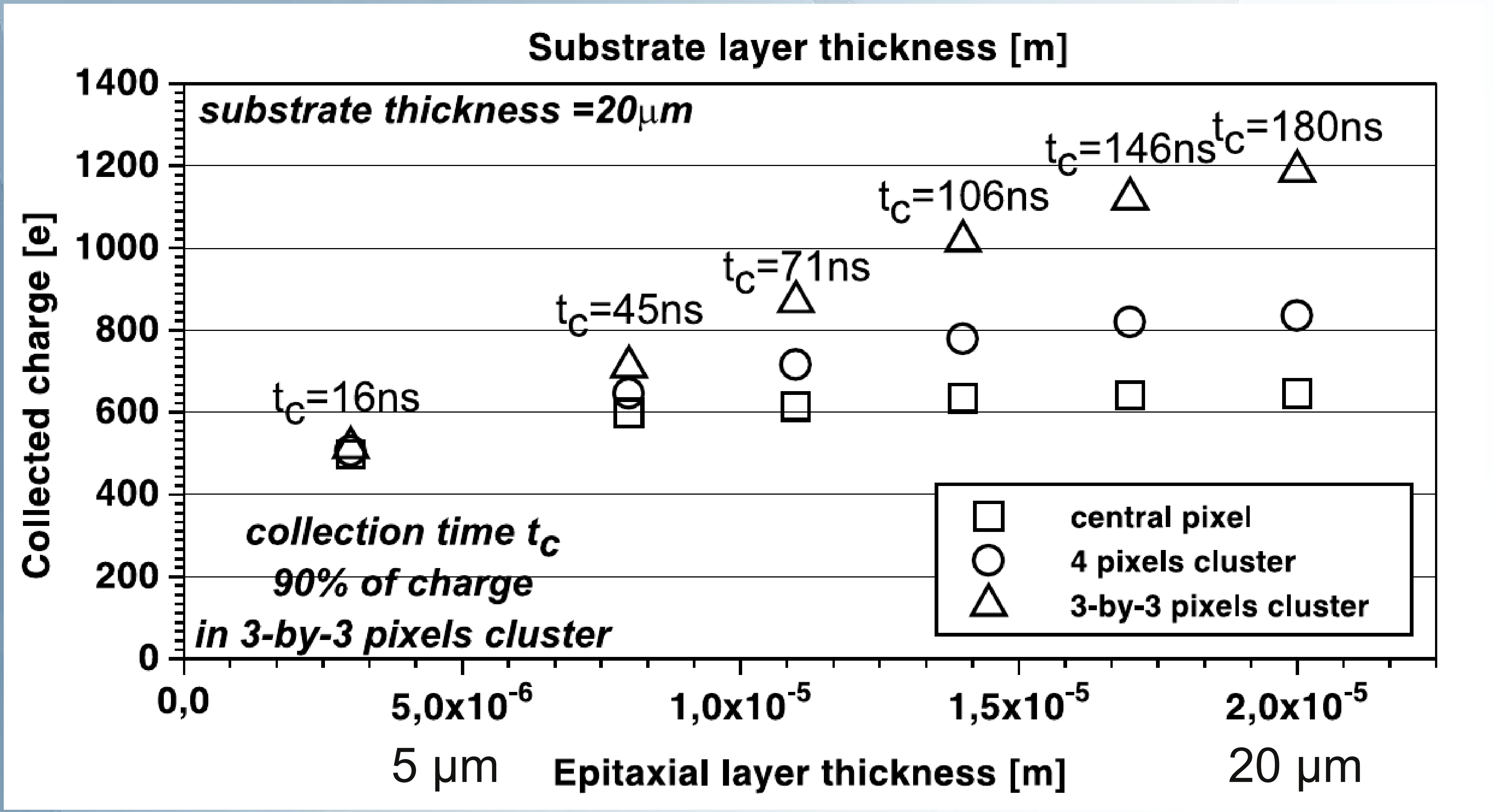


charge is spread over many pixels!

ENC = equivalent noise charge

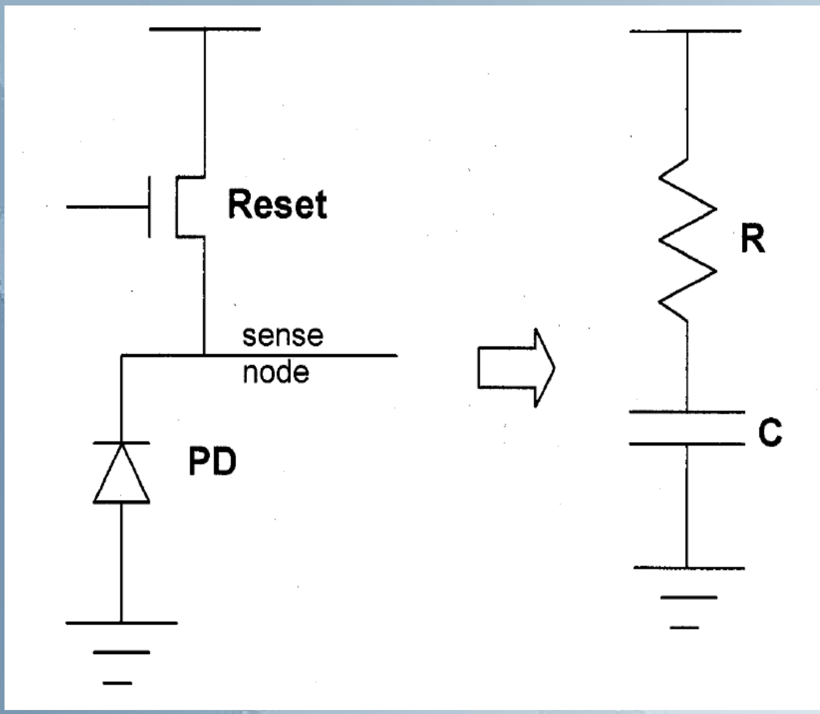
MAPS Charge Collection Time

Berst et al. (2001)



Noise in CMOS Sensors

usually dominant source is the so called Reset or Capacitive Noise:



$$V_{RMS} = \sqrt{\frac{kT}{C}}$$

$$Q = C\,V_{RMS}$$

$$\boxed{n_{RMS} = \frac{\sqrt{kTC}}{e}}$$

typical signal over noise: S/N=20-50

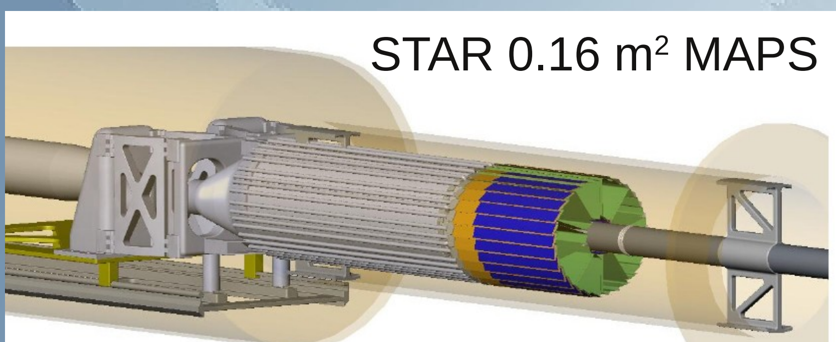
Other sources:

- **thermal noise** $S_v(w) = 4\mathrm{kTR}$
- **shot noise**
- **flickering noise (1/f)**

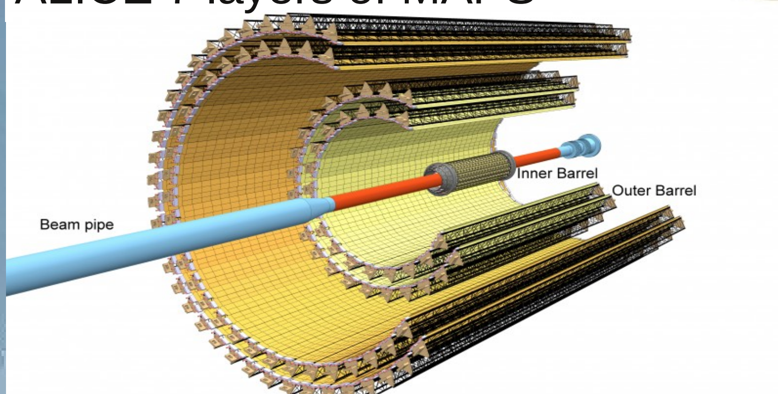
MAPS Applications

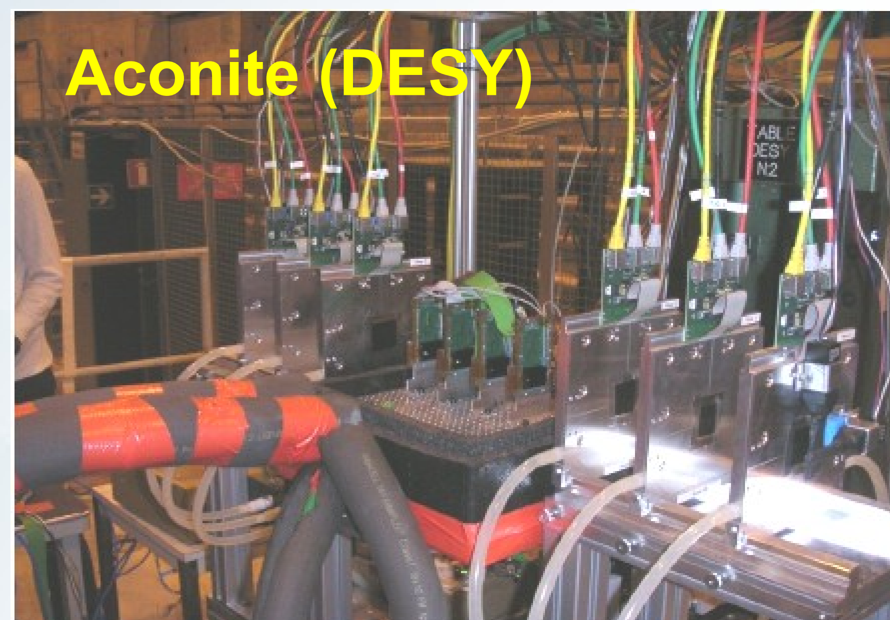
- MIMOSA originally proposed for ILD vertex detector
- used in DESY Aconite telescope (EUDET)
- STAR vertex detector (350 mill. pixel)
- new ALICE vertex detector (~ 10 m²)

applications where time resolution is not an serious issue



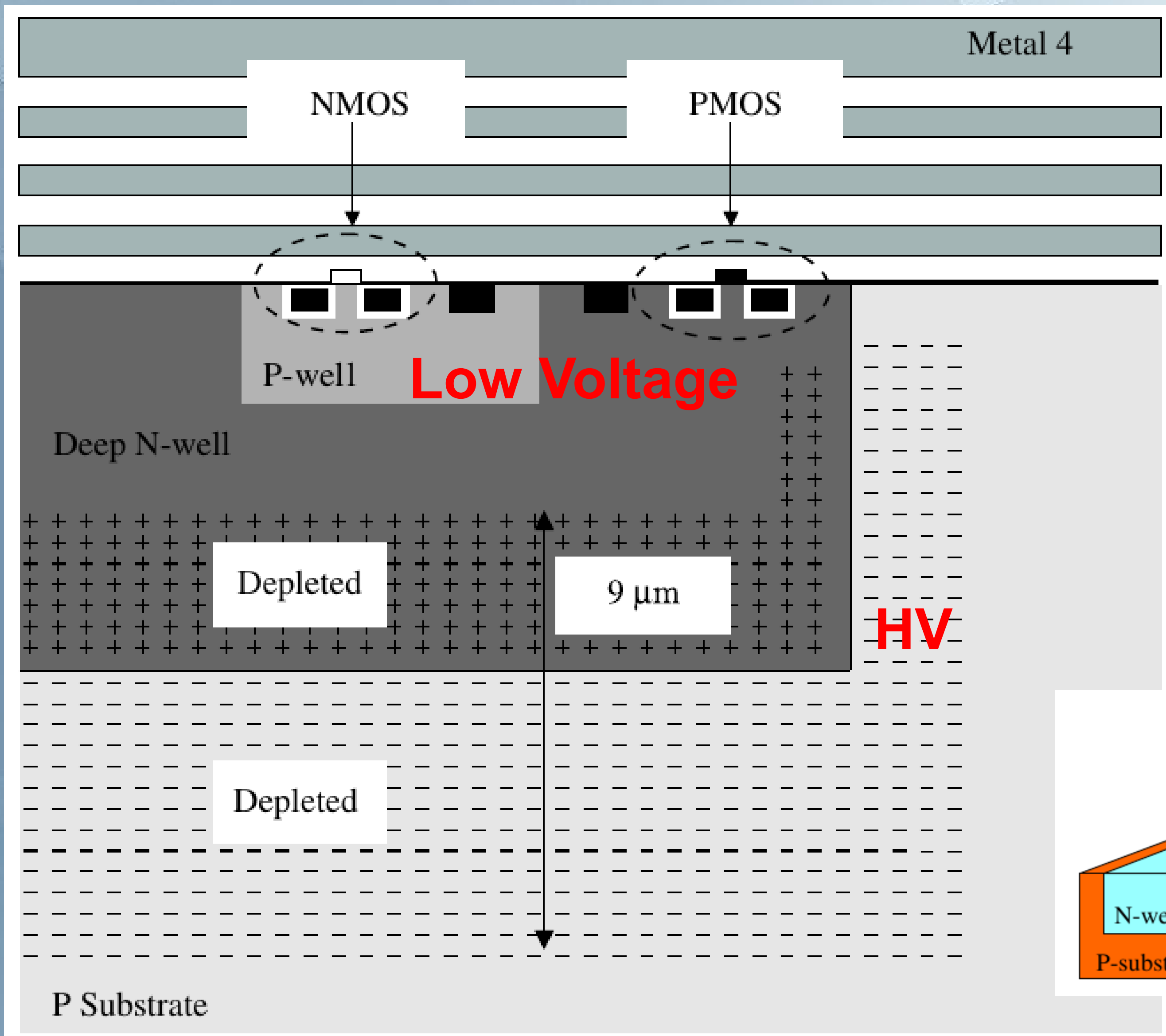
ALICE 7 layers of MAPS



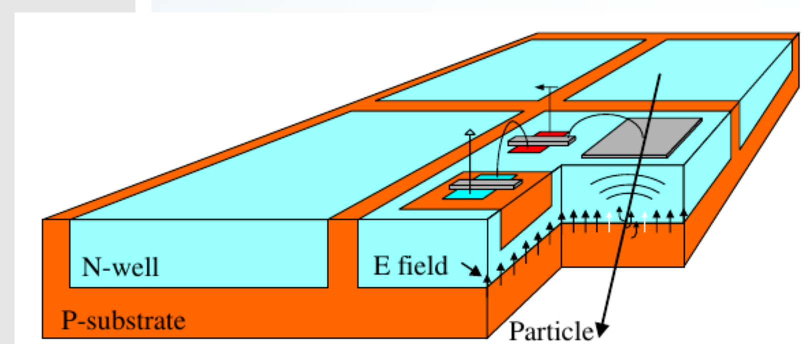


High Voltage MAPS

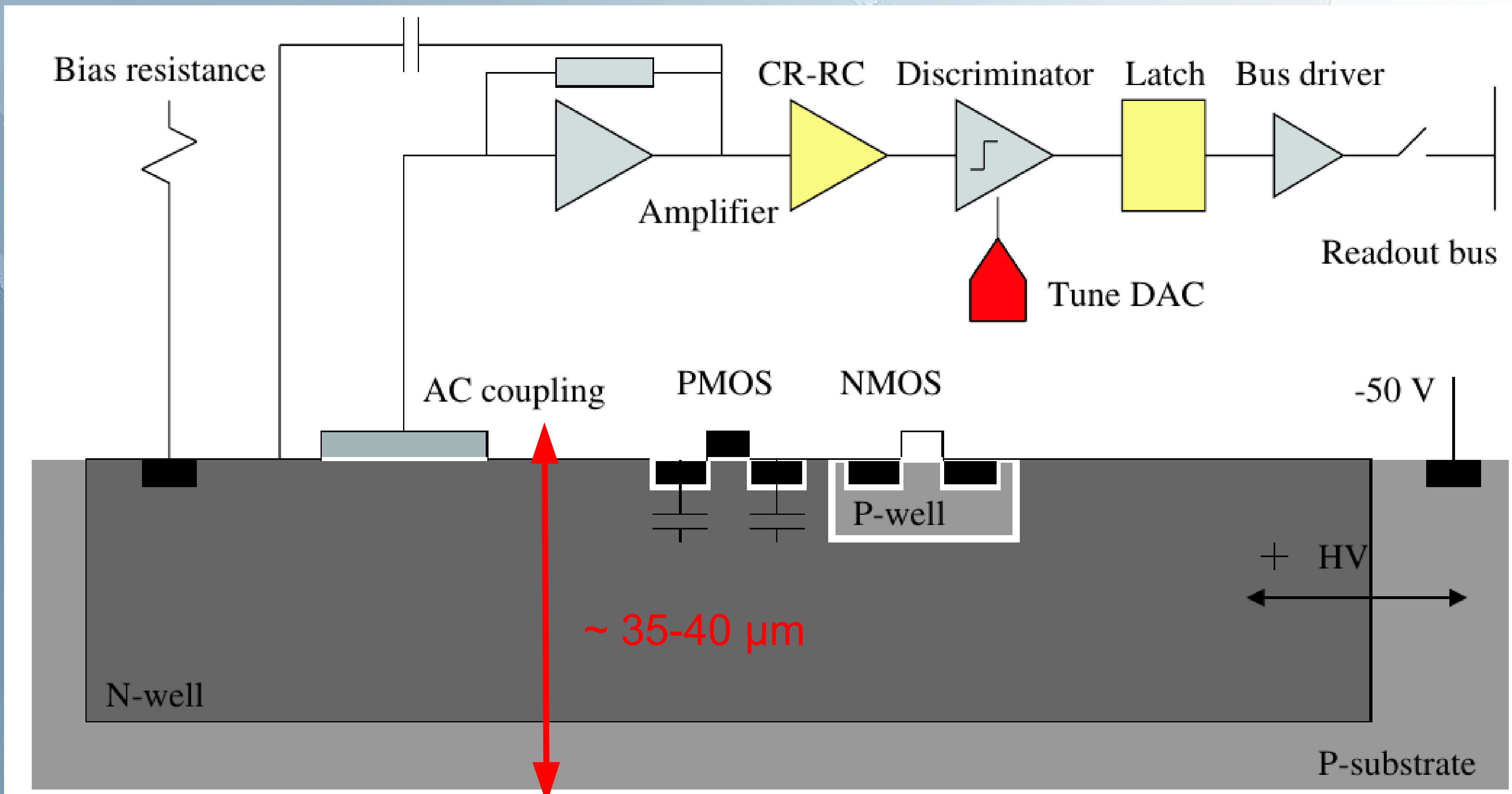
Ivan Perić, NIMA 582 (2007) 876



- **Floating structure**
- **MOSFETS in well**
- **100% fill factor**
- **high depletion at 50 V**



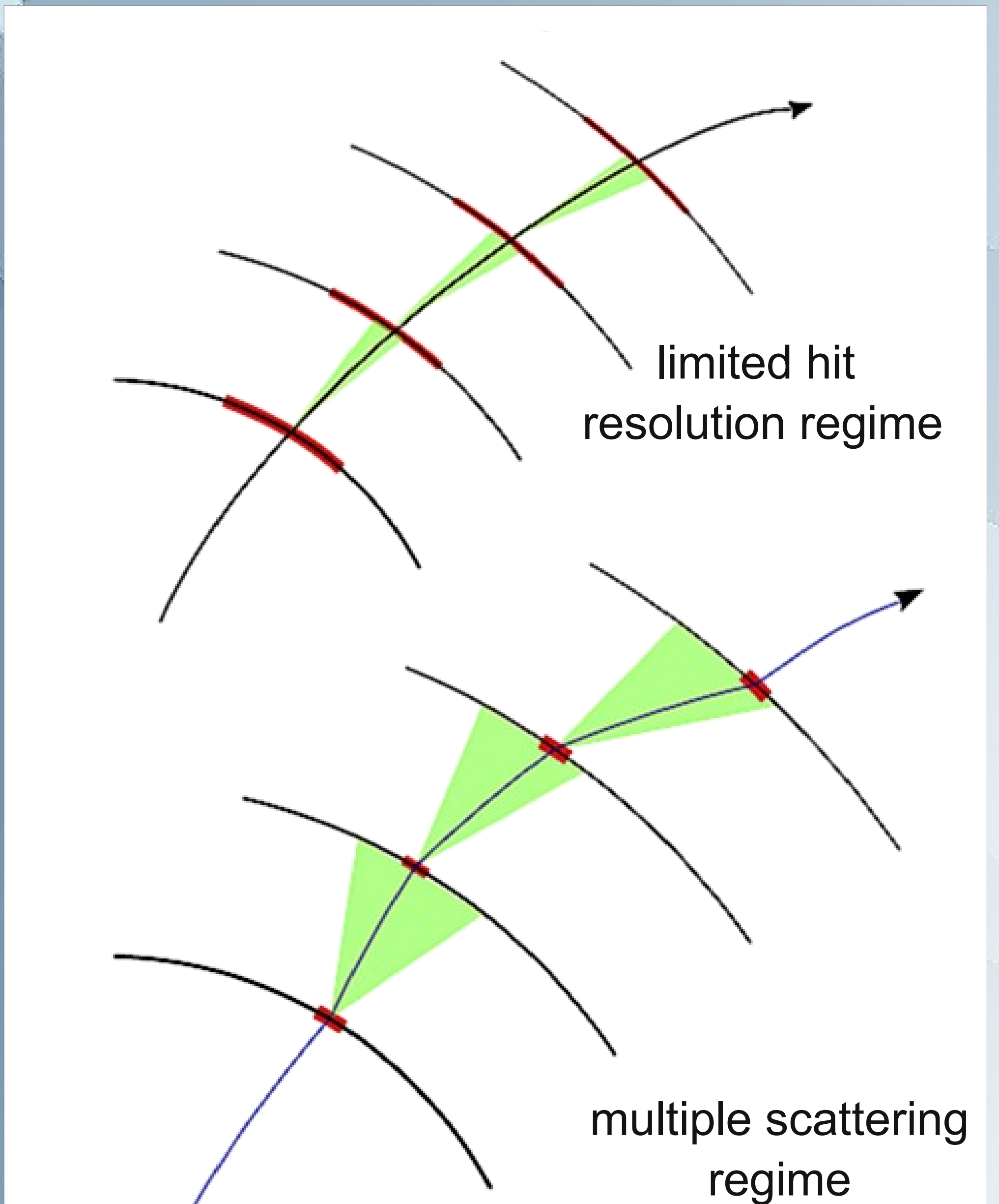
HV-MAPS Pixel Design



Fast circuit and thin sensor!

DAC = digital to analog converter → adjustment of threshold

HV-MAPS and Multiple Scattering



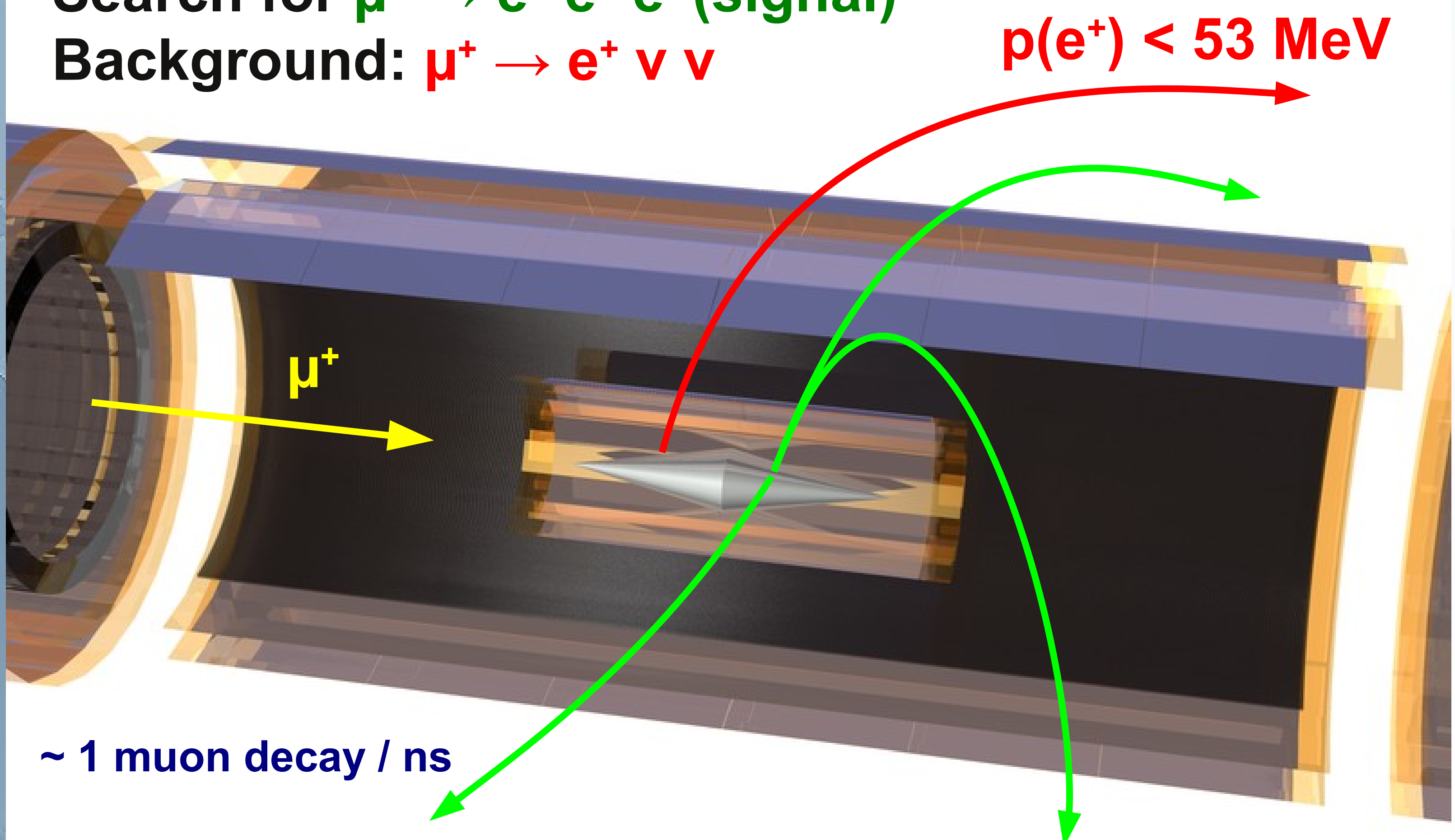
HV-MAPS:

- **allow for small pixel sizes**
- **can measure very low momentum tracks (thin sensor)**

→ multiple scattering regime

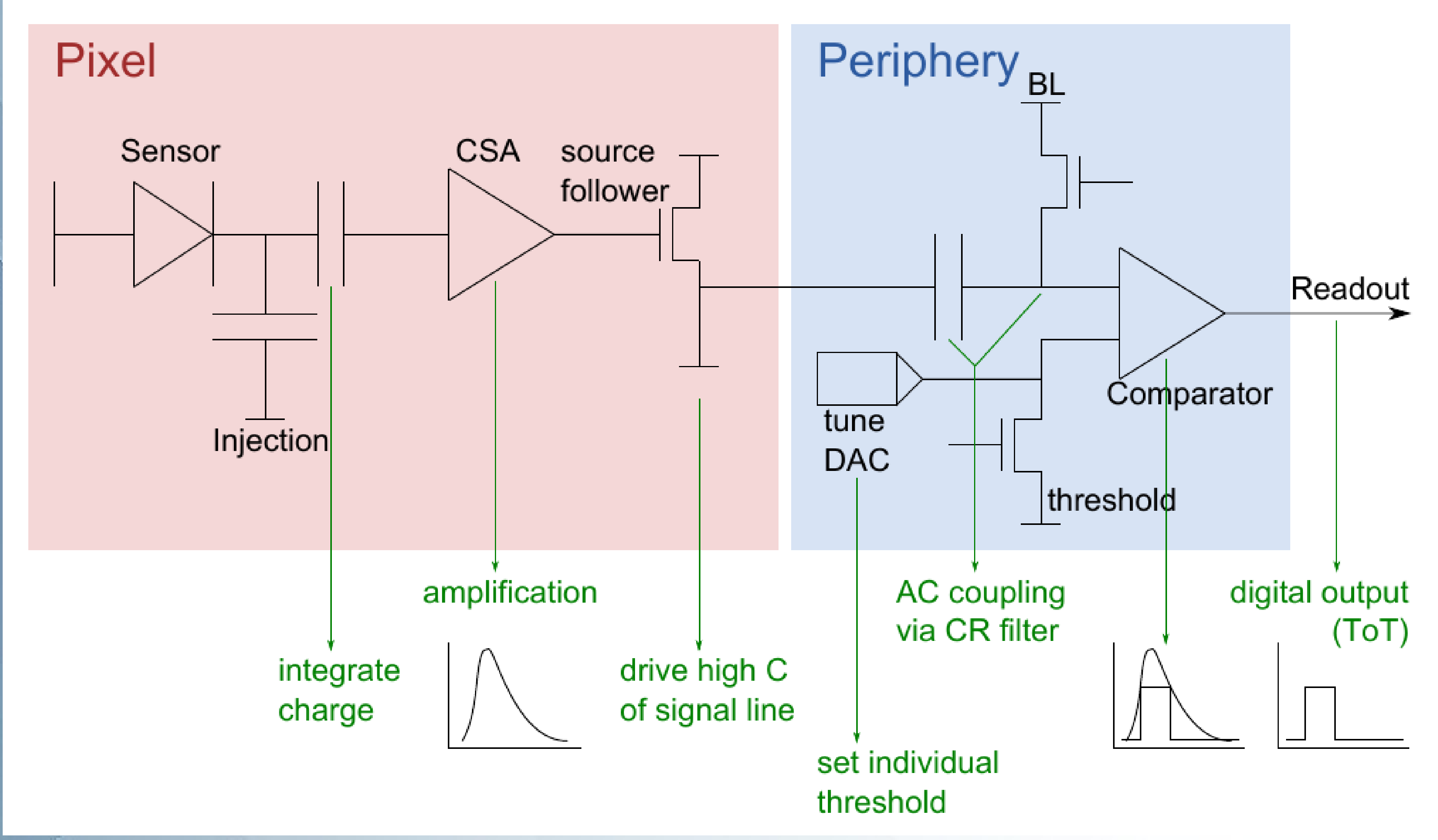
Mu3e Experiment

Search for $\mu^+ \rightarrow e^+ e^+ e^-$ (signal)
Background: $\mu^+ \rightarrow e^+ \nu \nu$



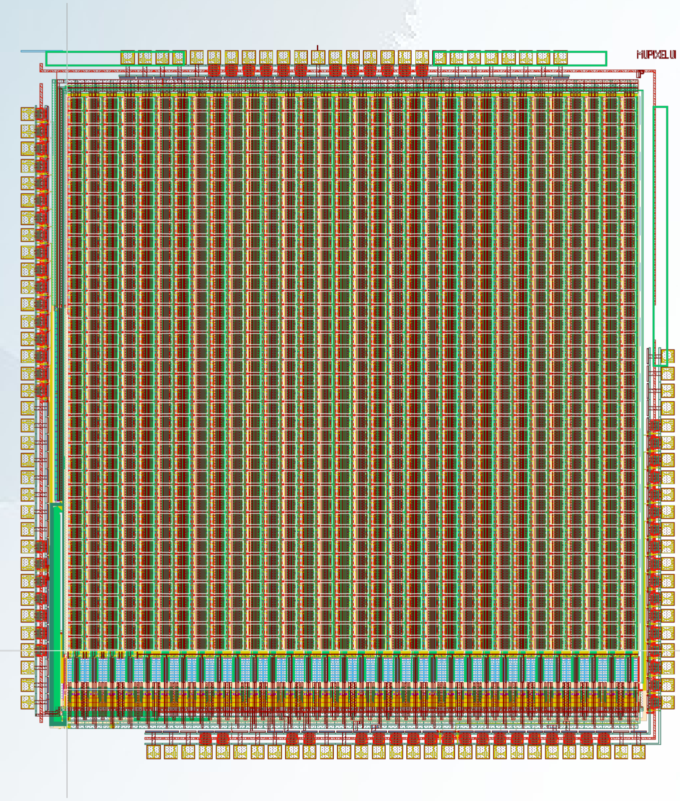
Fast and very thin detector required → MuPix sensor

Mupix Chip



Pixel
Periphery
BL
Sensor
CSA
source
follower
Readout
Injection
tune
DAC
Comparator
threshold
amplification
AC coupling
via CR filter
digital output
(ToT)
integrate
charge
drive high C
of signal line
set individual
threshold

Mupix Chip



Mupix7 prototype:

- ~ 3 x 3 mm^2
- ~1200 pixels
- pixel size ~ 80 x 100 µm^2

Mupix7 features:

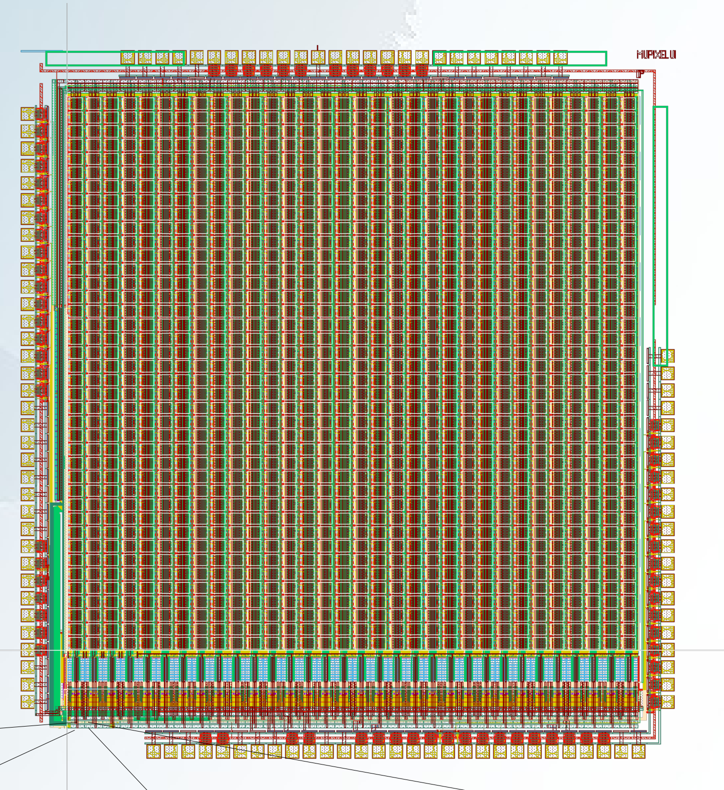
- Tune DACS for every pixel
- double stage amplifier (every pixel)
- zero suppression
- timestamp generation up to ~100 MHz → 10 ns
- 1.2 GHz PLL
- integrated 1.2 (2.4) Gbit/s link
- about 40 pads needed (wire bond)

System on Chip!

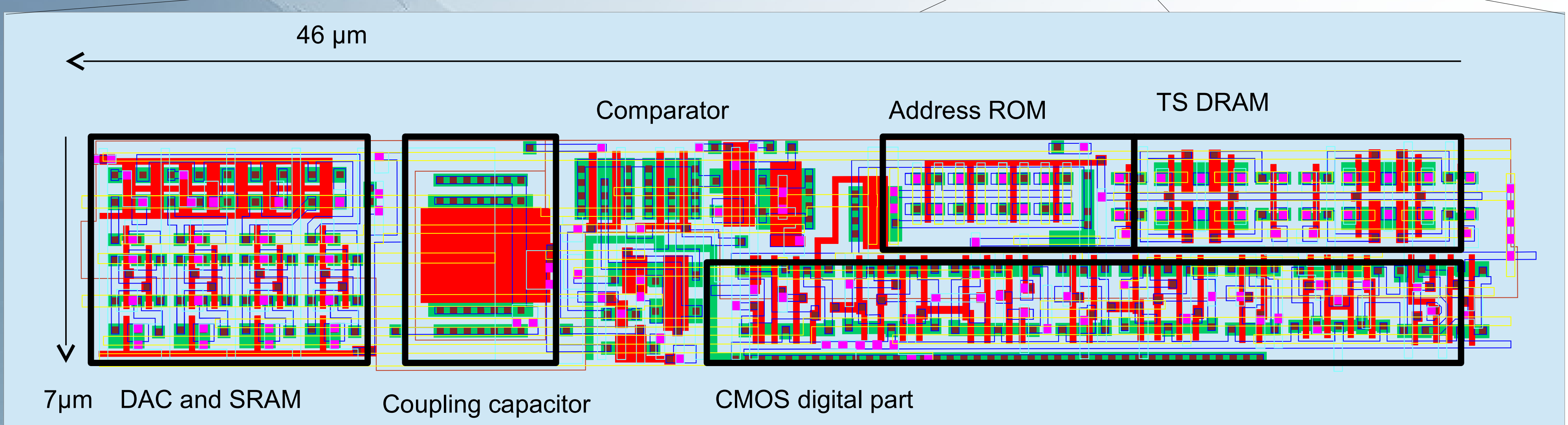
Mupix Readout Design

Mupix7 prototype:

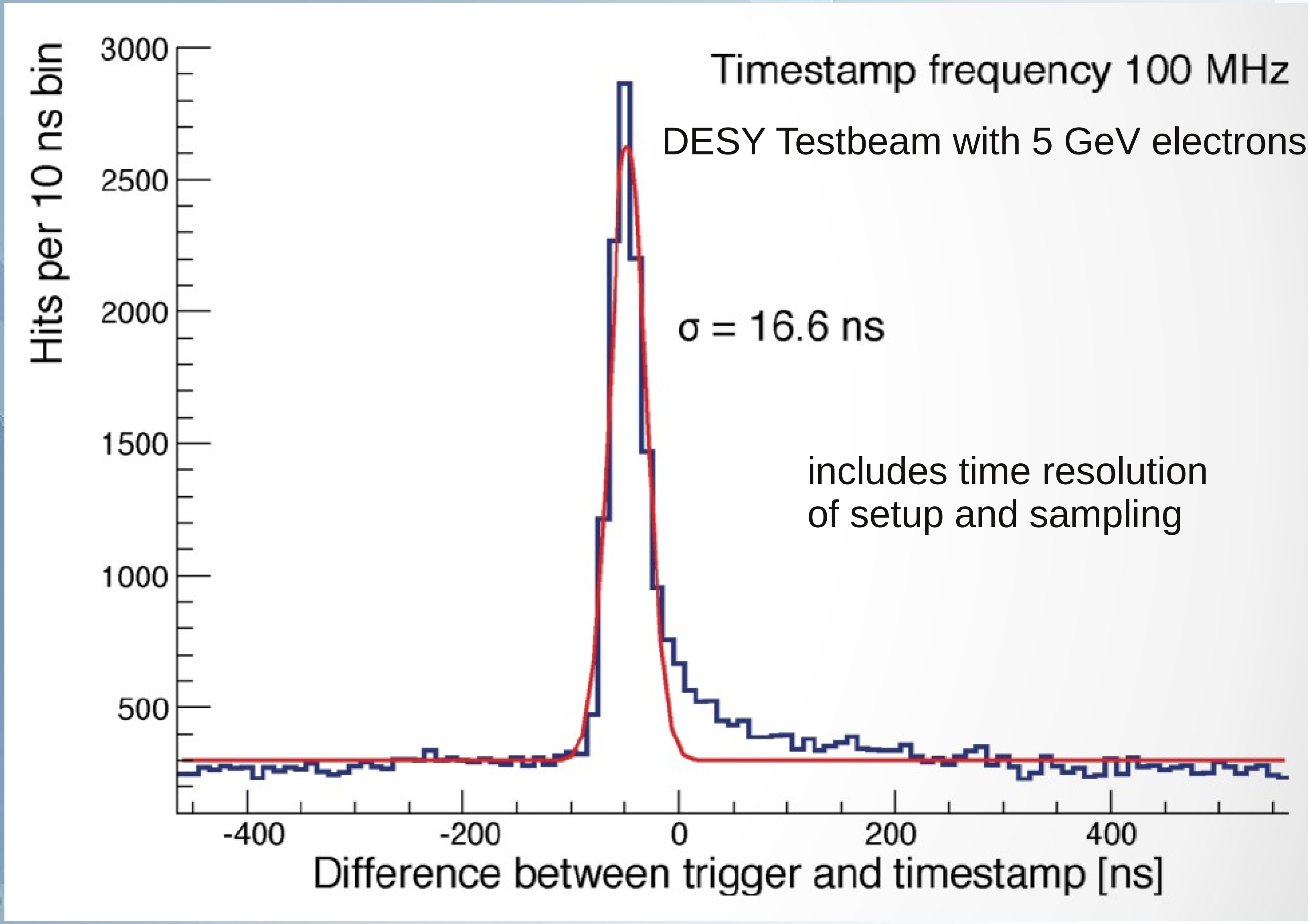
- ~ 3 x 3 mm²
- ~1200 pixels
- pixel size ~ 80 x 100 µm²



Readout periphery

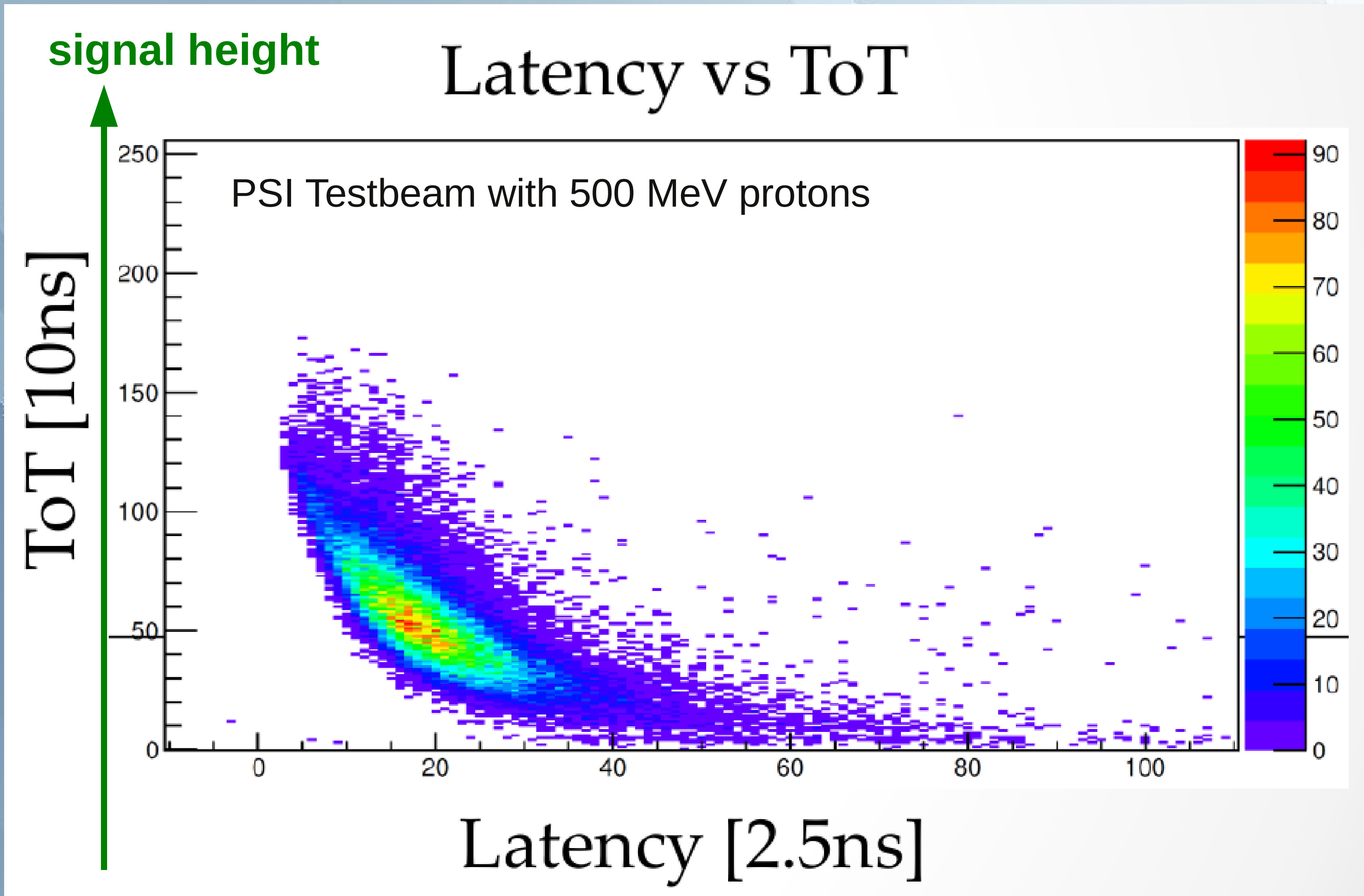


MuPix Time Resolution



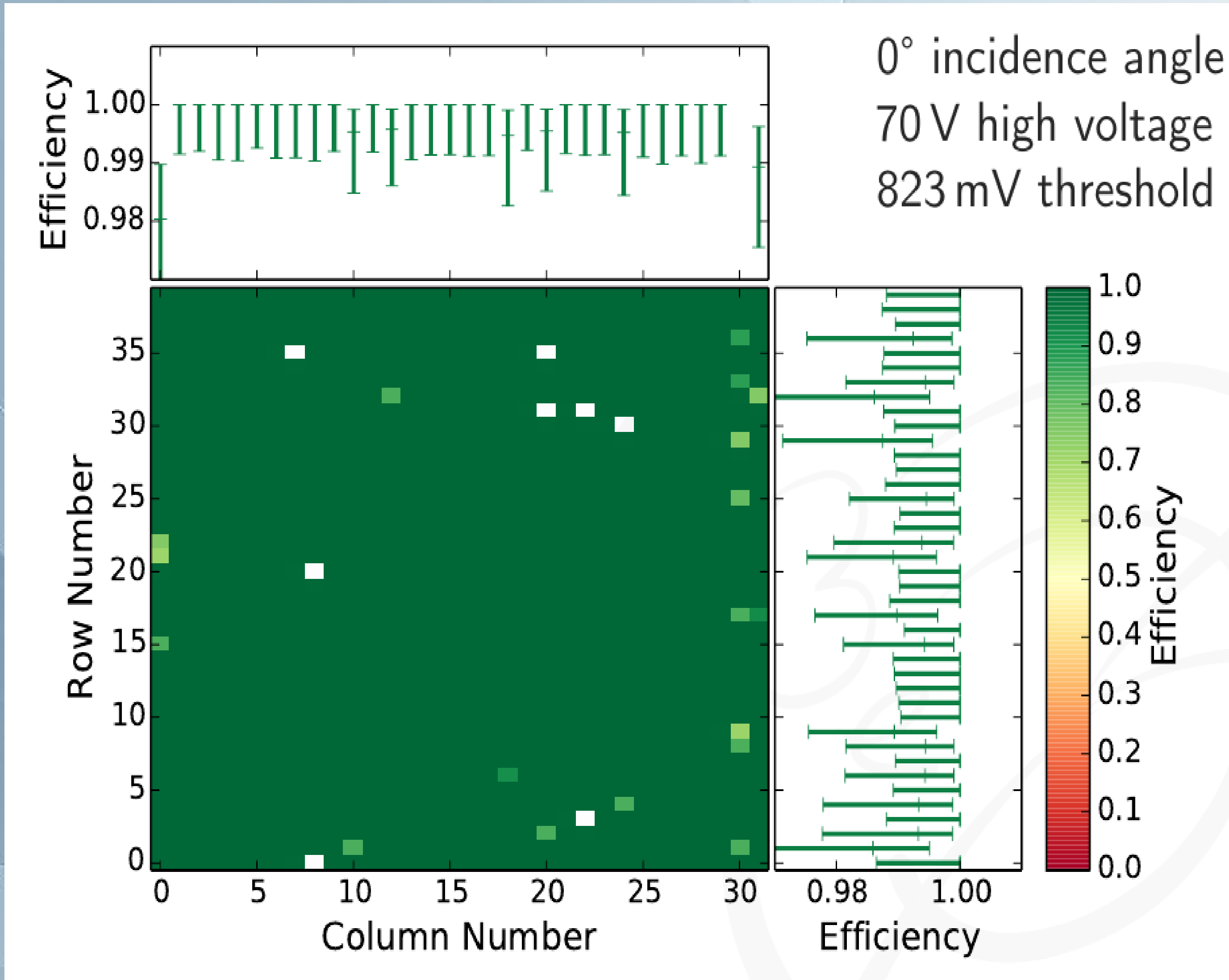
fastest monolithic pixel sensor!

MuPix Time Resolution



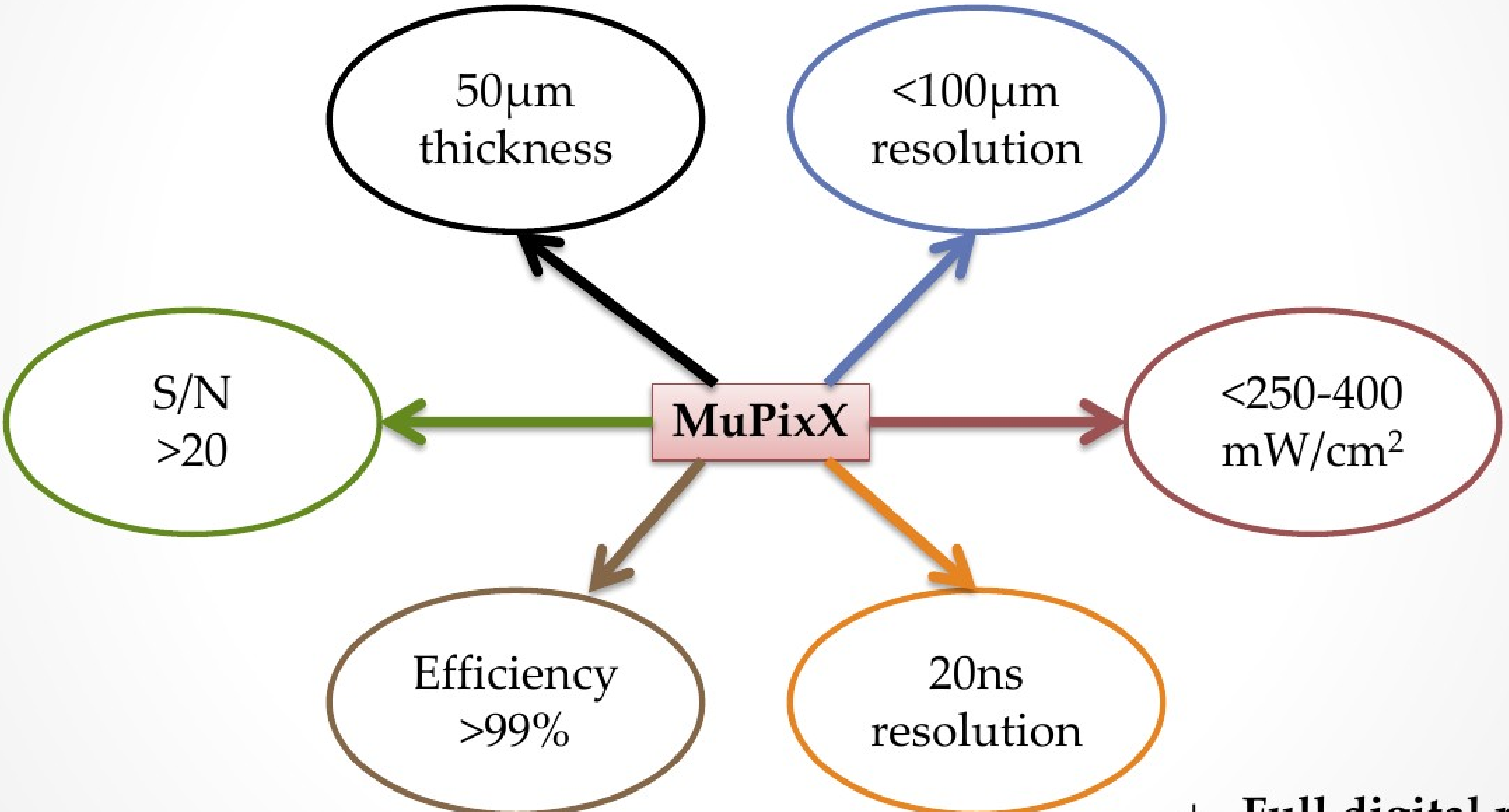
→ timewalk correction possible

MuPix Pixel Efficiency



Efficiency > 99.5%

MuPix Requirements

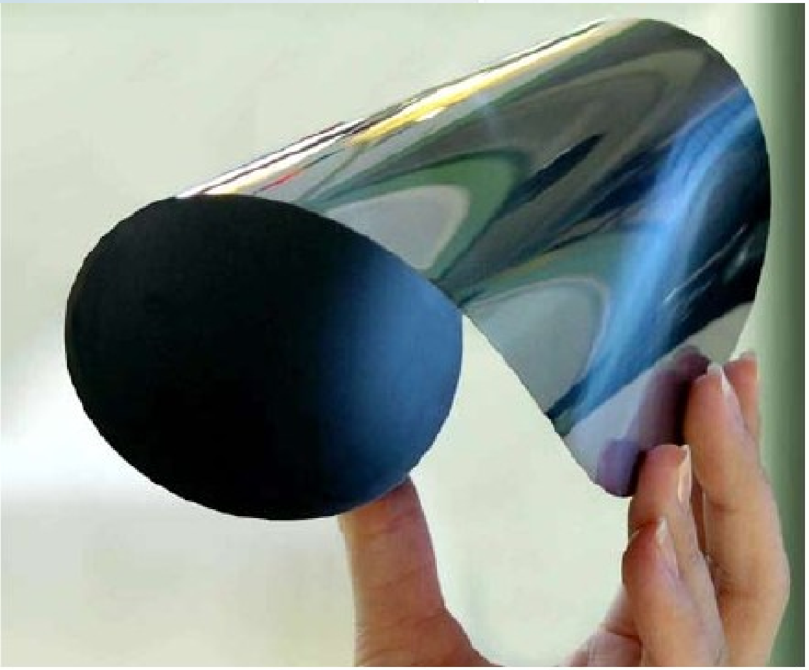


\+ **Full digital readout**

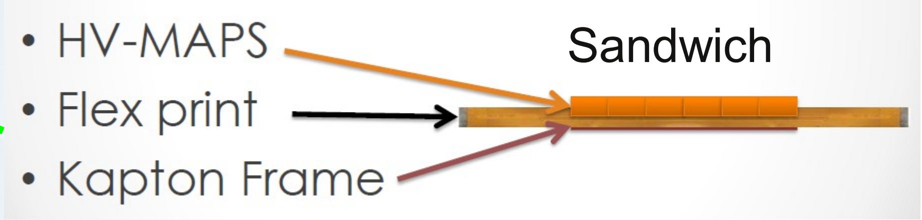
\+ **2x2 cm^2 size**

MuPix Tracker Construction

<u>Ultra-thin detector mock-up:</u>
- sandwich of 25 µm Kapton®
- 50/100 µm glass (instead of Si)



50 mu silicon wafer



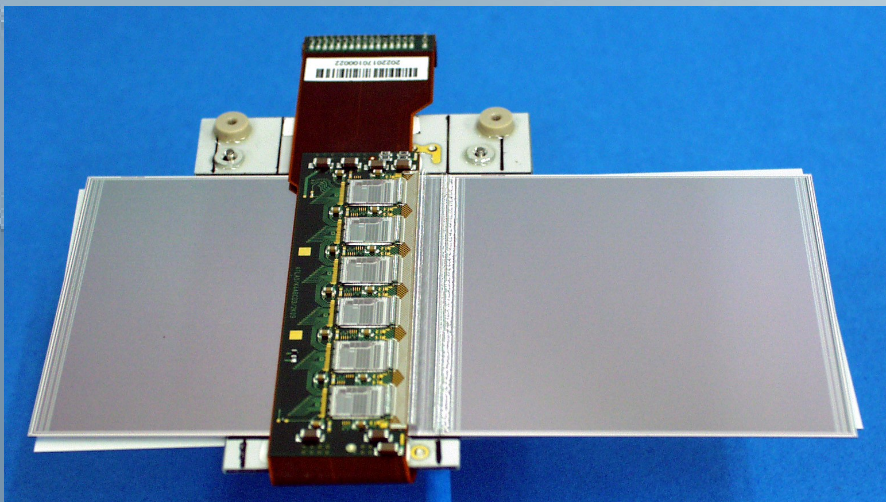
X/X_0 ~ 0.1% per layer

Summary

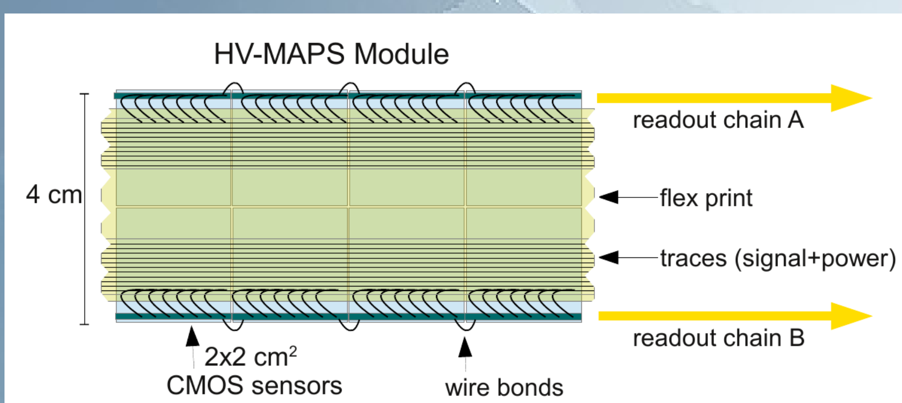
- CMOS detectors = System on Chip
- provides very thin sensors and small pixels
- used and/or considered for many upgrade projects
- HV-CMOS (HV-MAPS) solves timing and rate issues

→ clearly the way to go in future!

Outlook



ATLAS stereo strip module



HV-MAPS for LHC or FCC experiments?

ATLAS II tracker (ITK)

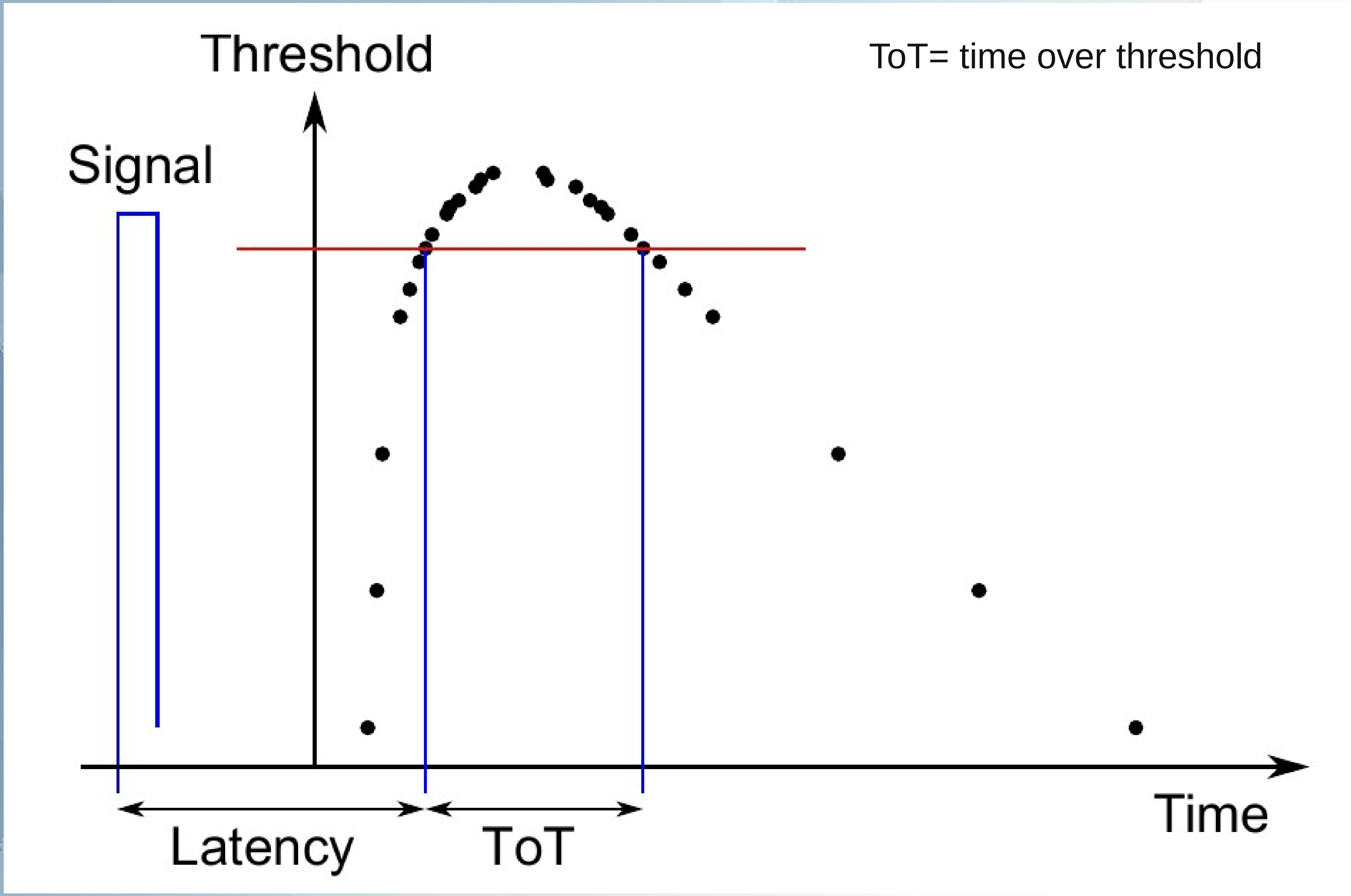
- costs ~130 MCHF
- 14 tracking layers (10 strip + 4 pixel)
- X/X_0 ~ 1-2% per layer

HV-MAPS Pixel only tracker ?

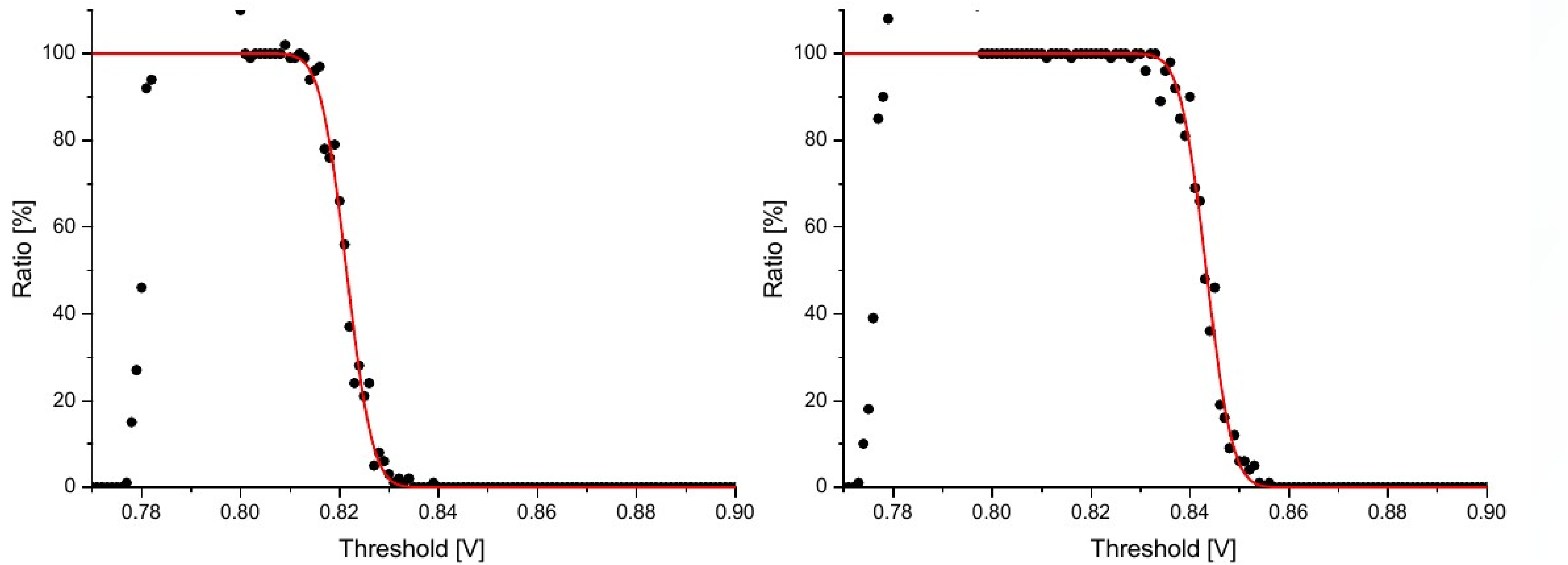
- only 6-9 pixel layers required
- 0.1- 1 % per radiation length
- reduced material costs
- reduced assembly costs
- 3D tracking → performance

BACKUP

Pulse Shape Measurement with ToT

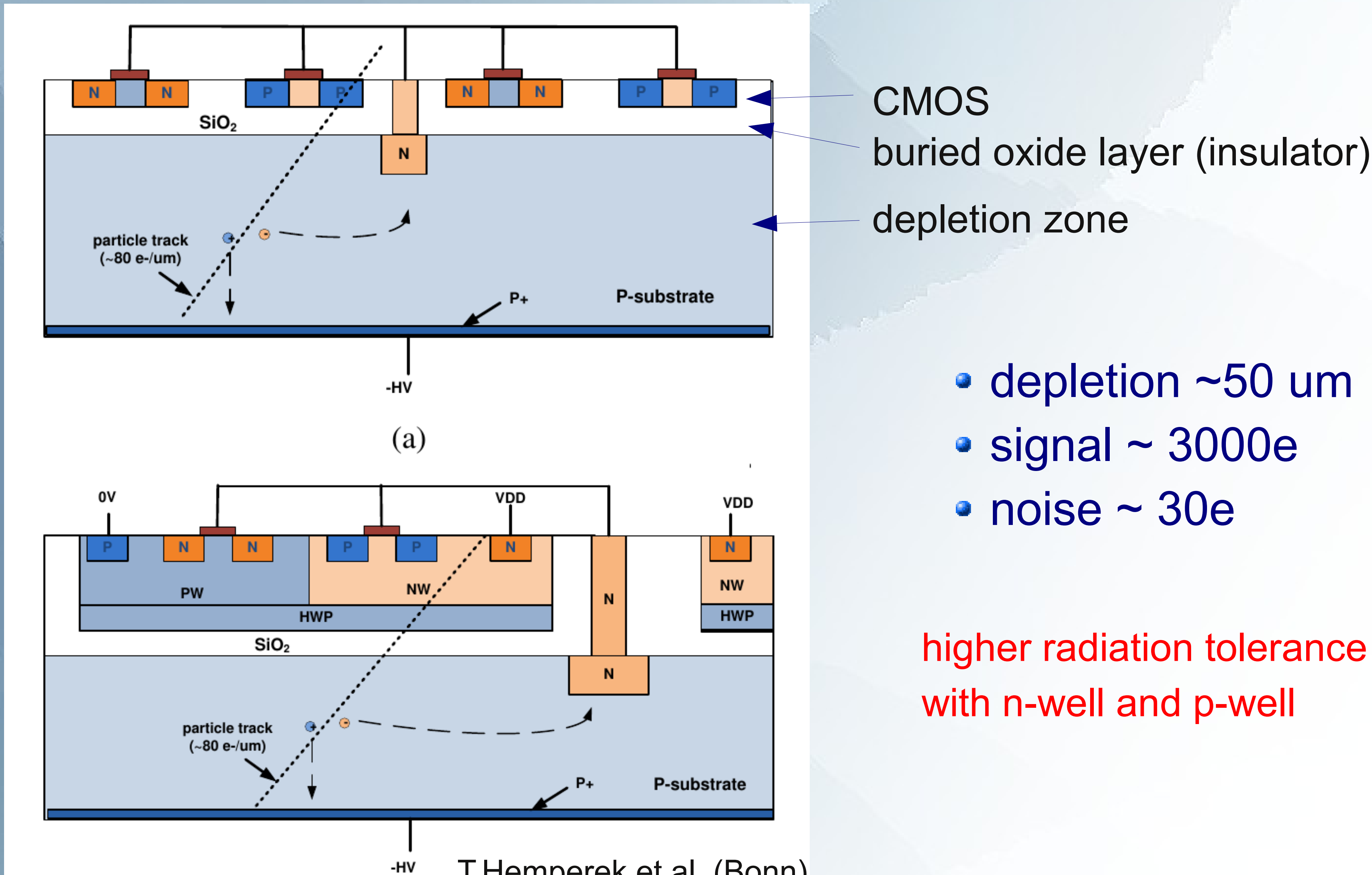


Noise Measurement with Threshold Scan



(a) HV: -1 V (b) HV: -70 V

Silicon on Insulator (SOI) Concept



T.Hemperek et al. (Bonn)

- depletion ~50 um
- signal ~ 3000e
- noise ~ 30e

higher radiation tolerance
with n-well and p-well

Austria Microsystems™ (AMS)

- High-Voltage CMOS technology
- H18 process 0.18 um available since March 20122
- 1.8V, 5V, 20V and 50V devices on a single chip without any process modifications

Mu3e Baseline Design

Long cylinder!

not to scale