March 23, 2004

Synchronization of the LHCb Outer Tracker Optical Links

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Abstract: The LHCb Outer Tracker uses the GOL serializer chip to send digitized drift-time data to the level-1 buffer board. This note describes the three-fold synchronization scheme to ensure byte and event synchronization of the data-transmision.

1 Introduction

The digitization of the Outer Tracker drift-tube signals is done with the ATLAS (DMIL) version of the 8-channel amplifier-dscriminator chip, ASD-BLR [1]. Four ASD chips are connected to one OTIS TDC chip [2]. To readout a drift-chamber module four of these 32-channel units are combined and connected to one GOL/Aux board [3]. The GOL/Aux board provides the power and control signals, and also carries the GOL serializer chip [4] connected to a VCSEL diode for optical data transmission. On a positive Level-0 trigger, the driftimes of the 128 channels of a module are transmitted within 900 ns to the TELL1 board [5] via the optical data link.
The TELL1 board can be equipped with 2 optical receiver cards [6], each carrying a 12-fold optical receiver connected to an optical ribbon cable used for the long-distance transmission of the optical signals. Every optical receiver is connected to a `TLK 2501` deserializer chip [7] To limit the data-volume processed by the TELL1 board in case of the Outer Tracker it is foreseen to use only 9 (18) links out of the 24 possible input links.

2 Data synchronization

Although the data is transmitted clock synchronous by the OTIS and the GOL chip, it cannot be assumed that the optical signals to a TELL1 board all arrive synchronous. Moreover, already for a single link the start of an event has to be indentitified within the bit stream sent. To ensure an easy and reliable synchronzation of all optical OT links a three level scheme is foreseen:

1. OTIS 1.1 [2] and later versions of the TDC provide a `data valid signal` used by the GOL serializer chip. Whenever there is valid data (including the comma descirbed below) on the 8-bit parallel output link of the OTIS chips the `data valid output signal` is set active.

   As the 4 OTIS chips connected to one GOL serializer chip all work synchronous, one of the 4 signals can be used as `valid data signal` for the GOL chip. Data is transmitted by the GOL only if the data valid signal is set. The 10Bit/8Bit encoding of the ethernet protocol used by the GOL chip ensures that any bit stream seen at the 16-bit wide receiver output corresponds to event data.

   The word synchronization between the GOL chip and the `TLK 2501` [7] deserializer relies on the emission of an `idle` sequence by the GOL chip. The `idle` sequence is send at start-up, after reset of the GOL, or if the data-valid (`Tx_En` is held low while `Tx_Er` being low too. The TLK synchronizes to 2 consecutive `idle` sets, corresponding to one 32-bit idle cycle (25 ns) for the GOL [**?**]. After a reset, a power-up, or a PLL-log lost the GOL sends `idle` words for a programmable period (`wait time`) between 2 and ??? cycles. The wait time `idle` sequence is also by the TLK 2501 for phase synchronization.

2. To detect the beginning of an event in an unambigous way the first byte of any OTIS data send to the GOL should be non-zero. This is not ensured by the format of the first bytes of the OTIS event data (event header).

   OTIS 1.1 and later versions of the TDC chip therefore have the possibility to transmit an additional `comma`, i.e. a byte set to `8'b11111111` proceeding an event of a non-consequtive read-out sequence. The restriction of the comma to events following a read-out gap is necessary to gurantee a maximum read-out rate of 1.11 MHz equivalent to 900 ns single event readout-time as specified in the L0 front-end specification.

   The received comma indicates the start of the event. The non-zero bytes of the comma are used for link synchronization. In the two possible read-out modes of the OTIS chip the comma is followed by 36 bytes of OTIS event data (in the "first hit mode" the 36 byte consist of 4 header bytes and 32 bytes of hit data). The fixed-event length ensures that the synchronization is kept as long as the data flow is continous. A break in the data-transmisson would lead first to a new synchronization comma.

3. The OTIS event header (see [2]) is used to verify and monitor the synchronization and the validity of the received OTIS data. The upper 10 bits of the OTIS ID are common for the 4 chips connected to one GOL chip. The 8-bit BX counter, as well as the 4-bit event counter should be synchronous for the 4 chips corresponding to one link. The event counter of subsequent events are ascending and should agree with the reference counter on the TELL1 board. The necessary verification and monitoring steps are performed on the input FPGAs of the TELL1 board. Also the "inter-link" synchronization is done here.

   Data links which are detected as having lost the synchronization are flagged. Eiher a TTC reset signal or a gap in between two transmitted events will automatically resynchronize the faulty links. It is not envisaged to resynchronize the faulty link "in flight" by searching the start of the event header.

   To simplify the commissioning and to have an additional cross check of the cabling the synchronization checks should not relie on pre-loaded OTIS IDs. The OTIS IDs used for the validity checks should be retrieved from the data of the first event.

3 Conclusion

The described three level scheme provides a redundant synchronization of the optical data-links. The FPGA code to verify the synchronization is currently being developed. The data-transmission including synchronization will be tested using OTIS 1.1.

References

[1] http://www.hep.upenn.edu/atlas/asdblr/
http://www.quark.lu.se/ãtlas/electronics/trt/chip_asdblr.html
http://www.hep.upenn.edu/atlas/asdblr/presentations/prr/DMILL_Fabs.pdf

[2] H.Deppe et al., The OTIS Reference Manual – Version 1.1, http://wwwasic.kip.uni-heidelberg.de/lhcbot/secure/Specifications/OTIS11-UserManual.pdf.

[3] D.Wiedner et al., Specification for a Prototype of the Auxiliary Board for the Outer Tracker, LHCb Internal Note LHCb-2003-129.

[4] P. Moreira et al., GOL Reference Manual, Gigabit Optical Link Transmitter manual http://proj-gol.web.cern.ch/proj-gol/manuals.htm

[5] G. Haefeli et al., TELL1 Specification for a common read out board for LHCb, LHCb Note LHCb-2003-007.

[6] D.Wiedner et al., Prototype for an Optical 12 input Receiver Card for the LHCb TELL1 Board, LHCb Internal Note LHCb-2003-137.

[7] TLK 2501 – 1.6 to 2.5 GHz deserializer, Texas Instruments; Revision July 2003; http://Jocus.ti.com/lit/ds/symlink/tlk2501.pdf.

[8] E. Aslanides et al., Synchronization of optical links using the GOL with the TLK2501 or StratixGX buffers., LHCb Technical Note, LHCb 2004-012.