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Specification of the OTIS-to-ASDBLR interface

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The Outer Tracker is using two ASICs to readout and to digitize the time information of the drift chambers:

- the ASDBLR chip [1] developed for the ATLAS TRT is used as amplifier, shaper and discriminator chip.
- the OTIS TDC chip [2] is developed specifically for the Outer Tracker readout. The chip measures the arrival time of the discriminated drift chamber pulses from the ASDBLR and digitizes the time information.

The front-end electronics is schematically shown in Fig. 1: It is planned to connect 2 amplifier boards, each with 2 ASD chips (8 channels each), to one OTIS board with a single OTIS chip (32 channels). Beside digitizing the ASD signals the OTIS chip also provides, via four DACs, the threshold voltages for the four connected ASD chips. This document describes the interface between ASD and OTIS chip.

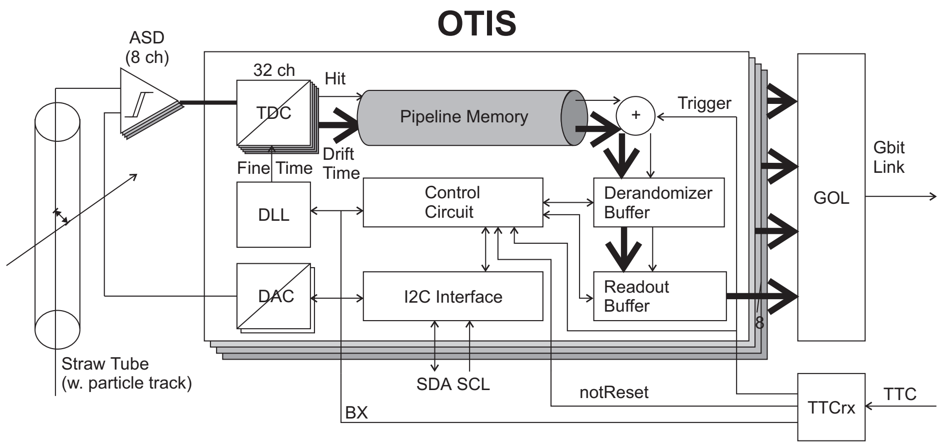

Figure 1: Outer tracker front-end electroncis

Hit signal levels

The ASDBLR has differential outputs based on ternary open-collector drivers. The maximum possible output currents provided on either output channel is 0.8 (1.6) mA for the low (high) threshold respectively. For the Outer Tracker only the low threshold setting is used.
As signal inputs the OTIS is using standard LVDS input pads. The maximum offsets of the differential inputs are not yet known for a larger sample of OTIS chips. Measurements of the same LVDS pads on a sample of BEETLE chips result in a 3 sigma offset variation of ± 27 mV [3].
To interface the ASD signals to the OTIS the termination and pull-up scheme of Fig. 2 is proposed. Pull-up resistors of 3.9 kΩ move the common signal level to about 1.46 V. A termination resistor of 120 Ω accross the two signal lines will lead for a maxiumum output current of 0.8 mA to a signal swing of $0.4\text{mA} \times 120\Omega = 48\text{mV}$. Assuming the above offset variation the signal swing is sufficient to reliably switch the LVDS inputs. The termination matches the line impedance and thus does not lead to an additional degradation of the signal rise-time.

Threshold DACs

The OTIS features four 8-bit DACs[1]. to supply the theshold voltages for connected ASD chips. The DACs provide voltages from 0 to 2.5 V in 256 steps of about 10 mV. The DACs cannot drive currents above 1μA.
As seen from Fig. 3 the ASD threshold currents reach values of 10μA in case a threshold voltage of 2.5 V is applied. This current cannot be supplied directly by the DACs. Source-followers are therefore foreseen to provide the necessary currents (also see addendum). The source-follower will limit the maximum threshold voltage to about 2.2 V. Whether this voltage is sufficient to suppress all pulses has still to be verified.
Fig. 4 shows the threshold characteristics of the ASDBLR. In the region of interest for the Outer Tracker operation between 2 and 6 fC the charge correspondence of the threshold voltage can be approximated by a linear function with a slope of 84 mV/fC. The DAC step-size of about 10 mV thus corresponds to a 0.12 fC, a value which seems to be sufficiently fine, particularly if one considers the channel-to-channel variation of the ASDBLR threshold characteristics: Fig. 5 shows the channel-to-channel variation of the treshold voltage corresponding to a charge of 2fC. The distribution has an RMS of 4% and a min-max spread of $\pm 10\%$. Converted to charge, the maximum channel-to-channel variations is in the order of ± 0.4 fC.

[1] In fact, the DACs are implemented as 10-bit DACs with the two LSBs not used.

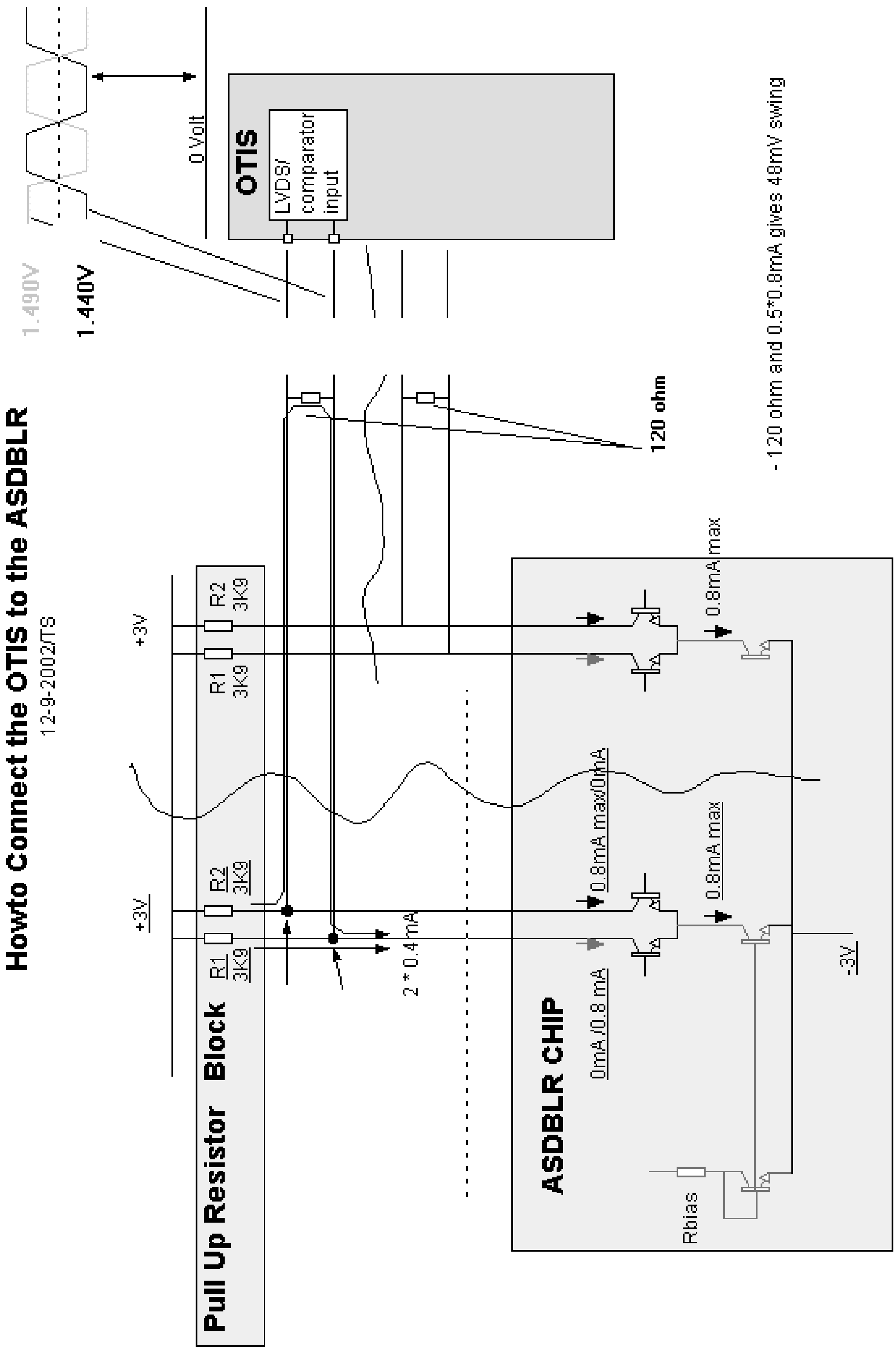

Figure 2: Termination scheme for ASDBLR signals

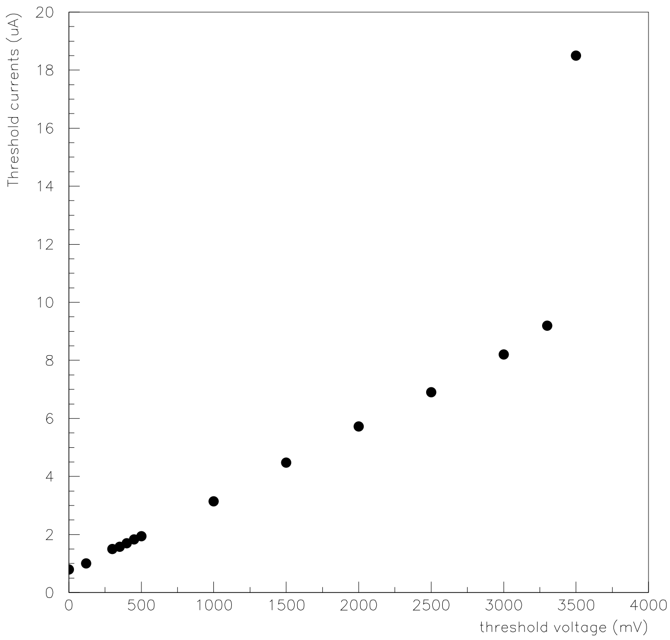

Figure 3: ASD threshold currents for different threshold voltages.

ASD test pulse supply

The ADSBLR forsees two separate test pulse inputs for odd and even channels. Contrary to the ATLAS DTMROC the OTIS chip is not involved in any test pulse generation. The test pulses will be generated by the TFC system. Together with other TFC signals the test pulses are distributed by the service box and received by the GOL/Aux card.

References

[1] http://www.hep.upenn.edu/atlas/asdblr/
http://www.quark.lu.se/ãtlas/electronics/trt/chip_asdblr.html
http://www.hep.upenn.edu/atlas/asdblr/presentations/prr/DMILL_Fabs.pdf

[2] http://www.physi.uni-heidelberg.de/ũwer/Otis/

[3] BEETLE friends, private communication.

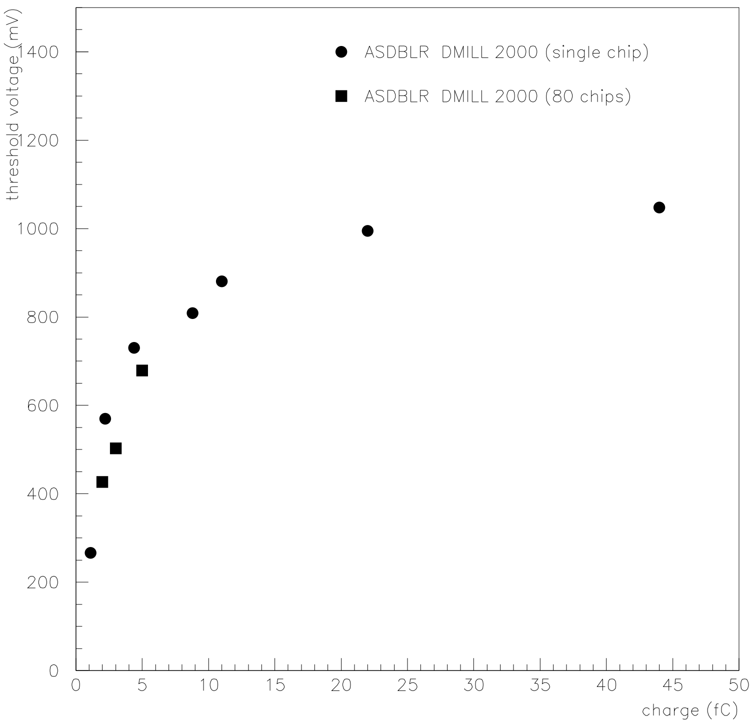

Figure 4: ASD charge characteristic of the threshold voltage.

Addendum

As re-measured by T.Sluik with the DMILL ASDblr2000 chisp the OTIS DACs (including source followers) have to supply positive currents for threshold voltages in the range between 0 V and 2.5 V. A current reversal happends only for negative threshold voltages:

U_{th}	I_{th}
+0.12 V	+1.0 μA
+0.00 V	+0.8 μA
-0.16 V	+0.5 μA
-0.33 V	+0.17 μA
-0.52 V	+0.0 μA
-0.57 V	-0.16 μA

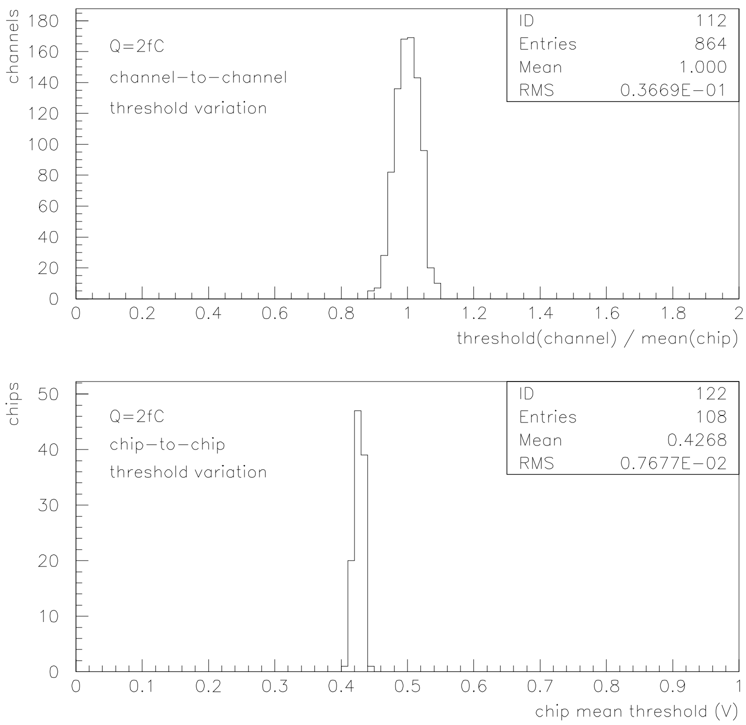

Figure 5: ASD threshold voltage variation for a threshold of 2fC. The upper plot shows the channel-to-channel variations normalized to the mean of the 8 channels of one chip. The lower plot shows the chip-to-chip variations of the channel means.