Test Pulse System for the LHCb Outer Tracker Detector

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Preliminary Version

Abstract:

This document describes the requirements and a proposal for the Outer Tracker Test Pulse System.

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1. Detector Requirements to the Test Pulse System

Test-pulses of defined pulse-height will be generated synchronous to the BX Clock. The Test-pulse phase with respect to the BX signal as well as the L0 Trigger must be programmable. The pulses are injected via a coupling capacitor into the test pulse inputs of the ASDBLR. They provide a powerful tool for commissioning and monitoring of the detector electronics:

- Test-pulses injected to the ASDBLR test the complete readout chain of the pulsed channels. During commissioning the test-pulses provide an easy tool to check the functionality of all boards inside the electronics boxes.
- A stable phase with respect to the BX signal allows to measure the time resolution of the channels.
- A precise time scan of the test-pulse signal with respect to the BX signal allows the measurement of the linearity of the OTIS channels.
- A scan of the ASDBLR thresholds during a test-pulse run allows the determination of the channel sensitivity. Electronics degradation can be seen by a variation of the 50% efficiency threshold.
- If in addition an in situ determination of the ASDBLR threshold characteristics is required, test-pulses with two different pulse-heights are necessary.

To provide the functionality given above, the Test-pulse System has to fulfill the following demands:

- Coarse time adjustment:
  The delay between a Test-pulse send to the Front End and the following L0 Trigger must be adjustable.
- Fine time adjustment of the Test-pulse phase with respect to the BX Clock:
  Time steps between 0.5 ns and 1 ns are sufficient as long as the reproducibility of the programmed delay is better than 300 ps for the complete delay range.
- Pulse height of the Test-pulse:
  To do the described time measurements the pulse height of the Test-pulse should be well above the nominal ASDBLR thresholds. For noisy channels this threshold can be as high as 4 fC. If a threshold scan is used to determine the channel sensitivity the pulse-height should be low enough that the corresponding ASDBLR threshold voltage still lies in the linear part of the threshold characteristic. From measurements of the characteristic threshold curve a save limit of the linear range of 8 fC is found. It is therefore suggested to use a pulse height of 8 fC injected to the inputs of the ASDBLR.
  If an in situ determination of the threshold characteristic should be done a second pulse height of about 4 fC should be available.

It must be clear that the distribution delays of the test-pulse signals as well as the TFC signals also contribute to the Test-pulse phase with respect to the BX Clock. Therefore the cables between the Control Box and Front-End Box should be of equal length.

2. Coarse Time Adjustment.

The course time adjustment between the Test-pulse and the corresponding L0 Trigger must be done centrally in our case in the TTCvi [1]. The TTCvi has four independent programmable timers (Inhibit <3:0>). The timers are controlled by the BX Clock and started at each Orbit signal. The duration of the timer is programmable with 12 bits resulting in a delay of 0 – 100 μs. In the test setup delay<0> is used for the generation of the L0 Trigger and delay<2> is used to start a ‘Calibration Pulse Broadcast’ [2], see figure 1.

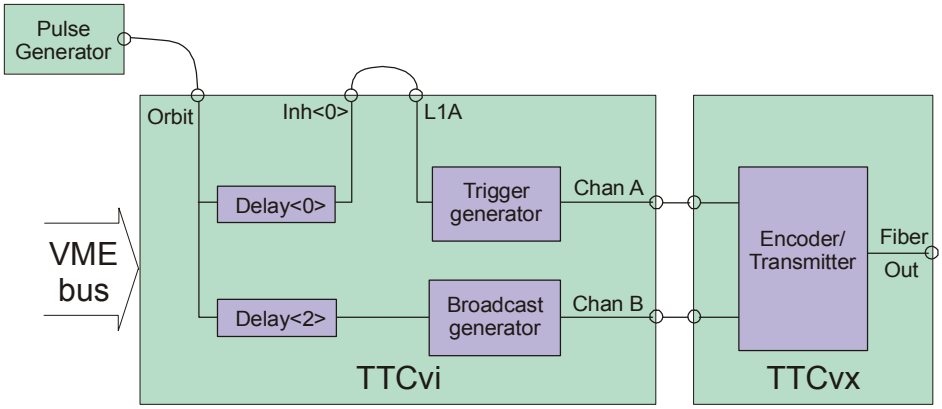

Figure 1: L0 Trigger and Test-pulse generation

3. Fine Time Adjustment

For the Fine Time adjustment the TTCrx [3] is occupied with two high resolution clock phase shifters to generate Clock40Des1 and Clock40Des2. Clock40Des1 is used as BX Clock for the Front-End while Clock40Des2 is used in the Broadcast decoding for the generation of the Test-pulse. As the jitter of the Clock40Des1 and Clock40Des2 can be up to 600 ps a QPLL [4] is needed to stabilize each clock. Figure 2 shows the block scheme of the TTCrx Adapter Board that is used in the test setup. Here only one Test-pulse is decoded the selection of the Odd or Even test-pulse is done at the GOL/AUX Board [5] by means of a jumper.

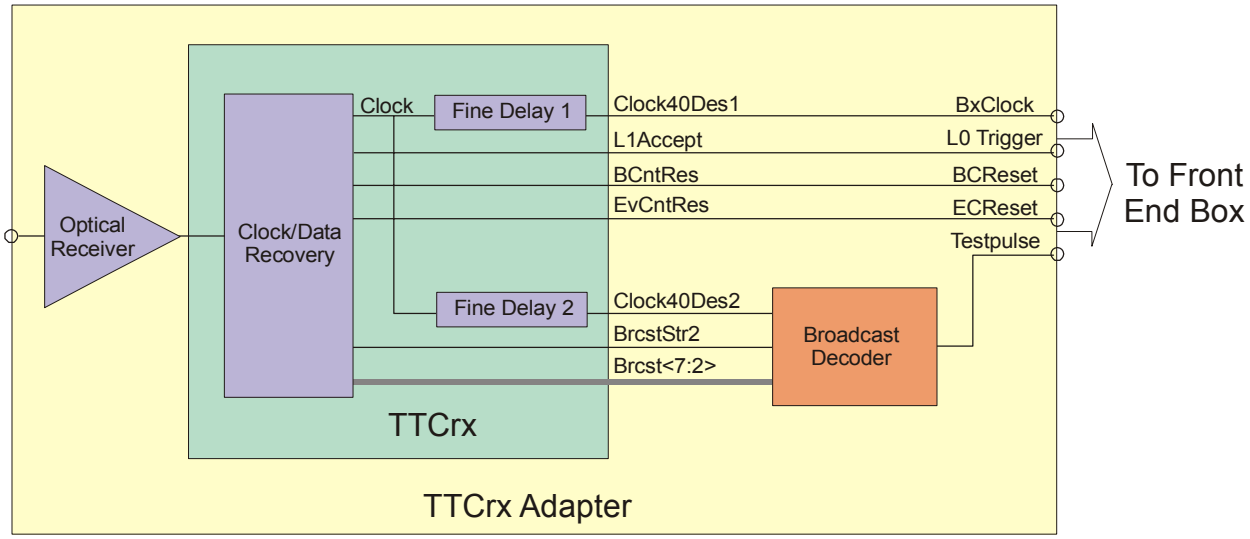

Figure 2: The TTCrx Adapter

Figure 3 shows test-pulse plots of wire 40 with two different fine delay 2 settings, measured with the test setup.

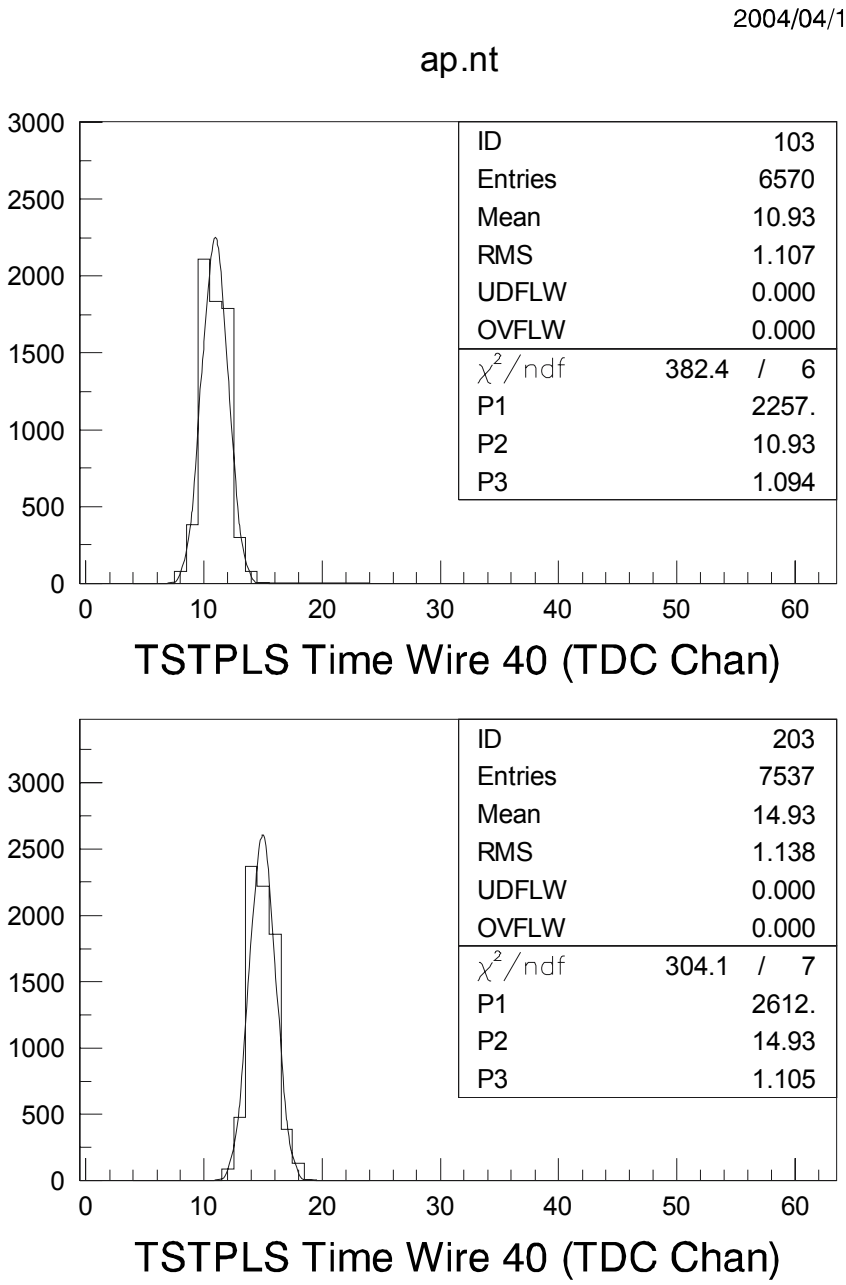

Figure 3: Test-pulse Plots

4. Pulse Height of the Test-pulse

The distribution of the Test-pulse signals to the Front-End boxes is done with digital (LVDS) signals thus 'Test-pulse-odd' (for the odd channels) and 'Test-pulse-even' (for the even channels) are separate signals and the pulse height of the Test-pulse is determined by a voltage divider in the Front-End. The selection of odd/even and high/low test-pulses can be done by means of Individually Addressed Data messages in the TTC System to access the Dout bus of the TTCrx, in this way the Test-pulse generation is fully controlled by the TTC System. Figure 4 shows the functional scheme of the Test-pulse generation and distribution.

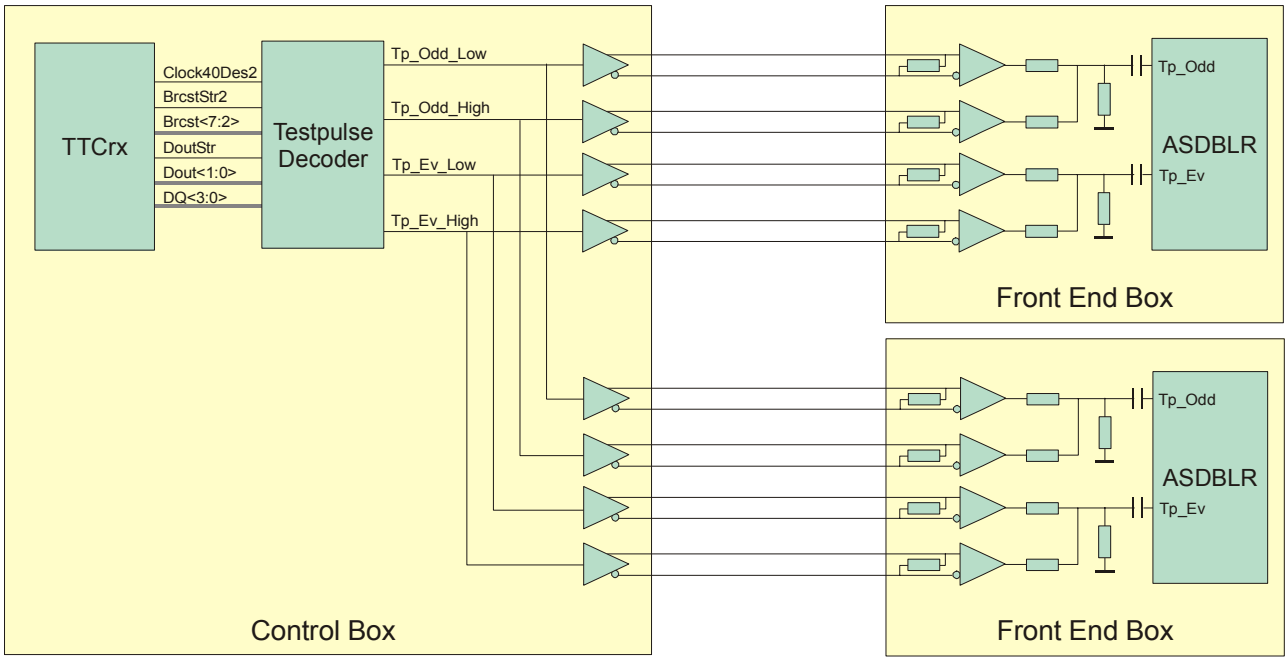

Figure 4: Test-pulse Generation and Distribution

5. References

[1] Ph.Farthouat, P.Gallno " TTC-VMEbus Interface TTCvi-MkII"

[2] Jorgen Christiansen "Requirements to the L0 front-end electronics" LHCb 2001-014

[3] J.Christiansen, A.Marchioro, P.Moreira, T.Toifl "TTCrx Reference Manual version 3.6"

[4] Paulo Moreira "QPLL User Manual" 2003-04-9

[5] U.Uwer, D.Wiedner "Auxiliary Board for the Outer Tracker"