The OTIS Reference Manual

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Abstract

This document describes the port definitions, electrical specifications, modes of operation and programming sequences of the TDC *OTIS*. The chip is developed for the Outer Tracker of the LHCb experiment. *OTIS 1.0* is the first full-scale prototype of this 32 channel TDC and has been submitted in April 2002 in a standard 0.25μm CMOS process. Within the clock driven architecture of the chip a DLL provides the reference for the drift time measurement. The drift time data of every channel is stored in the pipeline memory until a trigger decission arrives. A control unit provides memory and trigger management and handles data transmission to the subsequent DAQ stage. The current chip version is *OTIS 1.1* .

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1 Document and Chip Version History

Document Version	Date	Author	Description
0.5	17.06.2002	U.S.	document created
0.7	21.06.2002	U.S.	typos, electrical specs
1.0	24.09.2002	U.S.	1st public version
1.1	06.02.2004	U.T.	Include *OTIS 1.1*
Check `http://wwwasic.kip.uni-heidelberg.de/lhcbot/` for the latest version			

Chip Version	Submission Date	Changes relating to previous version
OtisDLL	19.10.2000	DLL prototype
OtisMEM1.0	21.03.2001	DLL & Memory prototype
OTIS1.0	15.05.2002	First full scale prototype
OTIS1.1	10.11.2003	TDC fix & various other improvements

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2 Conventions within this Document

- This document deals with the versions 1.0 to 1.1 of the *OTIS* chip.
- Registers are 8bit wide.
- The numbering of registers or bits within registers starts counting with zero. For example `TestReg[7:0] = 8'b00000001` stands for a register called `TestReg` which is loaded with the hexadecimal value `0x01`. The rightmost bit within this register (i.e. bit no. 0) is the least significant bit (LSB). In this example the LSB carries the value 1, all other bits including the most significant bit (MSB) are 0.

All exeptions from these conventions are noted.

3 Chip Architecture

The *OTIS* chip for the outer tracker of the LHCb experiment is developed at the University of Heidelberg. A first full-scale prototype of the chip has been submitted in April 2002. *OTIS* is a 32 channel TDC (Time to Digital Converter) manufactured in a standard 0.25μm CMOS process. In the LHCb experiment the signals from the straw tubes of the Outer Tracker are

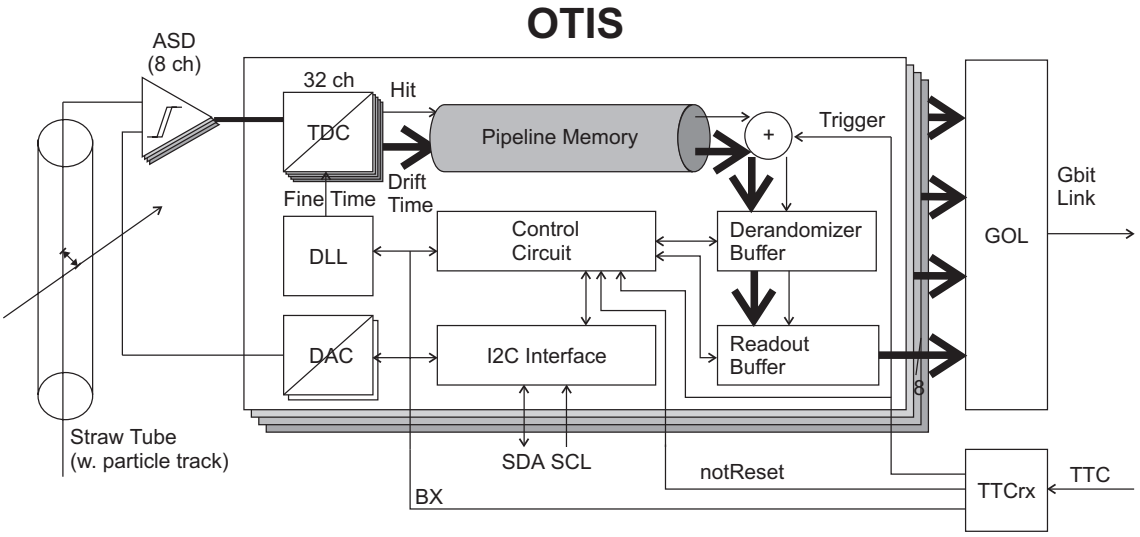

Figure 1: *OTIS* block diagram

digitised with discriminator chips of the *ASD* family [1]. The *OTIS* TDC measures the arrival time of the *ASD* signals with respect to the LHC clock. In the detector it is forseen to combine the output data of 4 *OTIS* chips and feed them to the *GOL* serialiser chip [2]. The *GOL* chip then transmits data optically to the off detector electronics at 1.2 Gbit/s net data rate. Figure 1 depicts how the *OTIS* chip is integrated into the Outer Tracker front end electronics. The data processing of the *OTIS* is clock driven: the chip operates synchronous to the 40MHz LHC clock. Main components of the *OTIS* chip are the TDC core, consisting of DLL, hit register and decoder and the pipeline plus derandomizing buffer. The last two are dual ported

SRAM memories to cover the L0 trigger latency [3] and to cope with trigger rate fluctuations. A control algorithm provides memory management and trigger handling. In addition the chip integrates several Digital to Analog Converters (DACs) providing the threshold voltages of the discriminator chips and a standard I^2C interface [4] for setup and slow control. The DLL (Delay Locked Loop) is a regulated chain of 32 delay elements consisting of two stages each. Since the output of every stage is used, the theoretical resolution is 390ps and the drift time data is 6 bit per channel. This data plus hit mask and status information is stored in the 240 bit wide pipeline memory. The capacity of the memory is 164 words to allow a maximum latency of 160 clock cycles. If a trigger occurs the corresponding data words are transferred to the derandomizing buffer which is able to store data for up to 16 consecutive triggers. The control unit's task is to read out the data of each triggered event within 900ns via a 8 bit wide bus running at 40MHz.

OTIS 1.1 had been submitted for manufacturing in November 2003. It features a modified TDC to overcome the problem of missing codes. Other changes visible to the user include changed readout header bits and register map and differential CMOS outputs. Further modifications include buffers for the ASD threshold outputs and a new implementation of the control algorithm and I^2C I/Os.

4 Electrical Specifications

4.1 DC characteristics

The OTIS chip needs two positiv operating voltages: analog and digital supplies of nominal +2.5V with respect to Ground (`gnd`, 0V) each. The operational range of `vdda` and `vdd` is predetermined by the manufacturing process. Minimum, maximum and nominal values for the supply voltages are listed in table 1.

Name	Explanation	Min.	Typ.	Max.	Unit
`vdd, vdd_*`[1]	Positiv digital supply	2.2	2.5	2.7	V
`vdda`	Positiv analog supply	2.2	2.5	2.7	V
`gnd`	Detector ground	0	0	0	V

[1] any power supply net having a name starting with "`vdd_`"

Table 1: DC characteristics of OTIS

All supply voltages should be thoroughly blocked against `gnd` (e.g. a 100nF ceramic capacity in parallel with a 68μF tantal capacity between `vdd/vdda` and `gnd`). The blocking capacitors should be placed as close as possible to the chip.

After powering the chip, the *OTIS* chip performs a power up reset (c.f. chapter 6.1). In this state the power consumption is 185mA (or 463mW). Power consumption rises to 220mA (or 550mW) when operating the chip at the nominal LHC bunch crossing frequency of 40MHz. It is not yet verified if power consumption rises while the chip transmits data to the following DAQ stage. But if so, it is expected that the power consumption will stay well below 1W which is an estimation for the upper bound of the power consumption per chip [5].

4.2 AC characteristics

The figures given in table 2 and 3 in this section represent standard values. Possible deviations from these numbers are not yet measured.

4.2.1 LVDS

Table 2: LVDS AC characteristics

Name	Explanation	Direction	Min.	Typ.	Max.	Unit
VCENTER	Center voltage	in		1.2		V
VLO	Logic 0 voltage	in		0.8		V
VHI	Logic 1 voltage	in		1.4		V
VLO	Logic 0 voltage	out		0.8		V
VHI	Logic 1 voltage	out		1.4		V

4.2.2 CMOS

Table 3: CMOS AC characteristics

Name	Explanation	Direction	Min.	Typ.	Max.	Unit
VLO	Logic 0 voltage	in		0		V
VHI	Logic 1 voltage	in		2.5		V
VLO	Logic 0 voltage	out		0		V
VHI	Logic 1 voltage	out		2.5		V

4.2.3 I^2C Interface

Table 4: I^2C (open drain) AC characteristics of *OTIS 1.0*

Name	Explanation	Direction	Min.	Typ.	Max.	Unit
VLO	Logic 0 voltage	in		0		V
VHI	Logic 1 voltage	in		2.5		V
VLO	Logic 0 voltage	out		0		V
VHI	Logic 1 voltage	out		2.5		V

Table 5: I^2C (open drain) AC characteristics of *OTIS 1.1*

Name	Explanation	Direction	Min.	Typ.	Max.	Unit
VLO	Logic 0 voltage	in		0		V
VHI	Logic 1 voltage	in			5.0	V
VLO	Logic 0 voltage	out		0		V
VHI	Logic 1 voltage	out			5.0	V

5 Slow Control

5.1 I²C-Interface

The slow control interface is a standard mode I²C-slave device performing a transfer rate of 100kbit/s. The chip address, necessary to access a single device on the I²C-bus, is assigned by means of the address pads `ID<0>` (LSB) to `ID<6>` (MSB). These pads (see table 10 and figure 7) contain internal pull down resistors. In this way one only needs to connect those pads to `vdd`, which corresponding bits have to be set to logic 1.

The internal registers can be accessed via the *pointer register*. This register contains the address of the following register to be written or read. The pointer is internally incremented by 1 after each transferred data frame. Thus registers with adjacent addresses are accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Figure 2 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data byte(s). After the transmission of one data frame, the pointer addresses the next register because of its auto-incrementing function. The transfer of the pointer register is mandatory in write mode. In read mode there are two possibilities:

- Preset pointer
  After initializing the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.
- Pointer set followed by immediate read-out
  After initializing the transfer and sending the chip address the pointer byte is transferred. The I²C-bus is re-initialized, the chip address is sent and data is read out.

Write mode:

S	Slave address	R/W: 0	A	Pointer Byte	A	D7	D6	D5	D4	D3	D2	D1	D0	A	(...)	P

Read mode:

Preset pointer

S	Slave address	R/W: 1	A	D7	D6	D5	D4	D3	D2	D1	D0	(...)	A	P

Pointer set followed by immediate read−out

S	Slave address	R/W: 0	A	Pointer Byte	A	Sr	Slave Address	R/W: 1	A	D7	D6	D5	D4	D3	D2	D1	D0	A	(...)	P

Figure 2: I²C-bus write and read sequences for accessing registers on the *OTIS*

Commercially available I²C-devices usually operate at 3.3V or 5V. To interconnect these devices with the *OTIS 1.0* 's I²C-interface a bidirectional level shifter is required. A simple solution is the use of a discrete MOS-FET for each bus line [6]. Fig. 3 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

OTIS 1.1 features a 5V compliant I²C interface. Thus the level shifter circuit depicted in fig. 3 can be omitted and the chip directly interfaces with commercial 5V or 3.5V I²C controllers.

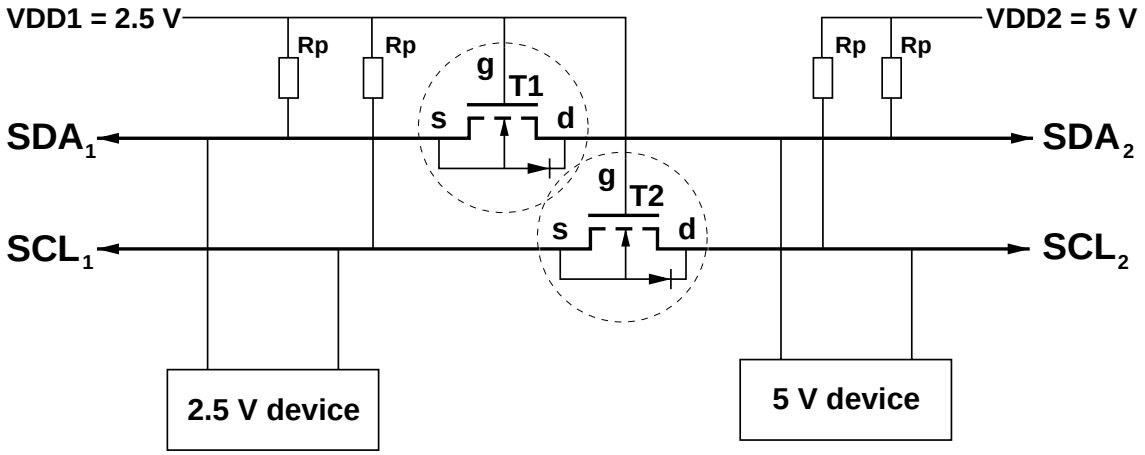

Figure 3: Bidirectional level shifter circuit to connect two different voltage level sections of an I^2C-bus system. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

5.2 Configuration Registers

5.2.1 Configuration Registers of *OTIS 1.0*

OTIS 1.0 provides 19 status and configuration registers. Registers number 0 to 4 are read-only, number 5 to 19 are read- and writeable via the I^2C-interface (see table 6). The first two registers (no. 0 and 1) contain the TDC ID and the register number 2 holds status information such as a full derandomizing buffer or a failed memory self test. The number of received and rejected triggers can be read from registers number 3 and 4 respectively. Each write access to the registers number 2, 3 or 4 resets them to 0. The search window, i.e. the number of data sets that are searched for hits upon a trigger, can be set with the bits number 0 (LSB) and 1 (MSB) of configuration register number 5 (called `ReadMode` register). One must remember that counting the number of data sets starts with 0. Bit number 2 of the `ReadMode` register selects one of two possible readout modes. But *OTIS 1.0* only provides the `single hit` mode (see section 6.2), which can be selected by setting the corresponding bit to 0. Selecting the other readout mode or turning on `truncation` mode (bit number 3 of the `ReadMode` register) will have no effect.

The functionality of the `DebugMode` and the `PBData` register is explained in section 6.3. The latency can be set with register number 7 and the 32 bits of the 4 `ChannelMask` registers are used to switch on or off individual channels. To switch off a channel, the corresponding bit must be set to 1.

The registers number 12 to 17 provide the interface to the DACs which control the comparators for the DLL (not yet implemented) or provide the threshold voltages for the ASD chips respectively. Remember that the DACs are not able to drive any electric currents. This will be fixed with the next chip release. *OTIS 1.1* includs current buffers which are able to drive $\leq 600\mu$A.

Table 6: *OTIS 1.0* status and configuration registers

Address	Name	Type	Bit Assignment/Description	
0	`PosID`	read only		Position ID
			7 - 5	0
			4 - 0	Position ID
1	`I2CID`	read only		I^2C ID
			7	0
			6 - 0	I^2C ID
2	`StatusReg`	read only		Status register
			7 - 4	0
			3	SEU[1]
			2	Buffer overflow
			1	DLL lock lost[1]
			0	Memory selftest failed
3	`RecievedT`	read only	7 - 0	Number of recieved trigger
4	`RejectedT`	read only	7 - 0	Number of rejected trigger
5	`ReadMode`	read/write		Read mode register
			7 - 4	X
			3	Truncation[1]
			2	SuppressZero / notSingleHit[1]
			1 - 0	Number of Events per trigger
6	`DebugMode`	read/write		Debug mode register
			7 - 6	X
			5 - 3	signal select
			2	Pads on/off
			1	Playback/SFT
			0	Debug mode on/off
7	`Latency`	read/write	7 - 0	Latency register
8 - 11	`ChannelMask`	read/write	7 - 0	Channel mask register
12, 13	`DLLDAC`	read/write	7 - 0	DLL DAC register
14 - 17	`ASDDAC`	read/write	7 - 0	ASD DAC register
18, 19	`PBData`	read/write	7 - 0	Playback data

[1] not implemented on *OTIS 1.0* .

5.2.2 Configuration Registers of *OTIS 1.1*

On *OTIS 1.1* the addresses of some configuration registers were changed according to table 7. Furtermore the following additional regesters were newly introduced or modified: The chip-ID was increased to 12 bits and is now readable via the `PosID0, PosID1` registers. The I^2C address has been separated from the chip-ID and made accessible via the `I2CID` register. The `Revision` register (3) gives access to the chip version used. The event counter (c.f. figs. 5 and 6) alredy present on *OTIS 1.0* can now be read via the `EventID` register (7). The total number of received triggers can be read from the `ReceivedT` register (5), while the `RejectedT` (6) contains number of rejected triggers due to an already full derandomiser buffer. Thus it holds true that `EventID + RejectedT = ReceivedT` if the there is no pending readout (i.e.

the derandomiser buffer is empty) and none of the counters were individually reset (true e.g. after a *PowerUp reset*). A write access to the registers 4,5,6 or 8 clears them, whil for the `EventID` register the corresponding external reset signal has to be applied. The `SEUCntr` register (8) contains the number of SEUs[1] detected in the I^2C -interface. Note that there is no SEU detection for the fast control circuit, TDC and datapath. The `DLL` rgister (11) was introduced to accomplish a DLL reset via the slow control interface. The `DLLDAC` registers are used to monitor the level of the DLL control voltage. These are intended to detect lock-lost states (c.f. sect. 6.2). The functionality of the `ASDDAC` registers has not changed, but the DAC-optputs now have buffers to permit a direct connection to the ASD's threshold input (Blocking these voltages is recomended!). The new set of 36 `ReadFIFO` registers hold a complete readout data frame, as described in fig. 4. The data frame latched is the first one sent, after the slow readout feature was enabled via the `DebugMode` register. Flushing of the `ReadFIFO` registers is accomplished by disabling and re-enabling the `RadFIFO` in the `DebugMode` register (10).

Table 7: *OTIS 1.1* status and configuration registers

Address	Name	Type	Bit Assignment/Description	
0	`PosID0`	read only		Position ID 0
1	`PosID1`	read only		Position ID 1
2	`I2CID`	read only		I^2C ID
			7	0
			6 - 0	I^2C ID
3	`Revision`	read only		Chip Version Register
			7 - 6	0
			5 - 3	Chip Version (`3'b001`)
			2 - 0	Chip Revision (`3'b001`)
4	`StatusReg`	read/write		Status register
			7 - 4	0
			3	SEU
			2	Buffer overflow
			1	DLL lock lost[1]
			0	Memory selftest failed
5	`RecievedT`	read/write	7 - 0	Number of recieved triggers
6	`RejectedT`	read/write	7 - 0	Number of rejected triggers
7	`EventID`	read only	7 - 0	EventID
8	`SEUCntr`	read/write	7 - 0	Number SEUs detected
9	`ReadMode`	read/write		Read mode register
			7	0
			6	Previous drift time
				0 → `11000000` for no hit
				1 → `11XXXXXX` (drift time of previous hit)
			5	DataValid (1=on, 0=off)
			4	Comma (1=on, 0=off)

[1] Single Event Upset

Table 7: *OTIS 1.1* status and configuration registers – cont.

Address	Name	Type	Bit Assignment/Description	
			3	Truncation[1]
			2	SuppressZero / notSingleHit[1]
			1 - 0	Number of Events per trigger
10	`DebugMode`	read/write		Debug mode register
			7 - 5	Pad info
				`3'b000` Memory pointer
				`3'b001` DBuf pointer
				`3'b010` SFT info
				`3'b011` Playback info
				`3'b100` Readout info
				`3'b101` DBuf info
				`3'b110` FIFO info
				`3'b111` DLL comp. info
			4	Servic pads (1=on, 0=off)
			3 - 1	Debug modes:
				`2'b001` ReadFIFO on
				`2'b010` SFT autoBankSelect
				`2'b011` SFT PadBankSelect
				`2'b100` PB autoBankSelect w/o FIFO
				`2'b101` PB autoBankSelect w FIFO
				`2'b010` PB PadBankSelect w/o FIFO
				`2'b010` PB PadBankSelect w FIFO
			0	Debug mode (1=on, 0=off, ignore bits 3-1)
11	`DLLReg`	read/write		DLL control register
			7 - 1	0
			0	DLL reset (1=active, 0=off)
12	`Latency`	read/write	7 - 0	Latency register
13	`Offset`	read/write	7 - 4	BX counter wrap-around (3556 - 3571)
				`4'b0111` for 3563 nominal value
			3 - 0	BX counter offset
				BX counter is pre-loaded to
				`Latency + Offset[3..0]` upon a BX reset
15 - 18	`ChannelMask`	read/write	7 - 0	Channel mask register
20 - 23	`DLLDAC`	read/write	7 - 0	DLL DAC register
24 - 27	`ASDDAC`	read/write	7 - 0	ASD DAC register
28, 29	`PBData`	read/write	7 - 0	Playback data
30 - 65	`ReadFIFO`	read/write	7 - 0	Slow event data readout

[1] not implemented on *OTIS 1.1* .

6 Modes of Operation

6.1 Reset

OTIS 1.0 : If the pad number 37 (see figure 7 and table 10) is coupled capacitively (10 - 100nF) to `gnd` , the chip performs a power up reset. Within this power up reset all status and configuration registers are set to 0 and the I^2C-interface is set into the idle state, thus the chip is ready for programming. The duration of the power up reset varies with the capacity connected to the `PwrUpReset` pad.

The pads number 35 and 36 are used to execute a fast reset. This is needed to synchronise the *OTIS 1.0* to the LHC bunch crossing clock or to reset the DLL if lock was lost. *OTIS 1.0* initiates a fast reset if the LVDS pad receives levels representing zero. There is no timing requirement between clock and reset whixh must be met as long as it is guaranteed that the clock is running while the chip gets resetted.

OTIS 1.1 : The function of the `PwrUpReset` pad (no. 130 in fig. 8 and tab. 11) was slightly modified: After the expiry of the RC-delay described above, an additional delay of 32 clock cycles was introduced to assure the locking of the DLL, which is only guaranteed if the clock is running when `PwrUpReset` or `DLLReset` are released. The latter (pad no. 165 in fig. 8 and tab. 11) was introduced to independently reset the DLL. The `L0Reset` (pad nos. 135 & 136 in fig. 8 and tab. 11) terminates any ongiong readout, resets the fast control to the *idle* state, resets all memory and derandomiser buffer pointers to zero and discards all pending triggers. However, it does not reset any on-chip counters. Thus the `EVReset` and `BXReset` signals (pad nos. 166...169 in fig. 8 and tab. 11) were introduced to perform this task on the Event- and BX-counters respectively.

6.2 Normal Operation Mode

To select normal (or `single hit`) operation mode, the content of the `ReadMode` register must be set to `8'bXXXX00xx`. The upper 4 bits have no function *OTIS 1.0* . On *OTIS 1.1* only bit number 7 is not used: Bit no. 4 turns on the transmission of a *Comma* (i.e. a byte set to `8'b11111111`) immediately preceeding a non-consecutive readout data frame. Bit no. 5 activates the `dataValid` output pad and bit no. 6 the ransmission of the previous drift time in the lower 6 bits of an unhit channel. On both, *OTIS 1.0* and *OTIS 1.1* , bits number 0 and 1 are used to program the number of data sets to search for hits. Bit number 2 selects `single hit` operation mode. For `suppress zero` mode this bit must be set to 1, but this mode is not implemented on *OTIS 1.0* and *OTIS 1.1* . For the latter mode the content of bit number 3 turns data stream truncation on or off. Figure 4 depicts how data and drift times are formatted in `single hit` operation mode. Figures 5 (*OTIS 1.0*) and 6 (*OTIS 1.1*) show how the status and hit information is organised in the header which preceeds every output data frame.

On *OTIS 1.1* a bit indicating truncation in the (not implemented) *SuppressZero* readout mode was added. The signals for *SFT, DLL lock lost* and the new *SEU* signal are ored together in a single error bit. The *DLL lock lost* bit is set, if the DLL's control voltage excceeds the votage range given by the `DLLDAC` registers (20 upper limit, 23 lower limit). The two other `DLLDAC` registers are used to set the bias of the corresponding discriminators (21 upper limit, 22 lower limit), which controls their speed and sensitivity. Furthermore, 4 bits indicating the data frame's position in the readout stream (`EventID`) are added. Also the `buffer overflow` bit was changed to a sticky behaviour, such that it can be only cleard with a `L0Reset` signal.

Output Data Format

Bit:	0 .. 31	32 ..39	...	280 .. 287
Data:	Header	Drift time 0	...	Drift time 31

Drift Time Encoding

Hit Position	Data
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	11XXXXXX

Figure 4: *OTIS 1.0* data format & drift time encoding in normal operation mode

6.3 Debugging Features

OTIS 1.0 provides several debugging features. First of all test data can be written to the pipeline via the I^2C-interface. Additionally one can start a memory self test or one can select status information such as full or empty derandomizing buffer to be observable at two debugging pads. To switch on the `debug` mode, the bit number 0 of the `DebugMode` register must be set to 1.

- Playback mode
  Test (or play back) data can be written to the registers number 18 and 19. If data is written to these registers via the I^2C-interface, the pointer does not proceed to the next register address. In combination with the fact that the two `PBData` registers are organised as shift registers, it is possible to store two independant sets of drift time and hit information which are then alternately written to the pipeline. To select `play back` operation while in `debug` mode, bit number 1 of the `DebugMode` register must be set to 0.

- Memory self test
  To start the memory self test while in `debug` mode, bit number 1 of the `DebugMode` register has to be set to 1. Run time information about the memory self test can be obtained from the two debug pads `WPWrap` and `RPWrap` (see next item). To exit from the memory self test, the user must clear bit number 1 of the `DebugMode` register.

- Status information
  To make status information visible at the pads `WPWrap` and `RPWrap` , the bit number

Header Data Format

Byte	1 (MSB … LSB)	2 (MSB … LSB)	3 (MSB … LSB)	4 (MSB … LSB)
Bit No.	0..11	12,13	14..17	18..21	22,23	24..31
Data	TDC ID	0	Status	RO	0	BX

Selftest failed	Buffer overflow	DLL lock lost	Single Event Upset	Number of BX	Read Mode	Playback Busy

Figure 5: Header data format of *OTIS 1.0* in normal operation mode

Header Data Format (OTIS1.1)

Byte	1 (MSB … LSB)	2 (MSB … LSB)	3 (MSB … LSB)	4 (MSB … LSB)
Bit No.	0..11	12	13..17	18,19	20..23	24..31
Data	TDC ID	1	RO	Err	Event-ID	BX

Read Mode	Number of BX	Truncation	Playback	SFT, DLL, SEU	Buffer Overflow

Figure 6: Header data format of *OTIS 1.1* in normal operation mode

2 of the `DebugMode` register has to be set to 0. The different combinations of status signals can be set with bits number 3 to 5 of the `DebugMode` register. The possible combinations are listet in table 8.

OTIS 1.1 includes basically the same debug features as *OTIS 1.0* , which are selected in the same way, except for changed register addresses and bit positions (c.f. tab. 7). Including the control mechanism of the `ReadFIFO` registers and DLL signals required a slightly different schema to activate the debug pads. It is given in table 9.

7 List of known Problems and Bugs

OTIS 1.0

- The `Data`-pads (pads number 13 to 28) are implemented as LVDS-pads though the receiver chip *GOL* [2] has single ended CMOS input pads.
- The memory self test shows a temperature dependency.

DebugMode[5:3]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Read out sequence	Start of sequence	End of sequence
3'b100	Derandomizing buffer fill level	Buffer empty	Buffer full

Table 8: Status information *OTIS 1.0*

DebugMode[5:3]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Playback info	PB mode enabled	*BankSelect*
3'b100	Read out sequence	Start of sequence	End of sequence
3'b101	Derandomizing buffer fill level	Buffer empty	Buffer full
3'b110	ReadFIFO information	FIFO enabled	FIFO has data
3'b111	DLL lock info	VCtrl $\leq$ DLLDAC3	VCtrl $\geq$ DLLDAC0

Table 9: Status information *OTIS 1.1*

- The measured drift times do not follow the detector signals arrival time linearily.

A Pad Positions (*OTIS 1.0*)

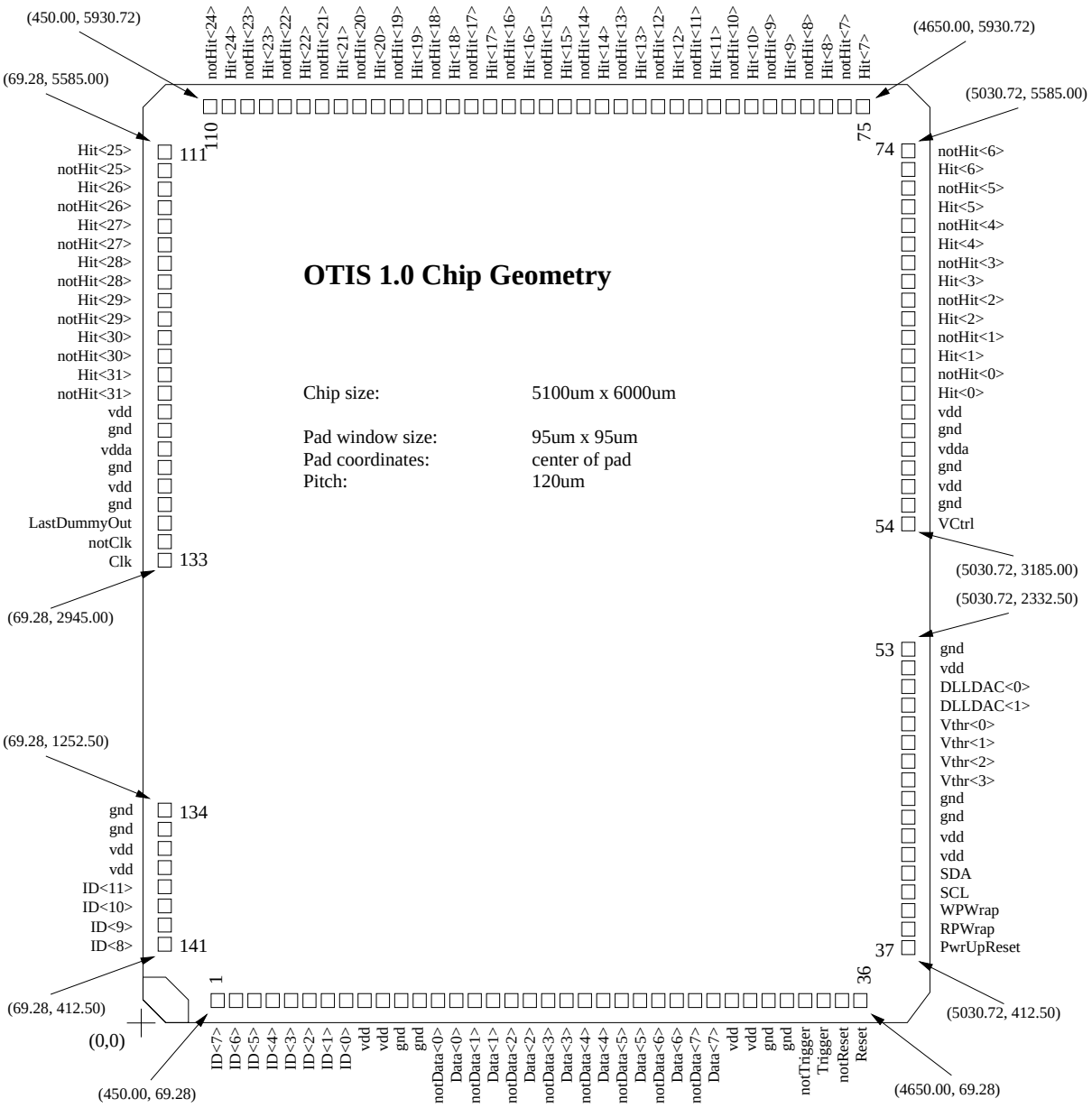

Figure 7: *OTIS 1.0* Pad Positions

B Pad Descriptions

Table 10: *OTIS 1.0* Pad Descriptions

Number	Name	X [μm]	Y [μm]	Type	Description
1	ID< 7 >	450.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 7)
2	ID< 6 >	570.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 6)
3	ID< 5 >	690.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 5)
4	ID< 4 >	810.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 4)
5	ID< 3 >	930.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 3)
6	ID< 2 >	1050.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 2)
7	ID< 1 >	1170.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 1)
8	ID< 0 >	1290.00	69.28	CMOS input (internal pull down)	TDC-ID (Bit No 0)
9	vdd	1410.00	69.28	input	positiv digital supply
10	vdd	1530.00	69.28	input	positiv digital supply
11	gnd	1650.00	69.28	input	negativ digital supply
12	gnd	1770.00	69.28	input	negativ digital supply
13	notData< 0 >	1890.00	69.28	LVDS output (neg.)	data output (LSB)
14	Data< 0 >	2010.00	69.28	LVDS output (pos.)	
15	notData< 1 >	2130.00	69.28	LVDS output (neg.)	data output
16	Data< 1 >	2250.00	69.28	LVDS output (pos.)	
17	notData< 2 >	2370.00	69.28	LVDS output (neg.)	data output
18	Data< 2 >	2490.00	69.28	LVDS output (pos.)	
19	notData< 3 >	2610.00	69.28	LVDS output (neg.)	data output
20	Data< 3 >	2730.00	69.28	LVDS output (pos.)	
21	notData< 4 >	2850.00	69.28	LVDS output (neg.)	data output
22	Data< 4 >	2970.00	69.28	LVDS output (pos.)	
23	notData< 5 >	3090.00	69.28	LVDS output (neg.)	data output
24	Data< 5 >	3210.00	69.28	LVDS output (pos.)	
25	notData< 6 >	3330.00	69.28	LVDS output (neg.)	data output
26	Data< 6 >	3450.00	69.28	LVDS output (pos.)	
27	notData< 7 >	3570.00	69.28	LVDS output (neg.)	data output (MSB)
28	Data< 7 >	3690.00	69.28	LVDS output (pos.)	
29	vdd	3810.00	69.28	input	positiv digital supply
30	vdd	3930.00	69.28	input	positiv digital supply
31	gnd	4050.00	69.28	input	negativ digital supply
32	gnd	4170.00	69.28	input	negativ digital supply

Table 10: *OTIS 1.0* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
33	notTrigger	4290.00	69.28	LVDS input (neg.)	L0 Trigger
34	Trigger	4410.00	69.28	LVDS input (pos.)	
35	notReset	4530.00	69.28	LVDS input (neg.)	Reset
36	Reset	4650.00	69.28	LVDS input (pos.)	
37	PwrUpReset	5030.72	412.50	input	Power Up Reset
38	RPWrap	5030.72	532.50	output	Read Pointer Wrap
39	WPWrap	5030.72	652.50	output	Write Pointer Wrap
40	SCL	5030.72	772.50	Input	I^2C Clock
41	SDA	5030.72	892.50	input/output	I^2C Data
42	vdd	5030.72	1012.50	input	positiv digital supply
43	vdd	5030.72	1132.50	input	positiv digital supply
44	gnd	5030.72	1252.50	input	negativ digital supply
45	gnd	5030.72	1372.50	input	negativ digital supply
46	Vthr< 3 >	5030.72	1492.50	output	Bias
47	Vthr< 2 >	5030.72	1612.50	output	Bias
48	Vthr< 1 >	5030.72	1732.50	output	Bias
49	Vthr< 0 >	5030.72	1852.50	output	Bias
50	DLLDAC< 1 >	5030.72	1972.50	output	Bias
51	DLLDAC< 0 >	5030.72	2092.50	output	Bias
52	vdd	5030.72	2212.50	input	positiv digital supply
53	gnd	5030.72	2332.50	input	negativ digital supply
54	VCtrl	5030.72	3185.00	output	Control Voltage
55	gnd	5030.72	3305.00	input	negativ digital supply
56	vdd	5030.72	3425.00	input	positiv digital supply
57	gnd	5030.72	3545.00	input	negativ digital supply
58	vdda	5030.72	3665.00	input	positiv analog supply
59	gnd	5030.72	3785.00	input	negativ digital supply
60	vdd	5030.72	3905.00	input	positiv digital supply
61	Hit< 0 >	5030.72	4025.00	LVDS input (pos.)	Hit Signal
62	notHit< 0 >	5030.72	4145.00	LVDS input (neg.)	
63	Hit< 1 >	5030.72	4265.00	LVDS input (pos.)	Hit Signal
64	notHit< 1 >	5030.72	4385.00	LVDS input (neg.)	
65	Hit< 2 >	5030.72	4505.00	LVDS input (pos.)	Hit Signal
66	notHit< 2 >	5030.72	4625.00	LVDS input (neg.)	
67	Hit< 3 >	5030.72	4745.00	LVDS input (pos.)	Hit Signal
68	notHit< 3 >	5030.72	4865.00	LVDS input (neg.)	
69	Hit< 4 >	5030.72	4985.00	LVDS input (pos.)	Hit Signal
70	notHit< 4 >	5030.72	5105.00	LVDS input (neg.)	
71	Hit< 5 >	5030.72	5225.00	LVDS input (pos.)	Hit Signal
72	notHit< 5 >	5030.72	5345.00	LVDS input (neg.)	
73	Hit< 6 >	5030.72	5465.00	LVDS input (pos.)	Hit Signal
74	notHit< 6 >	5030.72	5585.00	LVDS input (neg.)	
75	Hit< 7 >	4650.00	5930.72	LVDS input (pos.)	

Table 10: *OTIS 1.0* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
76	notHit< 7 >	4530.00	5930.72	LVDS input (neg.)	Hit Signal
77	Hit< 8 >	4410.00	5930.72	LVDS input (pos.)	Hit Signal
78	notHit< 8 >	4290.00	5930.72	LVDS input (neg.)	
79	Hit< 9 >	4170.00	5930.72	LVDS input (pos.)	Hit Signal
80	notHit< 9 >	4050.00	5930.72	LVDS input (neg.)	
81	Hit< 10 >	3930.00	5930.72	LVDS input (pos.)	Hit Signal
82	notHit< 10 >	3810.00	5930.72	LVDS input (neg.)	
83	Hit< 11 >	3690.00	5930.72	LVDS input (pos.)	Hit Signal
84	notHit< 11 >	3570.00	5930.72	LVDS input (neg.)	
85	Hit< 12 >	3450.00	5930.72	LVDS input (pos.)	Hit Signal
86	notHit< 12 >	3330.00	5930.72	LVDS input (neg.)	
87	Hit< 13 >	3210.00	5930.72	LVDS input (pos.)	Hit Signal
88	notHit< 13 >	3090.00	5930.72	LVDS input (neg.)	
89	Hit< 14 >	2970.00	5930.72	LVDS input (pos.)	Hit Signal
90	notHit< 14 >	2850.00	5930.72	LVDS input (neg.)	
91	Hit< 15 >	2730.00	5930.72	LVDS input (pos.)	Hit Signal
92	notHit< 15 >	2610.00	5930.72	LVDS input (neg.)	
93	Hit< 16 >	2490.00	5930.72	LVDS input (pos.)	Hit Signal
94	notHit< 16 >	2370.00	5930.72	LVDS input (neg.)	
95	Hit< 17 >	2250.00	5930.72	LVDS input (pos.)	Hit Signal
96	notHit< 17 >	2130.00	5930.72	LVDS input (neg.)	
97	Hit< 18 >	2010.00	5930.72	LVDS input (pos.)	Hit Signal
98	notHit< 18 >	1890.00	5930.72	LVDS input (neg.)	
99	Hit< 19 >	1770.00	5930.72	LVDS input (pos.)	Hit Signal
100	notHit< 19 >	1650.00	5930.72	LVDS input (neg.)	
101	Hit< 20 >	1530.00	5930.72	LVDS input (pos.)	Hit Signal
102	notHit< 20 >	1410.00	5930.72	LVDS input (neg.)	
103	Hit< 21 >	1290.00	5930.72	LVDS input (pos.)	Hit Signal
104	notHit< 21 >	1170.00	5930.72	LVDS input (neg.)	
105	Hit< 22 >	1050.00	5930.72	LVDS input (pos.)	Hit Signal
106	notHit< 22 >	930.00	5930.72	LVDS input (neg.)	
107	Hit< 23 >	810.00	5930.72	LVDS input (pos.)	Hit Signal
108	notHit< 23 >	690.00	5930.72	LVDS input (neg.)	
109	Hit< 24 >	570.00	5930.72	LVDS input (pos.)	Hit Signal
110	notHit< 24 >	450.00	5930.72	LVDS input (neg.)	
111	Hit< 25 >	69.28	5585.00	LVDS input (pos.)	Hit Signal
112	notHit< 25 >	69.28	5465.00	LVDS input (neg.)	
113	Hit< 26 >	69.28	5345.00	LVDS input (pos.)	Hit Signal
114	notHit< 26 >	69.28	5225.00	LVDS input (neg.)	
115	Hit< 27 >	69.28	5105.00	LVDS input (pos.)	Hit Signal
116	notHit< 27 >	69.28	4985.00	LVDS input (neg.)	
117	Hit< 28 >	69.28	4865.00	LVDS input (pos.)	Hit Signal
118	notHit< 28 >	69.28	4745.00	LVDS input (neg.)	

Table 10: *OTIS 1.0* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
119	Hit< 29 >	69.28	4625.00	LVDS input (pos.)	Hit Signal
120	notHit< 29 >	69.28	4505.00	LVDS input (neg.)	
121	Hit< 30 >	69.28	4385.00	LVDS input (pos.)	Hit Signal
122	notHit< 30 >	69.28	4265.00	LVDS input (neg.)	
123	Hit< 31 >	69.28	4145.00	LVDS input (pos.)	Hit Signal
124	notHit< 31 >	69.28	4025.00	LVDS input (neg.)	
125	vdd	69.28	3905.00	input	positiv digital supply
126	gnd	69.28	3785.00	input	negativ digital supply
127	vdda	69.28	3665.00	input	positiv analog supply
128	gnd	69.28	3545.00	input	negativ digital supply
129	vdd	69.28	3425.00	input	positiv digital supply
130	gnd	69.28	3305.00	input	negativ digital supply
131	LastDummyOut	69.28	3185.00	output	
132	notClk	69.28	3065.00	LVDS input (neg.)	LHC Clock
133	Clk	69.28	2945.00	LVDS input (pos.)	
134	gnd	69.28	1252.50	input	negativ digital supply
135	gnd	69.28	1132.50	input	negativ digital supply
136	vdd	69.28	1012.50	input	positiv digital supply
137	vdd	69.28	892.50	input	positiv digital supply
138	ID< 11 >	69.28	772.50	CMOS input (internal pull down)	TDC-ID (Bit No 11)
139	ID< 10 >	69.28	652.50	CMOS input (internal pull down)	TDC-ID (Bit No 10)
140	ID< 9 >	69.28	532.50	CMOS input (internal pull down)	TDC-ID (Bit No 9)
141	ID< 8 >	69.28	412.50	CMOS input (internal pull down)	TDC-ID (Bit No 8)

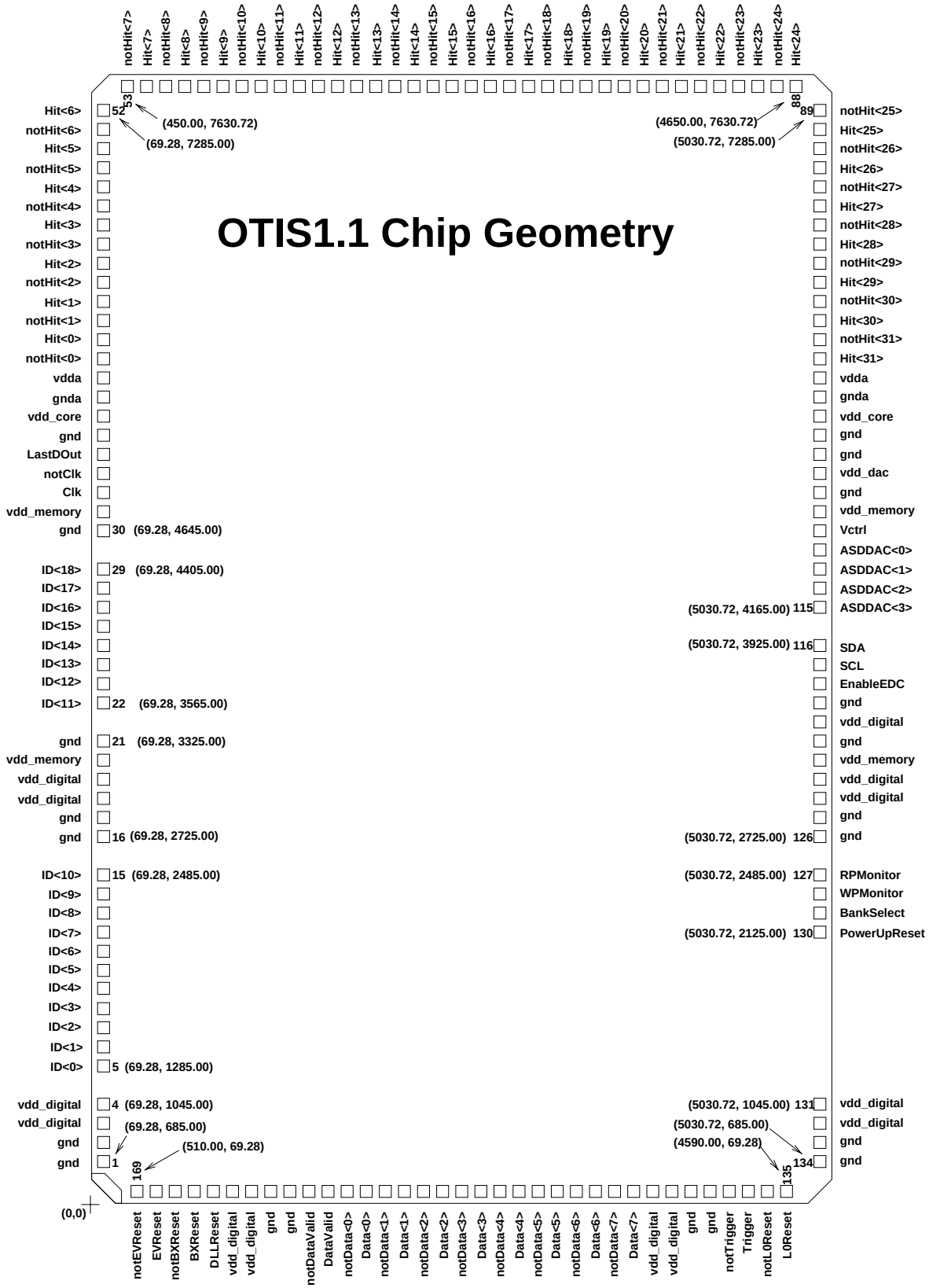

Figure 8: *OTIS 1.1* Pad Positions. Coordinates refer to the center of the pads, which are sized $95\mu\text{m} \times 95\mu\text{m}$ and feature a $120\mu\text{m}$ pitch.

C Pad Descriptions (*OTIS 1.1*)

Table 11: *OTIS 1.1* Pad Descriptions

Number	Name	X [μm]	Y [μm]	Type	Description
1	gnd	59.28	685.00	input	negative digital supply
2	gnd	59.28	805.00	input	negative digital supply
3	vdd_digital	59.28	925.00	input	positive digital supply
4	vdd_digital	59.28	1045.00	input	positive digital supply
5	ID< 0 >	59.28	1285.00	CMOS input internal pull-down	TDC ID (Bit no. 0)
6	ID< 1 >	59.28	1405.00	CMOS input internal pull-down	TDC ID (Bit no. 1)
7	ID< 2 >	59.28	1525.00	CMOS input internal pull-down	TDC ID (Bit no. 2)
8	ID< 3 >	59.28	1645.00	CMOS input internal pull-down	TDC ID (Bit no. 3)
9	ID< 4 >	59.28	1765.00	CMOS input internal pull-down	TDC ID (Bit no. 4)
10	ID< 5 >	59.28	1885.00	CMOS input internal pull-down	TDC ID (Bit no. 5)
11	ID< 6 >	59.28	2005.00	CMOS input internal pull-down	TDC ID (Bit no. 6)
12	ID< 7 >	59.28	2125.00	CMOS input internal pull-down	TDC ID (Bit no. 7)
13	ID< 8 >	59.28	2245.00	CMOS input internal pull-down	TDC ID (Bit no. 8)
14	ID< 9 >	59.28	2365.00	CMOS input internal pull-down	TDC ID (Bit no. 9)
15	ID< 10 >	59.28	2485.00	CMOS input internal pull-down	TDC ID (Bit no. 10)
16	gnd	59.28	2725.00	input	negative digital supply
17	gnd	59.28	2845.00	input	negative digital supply
18	vdd_digital	59.28	2965.00	input	negative digital supply
19	vdd_digital	59.28	3085.00	input	positive digital supply
20	vdd_memory	59.28	3205.00	input	positive memory supply
21	gnd	59.28	3325.00	input	negative digital supply
22	ID< 11 >	59.28	3565.00	CMOS input internal pull-down	TDC ID (Bit no. 11)
23	ID< 12 >	59.28	3685.00	CMOS input internal pull-down	TDC ID (Bit no. 12)
24	ID< 13 >	59.28	3805.00	CMOS input internal pull-down	TDC ID (Bit no. 13)
25	ID< 14 >	59.28	3925.00	CMOS input internal pull-down	TDC ID (Bit no. 14)

Table 11: *OTIS 1.1* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
26	ID< 15 >	59.28	4045.00	CMOS input internal pull-down	TDC ID (Bit no. 15)
27	ID< 16 >	59.28	4165.00	CMOS input internal pull-down	TDC ID (Bit no. 16)
28	ID< 17 >	59.28	4285.00	CMOS input internal pull-down	TDC ID (Bit no. 17)
29	ID< 18 >	59.28	4405.00	CMOS input internal pull-down	TDC ID (Bit no. 18)
30	gnd	59.28	4645.00	input	negative digital supply
31	vdd_memory	59.28	4765.00	input	positive memory supply
32	Clk	59.28	4885.00	LVDS input (pos.)	LHC Clock
33	notClk	59.28	5005.00	LVDS input (neg.)	
34	LastDOut	59.28	5125.00		
35	gnd	59.28	5245.00	input	negative digital supply
36	vdd_core	59.28	5365.00	input	positive TDC supply
37	gnda	59.28	5485.00	input	negative DLL supply
38	vdda	59.28	5605.00	input	positive DLL supply
39	notHit< 0 >	59.28	5725.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	59.28	5845.00	LVDS input (pos.)	
41	notHit< 1 >	59.28	5965.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	59.28	6085.00	LVDS input (pos.)	
43	notHit< 2 >	59.28	6205.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	59.28	6325.00	LVDS input (pos.)	
45	notHit< 3 >	59.28	6445.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	59.28	6565.00	LVDS input (pos.)	
47	notHit< 4 >	59.28	6685.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	59.28	6805.00	LVDS input (pos.)	
49	notHit< 5 >	59.28	6925.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	59.28	7045.00	LVDS input (pos.)	
51	notHit< 6 >	59.28	7165.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	59.28	7285.00	LVDS input (pos.)	
53	notHit< 7 >	450.00	7630.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	7630.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	7630.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	7630.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	7630.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	7630.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	7630.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	7630.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	7630.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	7630.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	7630.72	LVDS input (neg.)	

Table 11: *OTIS 1.1* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
64	Hit< 12 >	1770.00	7630.72	LVDS input (pos.)	Hit Signal
65	notHit< 13 >	1890.00	7630.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	7630.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	7630.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	7630.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	7630.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	7630.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	7630.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	7630.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	7630.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	7630.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	7630.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	7630.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	7630.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	7630.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	7630.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	7630.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	7630.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	7630.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	7630.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	7630.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	7630.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	7630.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	7630.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	7630.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	7285.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	7165.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	7045.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6925.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6805.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	6685.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	6565.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	6445.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	6325.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	6205.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	6085.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5965.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5845.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5725.00	LVDS input (pos.)	
103	vdda	5030.72	5605.00	input	positive DLL supply
104	gnda	5030.72	5485.00	input	negative DLL supply
105	vdd_core	5030.72	5365.00	input	positive TDC supply
106	gnd	5030.72	5245.00	input	negative digital supply

Table 11: *OTIS 1.1* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	gnd	5030.72	5125.00	input	negative digital supply
108	vdd_DAC	5030.72	5005.00	input	positive DAC supply
109	gnd	5030.72	4885.00	input	negative digital supply
110	vdd_memory	5030.72	4765.00	input	positive memory supply
111	VCtrl	5030.72	4645.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	4525.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	4405.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	4285.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	4165.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3925.00	input/output (5V open drain)	I^2C Data
117	SCL	5030.72	3805.00	CMOS input (5V)	I^2C Clock
118	EnableEDC	5030.72	3685.00	CMOS input (internal pull down)	enable I^2C EDC
119	gnd	5030.72	3565.00	input	negative digital supply
120	vdd_digital	5030.72	3445.00	input	positive digital supply
121	gnd	5030.72	3325.00	input	negative digital supply
122	vdd_memory	5030.72	3205.00	input	positive memory supply
123	vdd_digital	5030.72	3085.00	input	positive digital supply
124	vdd_digital	5030.72	2965.00	input	positive digital supply
125	gnd	5030.72	2845.00	input	negative digital supply
126	gnd	5030.72	2725.00	input	negative digital supply
127	RPMonitor	5030.72	2485.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	2365.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	2245.00	CMOS input	Bank Select
130	PowerUpReset	5030.72	2125.00	input	Power Up Reset
131	vdd_digital	5030.72	1045.00	input	positive digital supply
132	vdd_digital	5030.72	925.00	input	positive digital supply
133	gnd	5030.72	805.00	input	negative digital supply
134	gnd	5030.72	685.00	input	negative digital supply
135	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notL0Reset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	negative digital supply
140	gnd	3990.00	69.28	input	negative digital supply
141	vdd_digital	3870.00	69.28	input	positive digital supply
142	vdd_digital	3750.00	69.28	input	positive digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	

Table 11: *OTIS 1.1* Pad Descriptions contd.

Number	Name	X [μm]	Y [μm]	Type	Description
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	
159	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
160	notDataValid	1590.00	69.28	CMOS output (neg.)	
161	gnd	1470.00	69.28	input	negative digital supply
162	gnd	1350.00	69.28	input	negative digital supply
163	vdd_digital	1230.00	69.28	input	positive digital supply
164	vdd_digital	1110.00	69.28	input	positive digital supply
165	DLLReset	990.00	69.28	CMOS input	DLL Reset
166	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	notBXReset	750.00	69.28	LVDS input (neg.)	
168	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	notEVReset	510.00	69.28	LVDS input (neg.)	

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