Prototype for an Optical 12 input Receiver Card for the LHCb TELL1 Board

October 18, 2003

Abstract

The Optical Receiver Card for the LHCb TELL1 Board receives optical serial data coming from the cavern by optical ribbon fibers and transforms it to parallel electrical data. It is equipped with a 12 fiber optical receiver and 12 deserializer chips. It will be used by the Silicon Tracker, Trigger Tracker, Outer Tracker, Veto, Muon and Calorimeter. Two optical receiver cards fit on one LHCb TELL1 allowing a total of 24 optical inputs. The LHCb Inner and Outer tracker will use the Optical Receiver Card together with the GOL chip on the detector side. The Vertex Locator will use Analog Receiver Cards, two of which use the same space and connectors as one Optical Receiver Card.

LHCb Internal Note

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1 Introduction

Optical data arriving at 1.6 Gbit/s on a 12 fiber optical ribbon is de-serialized and 8/10 bit decoded to 12 ·16 bit parallel at 80 MHz. The optical receiver is a 12 input Paracer 2800 22RM [10] with an socket following the SNAP12 [11] industry standard. Deserializer is a TLK2501 [9] receiving 8/10 bit encoded serial data at 1.6 Gbit/s. It outputs 16 bit parallel data at 80 MHz plus data valid (RxDv), receive error (RxEr) and receive clock (RxClk) signals, through two high speed connectors Samtec QTS-100-03-L-D-A to the LHCb TELL1 Board [**?**]. The physical dimensions of the O-RxCard are 178 mm x 165 mm, the stack hight of the connectors between O-RxCard and TELL1 Board is 11 mm.

The O-RxCard uses analog 2.5 V, digital 2.5 V and digital 3.3 V, supplied by the LHCb TELL1 Board. Figure 1 shows the major components of the O-RxCard, the data flow is shown in figure 2.

2 Optical Receiver

The Paracer 2800 22 RM [10] is a 12 channel optical receiver with a 12 fiber optical ribbon input for data rates of up to 2.5 Gbit/s per channel, 1.6 Gbit/s will be the single fiber data rate.

2.1 Optical

The 2800 22 RM is produced for 62.5 μm fiber size and a center wavelength of 850 nm see table 1. The optical connector is MTP (MTO) compatible, a common type of optical ribbon cable for LHCb will be defined. Breakout cables from ribbon fiber to single LC, SMA or SC connectors will be used by sub detectors with single fiber inputs.

Table 1: Optical characteristic of the PR2800 receiver

Parameter	Min.	Typ	Max
Receiver saturation optical power	-3 dBm		
Receiver sensitivity	-16 dBm		-3 dBm
Wavelength	830 nm		860 nm
fiber	50/125 μm		62.5 μm

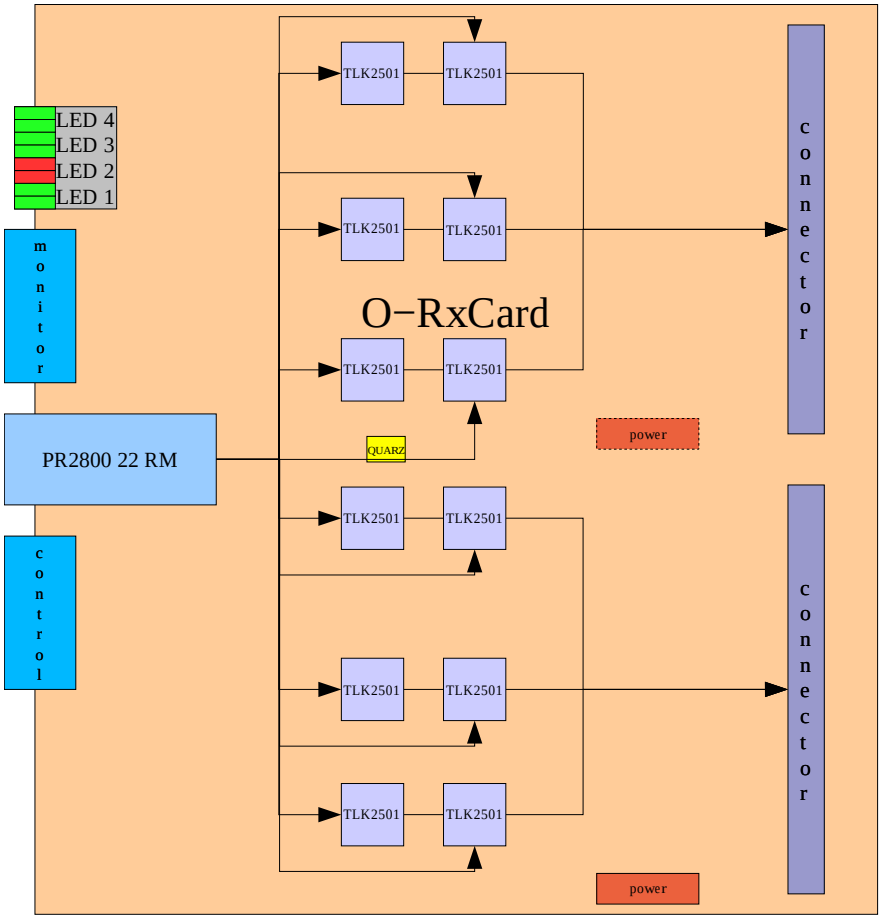

Figure 1: O-RxCard-overview, seen from top. Component side is bottom.

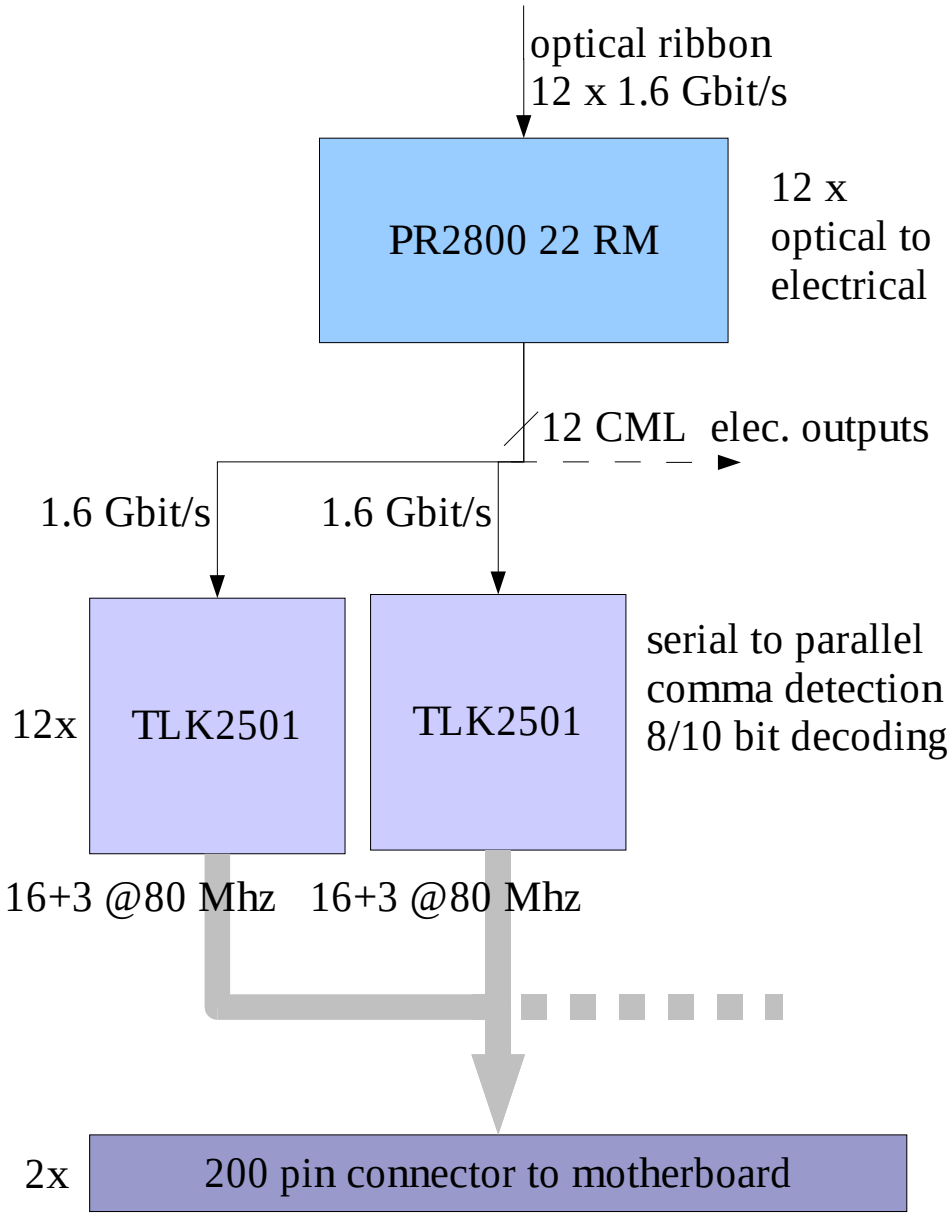

Figure 2: *Data flow O-RxCard. 12 fiber optical ribbon data is converted to high speed CML electrical signals, deserialized and 8/10 bit decoded.*

2.2 Electrical

The fast 1.6 Gbit/s outputs are AC-coupled high speed CML standard, summarized in table 2

Table 2: Electrical Characteristics of the PR2800

Parameter	Min.	Typ	Max
Supply voltage	3.135 V	3.3 V	3.465 V
Supply current		320 mA	400 mA
Power dissipation		1.1 W	1.4 W
supply noise			200 mV
Data output voltage (Differential pk-pk)	400 mV		650 mV
Data output rise/fall time 20%-80%		145 ps	160 ps
Low cut-off frequency	25 KHz		160 KHz
Total jitter (pk-pk)			120 ps
Deterministic jitter			45 ps

The high speed connection between optical receiver and deserializer are differential 100 Ohm traces (see section 8), with AC coupling (10 nF) and 50 Ohm termination to a termination voltage of 2 V at the deserializer inputs (see appendix B). Test pads with low capacity allow signal integrity checks for the twelve pairs of high speed traces. The receiver is mounted on a 100 pin BGA socked with connectivity shown in table 3. SD will de-assert (low) if one or more than one optical input has input power below -19 dBm. SQEN is the squelch enable input. If squelch enable (SQEN) is high (internal pull up), all outputs go to logic zero in case of signal detect = low. SQEN is pulled down by an external pull down resistor.

The 3.3 V power for the optical receiver is filtered with a low DC resistance ferrite bead plus six 4.7 μF and six 10 nF ceramic capacitors ensuring high immunity to switching noise from the TELL1 Board.

2.3 Mechanics

Utilizing a SNAP12 [11] standard Meg Array connector it can easily be mounted or replaced by receivers from other producers. The Meg Array connector has a 10x10 pin 1.27 mm pitch BGA footprint. Overall dimensions are 41.5 mm x 17.8 mm x 12.32 mm (LxWxH), with three screw holes (2.7 mm) and two positioning pin holes (1.7 mm) forseen. Mounting on the

Table 3: Pin Map for the PR2800

	J	I	H	G	F	E	D	C	B	A
1	NC	NC	NC	GND	GND	GND	GND	GND	GND	NC
2	NC	NC	NC	GND	GND	DO6	GND	GND	DO9	GND
3	NC	VCC	VCC	GND	DO5	DO6	GND	DO8	DO9	GND
4	NC	VCC	VCC	DO4	DO5	GND	DO7	DO8	GND	GND
5	NC	VCC	VCC	DO4	GND	DO3	DO7	GND	DO10	GND
6	NC	VCC	VCC	GND	DO2	DO3	GND	DO11	DO10	GND
7	NC	NC	SD	DO1	DO2	GND	DO12	DO11	GND	NC
8	NC	NC	NC	DO1	GND	GND	DO12	GND	GND	NC
9	NC	NC	NC	GND	GND	GND	GND	GND	GND	NC
10	SQEN	NC	NC	NC	NC	NC	DNC	DNC	DNC	NC

bottom side of the O-RxCard makes cut outs (45 mm x 25 mm) in the motherboard (Common L1) necessary, since the spacing is only 11 mm between both boards. More detailed information can be found in [10] and appendix A.

3 Deserializer

The TLK2501 [9] is a 1.5 to 2.5 Gbit/s serializer/deserializer. As one TLK2501 is needed per optical input, twelve deserializer are mounted on the O-RxCard in total. The TLK2501 performs serial to parallel data conversion and clock extraction. In addition 8/10 bit decoding following Gbit-Ethernet [12] is done. On 1.6 Gbit/s input data rate 16 bits, two control bits and the receive clock are output at 80 MHz. The receive clock (RxClk) is the recovered serial data clock divided by 20 (=80.16 MHz), data and control bits are valid on the rising edge of the RxClk. The control bits receive error (RxEr) and (RxDv) indicate idle mode, carrier extend, normal data or receive error propagation see table 4. Some sub detectors will use the RxDv signal for data synchronization. This implies that the front end chip (ie. OTIS, Beetle) has to pull high the tx_en input of the serializer (GOL) for the full time valid data is input to the serializer.

Table 4: Receive Status Signals, refer to [12] for details

Received 20 bit data	RxDv	RxEr
IDLE (<K28.5, D5.6>, <K28.5, D16.2>)	0	0
Carrier extend	0	1
Normal data character	1	0
Receive error propagation (<K30.7, K30.7>)	1	1

3.1 Electrical

The TLK2501 has serial differential receive inputs with a 200 mV input threshold see table 5 [1]

The input from the optical receiver to the TLK2501 is AC coupled 100 Ohm differential see 2.2, fulfilling all requirements.

Table 5: Receiver characteristics TLK2501

	Parameter	Min	Nom	Max	UNIT
V_{ID}	Differential receiver input voltage requirements, V_{ID}=—V_RXP-V_RXN—	200			mV
V_cmr	Receiver common mode voltage range, (V_RXP-V_RXN)/2	1500		V_{DD}-$V_{ID/2}$	mV
C_I	Receiver Input capacitance			2	pF
	Jitter tolerance	0.40			UI[1]
$t_{d(Rx\_latency)}$	Rx latency	76		107	bits

The 16-bit parallel data, control words and RxClk output signals are 2.5 V TTL compatible, shown in table 6.

The 80 MHz parallel data, RxEr, RxDv, RxClk are series terminated with 50 Ohm at the TLK2501 and have controlled impedance 50 Ohm traces to the Samtec QTS-100-03-L-D-A connector. Note that these traces are not matched in length, 200 ps skew between RxClk and RxData can be reached within one data group, the estimate for the maximum skew within the hole board is 500 ps corresponding to 10 cm maximum difference in trace length.

For debugging purposes the TLK2501 has four inputs described in table 7

[1] UI is the time interval of one serialized bit

Table 6: Parallel 16 bit data, control bit (RxDv, RxEr) and RxClk are 2.5 V TTL compatible

	Parameter	Test conditions	Min	Nom	Max	UNIT
V_{OH}	High-level output voltage	I_{OH}=-1 mA,V_{DD}=MIN	2.10	2.3		V
V_{Ol}	Low-level output voltage	I_{OL}=1 mA,V_{DD}=MIN	GND	0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of RxClk, RxEr RxDv, RxData	0.8 V to 2 V, C=5 pF	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of RxClk, RxEr RxDv, RxData	0.8 V to 2 V, C=5 pF	0.5			V/ns
t_{su}	RxData, RxEr, RxDv setup to ↑ RxClk	50% voltage swing, GTXClk=75 MHz	5.4			ns
t_h	RxData, RxEr, RxDv hold to ↑ RxClk	50% voltage swing, GTXClk=75 MHz	5.4			ns

The TTL inputs GtxClk, Enable, LckRef, LoopEn, PrbsEn are TTL compatible, table 8.

The TLK2501 needs 2.5 V power, coming over Cu plates on the Samtec high speed connector. For best operation a separate analog 2.5 V input is forseen. Each deserializer has two C/L/C low-pass filters for analog 2.5 V and extra blocking capacitors for digital 2.5 V. The relevant power supply parameters for the TLK2501 are summarized in table 9

Table 7: The input signals Enable, LckRef, LoopEn and PrsbsEn allow debugging the TLK2501

Signal	Type	description
Enable	input	Device Enable
	0	Enable low puts circuit in power down mode, signal detect circuit on serial receiver remains active
	1 jumper to pull up	Active high device enabled
LckRef	input	Lock to reference
	0	LckRef low locks transmitter part to GTXClk and puts receiver output to high impedance.
	1 internal pull-up	LckRef high locks receiver to receive data stream
LoopEn	input	LoopEn
	0 internal pull-down	LoopEn low means standard operation
	1	LoopEn active high activates internal loop-back
PrbsEn	input	Pseudo Random Bit Test Enable
	0 external pull-down	no pseudo random test
	1	PrbsEn high pseudo random bit stream can be monitored RxEr/PRBS_PASS high = valid PRBS received

Table 8: TTL input electrical characteristics over recommended operating conditions (unless otherwise noted), TTL signals: TXDO TXD15, GTXClk, LoopEn, LckRef, PrbsEn

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IH}	High-level input voltage		1.7		3.6	V
V_{IL}	Low-level input voltage				0.80	V
I_{IH}	Input high current	V_{DD} = MAX, V_{IN} =2 V			40	μA
I_{IL}	Input low current	V_{DD} = MAX, V_{IN} =0.4 V	-40			μA
C_I	Input capacitance	0.8 V to 2 V			4	pF
t_r	Rise time GTXClk, TxEn, TxEr, TXD	0.8 V to 2 V, C = 5 pF		1		ns
t_f	Fall time GTXClk, TxEn, TxEr, TXD	2 V to 0.8 V, C = 5 pF		1		ns
t_{su}	TXD, TxEn, TxEr setup to GTXClk		1.5			ns
t_h	TXD, TxEn, TxEr hold to GTXClk		0.4			ns

Table 9: TLK2501 power characteristic

Parameter	Min.	Typ	Max	UNIT
Supply voltage	2.3	2.5	2.7	V
Supply current		105		mA
Power dissipation		262	500	mW
Operating free air temperature	-40		85	°C
PLL startup lock time		0.1	0.4	ms

4 Input/Output

The Input and output of the O-RxCard comprises the following tasks:

- optical data input from the cavern
- parallel data output to the TELL1
- control signals from the TELL1 to the O-RxCard
- throughput of eight bits from the TELL1 to the front-side
- connection to the reset push button on the front-side
- power connector

The optical connector on the front side is a optical ribbon MTP (MTO) compatible type see [10]. Twelve optical fibers/channels are connected by this connector to the O-RxCard.

The parallel data output shares two connectors with the status and control bits for the TLK2501 and the receive clock. All other signals going from the TELL1 Board to the O-RxCard use these Samtec QTS-100-03-L-D-A high speed connectors as well see tables 10, 11, 12, 13. A large Cu power plane in the middle of the connector enhances signal quality. The signals are grouped to 24 pins for each TLK2501 deserializer using the same pins as for the analog receiver card ADC data. In one group are 16 data bits, the receive status bits, two out of four control bits and the receive clock. Additionally each connector carries

- 80.16 MHz input clock
- one Signal Detect bit coming from the optical receiver. Signal detect will de-assert (low), if one or more optical inputs are below -19 dBm optical input power.
- the reset signal from the front side push button
- Four bits going straight from the TELL1 Board to a front side connector "control", table 14
- I^2C (n.c. on O-RxCard) and JTAG
- one test point (TP pin 196)

In order to monitor the operation of the deserializers, the status of one deserializer (TLK2501-5) can be analyzed with the help of a front side connector "monitor" see table 14.

The buses for slow control, I^2C and JTAG, are not used on the O-RxCard. To ensure the usability of the JTAG chain the JTAG signal input (JTAGRX_TDI pin 199) and output (JTAGRX_TDO pin 200) are connected short.

In addition to the signals directly routed from the Common L1 Board to the front connectors, for each 200-pin connector one test point is accessible on the O-RxCard (TP pin 196). 41 pins per Samtec 200-pin connector remain not connected.

The connectivity for the power planes of the two Samtec 200-pin connectors is shown in table 15, the extra 12 pin power connector carries analog 2.5 V and digital 3.3 V see table 16.

Table 10: Signal distribution on receiver-card connector S1, 4 connectors with 200 pins each are foreseen (Samtec QTS-100-03-L-D-A on the O-Rx-card), the left side shows the corresponding signals on the analog RxCard 1/4

VELO				OT			
Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
ADC0(0)	S1-1	S1-2	ADC0(1)	Data0(15)	S1-1	S1-2	Data0(14)
ADC0(2)	S1-3	S1-4	ADC0(3)	Data0(13)	S1-3	S1-4	Data0(12)
ADC0(4)	S1-5	S1-6	ADC0(5)	Data0(11)	S1-5	S1-6	Data0(10)
ADC0(6)	S1-7	S1-8	ADC0(7)	Data0(9)	S1-7	S1-8	Data0(8)
ADC0(8)	S1-9	S1-10	ADC0(9)	Data0(7)	S1-9	S1-10	Data0(6)
ADC1(0)	S1-11	S1-12	ADC1(1)	Data0(5)	S1-11	S1-12	Data0(4)
ADC1(2)	S1-13	S1-14	ADC1(3)	Data0(3)	S1-13	S1-14	Data0(2)
ADC1(4)	S1-15	S1-16	ADC1(5)	Data0(1)	S1-15	S1-16	Data0(0)
ADC1(6)	S1-17	S1-18	ADC1(7)	RxEr0	S1-17	S1-18	RxDv0
ADC1(8)	S1-19	S1-20	ADC1(9)	LckRef0	S1-19	S1-20	Enable012
ADCClk0	S1-21	S1-22	ADCClk1	RxClk0	S1-21	S1-22	NC
GND	S1-23	S1-24	GND	GND	S1-23	S1-24	GND
ADC2(0)	S1-25	S1-26	ADC2(1)	LED3(2)	S1-25	S1-26	LED3(4)
ADC2(2)	S1-27	S1-28	ADC2(3)	LED3(6)	S1-27	S1-28	LED3(8)
ADC2(4)	S1-29	S1-30	ADC2(5)	NC	S1-29	S1-30	NC
ADC2(6)	S1-31	S1-32	ADC2(7)	NC	S1-31	S1-32	NC
ADC2(8)	S1-33	S1-34	ADC2(9)	NC	S1-33	S1-34	NC
ADC3(0)	S1-35	S1-36	ADC3(1)	NC	S1-35	S1-36	NC
ADC3(2)	S1-37	S1-38	ADC3(3)	NC	S1-37	S1-38	NC
ADC3(4)	S1-39	S1-40	ADC3(5)	NC	S1-39	S1-40	NC
ADC3(6)	S1-41	S1-42	ADC3(7)	NC	S1-41	S1-42	NC
ADC3(8)	S1-43	S1-44	ADC1(9)	NC	S1-43	S1-44	NC
ADCClk2	S1-45	S1-46	ADCClk3	NC	S1-45	S1-46	NC
GND	S1-47	S1-48	GND	GND	S1-47	S1-48	GND
ADC4(0)	S1-49	S1-50	ADC4(1)	Data1(15)	S1-49	S1-50	Data1(14)
ADC4(2)	S1-51	S1-52	ADC4(3)	Data1(13)	S1-51	S1-52	Data1(12)
ADC4(4)	S1-53	S1-54	ADC4(5)	Data1(11)	S1-53	S1-54	Data1(10)
ADC4(6)	S1-55	S1-56	ADC4(7)	Data1(9)	S1-55	S1-56	Data1(8)
ADC4(8)	S1-57	S1-58	ADC4(9)	Data1(7)	S1-57	S1-58	Data1(6)
ADC5(0)	S1-59	S1-60	ADC5(1)	Data1(5)	S1-59	S1-60	Data1(4)
ADC5(2)	S1-61	S1-62	ADC5(3)	Data1(3)	S1-61	S1-62	Data1(2)
ADC5(4)	S1-63	S1-64	ADC5(5)	Data1(1)	S1-63	S1-64	Data1(0)
ADC5(6)	S1-65	S1-66	ADC5(7)	RxEr1	S1-65	S1-66	RxDv1
ADC5(8)	S1-67	S1-68	ADC5(9)	LckRef1	S1-67	S1-68	LoopEn012
ADCClk4	S1-69	S1-70	ADCClk5	RxClk1	S1-69	S1-70	NC
GND	S1-71	S1-72	GND	GND	S1-71	S1-72	GND
ADC6(0)	S1-73	S1-74	ADC6(1)	Data2(15)	S1-73	S1-74	Data2(14)
ADC6(2)	S1-75	S1-76	ADC6(3)	Data2(13)	S1-75	S1-76	Data2(12)
ADC6(4)	S1-77	S1-78	ADC6(5)	Data2(11)	S1-77	S1-78	Data2(10)
ADC6(6)	S1-79	S1-80	ADC6(7)	Data2(9)	S1-79	S1-80	Data2(8)
ADC6(8)	S1-81	S1-82	ADC6(9)	Data2(7)	S1-81	S1-82	Data2(6)
ADC7(0)	S1-83	S1-84	ADC7(1)	Data2(5)	S1-83	S1-84	Data2(4)
ADC7(2)	S1-85	S1-86	ADC7(3)	Data2(3)	S1-85	S1-86	Data2(2)
ADC7(4)	S1-87	S1-88	ADC7(5)	Data2(1)	S1-87	S1-88	Data2(0)
ADC7(6)	S1-89	S1-90	ADC7(7)	RxEr2	S1-89	S1-90	RxDv2
ADC7(8)	S1-91	S1-92	ADC7(9)	LckRef2	S1-91	S1-92	PrbsEn012
ADCClk6	S1-93	S1-94	ADCClk7	RxClk2	S1-93	S1-94	ExClk1
GND	S1-95	S1-96	GND	GND	S1-95	S1-96	GND

Table 11: Signal distribution on receiver-card connector S1, 4 connectors with 200 pins each are foreseen (Samtec QTS-100-03-L-D-A on the O-Rx-card), the left side shows the corresponding signals on the analog RxCard 2/4

ADC8(0)	S1-97	S1-98	ADC8(1)	Data3(15)	S1-97	S1-98	Data3(14)
ADC8(2)	S1-99	S1-100	ADC8(3)	Data3(13)	S1-99	S1-100	Data3(12)
ADC8(4)	S1-101	S1-102	ADC8(5)	Data3(11)	S1-101	S1-102	Data3(10)
ADC8(6)	S1-103	S1-104	ADC8(7)	Data3(9)	S1-103	S1-104	Data3(8)
ADC8(8)	S1-105	S1-106	ADC8(9)	Data3(7)	S1-105	S1-106	Data3(6)
ADC9(0)	S1-107	S1-108	ADC9(1)	Data3(5)	S1-107	S1-108	Data3(4)
ADC9(2)	S1-109	S1-110	ADC9(3)	Data3(3)	S1-109	S1-110	Data3(2)
ADC9(4)	S1-111	S1-112	ADC9(5)	Data3(1)	S1-111	S1-112	Data3(0)
ADC9(6)	S1-113	S1-114	ADC9(7)	RxEr3	S1-113	S1-114	RxDv3
ADC9(8)	S1-115	S1-116	ADC9(9)	LckRef3	S1-115	S1-116	Enable345
ADCClk8	S1-117	S1-118	ADCClk9	RxClk3	S1-117	S1-118	NC
GND	S1-119	S1-120	GND	GND	S1-119	S1-120	GND
ADC10(0)	S1-121	S1-122	ADC10(1)	Data4(15)	S1-121	S1-122	Data4(14)
ADC10(2)	S1-123	S1-124	ADC10(3)	Data4(13)	S1-123	S1-124	Data4(12)
ADC10(4)	S1-125	S1-126	ADC10(5)	Data4(11)	S1-125	S1-126	Data4(10)
ADC10(6)	S1-127	S1-128	ADC10(7)	Data4(9)	S1-127	S1-128	Data4(8)
ADC10(8)	S1-129	S1-130	ADC10(9)	Data4(7)	S1-129	S1-130	Data4(6)
ADC11(0)	S1-131	S1-132	ADC11(1)	Data4(5)	S1-131	S1-132	Data4(4)
ADC11(2)	S1-133	S1-134	ADC11(3)	Data4(3)	S1-133	S1-134	Data4(2)
ADC11(4)	S1-135	S1-136	ADC11(5)	Data4(1)	S1-135	S1-136	Data4(0)
ADC11(6)	S1-137	S1-138	ADC11(7)	RxEr4	S1-137	S1-138	RxDv4
ADC11(8)	S1-139	S1-140	ADC11(9)	LckRef4	S1-139	S1-140	LoopEn345
ADCClk10	S1-141	S1-142	ADCClk11	RxClk4	S1-141	S1-142	NC
GND	S1-143	S1-144	GND	GND	S1-143	S1-144	GND
ADC12(0)	S1-145	S1-146	ADC12(1)	con1	S1-145	S1-146	con3
ADC12(2)	S1-147	S1-148	ADC12(3)	con5	S1-147	S1-148	con7
ADC12(4)	S1-149	S1-150	ADC12(5)	NC	S1-149	S1-150	NC
ADC12(6)	S1-151	S1-152	ADC12(7)	NC	S1-151	S1-152	NC
ADC12(8)	S1-153	S1-154	ADC12(9)	NC	S1-153	S1-154	NC
ADC13(0)	S1-155	S1-156	ADC13(1)	NC	S1-155	S1-156	NC
ADC13(2)	S1-157	S1-158	ADC13(3)	NC	S1-157	S1-158	NC
ADC13(4)	S1-159	S1-160	ADC13(5)	NC	S1-159	S1-160	NC
ADC13(6)	S1-161	S1-162	ADC13(7)	NC	S1-161	S1-162	NC
ADC13(8)	S1-163	S1-164	ADC13(9)	Reset	S1-163	S1-164	SD
ADCClk13	S1-165	S1-166	ADCClk13	NC	S1-165	S1-166	NC
GND	S1-167	S1-168	GND	GND	S1-167	S1-168	GND
ADC14(0)	S1-169	S1-170	ADC14(1)	Data5(15)	S1-169	S1-170	Data5(14)
ADC14(2)	S1-171	S1-172	ADC14(3)	Data5(13)	S1-171	S1-172	Data5(12)
ADC14(4)	S1-173	S1-174	ADC14(5)	Data5(11)	S1-173	S1-174	Data5(10)
ADC14(6)	S1-175	S1-176	ADC14(7)	Data5(9)	S1-175	S1-176	Data5(8)
ADC14(8)	S1-177	S1-178	ADC14(9)	Data5(7)	S1-177	S1-178	Data4(6)
ADC15(0)	S1-179	S1-180	ADC15(1)	Data5(5)	S1-179	S1-180	Data5(4)
ADC15(2)	S1-181	S1-182	ADC15(3)	Data5(3)	S1-181	S1-182	Data5(2)
ADC15(4)	S1-183	S1-184	ADC15(5)	Data5(1)	S1-183	S1-184	Data5(0)
ADC15(6)	S1-185	S1-186	ADC15(7)	RxEr5	S1-185	S1-186	RxDv5
ADC15(8)	S1-187	S1-188	ADC15(9)	LckRef5	S1-187	S1-188	PrbsEn345
ADCClk14	S1-189	S1-190	ADCClk15	RxClk5	S1-189	S1-190	NC
RXADDR5	S1-191	S1-192	RXADDR6	RXADDR5	S1-191	S1-192	RXADDR6
RXSDA	S1-193	S1-194	RXSCL	RXSDA	S1-193	S1-194	RXSCL
JTAGRX_TMS	S1-195	S1-196	T1	JTAGRX_TMS	S1-195	S1-196	T1
JTAGRX_TRSTB	S1-197	S1-198	JTAGRX_TCK	JTAGRX_TRSTB	S1-197	S1-198	JTAGRX_TCK
JTAGRX_TDI	S1-199	S1-200	JTAGRX_TDO	JTAGRX_TDI	S1-199	S1-200	JTAGRX_TDO

Table 12: Signal distribution on receiver-card connector S2, 4 connectors with 200 pins each are foreseen (Samtec QTS-100-03-L-D-A on the O-Rx-card), the left side shows the corresponding signals on the analog RxCard 3/4

VELO				OT			
Signal	Pin	Pin	Signal	Signal	Pin	Pin	Signal
ADC0(0)	S2-1	S2-2	ADC0(1)	Data6(15)	S2-1	S2-2	Data6(14)
ADC0(2)	S2-3	S2-4	ADC0(3)	Data6(13)	S2-3	S2-4	Data6(12)
ADC0(4)	S2-5	S2-6	ADC0(5)	Data6(11)	S2-5	S2-6	Data6(10)
ADC0(6)	S2-7	S2-8	ADC0(7)	Data6(9)	S2-7	S2-8	Data6(8)
ADC0(8)	S2-9	S2-10	ADC0(9)	Data6(7)	S2-9	S2-10	Data6(6)
ADC1(0)	S2-11	S2-12	ADC1(1)	Data6(5)	S2-11	S2-12	Data6(4)
ADC1(2)	S2-13	S2-14	ADC1(3)	Data6(3)	S2-13	S2-14	Data6(2)
ADC1(4)	S2-15	S2-16	ADC1(5)	Data6(1)	S2-15	S2-16	Data6(0)
ADC1(6)	S2-17	S2-18	ADC1(7)	RxEr6	S2-17	S2-18	RxDv6
ADC1(8)	S2-19	S2-20	ADC1(9)	LckRef6	S2-19	S2-20	Enable678
ADCClk0	S2-21	S2-22	ADCClk1	RxClk6	S2-21	S2-22	NC
GND	S2-23	S2-24	GND	GND	S2-23	S2-24	GND
ADC2(0)	S2-25	S2-26	ADC2(1)	LED4(2)	S2-25	S2-26	LED4(4)
ADC2(2)	S2-27	S2-28	ADC2(3)	LED4(6)	S2-27	S2-28	LED4(8)
ADC2(4)	S2-29	S2-30	ADC2(5)	NC	S2-29	S2-30	NC
ADC2(6)	S2-31	S2-32	ADC2(7)	NC	S2-31	S2-32	NC
ADC2(8)	S2-33	S2-34	ADC2(9)	NC	S2-33	S2-34	NC
ADC3(0)	S2-35	S2-36	ADC3(1)	NC	S2-35	S2-36	NC
ADC3(2)	S2-37	S2-38	ADC3(3)	NC	S2-37	S2-38	NC
ADC3(4)	S2-39	S2-40	ADC3(5)	NC	S2-39	S2-40	NC
ADC3(6)	S2-41	S2-42	ADC3(7)	NC	S2-41	S2-42	NC
ADC3(8)	S2-43	S2-44	ADC1(9)	NC	S2-43	S2-44	NC
ADCClk2	S2-45	S2-46	ADCClk3	NC	S2-45	S2-46	NC
GND	S2-47	S2-48	GND	GND	S2-47	S2-48	GND
ADC4(0)	S2-49	S2-50	ADC4(1)	Data7(15)	S2-49	S2-50	Data7(14)
ADC4(2)	S2-51	S2-52	ADC4(3)	Data7(13)	S2-51	S2-52	Data7(12)
ADC4(4)	S2-53	S2-54	ADC4(5)	Data7(11)	S2-53	S2-54	Data7(10)
ADC4(6)	S2-55	S2-56	ADC4(7)	Data7(9)	S2-55	S2-56	Data7(8)
ADC4(8)	S2-57	S2-58	ADC4(9)	Data7(7)	S2-57	S2-58	Data7(6)
ADC5(0)	S2-59	S2-60	ADC5(1)	Data7(5)	S2-59	S2-60	Data7(4)
ADC5(2)	S2-61	S2-62	ADC5(3)	Data7(3)	S2-61	S2-62	Data7(2)
ADC5(4)	S2-63	S2-64	ADC5(5)	Data7(1)	S2-63	S2-64	Data7(0)
ADC5(6)	S2-65	S2-66	ADC5(7)	RxEr7	S2-65	S2-66	RxDv7
ADC5(8)	S2-67	S2-68	ADC5(9)	LckRef7	S2-67	S2-68	LoopEn678
ADCClk4	S2-69	S2-70	ADCClk5	RxClk7	S2-69	S2-70	NC
GND	S2-71	S2-72	GND	GND	S2-71	S2-72	GND
ADC6(0)	S2-73	S2-74	ADC6(1)	Data8(15)	S2-73	S2-74	Data8(14)
ADC6(2)	S2-75	S2-76	ADC6(3)	Data8(13)	S2-75	S2-76	Data8(12)
ADC6(4)	S2-77	S2-78	ADC6(5)	Data8(11)	S2-77	S2-78	Data8(10)
ADC6(6)	S2-79	S2-80	ADC6(7)	Data8(9)	S2-79	S2-80	Data8(8)
ADC6(8)	S2-81	S2-82	ADC6(9)	Data8(7)	S2-81	S2-82	Data8(6)
ADC7(0)	S2-83	S2-84	ADC7(1)	Data8(5)	S2-83	S2-84	Data8(4)
ADC7(2)	S2-85	S2-86	ADC7(3)	Data8(3)	S2-85	S2-86	Data8(2)
ADC7(4)	S2-87	S2-88	ADC7(5)	Data8(1)	S2-87	S2-88	Data8(0)
ADC7(6)	S2-89	S2-90	ADC7(7)	RxEr8	S2-89	S2-90	RxDv8
ADC7(8)	S2-91	S2-92	ADC7(9)	LckRef8	S2-91	S2-92	PrbsEn678
ADCClk6	S2-93	S2-94	ADCClk7	RxClk8	S2-93	S2-94	ExClk2
GND	S2-95	S2-96	GND	GND	S2-95	S2-96	GND

Table 13: Signal distribution on receiver-card connector S2, 4 connectors with 200 pins each are foreseen (Samtec QTS-100-03-L-D-A on the O-Rx-card), the left side shows the corresponding signals on the analog RxCard 4/4. In the enumeration of the control signals 9AB stands for data block 9, A = 10, B = 11

ADC8(0)	S2-97	S2-98	ADC8(1)	Data9(15)	S2-97	S2-98	Data9(14)
ADC8(2)	S2-99	S2-100	ADC8(3)	Data9(13)	S2-99	S2-100	Data9(12)
ADC8(4)	S2-101	S2-102	ADC8(5)	Data9(11)	S2-101	S2-102	Data9(10)
ADC8(6)	S2-103	S2-104	ADC8(7)	Data9(9)	S2-103	S2-104	Data9(8)
ADC8(8)	S2-105	S2-106	ADC8(9)	Data9(7)	S2-105	S2-106	Data9(6)
ADC9(0)	S2-107	S2-108	ADC9(1)	Data9(5)	S2-107	S2-108	Data9(4)
ADC9(2)	S2-109	S2-110	ADC9(3)	Data9(3)	S2-109	S2-110	Data9(2)
ADC9(4)	S2-111	S2-112	ADC9(5)	Data9(1)	S2-111	S2-112	Data9(0)
ADC9(6)	S2-113	S2-114	ADC9(7)	RxEr9	S2-113	S2-114	RxDv9
ADC9(8)	S2-115	S2-116	ADC9(9)	LckRef9	S2-115	S2-116	Enable9AB
ADCClk8	S2-117	S2-118	ADCClk9	RxClk9	S2-117	S2-118	NC
GND	S2-119	S2-120	GND	GND	S2-119	S2-120	GND
ADC10(0)	S2-121	S2-122	ADC10(1)	Data10(15)	S2-121	S2-122	Data10(14)
ADC10(2)	S2-123	S2-124	ADC10(3)	Data10(13)	S2-123	S2-124	Data10(12)
ADC10(4)	S2-125	S2-126	ADC10(5)	Data10(11)	S2-125	S2-126	Data10(10)
ADC10(6)	S2-127	S2-128	ADC10(7)	Data10(9)	S2-127	S2-128	Data10(8)
ADC10(8)	S2-129	S2-130	ADC10(9)	Data10(7)	S2-129	S2-130	Data10(6)
ADC11(0)	S2-131	S2-132	ADC11(1)	Data10(5)	S2-131	S2-132	Data10(4)
ADC11(2)	S2-133	S2-134	ADC11(3)	Data10(3)	S2-133	S2-134	Data10(2)
ADC11(4)	S2-135	S2-136	ADC11(5)	Data10(1)	S2-135	S2-136	Data10(0)
ADC11(6)	S2-137	S2-138	ADC11(7)	RxEr10	S2-137	S2-138	RxDv10
ADC11(8)	S2-139	S2-140	ADC11(9)	LckRef10	S2-139	S2-140	LoopEn9AB
ADCClk10	S2-141	S2-142	ADCClk11	RxClk10	S2-141	S2-142	NC
GND	S2-143	S2-144	GND	GND	S2-143	S2-144	GND
ADC12(0)	S2-145	S2-146	ADC12(1)	con9	S2-145	S2-146	con11
ADC12(2)	S2-147	S2-148	ADC12(3)	con13	S2-147	S2-148	con15
ADC12(4)	S2-149	S2-150	ADC12(5)	NC	S2-149	S2-150	NC
ADC12(6)	S2-151	S2-152	ADC12(7)	NC	S2-151	S2-152	NC
ADC12(8)	S2-153	S2-154	ADC12(9)	NC	S2-153	S2-154	NC
ADC13(0)	S2-155	S2-156	ADC13(1)	NC	S2-155	S2-156	NC
ADC13(2)	S2-157	S2-158	ADC13(3)	NC	S2-157	S2-158	NC
ADC13(4)	S2-159	S2-160	ADC13(5)	NC	S2-159	S2-160	NC
ADC13(6)	S2-161	S2-162	ADC13(7)	NC	S2-161	S2-162	NC
ADC13(8)	S2-163	S2-164	ADC13(9)	Reset	S2-163	S2-164	SD
ADCClk13	S2-165	S2-166	ADCClk13	NC	S2-165	S2-166	NC
GND	S2-167	S2-168	GND	GND	S2-167	S2-168	GND
ADC14(0)	S2-169	S2-170	ADC14(1)	Data11(15)	S2-169	S2-170	Data11(14)
ADC14(2)	S2-171	S2-172	ADC14(3)	Data11(13)	S2-171	S2-172	Data11(12)
ADC14(4)	S2-173	S2-174	ADC14(5)	Data11(11)	S2-173	S2-174	Data11(10)
ADC14(6)	S2-175	S2-176	ADC14(7)	Data11(9)	S2-175	S2-176	Data11(8)
ADC14(8)	S2-177	S2-178	ADC14(9)	Data11(7)	S2-177	S2-178	Data11(6)
ADC15(0)	S2-179	S2-180	ADC15(1)	Data11(5)	S2-179	S2-180	Data11(4)
ADC15(2)	S2-181	S2-182	ADC15(3)	Data11(3)	S2-181	S2-182	Data11(2)
ADC15(4)	S2-183	S2-184	ADC15(5)	Data11(1)	S2-183	S2-184	Data11(0)
ADC15(6)	S2-185	S2-186	ADC15(7)	RxEr11	S2-185	S2-186	RxDv11
ADC15(8)	S2-187	S2-188	ADC15(9)	LckRef11	S2-187	S2-188	PrbsEn9AB
ADCClk14	S2-189	S2-190	ADCClk15	RxClk11	S2-189	S2-190	NC
RXADDR5	S2-191	S2-192	RXADDR6	RXADDR5	S2-191	S2-192	RXADDR6
RXSDA	S2-193	S2-194	RXSCL	RXSDA	S2-193	S2-194	RXSCL
JTAGRX_TMS	S2-195	S2-196	T2	JTAGRX_TMS	S2-195	S2-196	T2
JTAGRX_TRSTB	S2-197	S2-198	JTAGRX_TCK	JTAGRX_TRSTB	S2-197	S2-198	JTAGRX_TCK
JTAGRX_TDI	S2-199	S2-200	JTAGRX_TDO	JTAGRX_TDI	S2-199	S2-200	JTAGRX_TDO

Table 14: One Control and one Monitor connector are placed on the front side of the TO-RxCard. The connectors are 16 pin 1/10 inch connectors from 3M.

pin	Control	Monitor
1	S1-145	RXDV4
2	GND	GND
3	S1-146	RXER4
4	GND	GND
5	S1-147	LCKREF4
6	GND	GND
7	S1-148	LOOPEN345
8	GND	GND
9	S2-145	ENABLE345
10	GND	GND
11	S2-146	PRBSEN345
12	GND	GND
13	S2-147	Rx-Clk4
14	GND	GND
15	S2-148	Clk-80-Mon
16	GND	GND

Table 15: Power Plates of 200 Pin Samtec connector, here O-RxCard implementation

Plate	Name	A-RxCard	O-RxCard
0	VccRx	3.3 V	2.5 V
1	GND		
2	VccRx	3.3 V	2.5 V
3	GND		

Table 16: Power Connector, 1/10 inch 2x10 pin socket on the O-Rx board side foreseen

signal	pin	signal	pin
AP5V	1	AP5V	2
AGND	3	AGND	4
AN5V	5	AN5V	6
AGND	7	AGND	8
A2P5	9	A2P5	10
D3V3	11	D3V3	12

5 LEDs

In addition to the control and monitor connectors a set of 4x4 LEDs has been placed on the front plate, see table 17. The first 4 LEDs show the power supply to the O-RxCard, the second 4 LEDs go red when more than 2.5 V are applied to the power plate 2.5 V digital inputs. The third and fourth LED indicate signals coming from the L1 Common Board via the two Samtec connectors. 4 signals can so be controlled by each preprocessing FPGA on the Common L1 Board.

Table 17: LEDs placed on the front side of the O-Rx Card. The LEDs are arranged in groups of four

pin	LED 1	LED 2	LED 3	LED 4
1	GND	GND	GND	GND
2	+3.3 V	2.5 V OVER	S1-25	S2-25
3	GND	GND	GND	GND
4	+5 V	2.5 V OVER	S1-26	S2-26
5	GND	GND	GND	GND
6	2.5 V	2.5 V OVER	S1-27	S2-27
7	-5 V	GND	GND	GND
8	GND	2.5 V OVER	S1-28	S2-28

6 Clock distribution

The TLK2501 extract the clock (RxClk) from the received serial data and outputs it to the Common L1 board via controlled 50 Ohm traces and the two high speed connectors. On the Common L1 board the RxClk of every deserializer will be input to a dedicated clock input of the corresponding PreProcessor FPGA. In addition a clock (GTXClk) has to be supplied to the TLK2501, in order to make clock locking on the input data possible. A local oscillator [2] as well as a clock from the Common L1 board can be used. To drive all twelve inputs an extra IC amplifies, the clock signal on the O-RxCard, the Fairchild 74LCX00 is a 3.3 V V_{CC} type with 5.3 ns maximum propagation delay.

[2]Custom 80.16 MHz oscillators are necessary here, for the Prototype an 80.00 MHz quartz will be employed

7 Power

The power consumption on the O-RxCard is dominated by the 12 deserializer TLK2501 and the optical receiver. In addition the clock driver, the quartz and the LEDs have to be accounted for, table 18.

Table 18: Power consumption of all parts on the O-RxCard

Device	Name	Qty	Voltage [V]			current [mA]			[W]
			min.	typ.	max.	min.	typ.	max.	
deserializer	TLK2501	12	2.3	2.5	2.7		105	< 190	<6
optical receiver	PR2800 22RM	1	3.135	3.3	3.465		320	400	<1.4
quartz	IQXO-71	1	3.0	3.3	3.6		30		<0.1
clock driver	74LCX00	1	2.0	3.3	3.6			100	<0.36
LEDs	2X4(Farnell)	16	1.8	2.5	3.6	5	10	15	<0.054
sum (2.5 V)			2.3	2.5	2.7		1270	2300	<6.2
sum (3.3 V)			3.135	3.3	3.465		400	540	<1.9
sum O-RxCard									<8.5

The O-RxCard uses 2.5 V for the deserializers and 3.3 V for the optical receiver, the quartz and clock driver. To ensure reliable operation in a noisy environment, the 2.5 V power for the digital part of the TLK2501 deserializer is connected via power planes of the high speed Samtec connectors (see table 15), analog 2.5 V and digital 3.3 V are supplied by an extra power connector, table 16. Using the same path for the 2.5 V power and the 80 MHz 2.5 V signals avoids additional skew and loops. The analog 2.5 V for the TLK2501 is filtered with two C L C combinations for each device, special care is taken on the TELL1 board for the generation of the analog 2.5 V too. The 3.3 V digital for the optical receiver has a C L C blocking, the quartz and oscillator share a 4.7 μF capacitor. To further improve the power distribution, layers 2 and 7 are ground, layer 3 is analog 2.5 V, layer 6 is 2.5 V digital and 3.3 V digital. Around the optical receiver layer 6 is reserved to the inductive filtered part of the 3.3 , figure 15.

As the analog receiver card (A-RxCard) for the TELL1 board uses a different voltage (3.3 V) on the power planes table 15, a set of LEDs (2.5 V over) will warn the user when combining a TELL1 board configured for the A-RxCard with an O-RxCard, see figure 9. Mind that the TLK2501 is specified for an absolute maximum 3.0 V input voltage, so 3.3 V will eventually destroy the deserializers!

8 PCB technology

The PCB is a eight layer type with controlled impedance layout on the top and bottom see table 19. In order to achieve 50 Ohms for the single ended LVTTL level parallel signal coming from the TLK2501 and the differential 100 Ohm for the fast 1.6 GHz going from the optical receivers to the TLK2501 dimensions have been chosen as shown in figure 3.

Table 19: The PCB consists of 8 layers, controlled impedance data on the top and bottom side, two control signal layers in the middle, analog power, digital power and two ground layers

layer	signals
1	Signal (1.6 GHz + 80 MHz)
2	GND
3	A2P5 (Analog +2.5 V)
4	Signal
5	Signal
6	GND
7	VccRx = D2V5, D3V3 (Digital +2.5 V , +3.3 V
8	Signal (1.6 GHz + 80 MHz)

Table 20: Trace dimensions for the 1.6 GHz differential traces

parameter	abbreviation	dimension
trace width	W	6 mil = 0.150 mm
space between traces	S	0.45 mm
Cu	t	1 mil = 0.035 mm
prepreg	h	0.1 mm
dielectric constant FR4	ϵ_r	4.1
impedance	Z_0	49.6 Ohm
differential impedance	Z_{diff}	98.5 Ohm

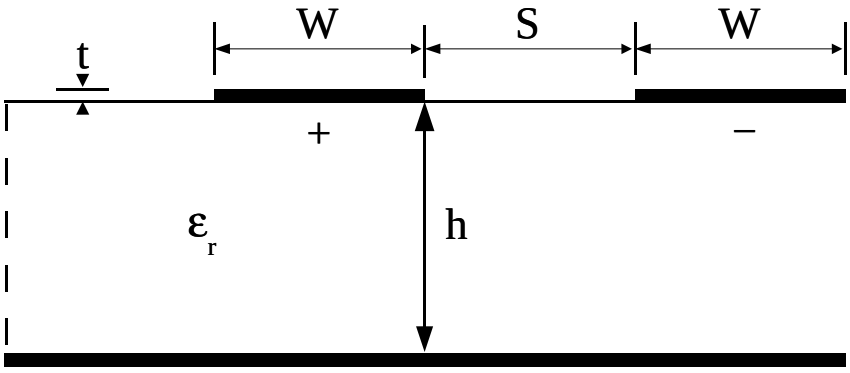

Figure 3: *Trace dimensions for the 1.6 GHz signals, see table 20. The high speed signals are led in differential pairs on the surface of the PCB.*

A Mechanical dimensions

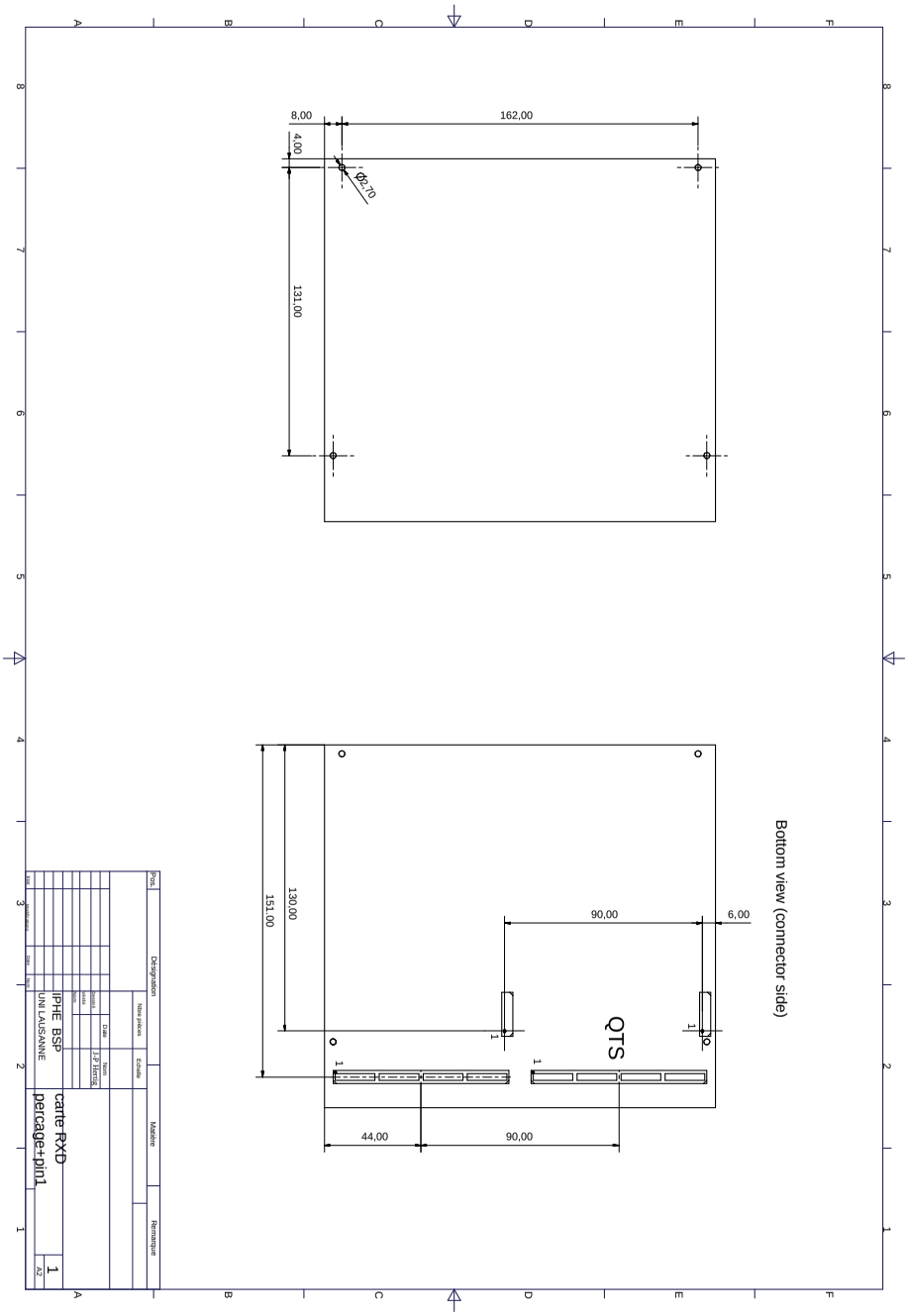

Figure 4: *Mechanical dimension for the O-RxCard - TELL1 interface*

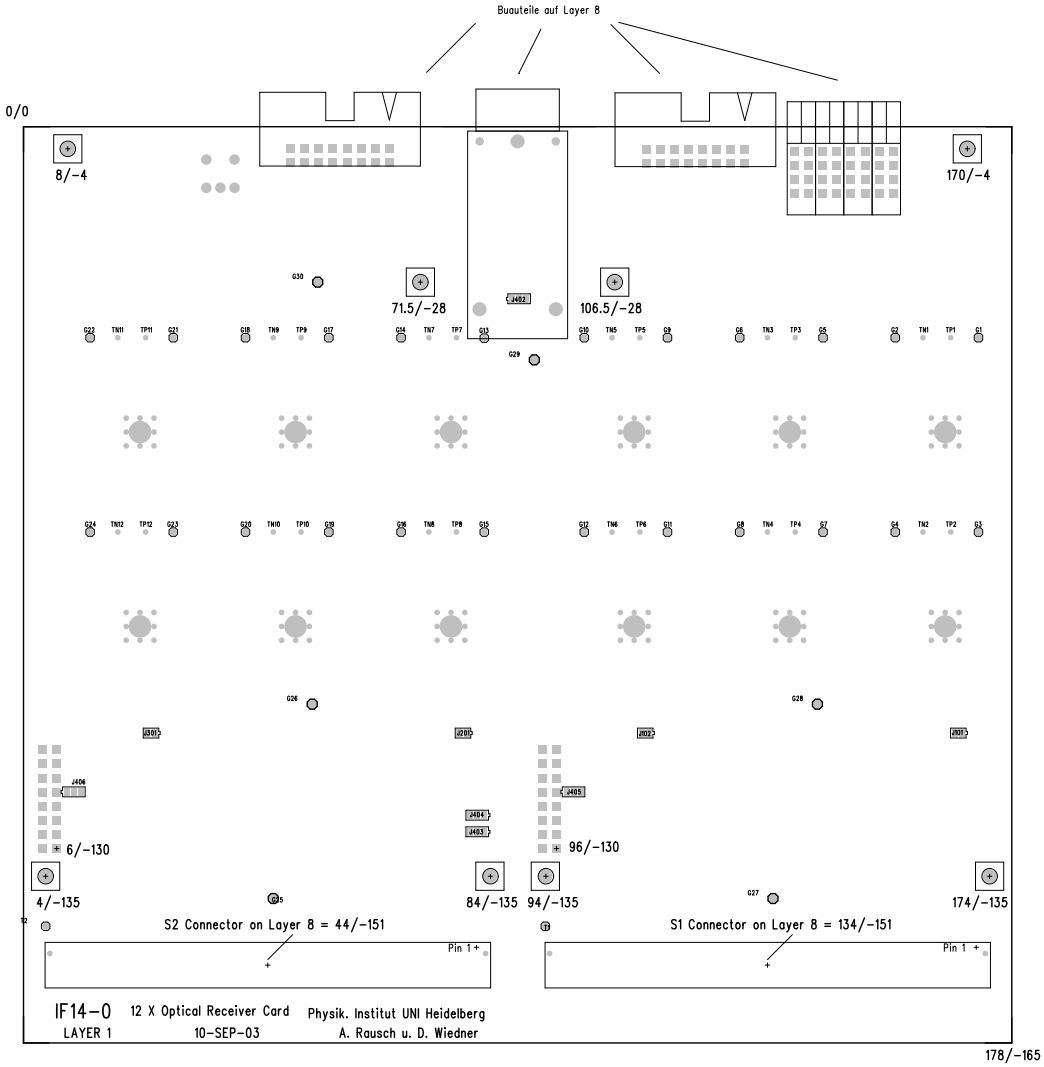

Figure 5: *Mechanical dimension of the O-RxCard, all dimensions use relative coordinates in mm from top left corner*

B Schematics

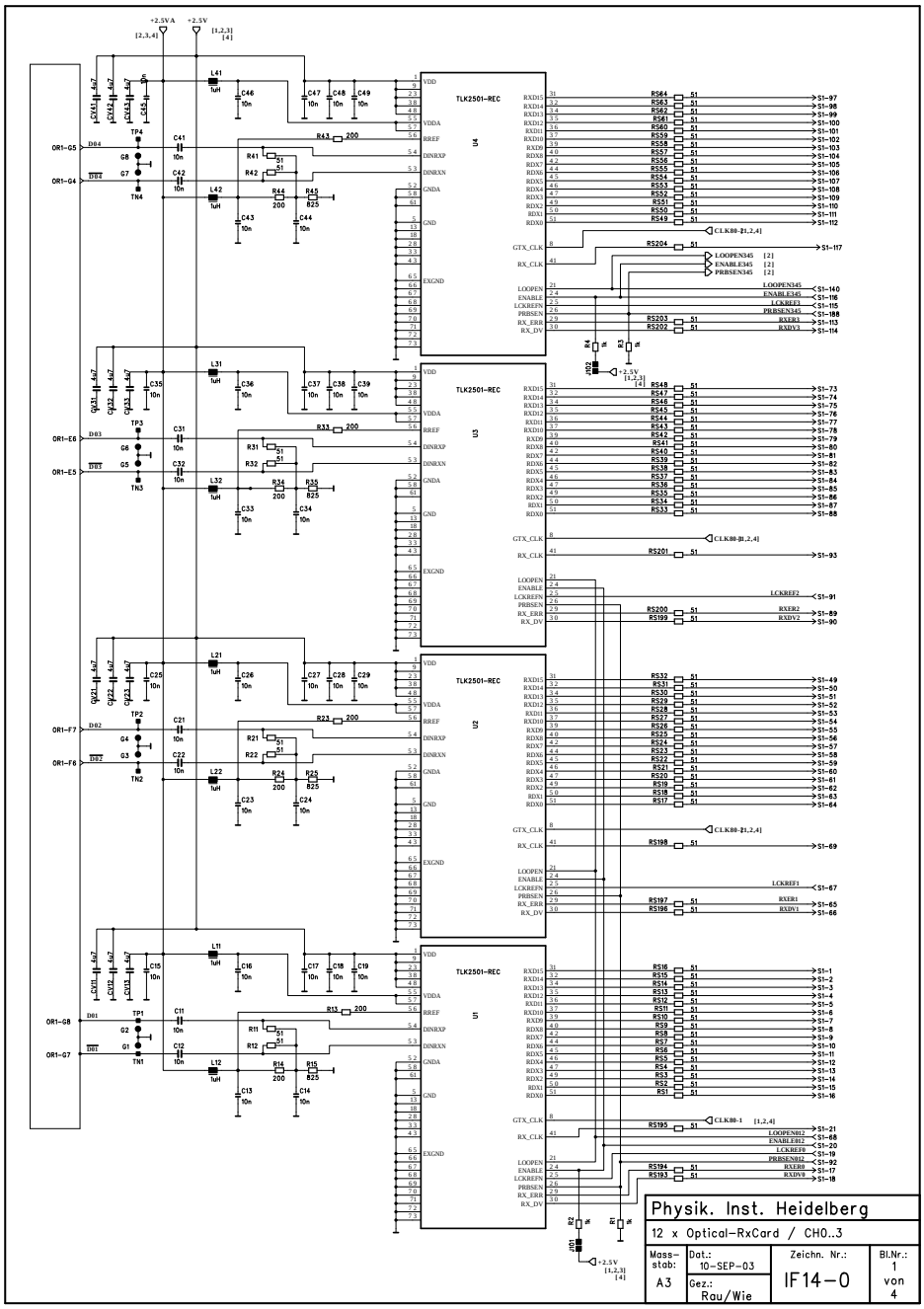

Figure 6: *Schematics 1/4*

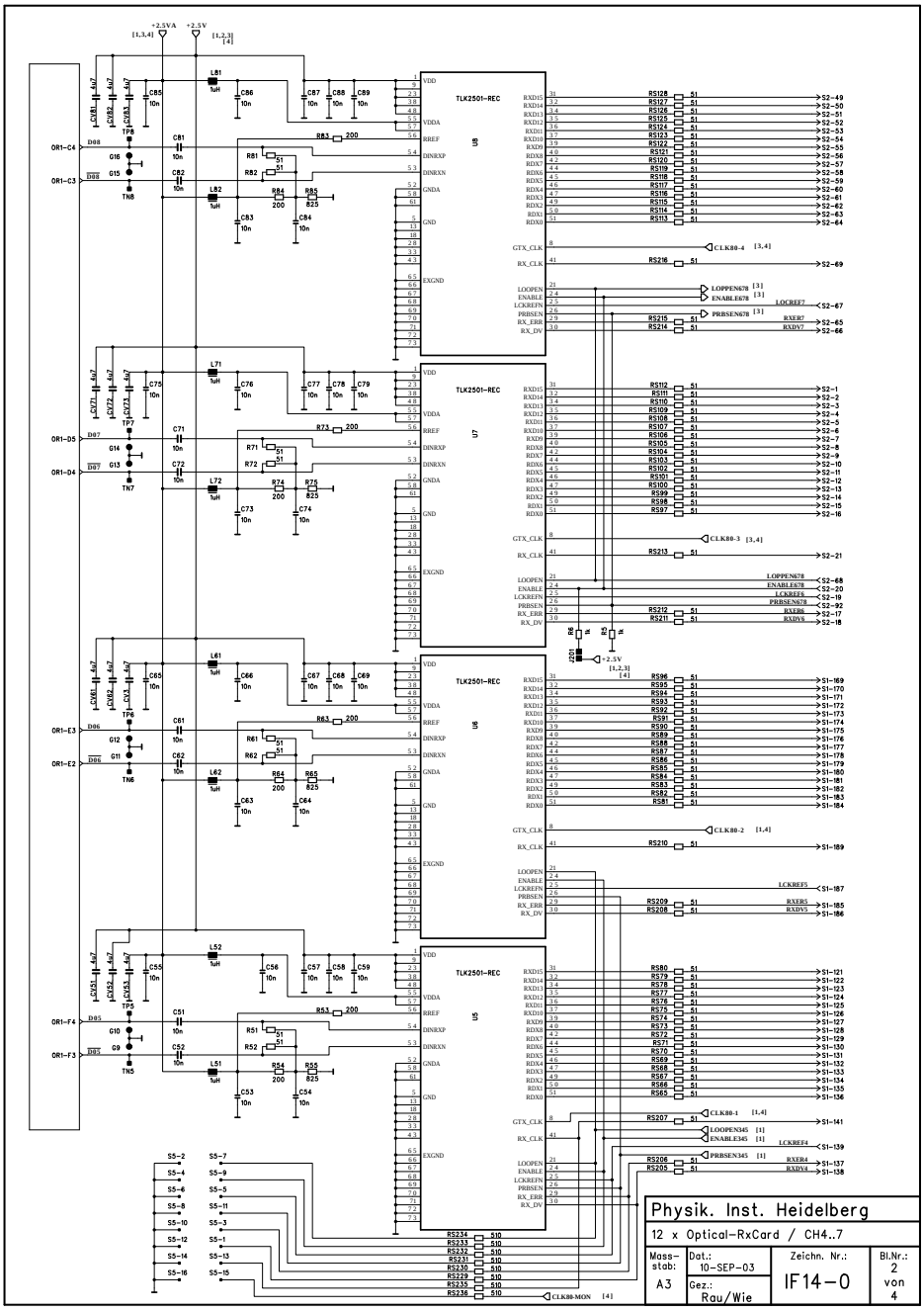

Figure 7: *Schematics 2/4*

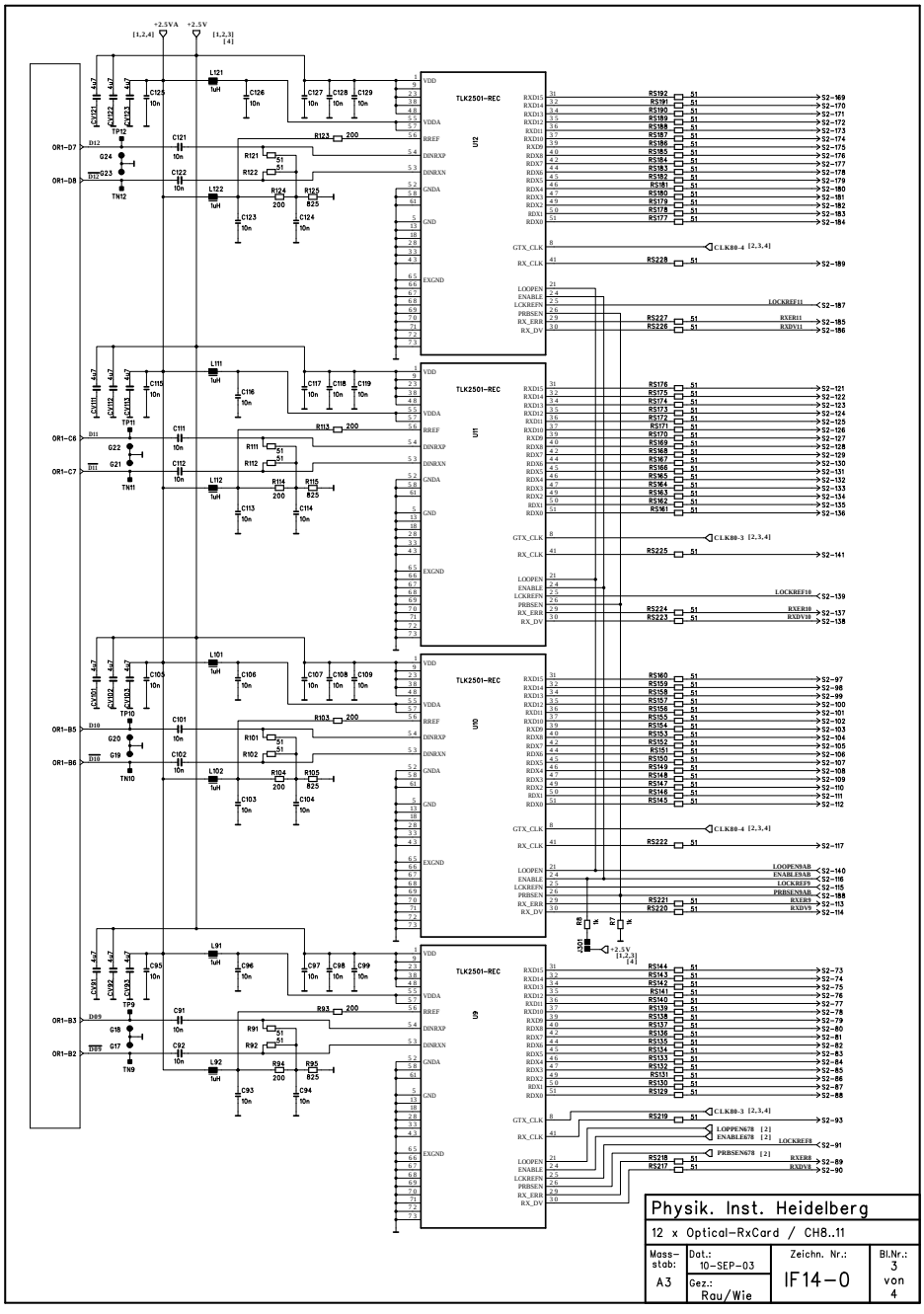

Figure 8: *Schematics 3/4*

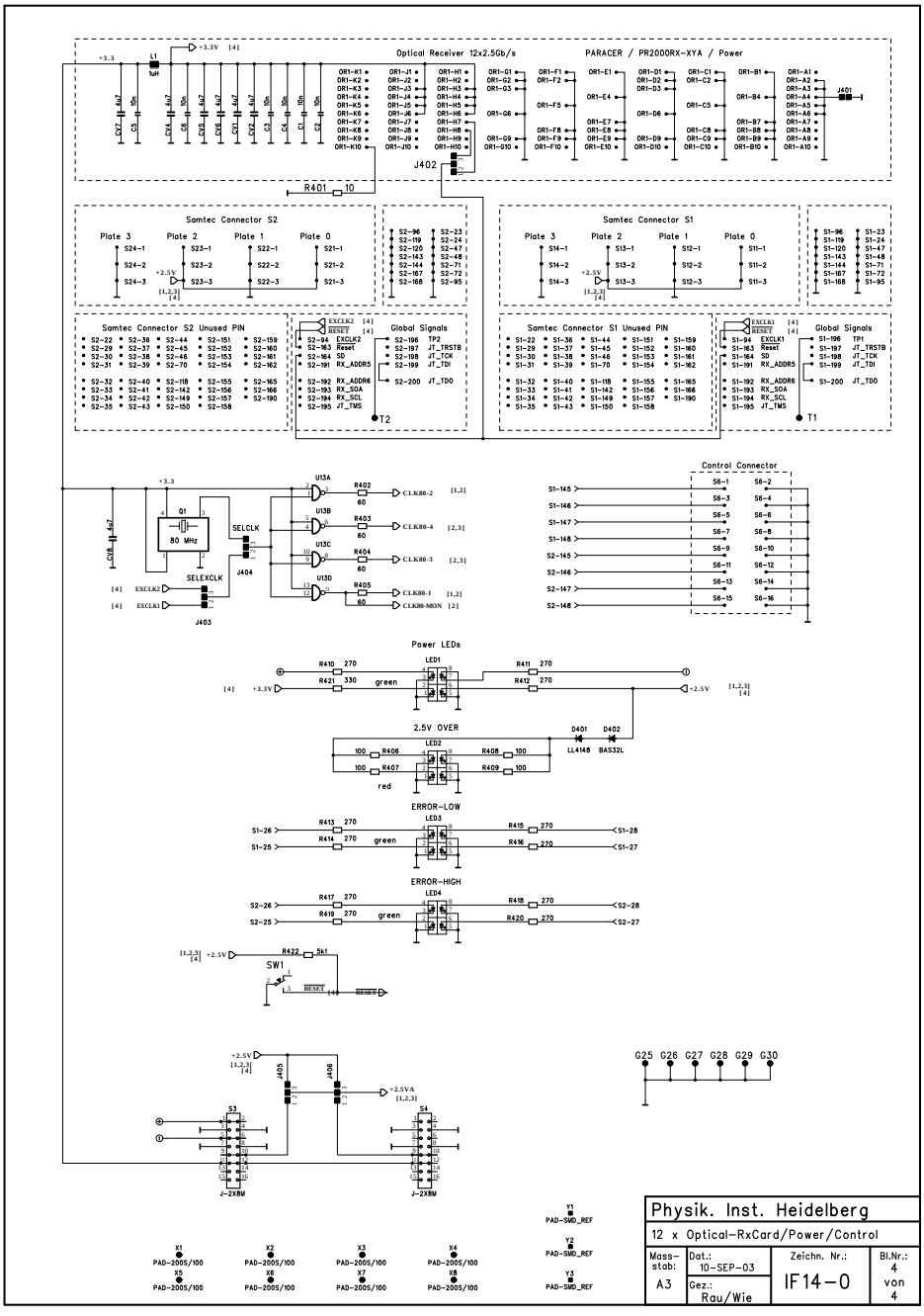

Figure 9: *Schematics 4/4*

C Layout

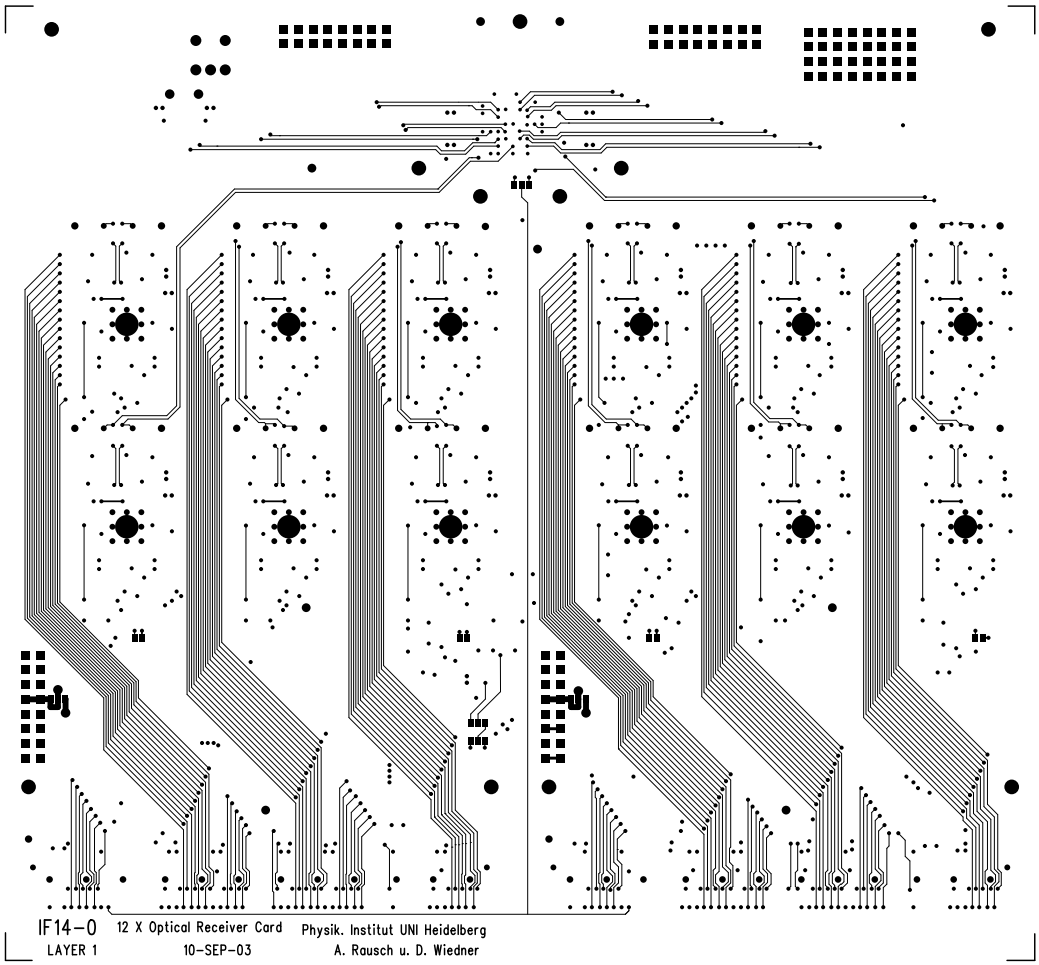

Figure 10: *Layout layer 1/8*

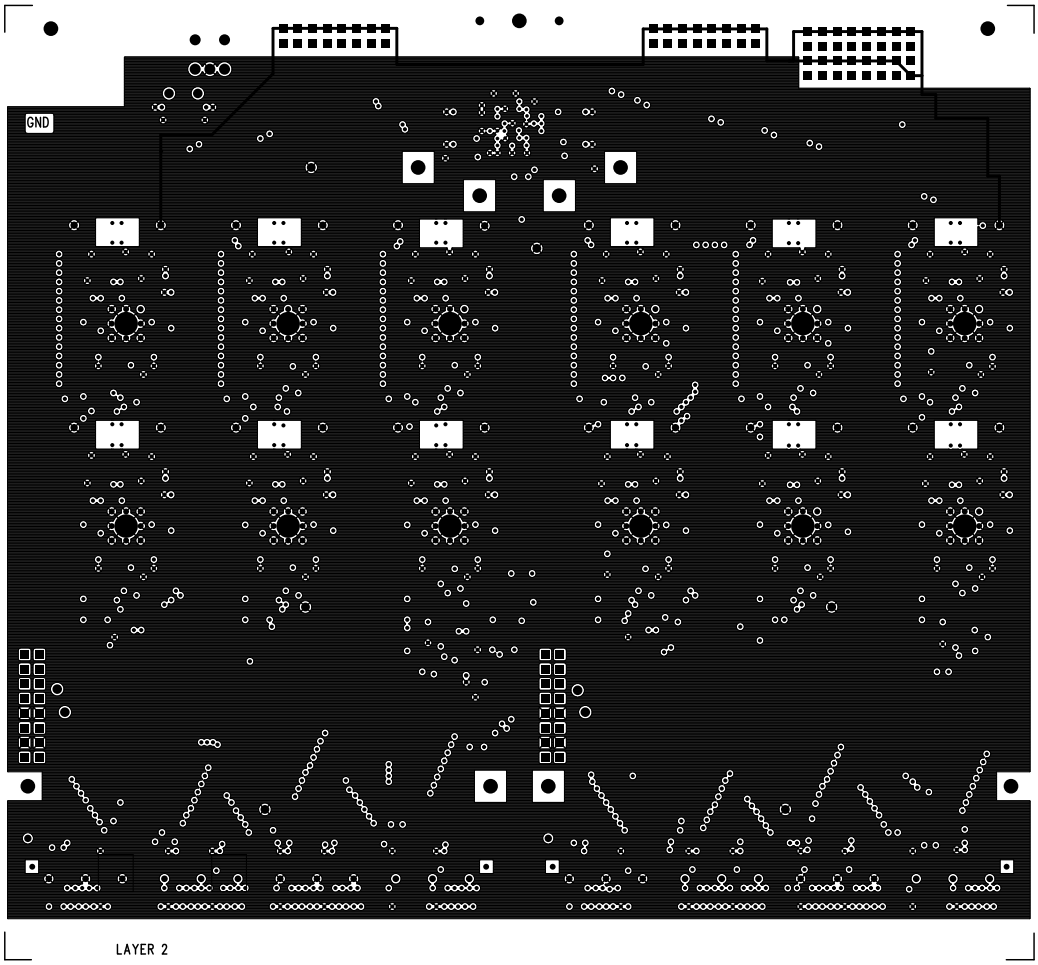

Figure 11: *Layout layer 2/8*

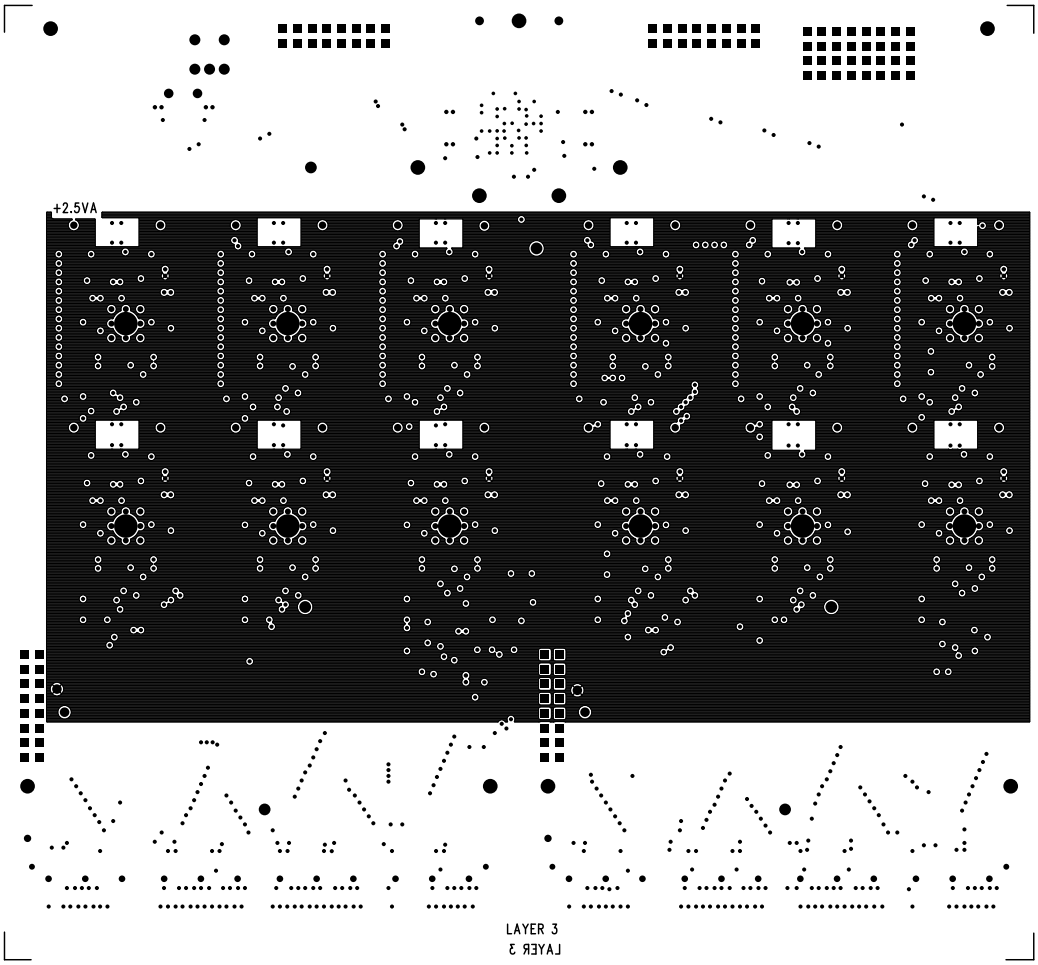

Figure 12: *Layout layer 3/8*

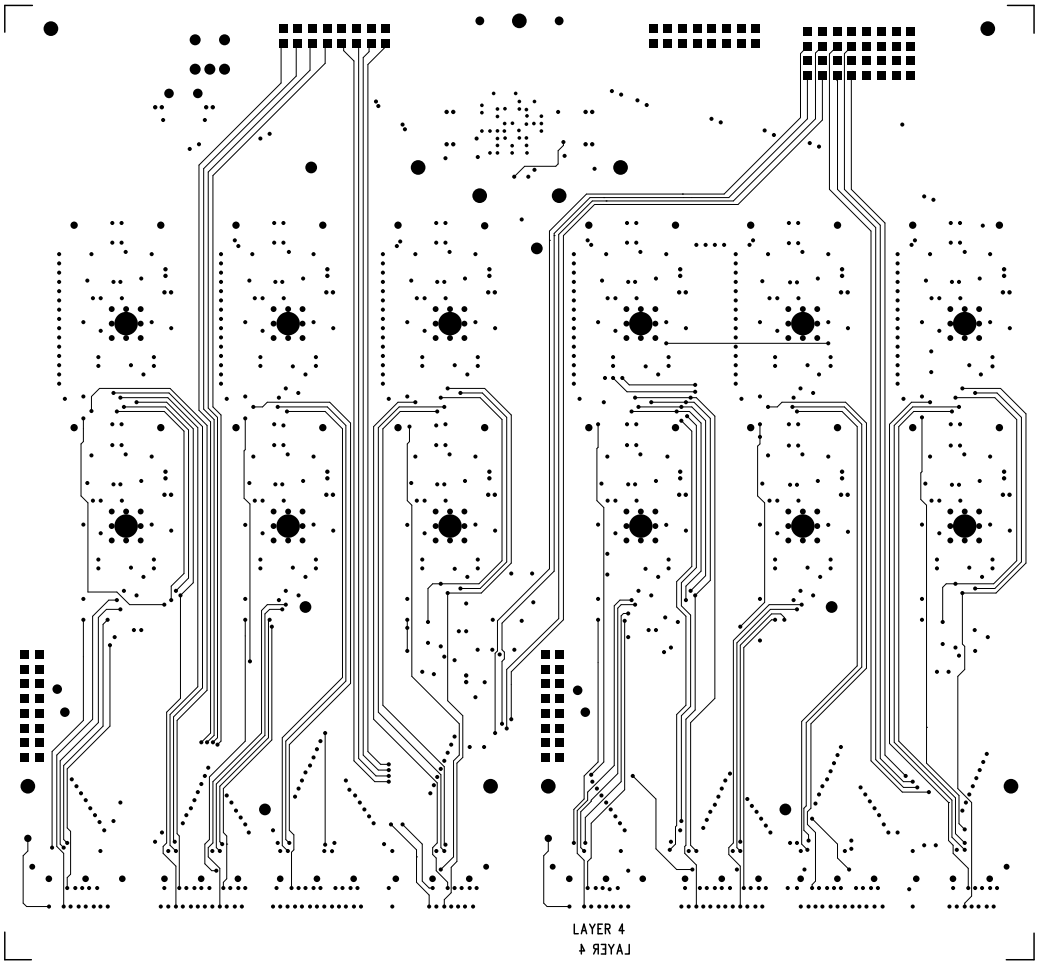

Figure 13: *Layout layer 4/8*

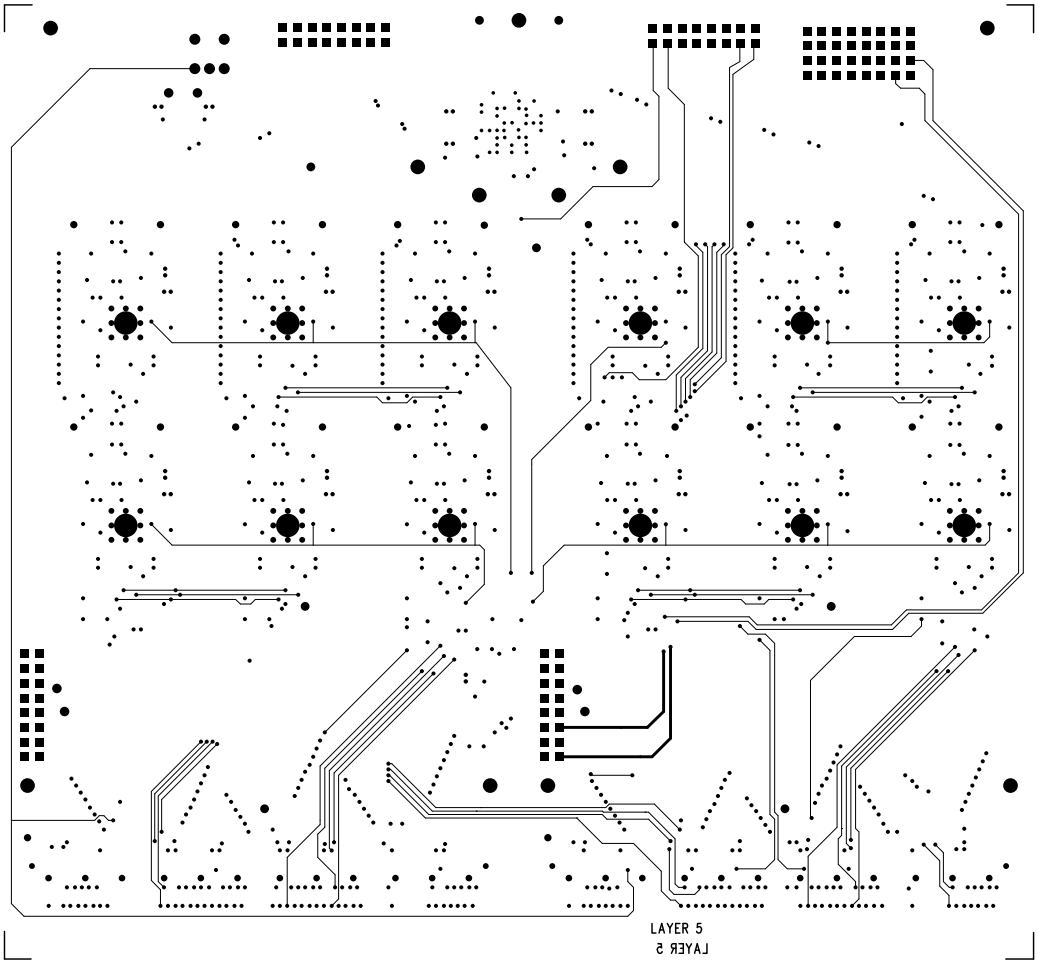

Figure 14: *Layout layer 5/8*

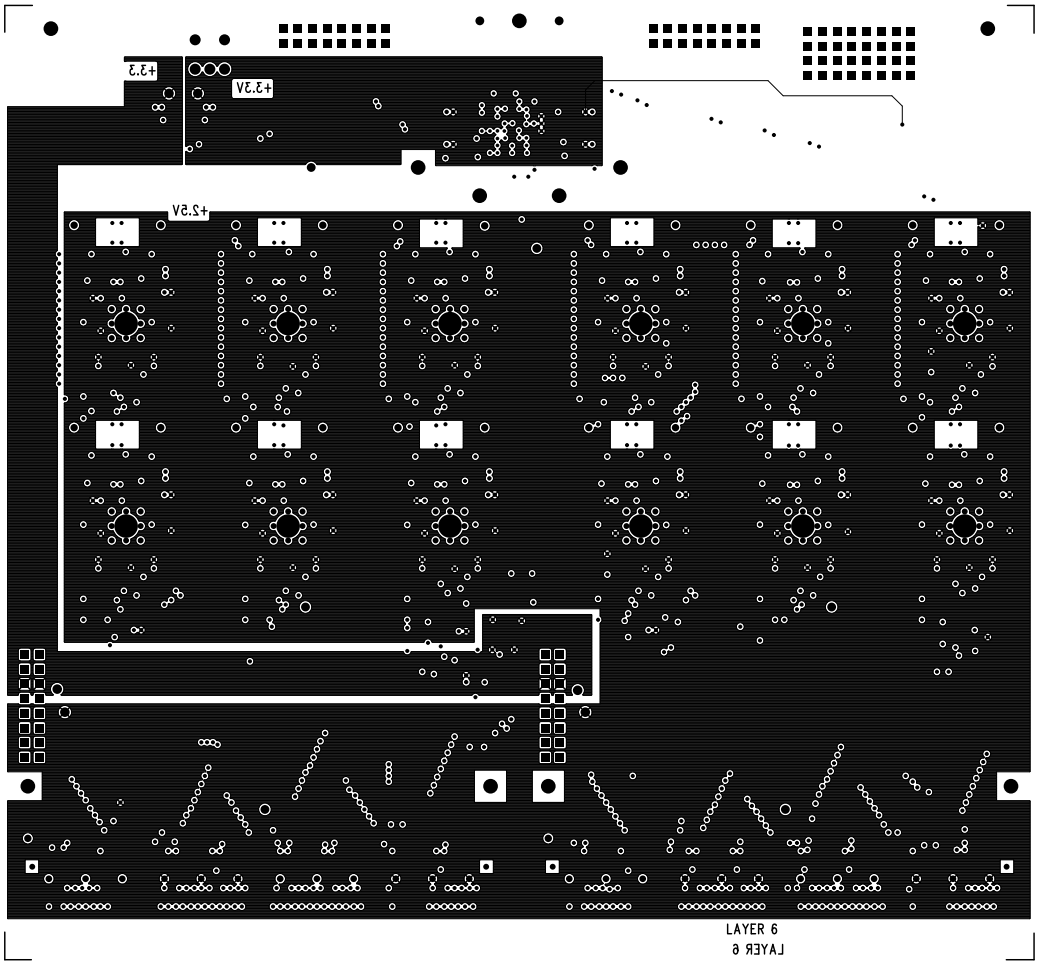

Figure 15: *Layout layer 6/8*

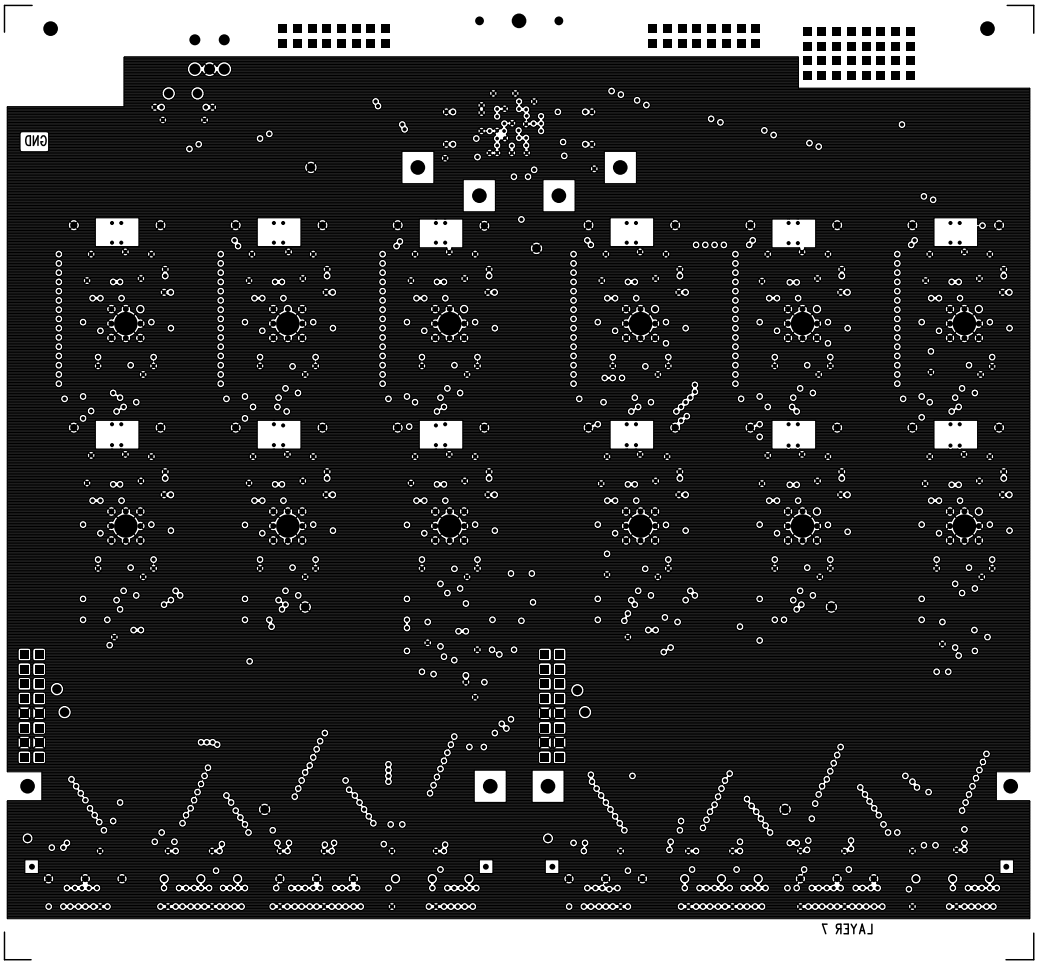

Figure 16: *Layout layer 7/8*

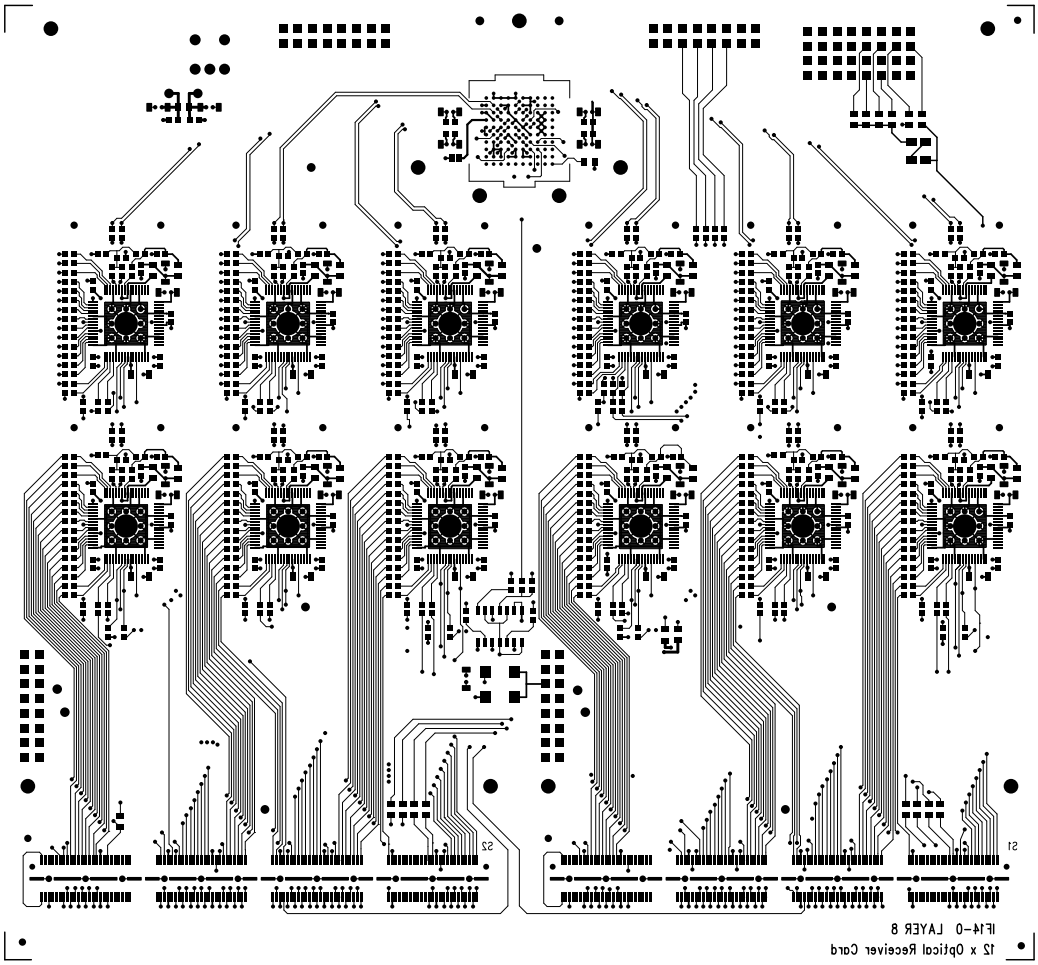

Figure 17: *Layout layer 8/8*

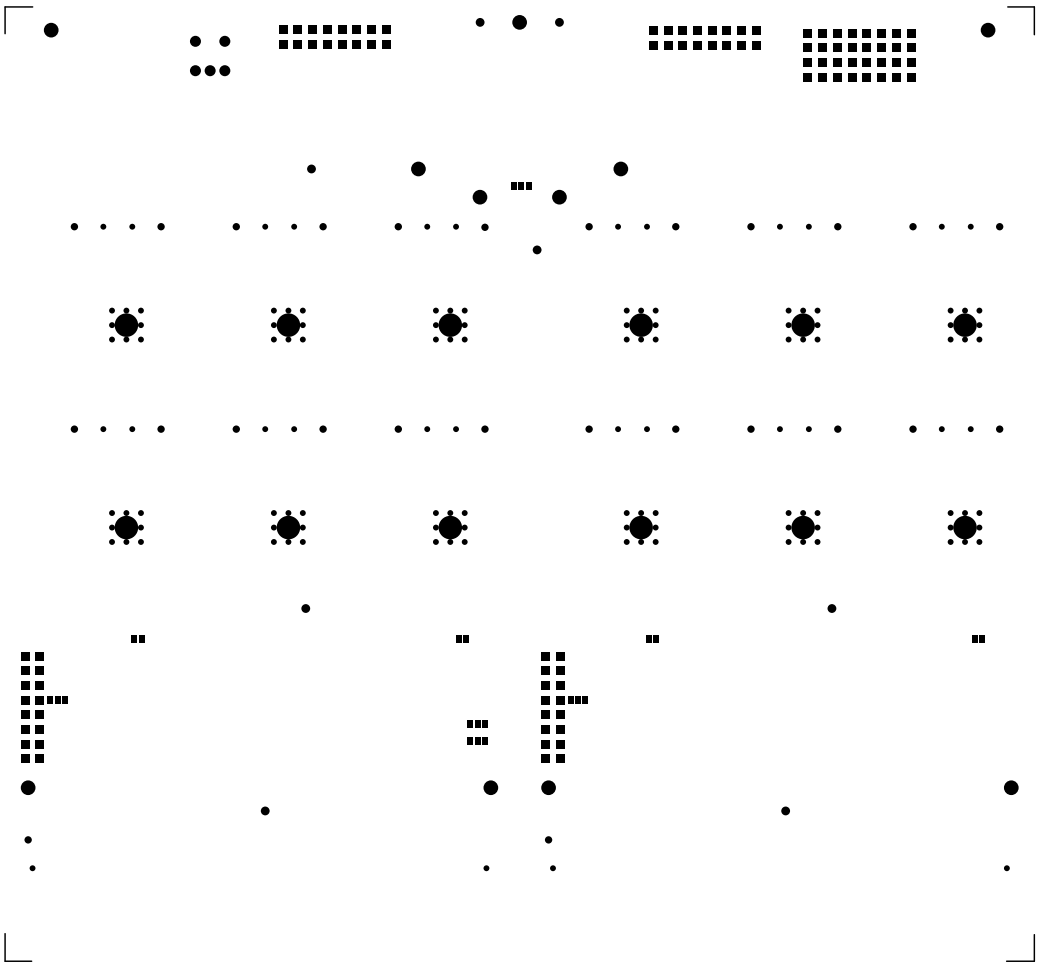

Figure 18: *Soldermask layer 1*

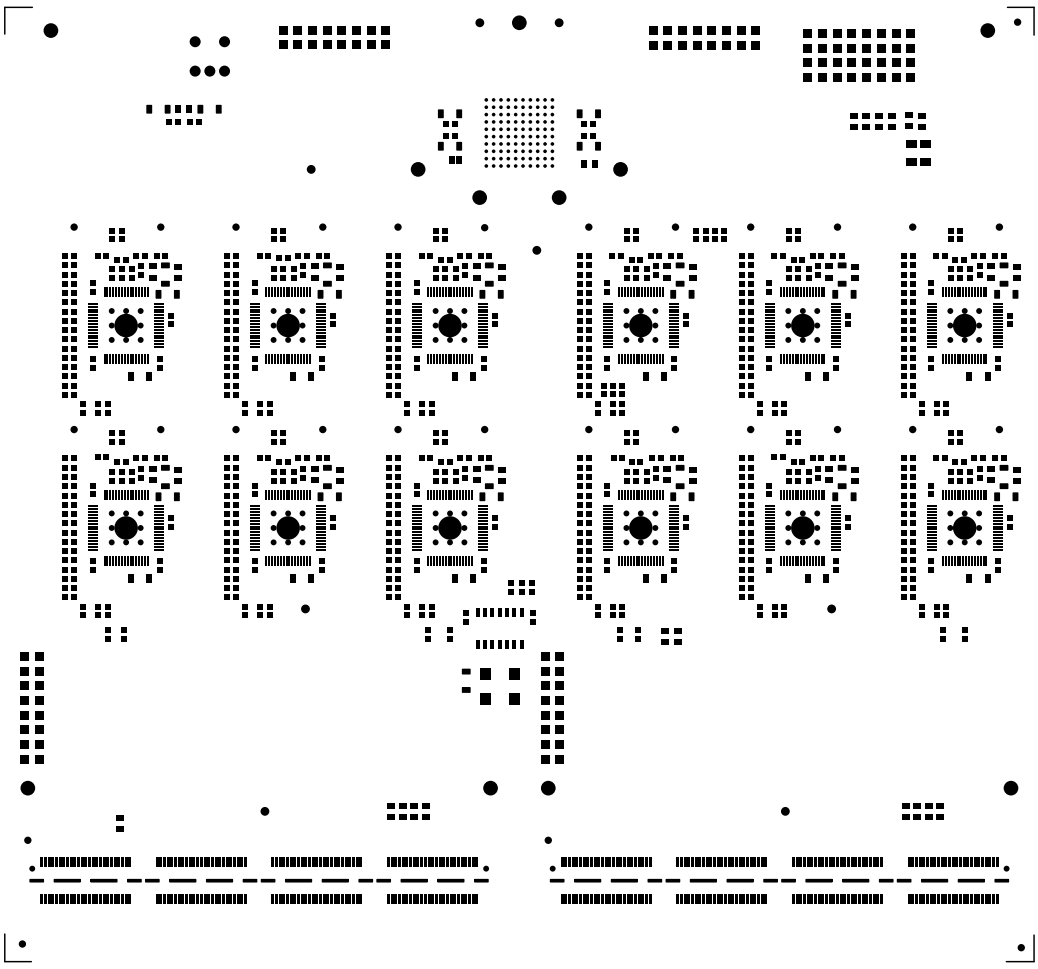

Figure 19: *Soldermask layer 8*

D Component placement specification

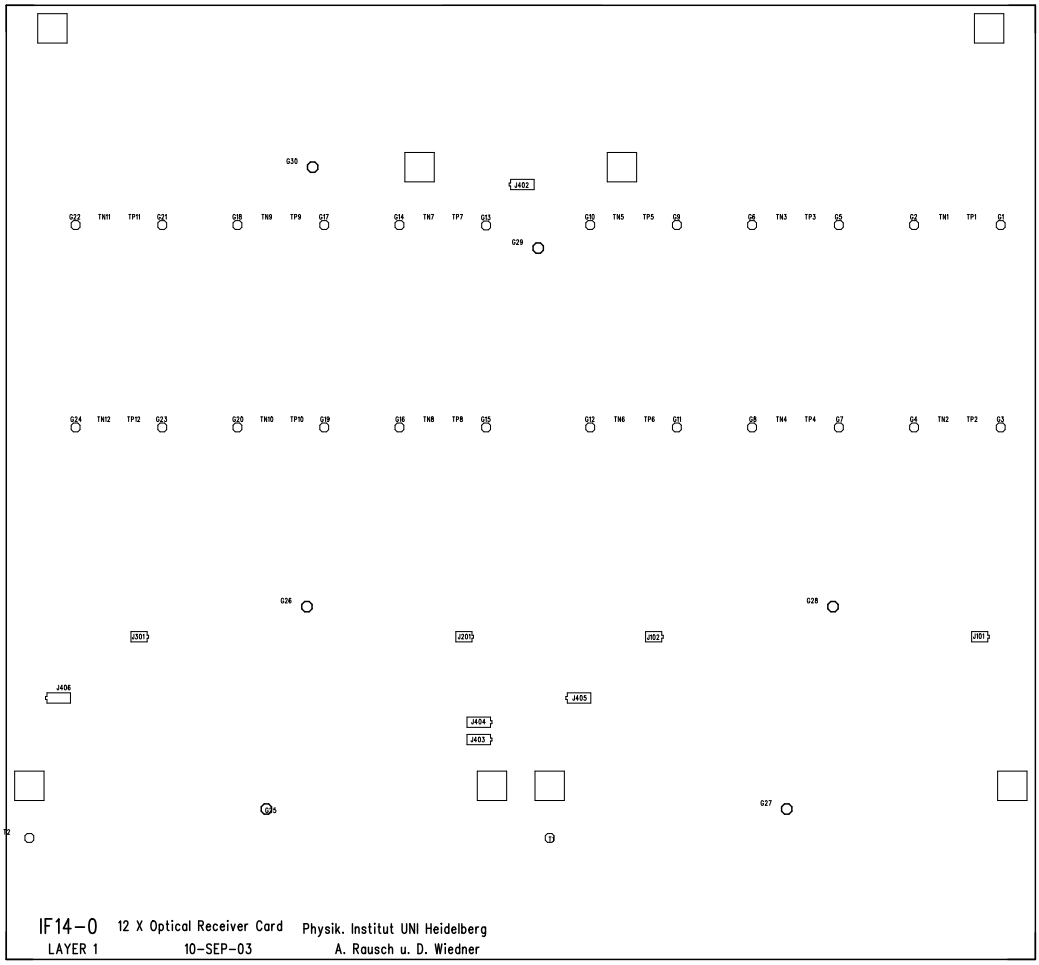

Figure 20: *Component placement specification top*

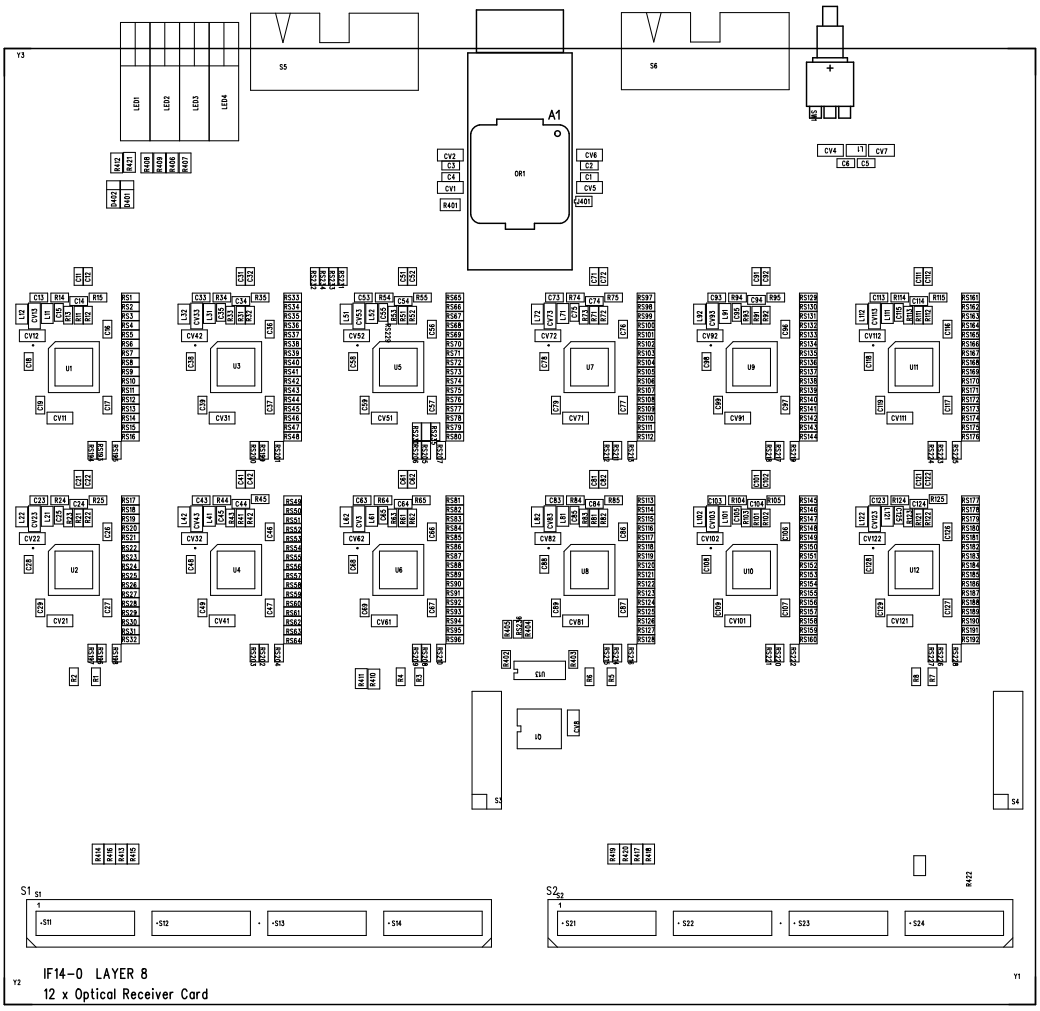

Figure 21: *Component placement specification bottom*

E Bill of materials

Table 21: Bill Of Materials 1/2

Qty:	Part-Nr.:	Part-Typ:	Val.:	Int.-Nr:	Decal:	Part-Description:
1	OR1	SNAP12-REC			SNAP12-REC	12-input Optical-Receiver PR2800
12	U1-12	TLK2501-REC			QFP10X10-64	Deserializer
1	Q1	Q-SG8002CA			Q-SG8002CA	Oscillator IQXO-71B 80 MHz
1	U13	74LCX00M			DIP14-SO	QUAD 2-INPUT POS-NAND GATE
4	LED1-4	LED-2X2			LED2X2	
1	D401	LL4148		4648	D-1206SMD	Diode 1N4148 in SMD 1206-package
1	D402	BAS32L		4225	D-1206SMD	Silicium SMD-Minimelf-Diode
2	S1-2	ST-200-QTS			ST-200-QTS	High Speed Connector QTS 200 pol. 0.635 mm
2	S3-4	J-2X8M			J-2X8M	2 row. Jumper 8 pins ea.
2	S5-6	ST-16-3MK			ST-16-3MK	16 pol Connector
1	SW1	SW-TASTERUM		4546	SW-TASTERUM	Reset Button
114	C1-6 C11-19 C21-29 C31-39 C41-49 C51-59 C61-69 C71-79 C81-89 C91-99 C101-109 C111-119 C121-129	CK-0603SMD	10n		CK0603SMD	SMD-Cap. l=1,6mm b=0,8mm
43	CV1-8 CV11-13 CV21-23 CV31-33 CV41-43 CV51-53 CV61-62 CV71-73 CV81-83 CV91-93 CV101-103 CV111-113 CV121-123	CK-1206SMD	4u7	4496, 4500, 4798..99,	CK1206SMD, CK1206SMD-A	SMD-Cap. l=3,2mm b=1,6mm

Table 22: Bill Of Materials 2/2

Qty:	Part-Nr.:	Part-Typ:	Val.:	Int.-Nr:	Decal:	Part-Description:
25	L1 L11-12 L21-22 L31-32 L41-42 L51-52 L61-62 L71-72 L81-82 L91-92 L101-102 L111-112 L121-122	IND-0805SMD	1uH		CK0805SMD	SMD-Bead l=4,4mm; b=2,7mm
8	R1-8	R-0603RAU	1k		CK0603SMD	SMD-Resistor
252	R11-12 R21-22 R31-32 R41-42 R51-52 R61-62 R71-72 R81-82 R91-92 R101-102 R111-112 R121-122 RS1-228	R-0603RAU	51		CK0603SMD	SMD-Resistor
24	R13-14 R23-24 R33-34 R43-44 R53-54 R63-64 R73-74 R83-84 R93-94 R103-104 R113-114 R123-124	R-0603RAU	200		CK0603SMD	SMD-Resistor
12	R15 R25 R35 R45 R55 R65 R55 R65 R75 R85 R95 R105 R115 R125	R-0603RAU	825		CK0603SMD	SMD-Resistor
4	R402-405	R-0603RAU	60		CK0603SMD	SMD-Resistor
8	RS229-236	R-0603RAU	510		CK0603SMD	SMD-Resistor
1	R401	R-0805RAU	10	4487	CK0805SMD	SMD-Resistor
4	R406-409	R-0805RAU	100	4487	CK0805SMD	SMD-Resistor
11	R410-420	R-0805RAU	270	4487	CK0805SMD	SMD-Resistor
1	R421	R-0805RAU	330	4487	CK0805SMD	SMD-Resistor
1	R422	R-0805RAU	5k1	4487	CK0805SMD	SMD-Resistor

F Prices

Table 23 lists the prices of the major components for the O-RxCard. The prices are based on offers for the amount in brackets, the price for prototype quantities (5 pc.) is around 850 USD for the O-RxCard with all components.

Table 23: Prices for the components of the o-RxCard

Component	Vendor	Product Name	Cost [min. order]	Quantity
Otical Receiver	Stratos Lightwave	Paracer 2800 22RM	295 USD [200]	1
Deserializer	Texas Instruments	TLK2501	12 USD [36]	12
Quartz	Farnell	QXO-71B 424-6032	4.86 Euro [100]	1
High Speed Connectors	Samtec	QTS-100-03-L-D-A	17.27 Euro [4]	2
Power Connector	Farnell	M20 Socket 2x8 512-280	1.20 [10]	2
Clock Amplifier	Farnell	74LCX00M 111-867	0.30 Euro[100]	1
Rs, Cs, Ls	different		0.06 USD [2000]	600
Board	Haefele	8 layer board	<50 USD [50]	1
Mounting	QPRINT	SMD and BGA, one side	<30 USD[50]	1
Sum			<600 USD [200]	1

G Adapter Board

In order to easily access all signals that run from the O-RxCard to the TELL1 motherboard or vice versa, an adapter board has been designed. It has one high speed Samtec QSS-100-01-L-D-A connector to receive all 80 MHz digital data from 6 TLK 2501 deserializers, plus control signals. The signals are fanned out to 40-pin connectors with 1/10 inch pitch, one for each TLK deserializer (table 24-24) and one for LEDs, front panel connector signals, reset and SD. The TLK control signals Enable, LoopEnable, PrbsEn and LckRef are joined for three TLKs and controlled by jumpers on the adapter board. The adapter board has a LV power connector and input pads for 2.5 V, 2.5 V analog and 3.3 V. It is possible to connect the analog 2.5 V to the 2.5 V digital. The adapter board is a cheap 2 layer board, using only passive components. Figure 22 shows the schematics of the adapter board, figure 23 and 24 show the placement specifications of the adapter board, figures 25 to 27 show the layout.

Table 24: Connectivity adapter board 1/4, Connector J1 for Data 0 and connector J2 for Data 1

connector	pin	connectivity O-RxCard	description	connector	pin	connectivity O-RxCard	description
J1 (Data 0)	1	S1-1	Data0(15)	J2 (Data 1)	1	S1-49	Data1(15)
	2	GND	GND		2	GND	GND
	3	S1-2	Data0(14)		3	S1-50	Data1(14)
	4	GND	GND		4	GND	GND
	5	S1-3	Data0(13)		5	S1-51	Data1(13)
	6	GND	GND		6	GND	GND
	7	S1-4	Data0(12)		7	S1-52	Data1(12)
	8	GND	GND		8	GND	GND
	9	S1-5	Data0(11)		9	S1-53	Data1(11)
	10	GND	GND		10	GND	GND
	11	S1-6	Data0(10)		11	S1-54	Data1(10)
	12	GND	GND		12	GND	GND
	13	S1-7	Data0(9)		13	S1-55	Data1(9)
	14	GND	GND		14	GND	GND
	15	S1-8	Data0(8)		15	S1-56	Data1(8)
	16	GND	GND		16	GND	GND
	17	S1-9	Data0(7)		17	S1-57	Data1(7)
	18	GND	GND		18	GND	GND
	19	S1-10	Data0(6)		19	S1-58	Data1(6)
	20	GND	GND		20	GND	GND
	21	S1-11	Data0(5)		21	S1-59	Data1(5)
	22	GND	GND		22	GND	GND
	23	S1-12	Data0(4)		23	S1-60	Data1(4)
	24	GND	GND		24	GND	GND
	25	S1-13	Data0(3)		25	S1-61	Data1(3)
	26	GND	GND		26	GND	GND
	27	S1-14	Data0(2)		27	S1-62	Data1(2)
	28	GND	GND		28	GND	GND
	29	S1-15	Data0(1)		29	S1-63	Data1(1)
	30	GND	GND		30	GND	GND
	31	S1-16	Data0(0)		31	S1-64	Data1(0)
	32	GND	GND		32	GND	GND
	33	S1-17	RXER0		33	S1-65	RXER1
	34	GND	GND		34	GND	GND
	35	S1-18	RXDV0		35	S1-66	RXDV1
	36	GND	GND		36	GND	GND
	37	S1-21	RXCLK0		37	S1-69	RXCLK1
	38	GND	GND		38	GND	GND
	39	N.C.	N.C.		39	N.C.	N.C.
	40	GND	GND		40	GND	GND

Table 25: Connectivity adapter board 2/4, Connector J3 for Data 2 and connector J4 for Data 3

connector	pin	connectivity O-RxCard	description	connector	pin	connectivity O-RxCard	description
J3 (Data 0)	1	S1-73	Data2(15)	J4 (Data 1)	1	S1-97	Data3(15)
	2	GND	GND		2	GND	GND
	3	S1-74	Data2(14)		3	S1-98	Data3(14)
	4	GND	GND		4	GND	GND
	5	S1-75	Data2(13)		5	S1-99	Data3(13)
	6	GND	GND		6	GND	GND
	7	S1-76	Data2(12)		7	S1-100	Data3(12)
	8	GND	GND		8	GND	GND
	9	S1-77	Data2(11)		9	S1-101	Data3(11)
	10	GND	GND		10	GND	GND
	11	S1-78	Data2(10)		11	S1-102	Data3(10)
	12	GND	GND		12	GND	GND
	13	S1-79	Data2(9)		13	S1-103	Data3(9)
	14	GND	GND		14	GND	GND
	15	S1-80	Data2(8)		15	S1-104	Data3(8)
	16	GND	GND		16	GND	GND
	17	S1-81	Data2(7)		17	S1-105	Data3(7)
	18	GND	GND		18	GND	GND
	19	S1-82	Data2(6)		19	S1-106	Data3(6)
	20	GND	GND		20	GND	GND
	21	S1-83	Data2(5)		21	S1-107	Data3(5)
	22	GND	GND		22	GND	GND
	23	S1-84	Data2(4)		23	S1-108	Data3(4)
	24	GND	GND		24	GND	GND
	25	S1-85	Data2(3)		25	S1-109	Data3(3)
	26	GND	GND		26	GND	GND
	27	S1-86	Data2(2)		27	S1-110	Data3(2)
	28	GND	GND		28	GND	GND
	29	S1-87	Data2(1)		29	S1-111	Data3(1)
	30	GND	GND		30	GND	GND
	31	S1-88	Data2(0)		31	S1-112	Data3(0)
	32	GND	GND		32	GND	GND
	33	S1-89	RXER2		33	S1-113	RXER3
	34	GND	GND		34	GND	GND
	35	S1-90	RXDV2		35	S1-114	RXDV3
	36	GND	GND		36	GND	GND
	37	S1-93	RXCLK2		37	S1-117	RXCLK3
	38	GND	GND		38	GND	GND
	39	N.C.	N.C.		39	N.C.	N.C.
	40	GND	GND		40	GND	GND

Table 26: Connectivity adapter board 3/4, Connector J5 for Data 4 and connector J6 for Data 5

connector	pin	connectivity O-RxCard	description	connector	pin	connectivity O-RxCard	description
J5 (Data 4)	1	S1-121	Data4(15)	J6 (Data 5)	1	S1-169	Data5(15)
	2	GND	GND		2	GND	GND
	3	S1-122	Data4(14)		3	S1-170	Data5(14)
	4	GND	GND		4	GND	GND
	5	S1-123	Data4(13)		5	S1-171	Data5(13)
	6	GND	GND		6	GND	GND
	7	S1-124	Data4(12)		7	S1-172	Data5(12)
	8	GND	GND		8	GND	GND
	9	S1-125	Data4(11)		9	S1-173	Data5(11)
	10	GND	GND		10	GND	GND
	11	S1-126	Data4(10)		11	S1-174	Data5(10)
	12	GND	GND		12	GND	GND
	13	S1-127	Data4(9)		13	S1-175	Data5(9)
	14	GND	GND		14	GND	GND
	15	S1-128	Data4(8)		15	S1-176	Data5(8)
	16	GND	GND		16	GND	GND
	17	S1-129	Data4(7)		17	S1-177	Data5(7)
	18	GND	GND		18	GND	GND
	19	S1-130	Data4(6)		19	S1-178	Data5(6)
	20	GND	GND		20	GND	GND
	21	S1-131	Data4(5)		21	S1-179	Data5(5)
	22	GND	GND		22	GND	GND
	23	S1-132	Data4(4)		23	S1-180	Data5(4)
	24	GND	GND		24	GND	GND
	25	S1-133	Data4(3)		25	S1-181	Data5(3)
	26	GND	GND		26	GND	GND
	27	S1-134	Data4(2)		27	S1-182	Data5(2)
	28	GND	GND		28	GND	GND
	29	S1-135	Data4(1)		29	S1-183	Data5(1)
	30	GND	GND		30	GND	GND
	31	S1-136	Data4(0)		31	S1-184	Data5(0)
	32	GND	GND		32	GND	GND
	33	S1-137	RXER4		33	S1-185	RXER5
	34	GND	GND		34	GND	GND
	35	S1-138	RXDV4		35	S1-186	RXDV5
	36	GND	GND		36	GND	GND
	37	S1-141	RXCLK4		37	S1-189	RXCLK5
	38	GND	GND		38	GND	GND
	39	N.C.	N.C.		39	N.C.	N.C.
	40	GND	GND		40	GND	GND

Table 27: Connectivity adapter board 4/4, Connector J7 for LEDs, feed through signals (con), Reset, SD, jumpers T1-T8 for TLK2501 enable etc. and Pad1-6 for auxiliary signals

connector	pin	connectivity O-RxCard	description	connector	pin	connectivity O-RxCard	description
J2 (AUX)	1	S1-25	LED3-2	T1	1	+2.5 V	high
	2	+2.5 V	+2.5 V		2	S1-20	Enable012
	3	S1-26	LED3-4		3	GND	low
	4	+2.5 V	+2.5 V	T2	1	+2.5 V	+2.5 V
	5	S1-27	LED3-6		2	S1-68	LoopEn012
	6	+2.5 V	+2.5 V		3	GND	GND
	7	S1-28	LED3-8	T3	1	+2.5 V	+2.5 V
	8	+2.5 V	+2.5 V		2	S1-92	PrbsEn012
	9	S1-94	ExClk1		3	GND	GND
	10	GND	GND	T4	1	+2.5 V	+2.5 V
	11	S1-145	con1		2	S1-116	Enable345
	12	GND	GND		3	GND	GND
	13	S1-146	con3	T5	1	+2.5 V	+2.5 V
	14	GND	GND		2	S1-140	LoopEn345
	15	S1-147	con5		3	GND	GND
	16	GND	GND	T6	1	+2.5 V	+2.5 V
	17	S1-148	con7		2	S1-188	PrbsEn345
	18	GND	GND		3	GND	GND
	19	S1-163	Reset	T7	1	+2.5 V	+2.5 V
	20	GND	GND		2	S1-19, 67, 91	LckRef012
	21	S1-164	SD		3	GND	GND
	22	GND	GND	T8	1	+2.5 V	+2.5 V
	23	N.C.	N.C.		2	S1-115, 139, 187	LckRef345
	24	GND	GND		3	GND	GND
	25	N.C.	N.C.	J7	1	+2.5 V	+2.5 V
	26	GND	GND		2	S3-9	A2P5
	27	N.C.	N.C.		3	+2.5 VA	+2.5 VA
	28	GND	GND	Pad1	1	S1-157	aux
	29	N.C.	N.C.	Pad2	1	S1-158	aux
	30	GND	GND	Pad3	1	S1-159	aux
	31	N.C.	N.C.	Pad4	1	S1-160	aux
	32	GND	GND	Pad5	1	S1-161	aux
	33	N.C.	N.C.	Pad6	1	S1-162	aux
	34	GND	GND				
	35	S1-196	TP1				
	36	GND	GND				
	37	S1-199	TDI				
	38	GND	GND				
	39	S1-200	TDO				
	40	GND	GND				

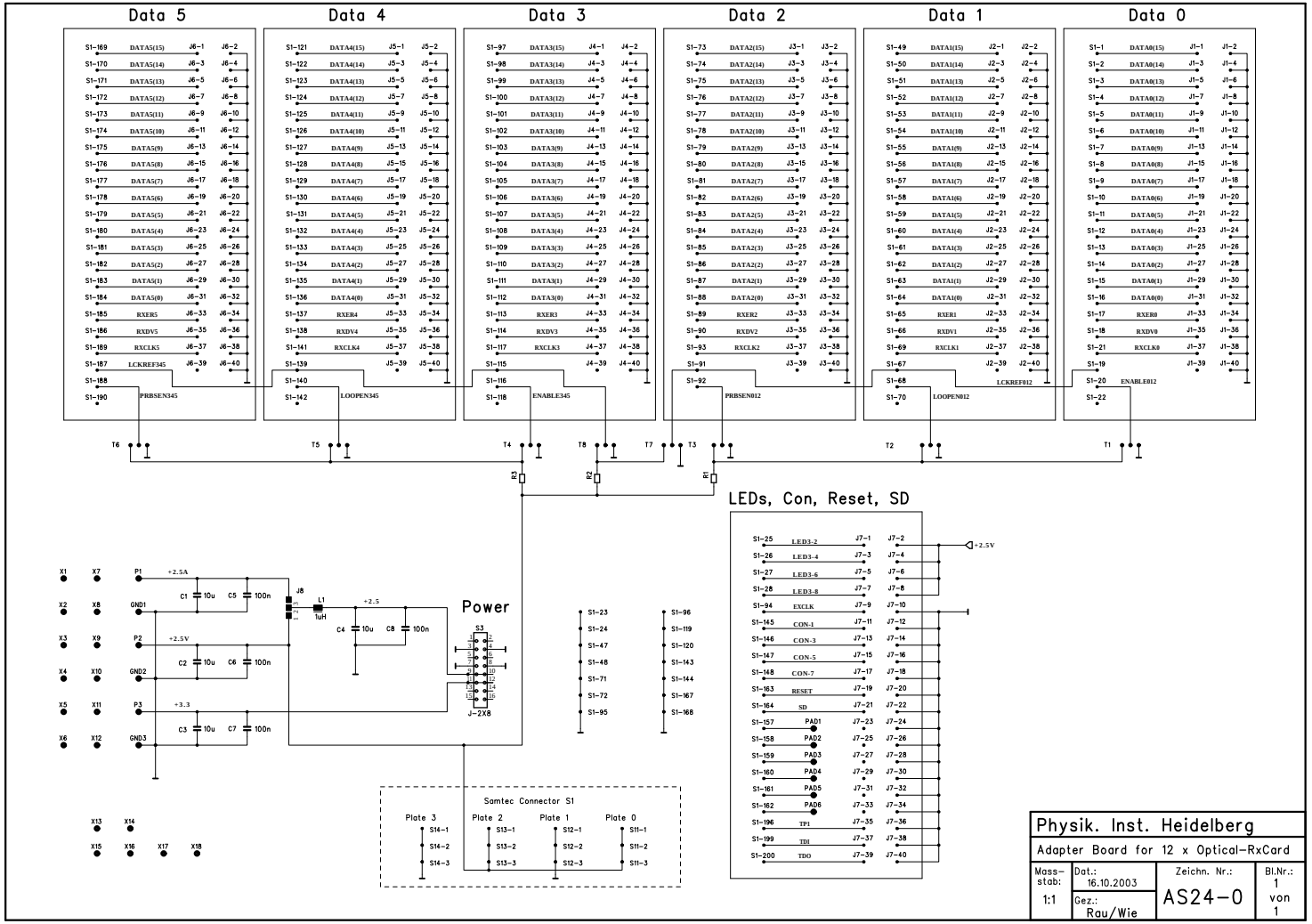

Figure 22: *Schematics Adapter Board*

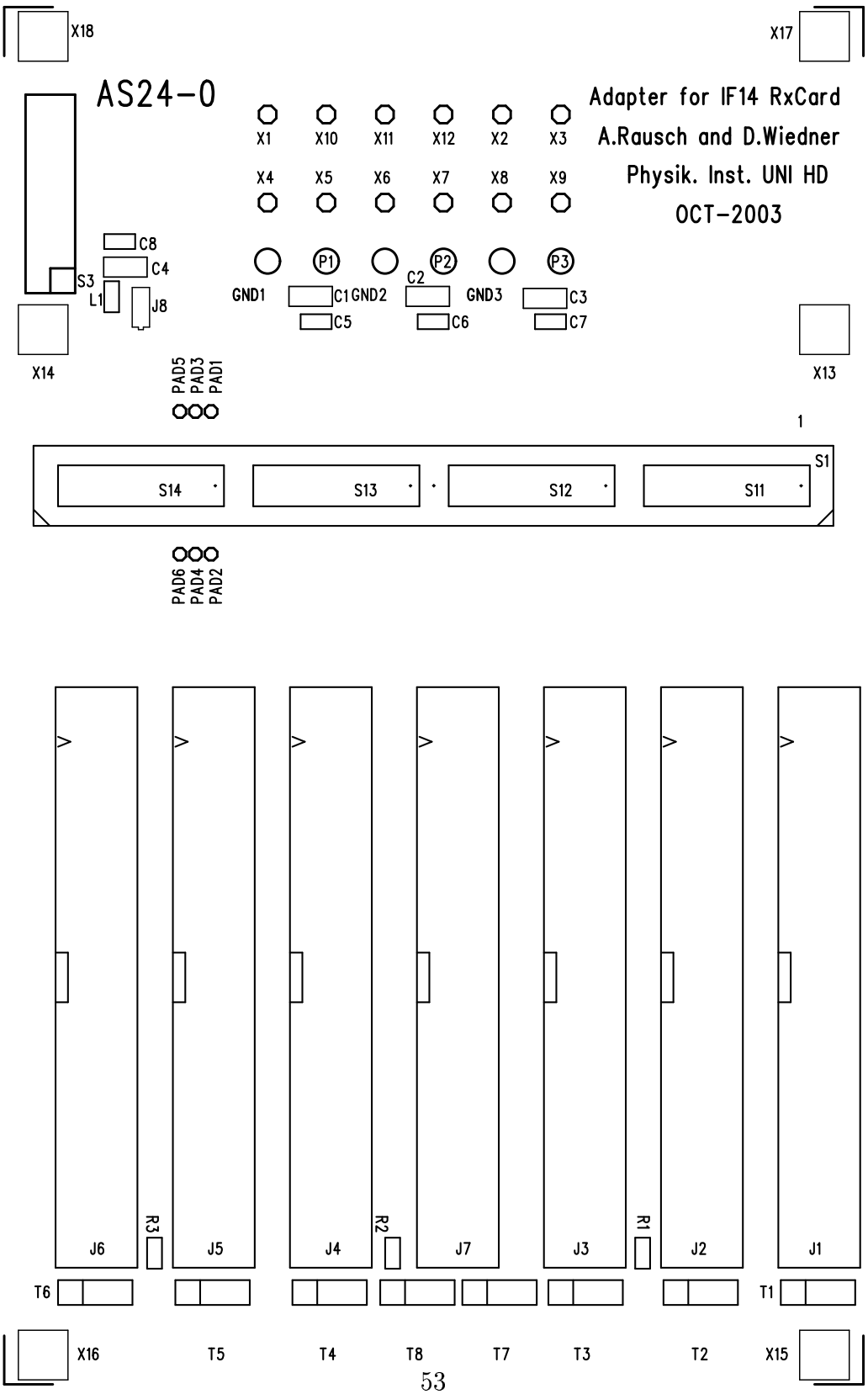

Figure 23: *Adapter Board component placement specification top*

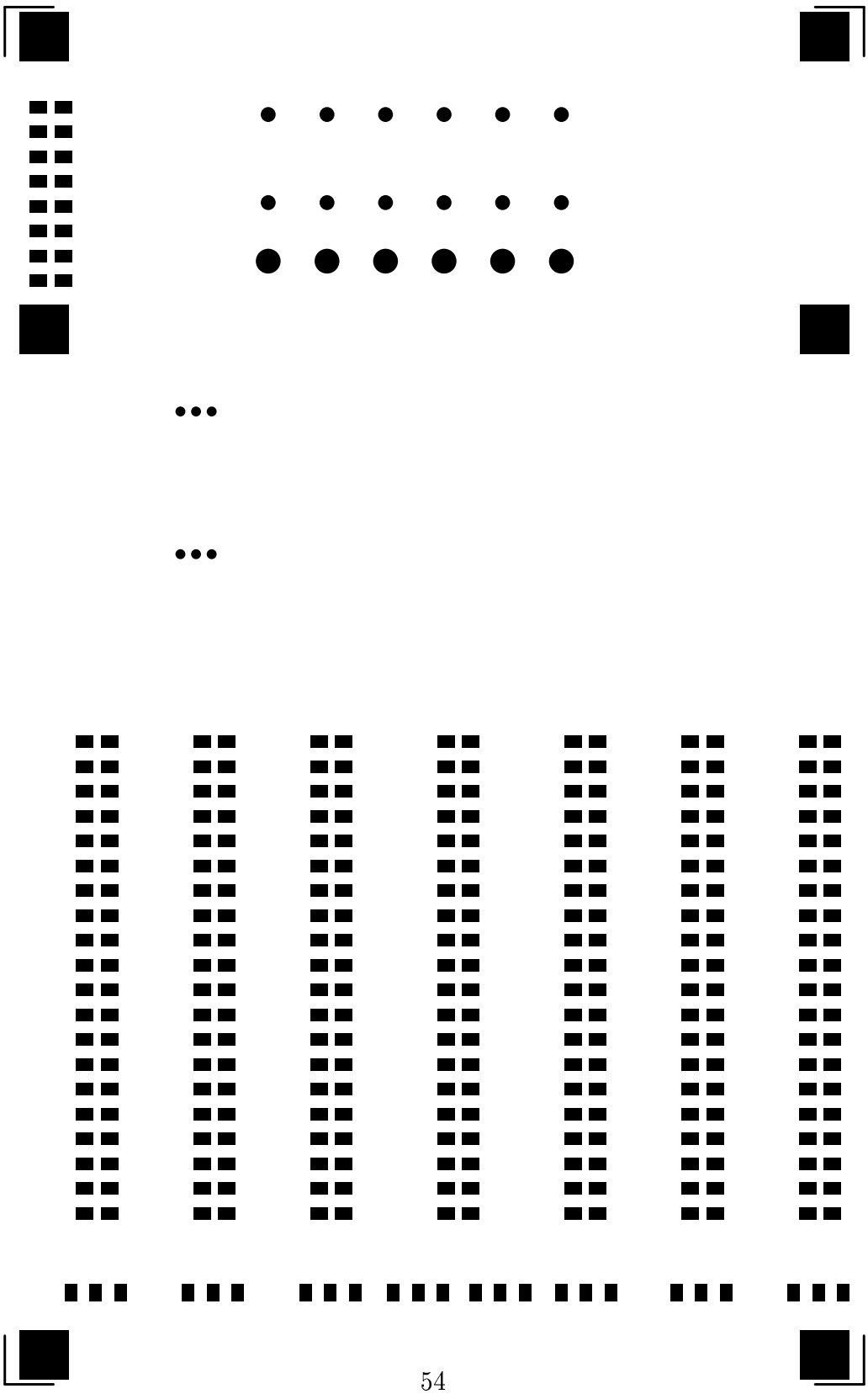

Figure 24: *Adapter Board component placement specification bottom*

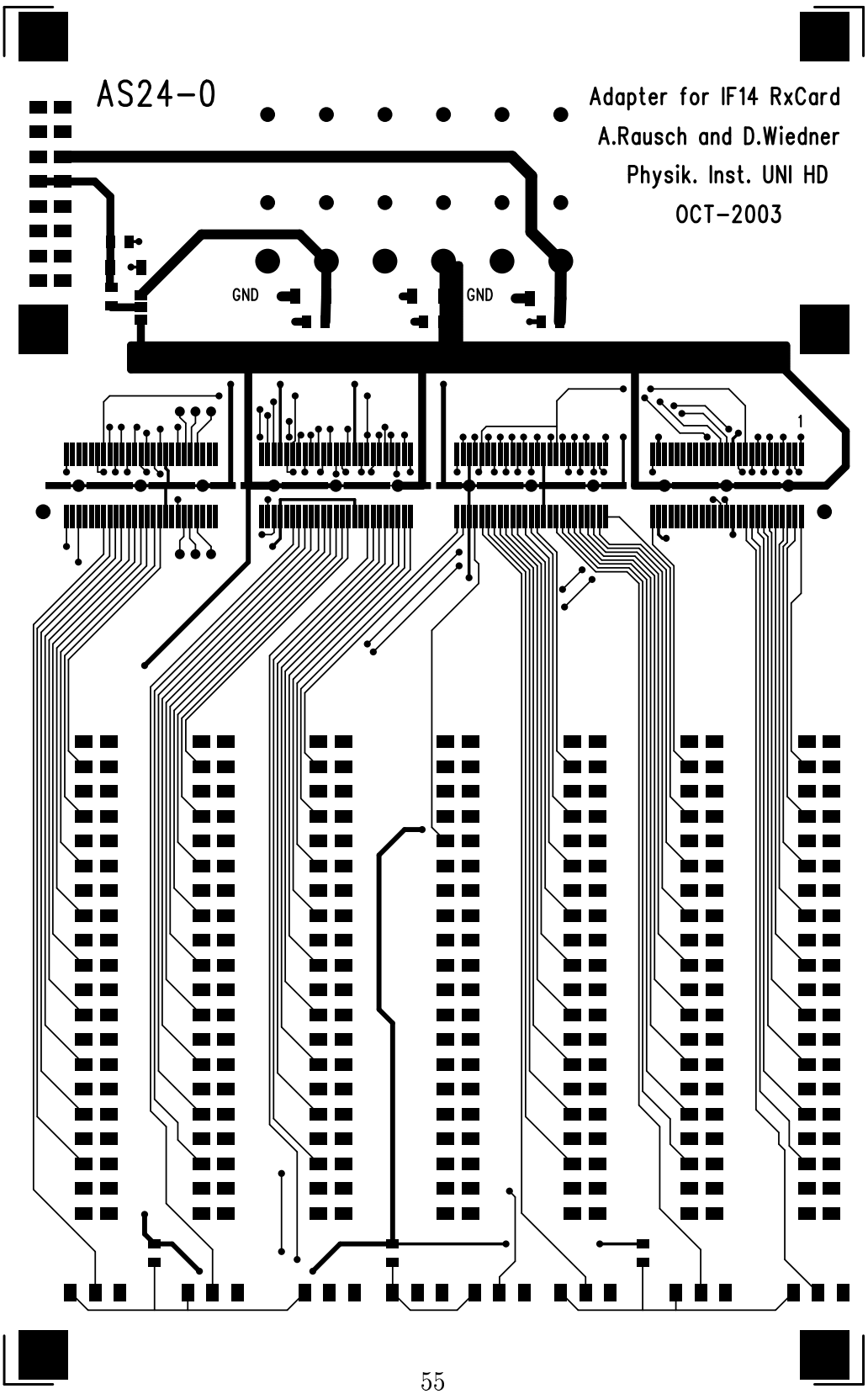

Figure 25: *Adapter Board layout top*

Figure 26: *Adapter Board layout bottom*

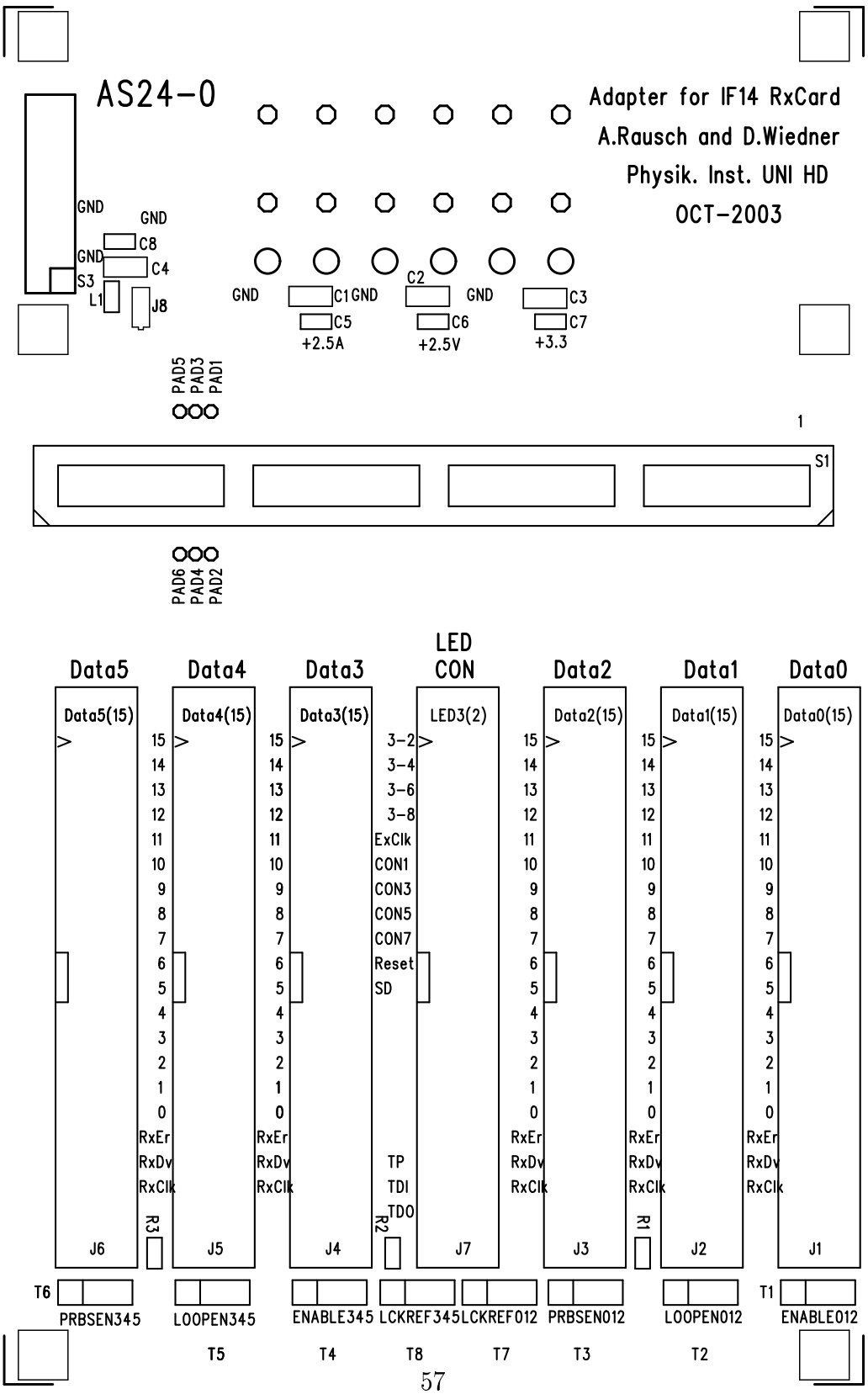

Figure 27: *Adapter Board Text*

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