LHCb Outer Tracker FE Electronics – Prototype of the ASDBLR Board

April 15, 2004

Abstract

The ASDBLR Board is an integral part of the LHCb Outer Tracker Front-End Electronics. The essential function of the board is to host two ASDBLR preamplifier-discriminator chips, which receive the small hit charges from the Outer Tracker anode wires and send their digital outputs to a Time-to-Digital Converter. The board design is described and the detailed schematics included in the Appendix.

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1 Introduction

This document describes a component of the FE Electronics of the Outer Tracker (OT) of the LHCb detector, namely the "ASDBLR Board". A general description of the Outer Tracker detector can be found in Ref. [1]. Essentially it consists of several arrays of drift tubes, arranged in a double-layer structure in sealed gas boxes ("modules"), as shown in Fig. 1. The detector volume is filled with the gas mixture of Ar/CO_2/CF_4. The straw cathodes (4.9 mm diameter) are kept at the ground potential, while the anode wires (25.4 μm diameter) at a positive potential of approximately 1600 V.

A minimum ionizing particle (m.i.p.) leaves a track of primary electron clusters when it traverses the straw volume. In the straw tube electrical field, these electrons "drift" towards the anode wire and, when approaching its close neighborhood, can be multiplied in an avalanche process. Then electroncs move further towards the anode wire at very high speed, while positive ions move away producing an electrical signal induction in all electrodes around: anode wire, straw tube cathode, ground plane and even neighboring straws! The resulting electrical signals has therefore two completely different components: a steep leading edge, resulting from the fast charge motion in the strong electric field close to the anode wire, and a slowly-sloping trailing edge, resulting from the slow motion of the positive ions towards the cathode straw tube in the course of a few hundreds nanoseconds.

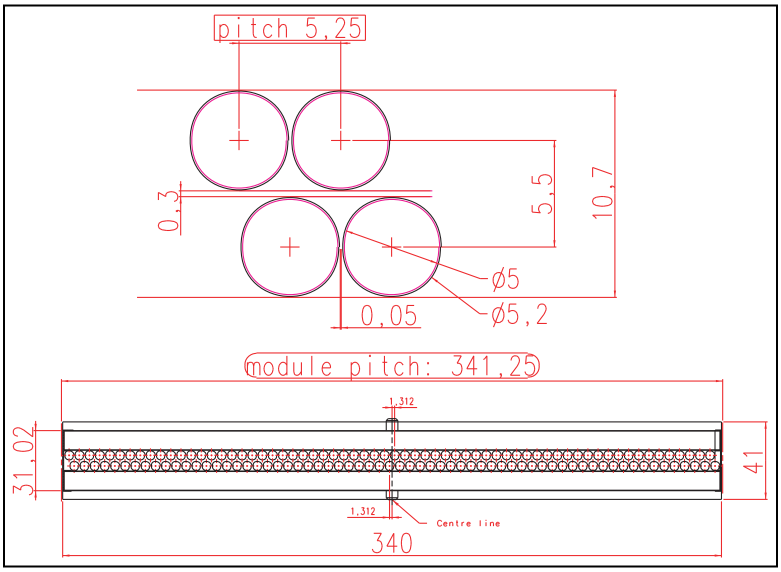

Figure 1: Cross section of a straw-tube module.

2 Front-End Electronics

Each OT module is equipped with a set of Front-End boards, grouped into compact mechanical constructions, referred to as "Front-End Electronics Box", shown schematically in Fig. 2.

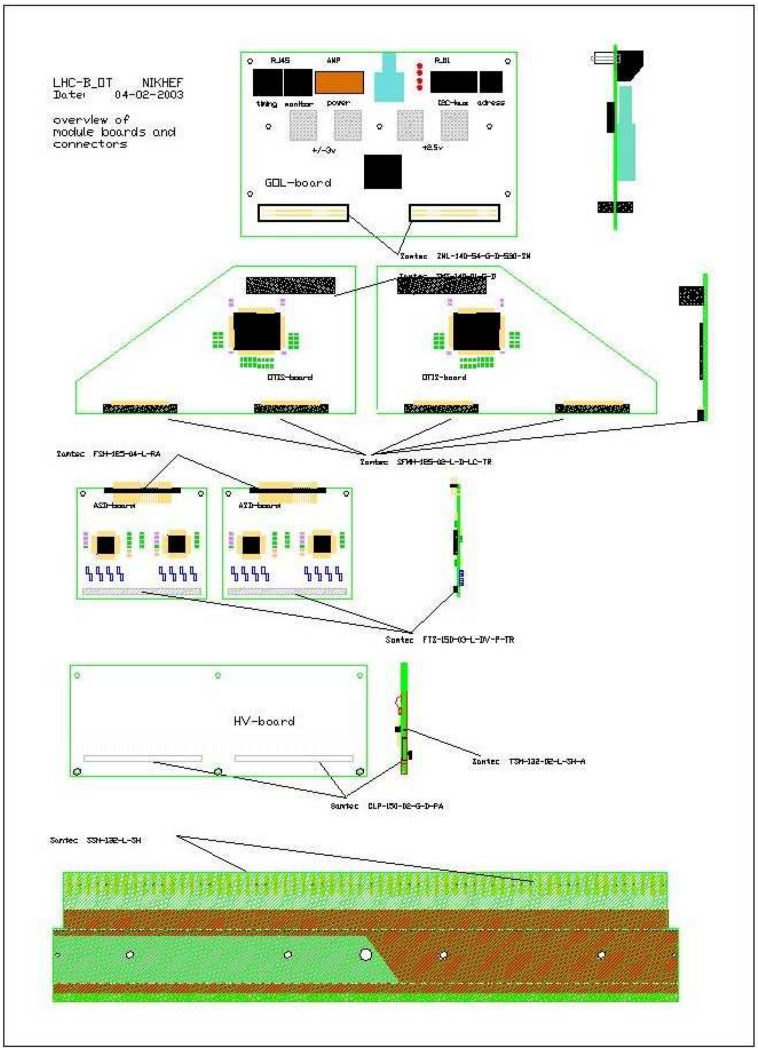

Figure 2: Overview of the OT Front-Electronics boards.

The Feed-Through Boards [2] are built in the straw-tube modules and provide contact pads to and from the cathode straws and the anode wires, while electrical components are kept outside of the sealed detector volume. Through mating SMD connectors, the anode wires are connected to the HV

Boards [3]. Here high voltage ($V_{HV} \simeq 1600\,V$) is applied to the anode wires, while the small hit charges are sent to the pre-amplifier inputs via 330 pF capacitors. From the HV Board, the hit charges are sent to the ASDBLR chips [4] located on the ASDBLR Board, where they are amplified, re-shaped to achieve a fast response, and finally discriminated against fixed thresholds. The resulting digital hit signals, that are the outputs of the ASDBLR Boards, are fed to the OTIS Board [5], where their occurrence in time with respect to the accelerator clock is measured.

3 ASDBLR Board Design

The essential function of the ASDBLR Board is to host two ASDBLR preamplifier-discriminator Application-Specific Integrated Circuits (ASICs). The choice of placing two ASDBLRs per board is a trade-off between two extreme scenarios: having eight ASDBLR's and two OTIS's on a single FE board, and having one single ASIC per board.

Complete studies of the operational properties of the ASDBLR chip for the readout of Outer Tracker straw tubes can be found in Refs. [7, 8]; the design principles of the ASDBLR Board are largely based on the results of those studies. The functional diagram of the ASDBLR Board is shown in Fig.3. The board is implemented as a 4-layer multilayer board; the detailed schematics in included in Appendix C.

3.1 The ASDBLR ASIC

The ASDBLR ASIC is an eight-channels amplifier-shaper-discriminator with baseline restoration designed for the read-out of the ATLAS Transition Radiation Tracker (TRT) [6]. The ASDBLR is a radiation-hard (7 MRad), high hit-rate (20 MHz with stable threshold, 100:1 dynamic range) amplifier. The basic chip functionalities are shown in Fig. 4. The current inputs are amplified, passed to a fast (25 ns) shaping stage to perform the slow-ions tail cancellation, then through a non-linear differentiation circuit called BaseLine-Restorer (BLR) to break the path from the shaper to the comparator and prevent that DC offsets or low-frequency noise can reach the comparator stage, and finally passed through two ("low" and "high") comparators. The digital comparator outputs are summed as current steps to form a differential ternary output with sharp turn-on (1 ns risetime).

A detailed description of the chip design, construction and performance can be found in Ref. [4]. The ASIC consists of eight identical channels on 340 μm pitch, implemented in radiation tolerant 0.8 μm BiCMOS Technology

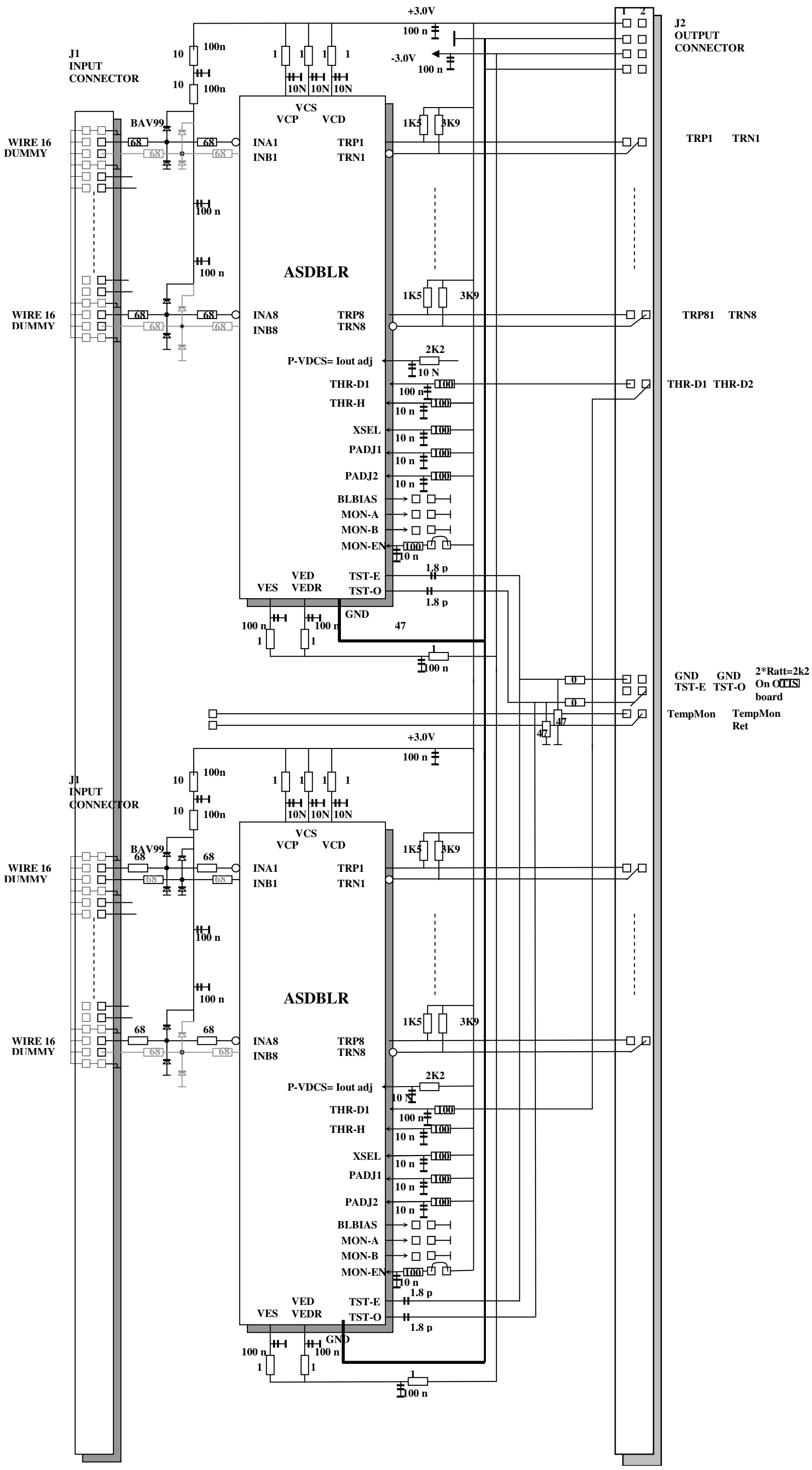

Figure 3: Functional Diagram of the ASDBLR Board.

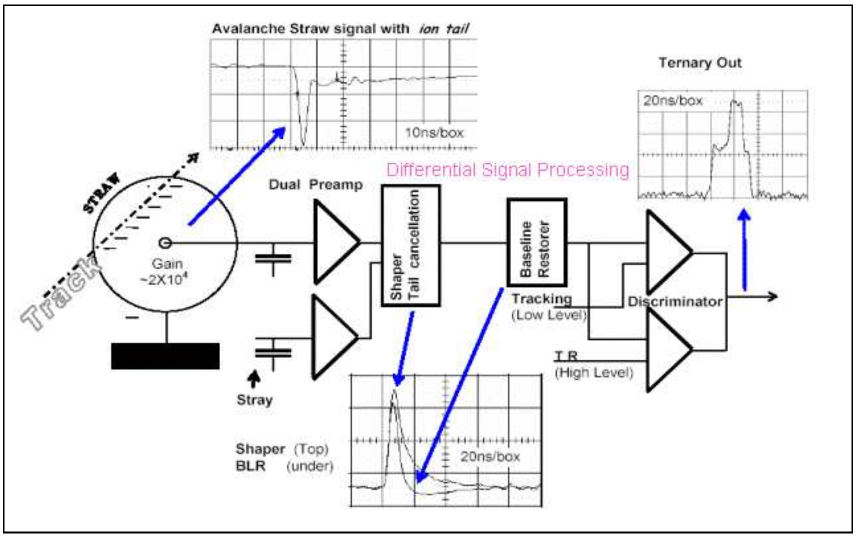

Figure 4: Functional Scheme of the ASDBLR ASIC.

(DMILL). It operates on ± 3 V supplies (preamp positive VCP, shaper positive and negative VCS and VES, discriminator positive and negative VCD and VED, output drive negative VEDR), with a typical power requirement of about 40 mW per channel (the exact value depending on the programmed value of the Ternary and Monitor outputs). The comparator thresholds are voltage sensitive, so care must be taken to keep supplies stable.

The inputs are self-biasing at 0.75 V and have an input impedance of about 250 Ω. The ASDBLR is a differential amplifier, each channel having an active negative-current input (InA), where the anode straw connects, and a "dummy" positive-current input (InB), for Common-Mode rejection. The input capacitance is about 5 pF (depending on the internal input-protection circuit). The amplifier input noise can be characterized as follows [4]: ENC $\simeq$ $2100\,e + 100\,e/\mathrm{pF} \times \mathrm{C}_{\mathrm{in}}\,[\mathrm{pF}]$.

Test-pulse input lines are provided, capacitively (200 fF) coupled to the odd (TST_O) and even (TST_E) channels, respectively. Differential monitor outputs of channel 1 (MON_A1, MON_B1) and channel 8 (MON_A2, MON_B2) are provided, where either the shaper or the BLR output are available (selected via PEN_SH, PEN_BL, resp.)

The detailed behavior of the ion-tail compensation can be controlled by three digital inputs (XESEL, PADSJ1, PADSJ2).

Threshold inputs (0-3 V) provide a reference for all channels: in our application, we use only the low ("track") comparator threshold (PTH_D) ($\sim$720 mV for 3 fC).

Each channel has a differential ternary open-collector output (TRN, TRP). Output current can be adjusted via a current-reference input (PVCDS).

The details of the ASDBLR pad assignment are shown in Fig. 5. The ASIC's will be delivered packaged in full custom Fine Pitch Ball Grid Arrays (FBGA). The details of the bonding on the FBGA substrate and of the ball-to-signal mapping can be found in Appendix A and in Ref. [4].

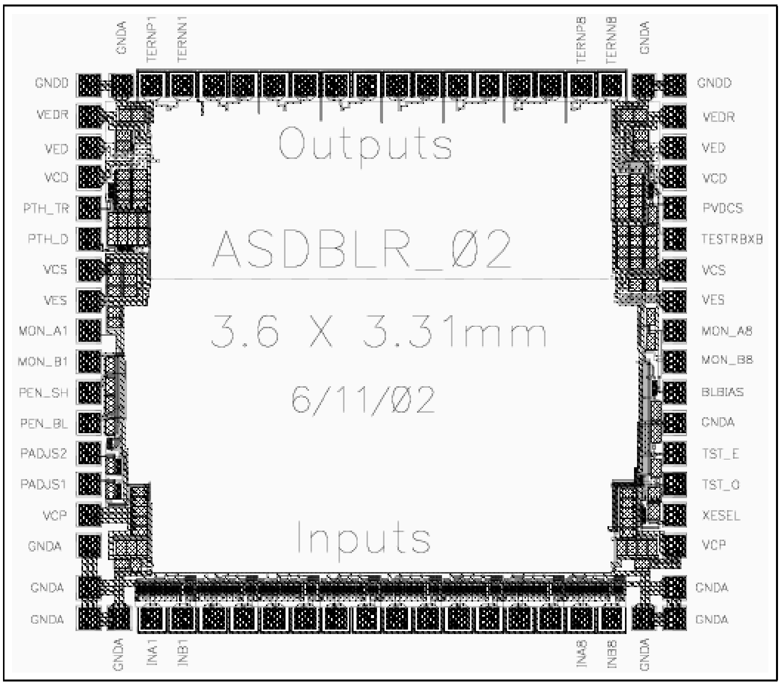

Figure 5: Bonding diagram of the ASDBLR chip in the FBGA packaging.

3.2 Inputs

From the electrical signal-transmission point of view, a straw drift-tube behaves like a transmission line, as shown schematically in Fig. 6 [7, 8]. For an ideal (lossless) transmission line, the characteristic impedance can be calculated (in vacuum) from the formula $Z_0 = 60 \times \log(r_{out}/r_{in})\,[\Omega]$, which, in our case, gives about $316\,\Omega$. In reality, the 6%-Au plated, $25.4\,\mu$m diameter, tungsten anode wire has a conductivity of about $110\,\Omega$/m, which makes the characteristic impedance of the straw transmission line frequency-dependent and not easy to match with ordinary RC-circuitry. The results of previous dedicated studies [7] showed that, in our application, the best overall termination of the straw transmission line can be achieved with a resistor of

300 Ω.

The 25% carbon volume doping of the Kapton XC-160 of the inner straw winding is sufficiently conductive (200 Ω/□, roughly equivalent to about 60 KΩ per meter of straw tube) to be able to remove the charge deposited by the slow ions on the straw cathode. The 12 μm Aluminum of the outer straw winding provide a good signal trasmission for the fast part (leading edge) of the signal.

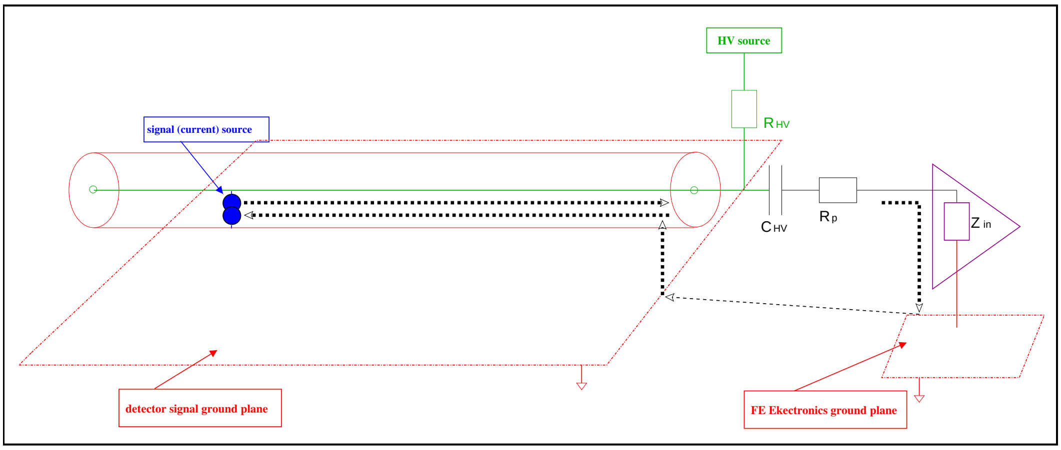

Figure 6: The signal path in the straw-tubes detector.

3.2.1 Input Connectors

The small hit charges from 32 straw drift tubes go from the HV Board [3] to two ASDBLR boards via mating SMD connectors, as shown in Fig.2. The detailed pin assignments of these connectors can be found in Appendix B.

The correspondence between the ASDBLR (negative current) input pads (InA1–8) (numbering fixed by the ASIC designers) and the anode wires (numbering fixed by the designers of the Outer Tracker modules) depends on which side of the board the ASDBLR chip is placed (given that one wants straight, short, non-crossing traces to go from the input connector to the chip input pads).

Keeping all traces and especially the sensitive input lines as short as possible reduces the capacitive and inductive cross talk. Additionally, to reduce the channel-to-channel cross-talk [8], each signal pin on the connector is sourrounded by ground pins on either side. Moreover, the ground planes of the HV and ASDBLR Boards are directly coupled over the full board widths via special contact springs, as shown schematically in Fig. **??**.

3.2.2 Input Protection

The ASDBLR input are internally protected by a protection network of only few mJ, in order to keep the input capacitance low ($\sim 5\,\mathrm{pF}$). However, the high-voltage signal separation capacitor of $\mathrm{C_{HV}} = 330\,\mathrm{pF}$ is charged to $\mathrm{V_{HV}} = 1600\,\mathrm{V}$ and, if a spark occurring in the straw "shorts" the anode wire to ground (with the low impedance corresponding to the conductivity of the ions in the gas), it will discharge on the amplifier input. Therefore, an extra protection circuit has been implemented on the ASDBLR Board, based on voltage-clamping diodes combined with resistive current limiting.

If $\mathrm{R_s}$ is the total series resistance seen by the amplifier input, then a charge of $\delta Q_{spark} = \mathrm{C_{HV}}\,\mathrm{V_{HV}}$ would be discharged with a characteristic time constant $\tau = \mathrm{R_s}\,\mathrm{C_{HV}}$, thus generating an enormous negative input current pulse $\delta \mathrm{I_{spark}} \approx \mathrm{V_{HV}}/\mathrm{R_s}$. This current is limited by the value of $\mathrm{R_s}$, the sum of the anode-wire resistance and the current-limiting resistance on the ASDBLR Board. In the least favorable case in which the spark occurs at the wire end closer to the amplifier, the current limitation is provided by the board series resistance.

The protection circuitry actually implemented on the ASDBLR Board is shown schematically in Fig. 7; the details can be found on the schematics in Appendix C. A diode limiter is used to limit the input voltage excursion. A high-speed, fast-recovery diode (type BAV 99) clamping to ground will short any negative voltage lower than -0.7 V to ground, thus limiting negative voltage excursions at the amplifier inputs (self-biasing at 0.75 V) to -0.7 V. In order to limit positive voltage "swings", a second diode clamps to the +3 V supply, thus limiting the positive voltage excursion to +3.7 V. In practice, the diode limiter becomes only active when the input voltage is outside the range (-0.7,3.7) V. To limit the current, two $\mathrm{R_{s1}} = \mathrm{R_{s2}} = 68\,\Omega$ series resistors are used: the first one is limiting the current to the diodes, while the second one limits the current to the ASDBLR input ($\delta \mathrm{I_{spark}} \simeq 23\,\mathrm{A}$). Care is taken that the discharge cannot transmit through the diode supply circuitry by decoupling this latter separately from the rest of the supply circuitry (see Sect. 3.6).

3.2.3 Input Capacitance

The amplifier input sees the contribution of several parasitic capacitances. In the approximation in which the signal transmission from the straw tube to the amplifier input takes place along an ideal lossless cable, the main contributions come from the straw-tube itself, the signal traces in the PCBs, the ASDBLR input capacitance and the contribution from the extra input-

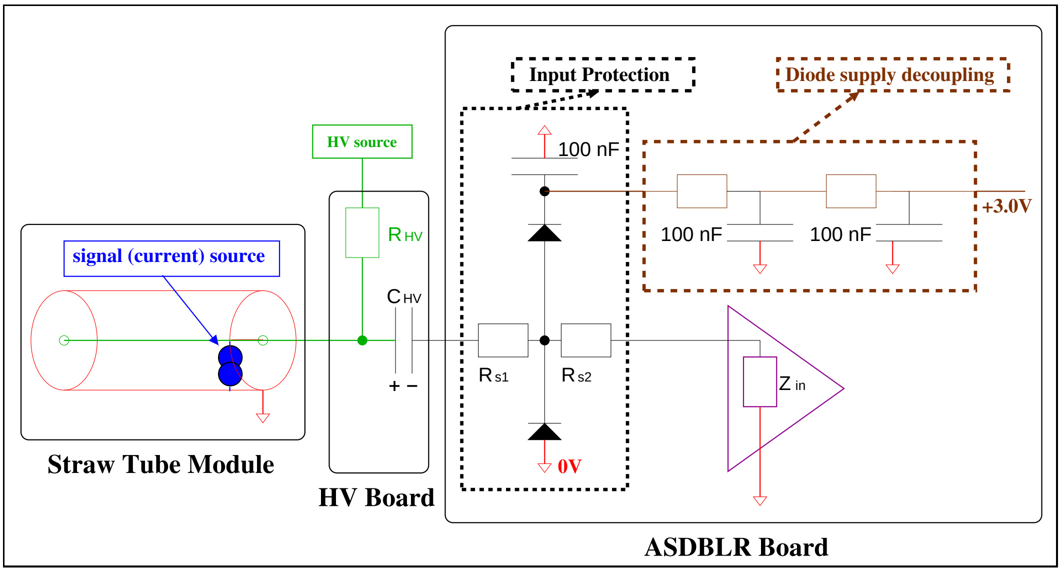

Figure 7: Amplifier input protection circuitry on the ASDBLR Board.

protection circuitry (see Sect. 3.2.2).

The capacitance of the straw-tube itself can be estimated (in vacuum) from the formula: $\mathrm{C} \simeq 55.6 / \log(\mathrm{r_{out}}/\mathrm{r_{in}})$ [pF/m]; in our case this gives about 11 pF/m and thus a total of 26 pF for the whole straw length. The total contribution of the FE Electronics has been estimated to be about 20 pF (7 pF from the traces of the Feed-Through Board, 7 pF from those of the HV Board, and 6 pF from the ASDBLR Board traces and extra protection circuitry). As described in Sect. 3.1, the ASDBLR input capacitance is about 5 pF; assuming $\mathrm{ENC} \simeq 1600\,e + 100\,e/\mathrm{pF} \times \mathrm{C_{in}}$ [pF] and $\mathrm{C_{in}} \simeq 51$ pF, would result in a total input noise $\mathrm{ENC} \simeq 6700\,e \simeq 1.07$ fC. Only 30% of this ENC ($2000\,e \simeq 0.32$ fC) is contributed by the FE Electronics Boards.

3.2.4 Input Impedance

As already mentioned in the introduction, although signal transmission from the straw tube to the amplifier input suffers from losses due to the resistivity of the conductors (and the conductivity of the dielectrics), which in turn make the signal propagation velocity frequency-dependent, in our application the characteristic impedance of the straw-tube transmission line can be considered a constant 300 Ω.

The dependence of the ASDBLR input impedance on the signal frequency is discussed in detail in Ref. [4]; at the frequencies of interest (20-30 MHz) is about 200 Ω, somewhat lower than the characteristic impedance of the straw tube transmission line. The values of the two (current-limiting) series resistors in Fig. 7, $R_{s1} = R_{s2} = 68\,\Omega$, were also chosen to provide a good impedances match.

3.2.5 Dummy Inputs

As discussed in Sect. 3, the input stage of the ASDBLR is a differential amplifier: a dummy line which is connected to a positive-current input (InB) of this amplifier and runs along the signal trace gets the same pickup from the environment as the signal trace itself; this noise will be seen as a common-mode signal and will be rejected by the differential amplifier.

Therefore, in the design special care has been taken for a correct connection of the "dummy" inputs (InB1–8). The differential traces have been routed in parallel ways and kept on the same layer all the way from the input connector to the ASDBLR inputs (in fact, all the way from the high-voltage capacitor on the HV Board!)

In order not to introduce large gain differences between the two differential inputs, the capacitive load due to the straw tube (see Sect. 3.2.3) has been simulated by adding a 22 pF capacitor to the dummy inputs and the input protection circuitry (see Sect. 3.2.2) has been replicated for the dummy inputs.

3.3 Tail Compensation Control

The tail-compensation mechanism of the ASDBLR ASIC (see Sect. 3) can be controlled via three digital inputs: XESEL selects between two shaping stages within the shaper, while PADJS1 (resp. PADJS2) adds an integration network in collectors of the Second (resp. Third) Shaper Stage. In our application ($Ar/CO_2/CF_4$), all these digital inputs are connected to +3 V.

3.4 Outputs

As discussed in Sect. 3.1, the two-levels ASDBLR discriminators switch separate 200 μA (open-collector) current sources between shared differential outputs to form a current sum of the combined discriminator outputs, according to a ternary encoding scheme. In our application, the high-threshold is "silenced" (PTH_TR1 and PTH_TR2 tied to +3 V) such that the differential outputs, TRN1–8 and TRP1–8, contain only the low-threshold output, switching between 0 and 200 μA, at the nominal current setting. This current setting can be programmed in the ASDBLR ASIC, via the PVCDS pad, between 0 and 0.9 mA.

In principle, the ASDBLR open-collector outputs are versatile: for a given current output, one can obtain any desired voltage swing adjusting the connected load. In practice, if all resistors are attached to a common level and if their value is too low, channel-to-channel injection can occur and eventually, for a sufficiently large number of switching channels, oscillation.

The circuitry shown schematically in Fig. 8 has been adopted in our application; the detailed schematics can be found in Appendix C. In the figure, an ASDBLR current output switching between 0 and $I_o = 0.8\,\mathrm{mA}$ is assumed. Pull-up resistors, $R_L = 3.9\,\mathrm{K}\Omega$, connected to the common +3 V level are used on the ASDBLR board in combination with termination resistors, $R_t = 120\,\Omega$, on the OTIS Board [5]. The large values of the pull-up resistors prevents channel-to-channel injection. The differential outputs are then brought completely floating to the differential receiver on the OTIS TDC [10]. The peak-to-peak voltage swing is given by the product $R_t\, I_o/2$. This simple scheme is sufficient to drive the OTIS differential receivers, as discussed in detail in Ref. [12].

Assuming the parasitic capacitance seen by the output signal (traces and OTIS input) to be about 10 pF, the 120 Ω termination resistance guarantees a fast rise-time of little over 1 ns.

3.5 ASDBLR Monitoring and Test-Pulse

In the ASDBLR ASIC packaged in FBGA, differential outputs are available for the analog monitoring of channel 1 (MON_A1, MON_B1). The BLR output can be made available at these monitor outputs by pulling high PEN_BL. On the ASDBLR board, the differential outputs are made available on pads and the monitoring can be enabled by connecting PEN_BL to +3 V with a jumper.

On the ASDBLR board, the ASDBLR test-pulse inputs (TST_E and TST_O) are capacitively ($\mathrm{C_{inj}} = 1.8\,\mathrm{pF}$) coupled and made available on the SMD connector towards the OTIS Board. These test-pulse inputs can be used with a calibrate voltage to inject a calibrate charge in a short time ($\mathrm{Q_{inj}} = \mathrm{C_{inj}}\,\mathrm{V_{inj}}$). The details of the Test-Pulse scheme shall be described elsewhere [13].

3.6 Low-Voltage Supplies

As discussed in Sect. 3.1, the ASDBLR operates on ±3 V supplies. These are supplied by radiation-hard voltage regulators locally residing in the Outer

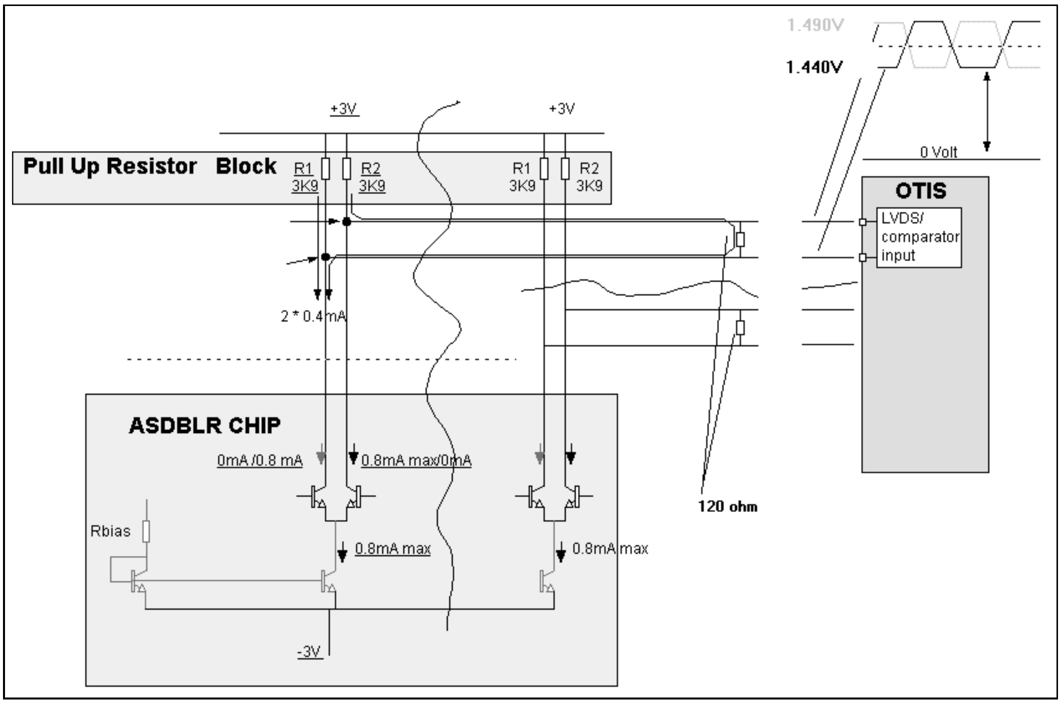

Figure 8: Pull-up and termination circuitry for the ASDBLR-to-OTIS interface.

Tracker Front-End Electronics [9]. Special care has been taken by the ASDBLR ASIC designers to separate the supply of the cascading stages (preamp positive VCP, shaper positive and negative VCS and VES, discriminator positive and negative VCD and VED, output drive negative VEDR) to avoid feedback and oscillations. As shown in the detailed schematics in Appendix C, on the ASDBLR Board each supply voltage has been individually decoupled by its own load resistor and filter capacitor.

The supply current consumption per ASDBLR chip is about 80 mA for the negative current and about 80 mA for the positive current.

3.7 Cooling

The Outer Tracker Front-End Electronics boards are grouped into housing boxes (see Sect. 2). Each FE Electronics box will be water cooled with closed-circuit, demineralized water at about 20 °C. The details of the FE Electronics cooling scheme shall be described elsewhere [11].

The main contribution to the power consumption on the ASDBLR board is expected to come from the ASDBLR ASIC. This has been estimated to be $\delta P_+ \simeq \delta P_- \simeq 80\,\mathrm{mA} \times 3\,\mathrm{V} = 240\,\mathrm{mW}$, which gives a total of 960 mW per ASDBLR board. The ASDBLR Board has been provided with a heat-spreading layer in the PCB, to which heat-conducting mounting posts are coupled. These cooling posts are then intended to be coupled to the internal cooling chassis of the FE Electronics box [11]. The main contributions to the cooling losses were estimated to come from the cooling chassis ($\delta T \sim 15\,^{\circ}\mathrm{C}$), from the heat spreading layer ($\delta T \sim 15\,^{\circ}\mathrm{C}$), and from the grid of balls under the ASDBLR ASIC ($\delta T \sim 15\,^{\circ}\mathrm{C}$), while the cooling posts contribution should be negligible. According to these estimates, the ASDBLR chip internal temperature would end up about $45\,^{\circ}\mathrm{C}$ above the cooling-surface temperature ($\sim 20\,^{\circ}\mathrm{C}$), which seems acceptable.

Provision for the placement of a temperature sensor on the board has been made.

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A ASDBLR FBGA Package

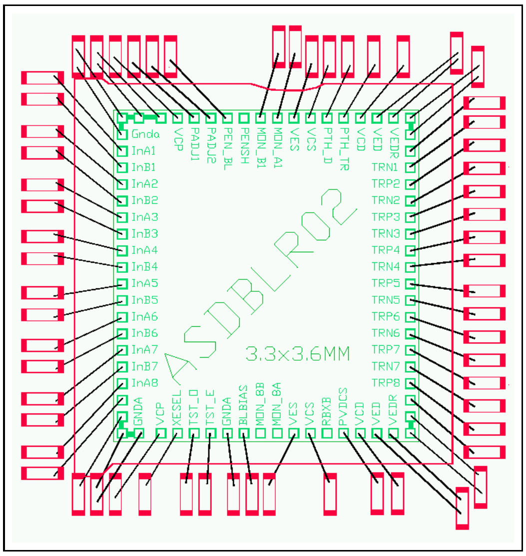

Figure 9: Bonding diagram of the ASDBLR chip in the FBGA packaging.

	A	B	C	D	E	F	G	H	J	K	L	M
1 1	INB1	INA1	VCP	ADJ1	MON_B1	MON_A1	VCS	THR_D	THR_TR	VED VEDR	TRN1	TRP1
2 2	INA2	INB2	X	ADJ3	MON_EN	X	VES	VCD	VED VEDR	X	TRP2	TRN2
3 3	INB3	INA3	X	X	GND	X	X	X	X	X	TRN3	TRP3
4 4	INA4	INB4	X	X	GND	GND	GND	GND	X	X	TRP4	TRN4
5 5	X	X	X	X	GND	GND	GND	GND	X	X	X	X
6 6	INB5	INA5	X	X	GND	GND	GND	GND	X	X	TRN5	TRP5
7 7	INA6	INB6	X	X	GND	X	X	X	X	X	TRP6	TRN6
8 8	INB7	INA7	X	X	X	X	VES	VCD	X	X	TRN7	TRP7
9 9	INA8	INB8	VCP	XESL	TST_O	TST_E	BLBIAS	VCS	VDCS	VED VEDR	TRP8	TRN8

Figure 10: Ball to signal mapping.

B Connector Pin Assignment

ASDBLR Board Input Connector J1				ASDBLR Board Input Connector J1			
Pin Nr	Signal	Pin Nr	Signal	Pin Nr	Signal	Pin Nr	Signal
J1-1	GND	J1-2	GND	J1-51	GND	J1-52	GND
J1-3	wire-16	J1-4	GND	J1-53	wire-8	J1-54	GND
J1-5	dummy-16	J1-6	GND	J1-55	dummy-8	J1-56	GND
J1-7	GND	J1-8	GND	J1-57	GND	J1-58	GND
J1-9	wire-15	J1-10	GND	J1-59	wire-7	J1-60	GND
J1-11	dummy-15	J1-12	GND	J1-61	dummy-7	J1-62	GND
J1-13	GND	J1-14	GND	J1-63	GND	J1-64	GND
J1-15	wire-14	J1-16	GND	J1-65	wire-6	J1-66	GND
J1-17	dummy-14	J1-18	GND	J1-67	dummy-6	J1-68	GND
J1-19	GND	J1-20	GND	J1-69	GND	J1-70	GND
J1-21	wire-13	J1-22	GND	J1-71	wire-5	J1-72	GND
J1-23	dummy-13	J1-24	GND	J1-73	dummy-5	J1-74	GND
J1-25	GND	J1-26	GND	J1-75	GND	J1-76	GND
J1-27	dummy-12	J1-28	GND	J1-77	dummy-4	J1-78	GND
J1-29	wire-12	J1-30	GND	J1-79	wire-4	J1-80	GND
J1-31	GND	J1-32	GND	J1-81	GND	J1-82	GND
J1-33	dummy-11	J1-34	GND	J1-83	dummy-3	J1-84	GND
J1-35	wire-11	J1-36	GND	J1-85	wire-3	J1-86	GND
J1-37	GND	J1-38	GND	J1-87	GND	J1-88	GND
J1-39	dummy-10	J1-40	GND	J1-89	dummy-2	J1-90	GND
J1-41	wire-10	J1-42	GND	J1-91	wire-2	J1-92	GND
J1-43	GND	J1-44	GND	J1-93	GND	J1-94	GND
J1-45	dummy-9	J1-46	GND	J1-95	dummy-1	J1-96	GND
J1-47	wire-9	J1-48	GND	J1-97	wire-1	J1-98	GND
J1-49	GND	J1-50	GND	J1-99	GND	J1-100	GND

Table 1: Pin assignment of Input Connector J1 (Samtec FTS-150-03-L-DV-P).

ASDBLR Board Output Connector J2			
Pin Nr	Signal	Pin Nr	Signal
J2-1	+3V	J2-2	+3V
J2-3	GND	J2-4	GND
J2-5	-3V	J2-6	-3V
J2-7	GND	J2-8	GND
J2-9	TRN1-1	J2-10	TRP1-1
J2-11	TRN2-1	J2-12	TRP2-1
J2-13	TRN3-1	J2-14	TRP3-1
J2-15	TRN4-1	J2-16	TRP4-1
J2-17	TRN5-1	J2-18	TRP5-1
J2-19	TRN6-1	J2-20	TRP6-1
J2-21	TRN7-1	J2-22	TRP7-1
J2-23	TRN8-1	J2-24	TRP8-1
J2-25	TRN1-2	J2-27	TRP1-2
J2-27	TRN2-2	J2-28	TRP2-2
J2-29	TRN3-2	J2-30	TRP3-2
J2-31	TRN4-2	J2-32	TRP4-2
J2-33	TRN5-2	J2-34	TRP5-2
J2-35	TRN6-2	J2-36	TRP6-2
J2-37	TRN7-2	J2-38	TRP7-2
J2-39	TRN8-2	J2-40	TRP8-2
J2-41	GND	J2-42	GND
J2-43	TST_E	J2-44	TST_O
J2-45	THR_D-1	J2-46	THR_D-2
J2-47	TempMonR	J2-48	TempMonRet
J2-49	GND	J2-50	GND

Table 2: Pin assignment of Output Connector J2 (Samtec FSH-125-04-L-DH-SL).

C ASDBLR Board Schematics

The detailed schematics of the ASDBLR Board prototype is shown in this Appendix. The design has been carried out with the aid of the MentorGraphics CAD Station running under Solaris. The complete set of drawings can be found at
http://www.nikhef.nl/user/otr/Electronics/ASDBLR-Prototype-Board.

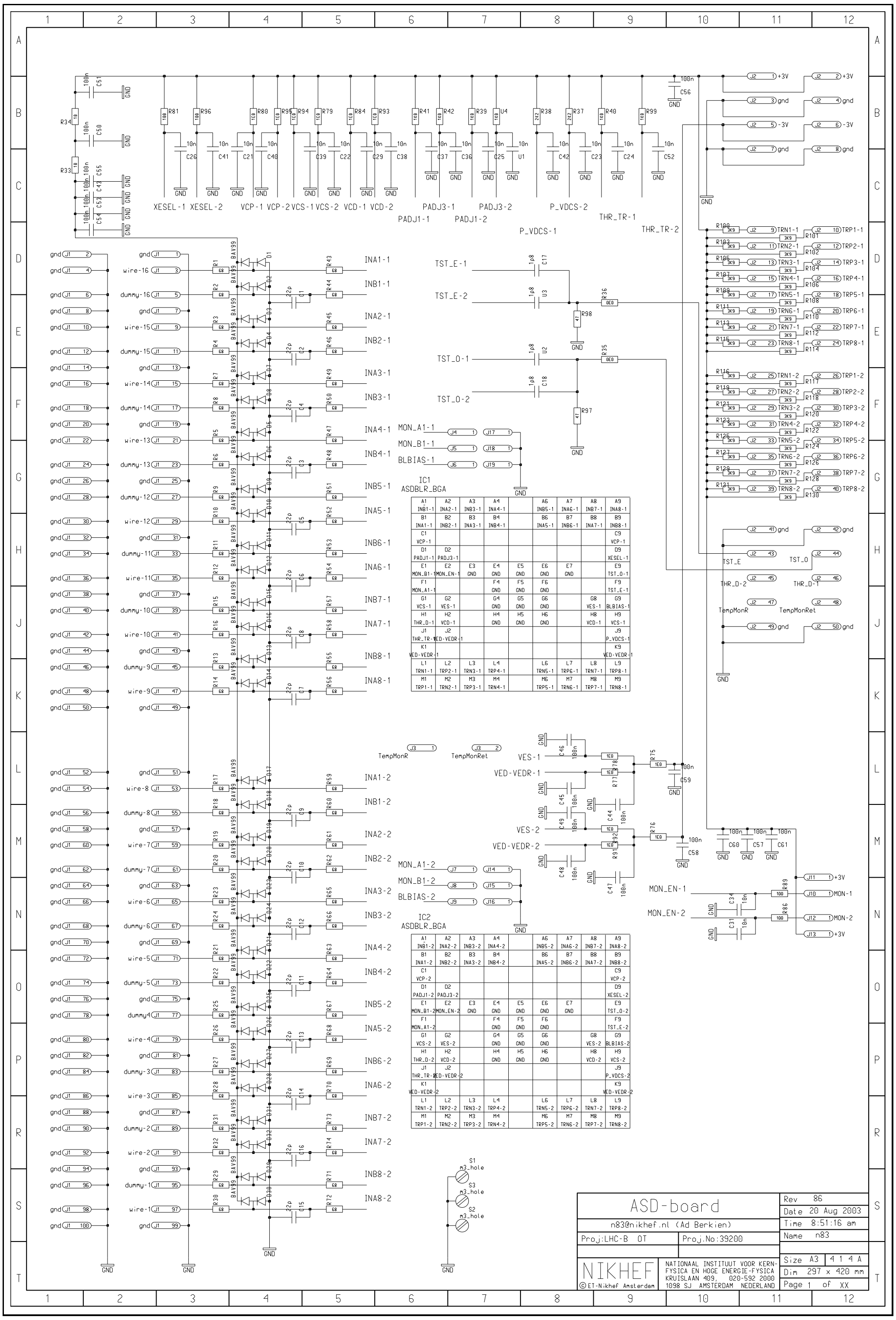

Figure 11: ASDBLR Board Schematics.

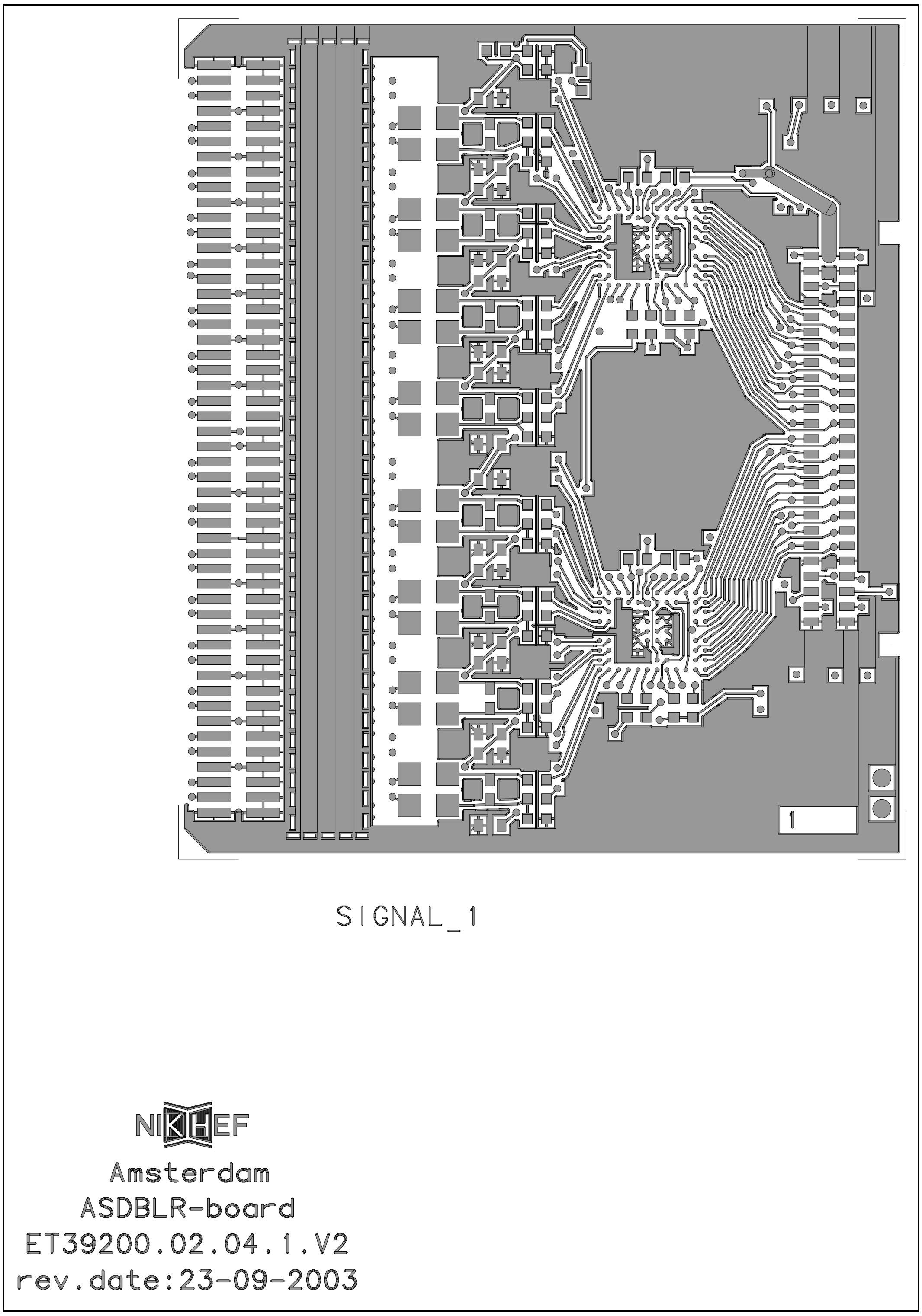

Figure 12: ASDBLR Board Signal Layer 1.

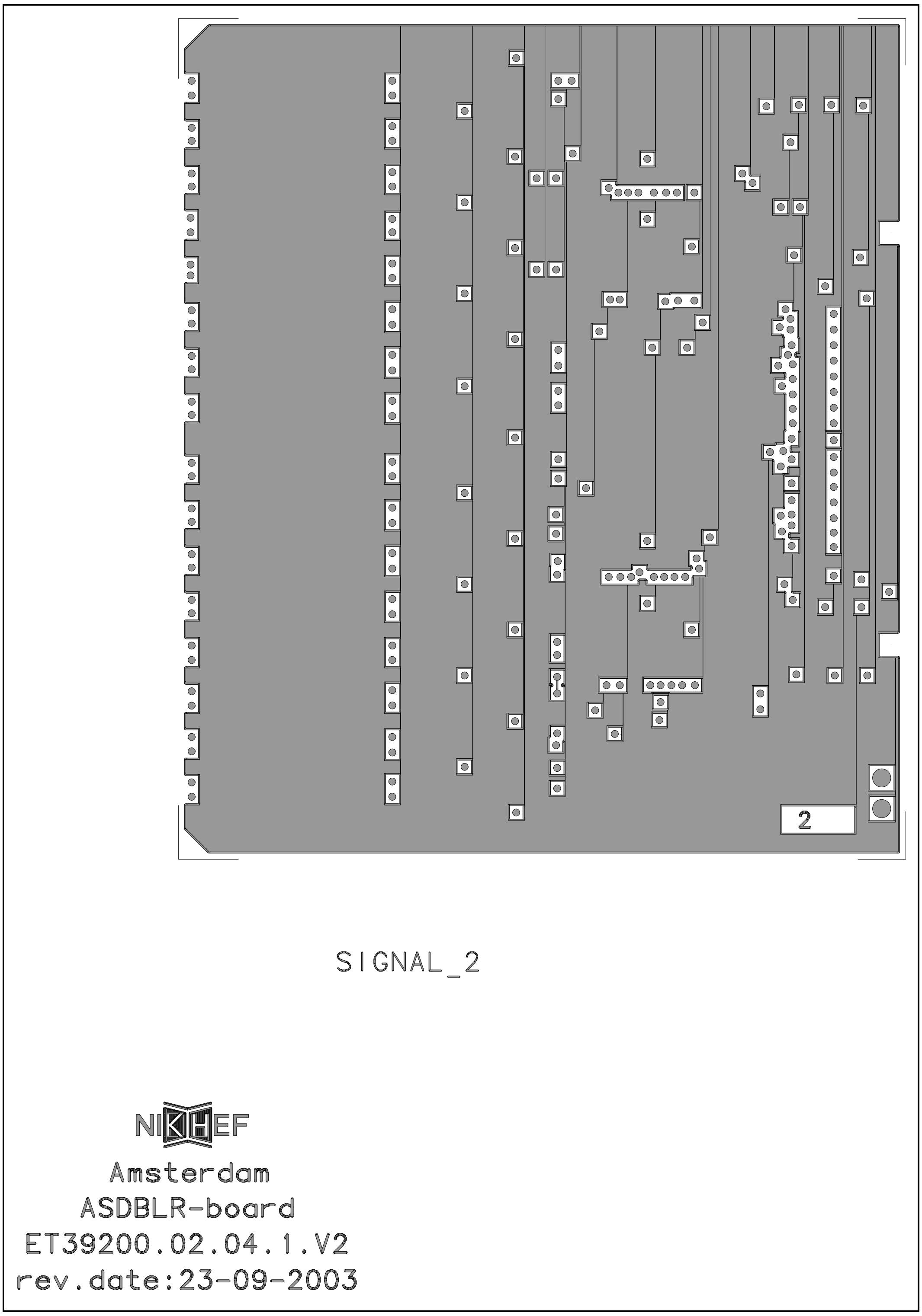

Figure 13: ASDBLR Board Signal Layer 2.

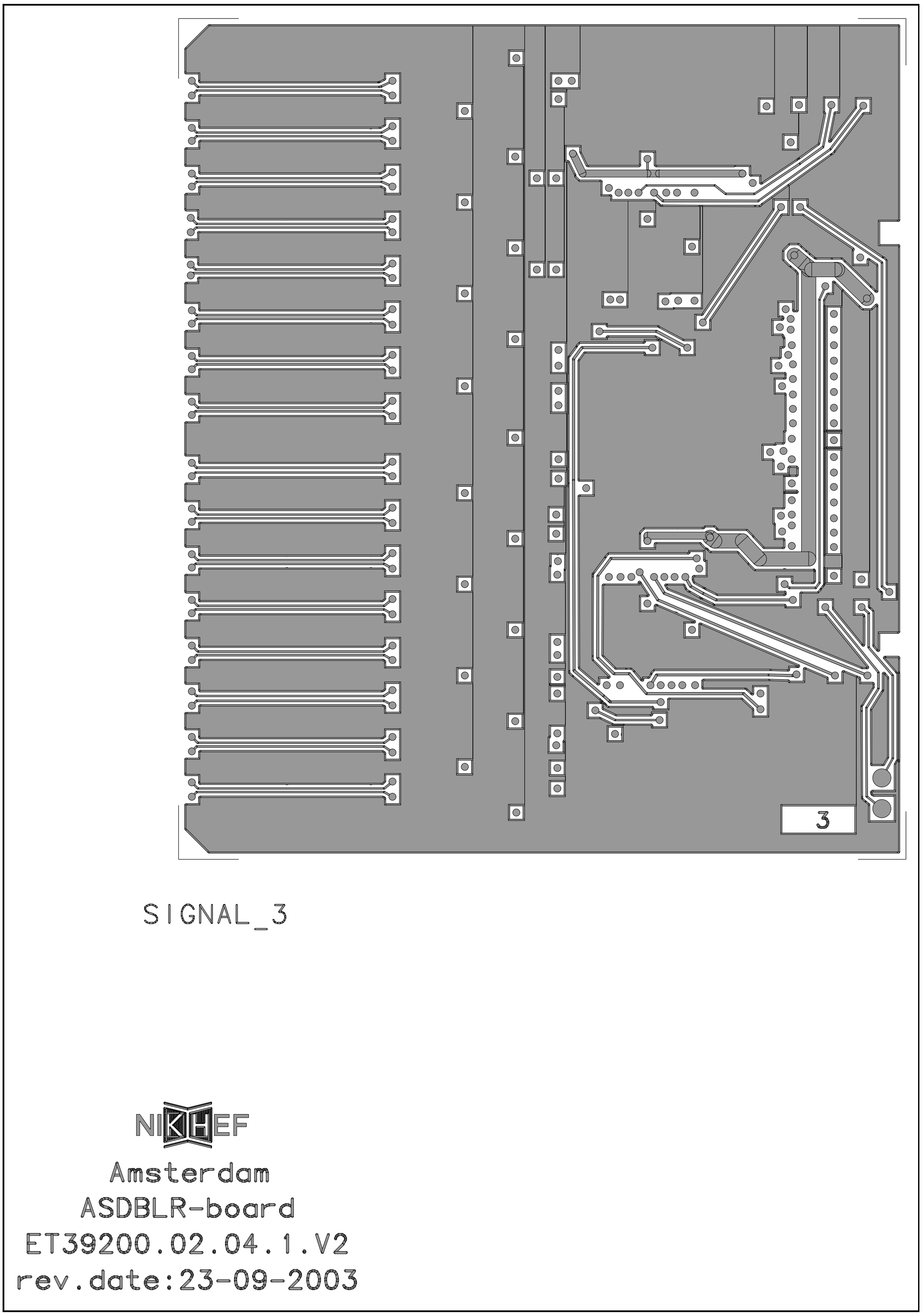

Figure 14: ASDBLR Board Signal Layer 3.

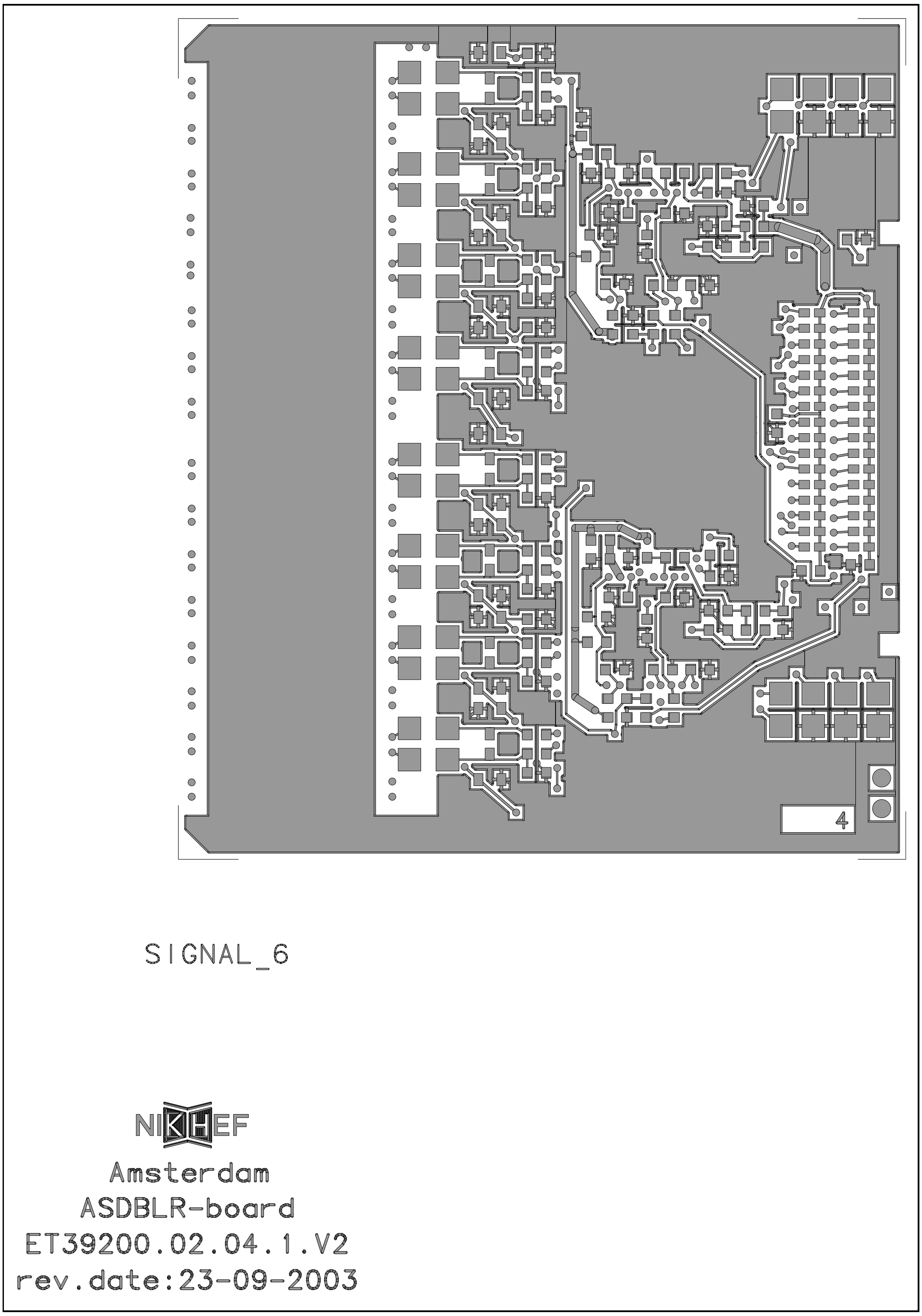

Figure 15: ASDBLR Board Signal Layer 6.