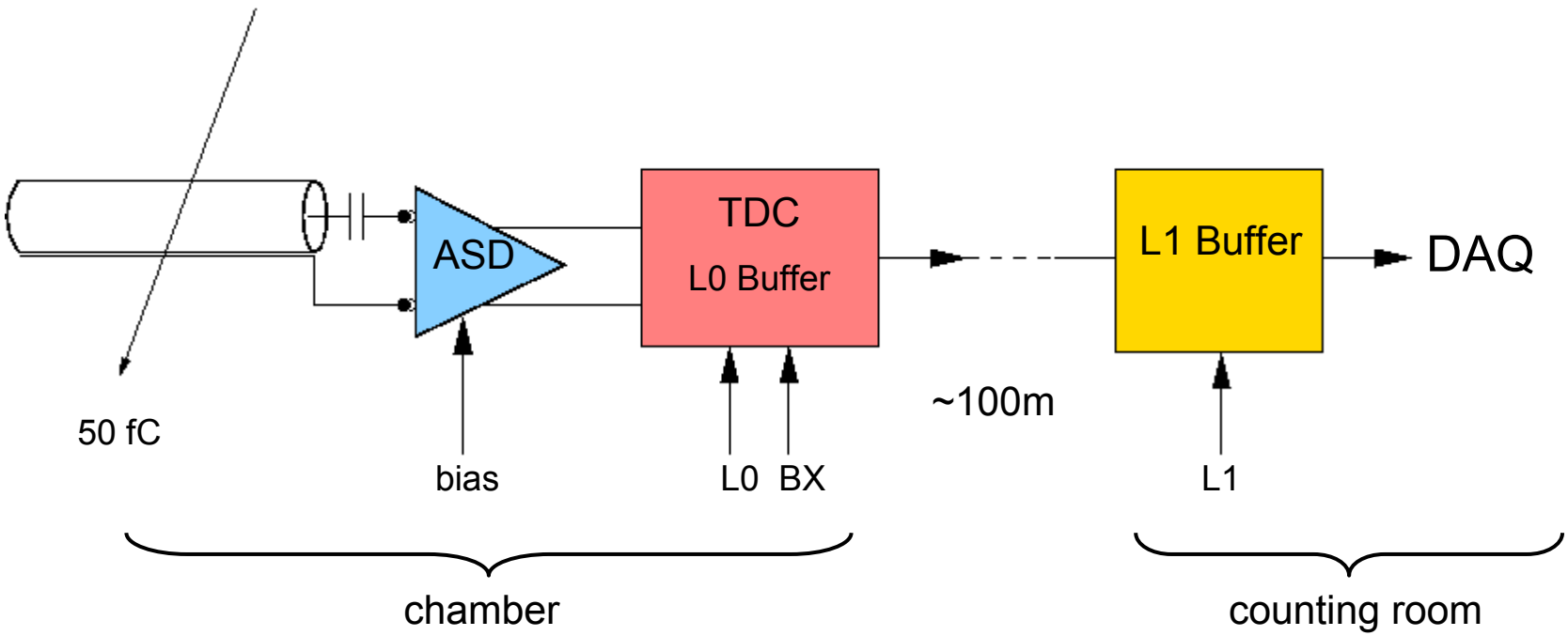
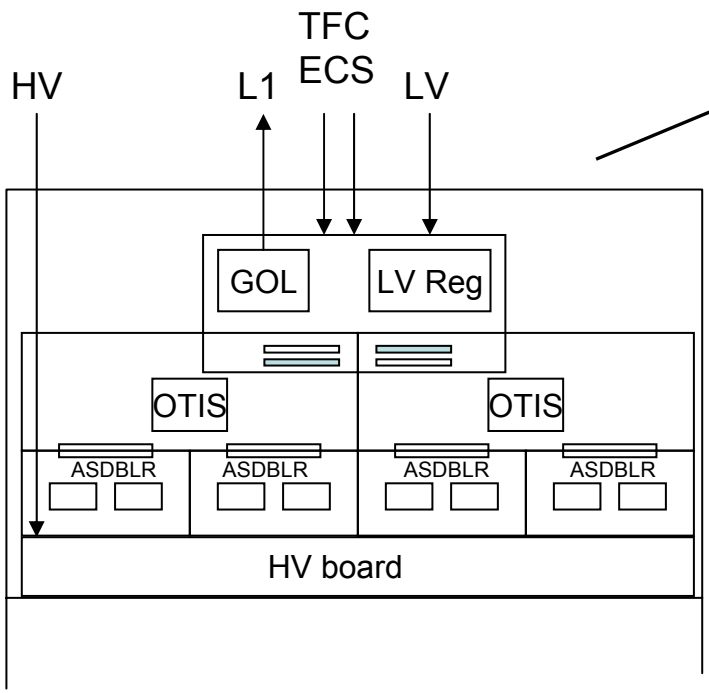
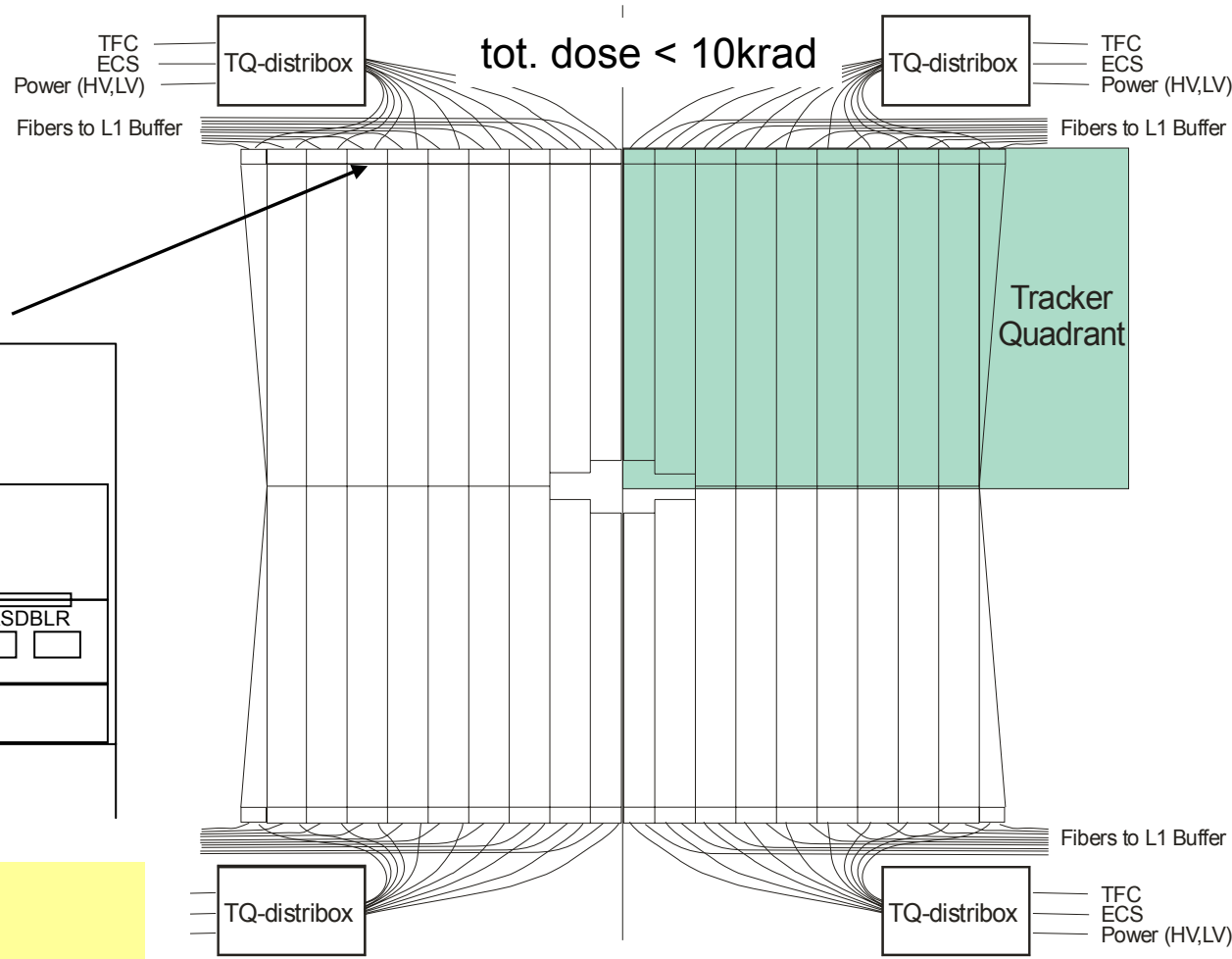
Ulrich Uwer
University of Heidelberg

Outer Tracker Electronics







<u>Module End:</u>

128 channels

16 ASDBLR chips

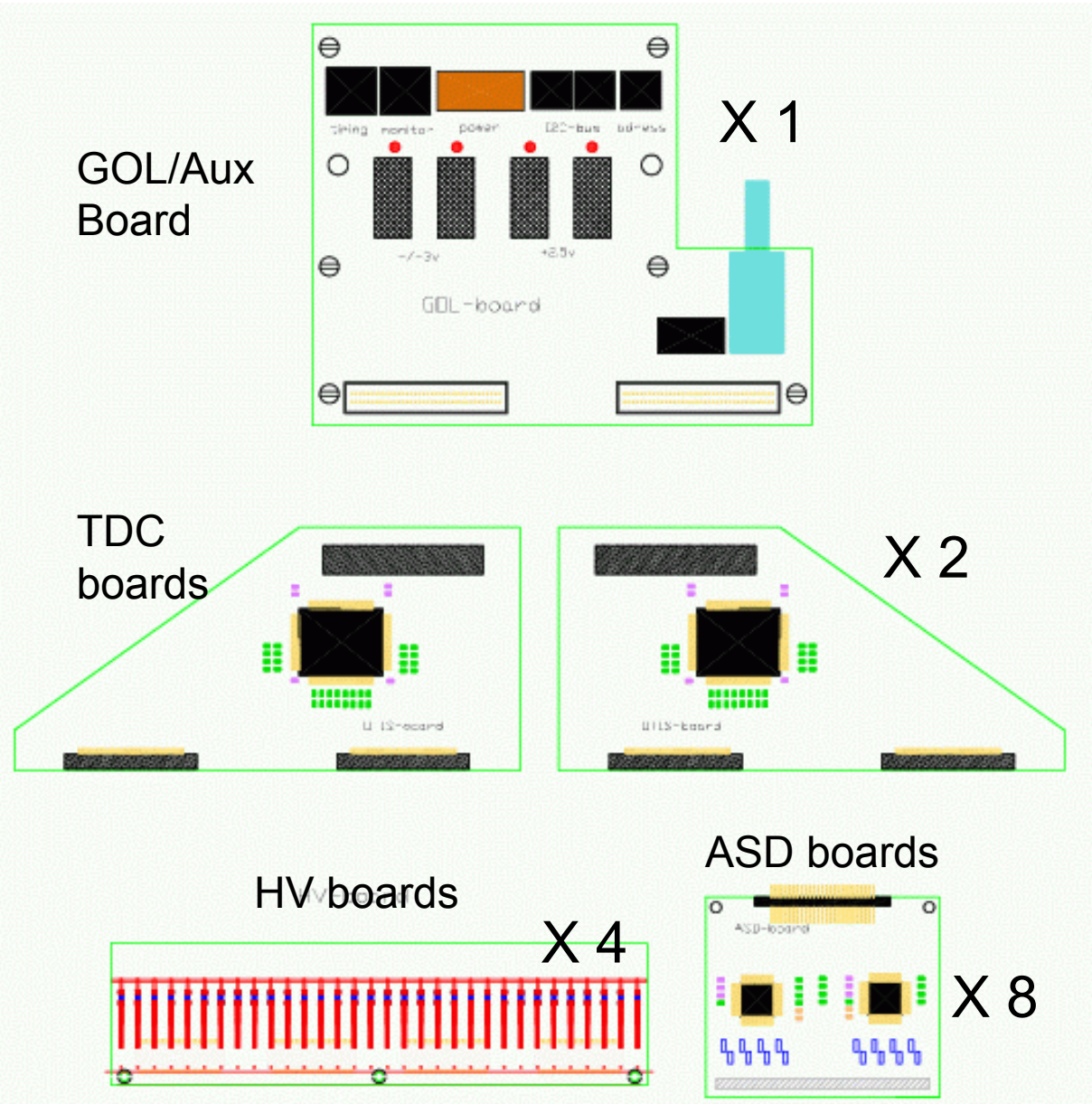
4 OTIS TDC chips

1 optical link: 1.28 Gbit/s

<u>Outer Tracker:</u> ST1…3

56000 channels

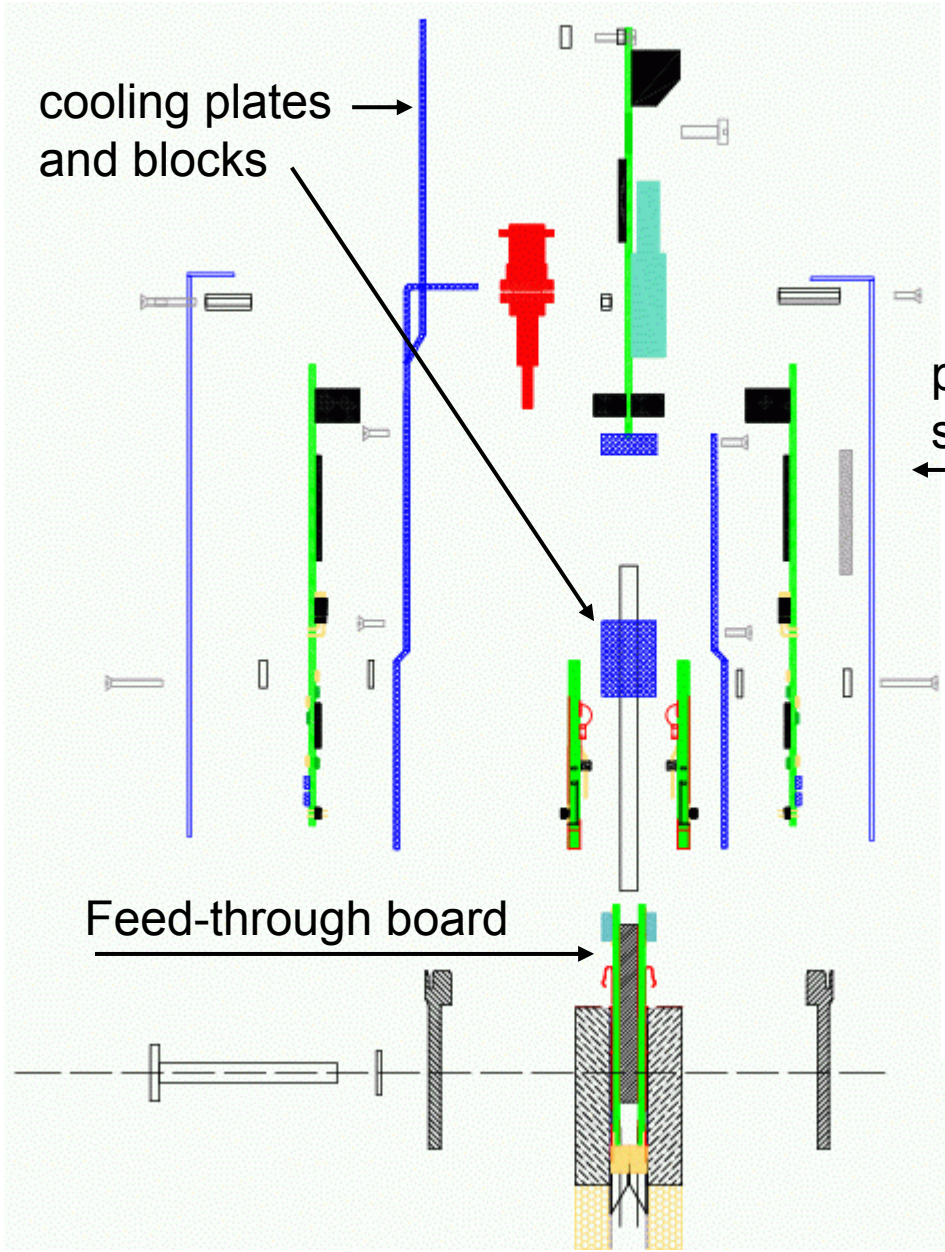
432 optical links

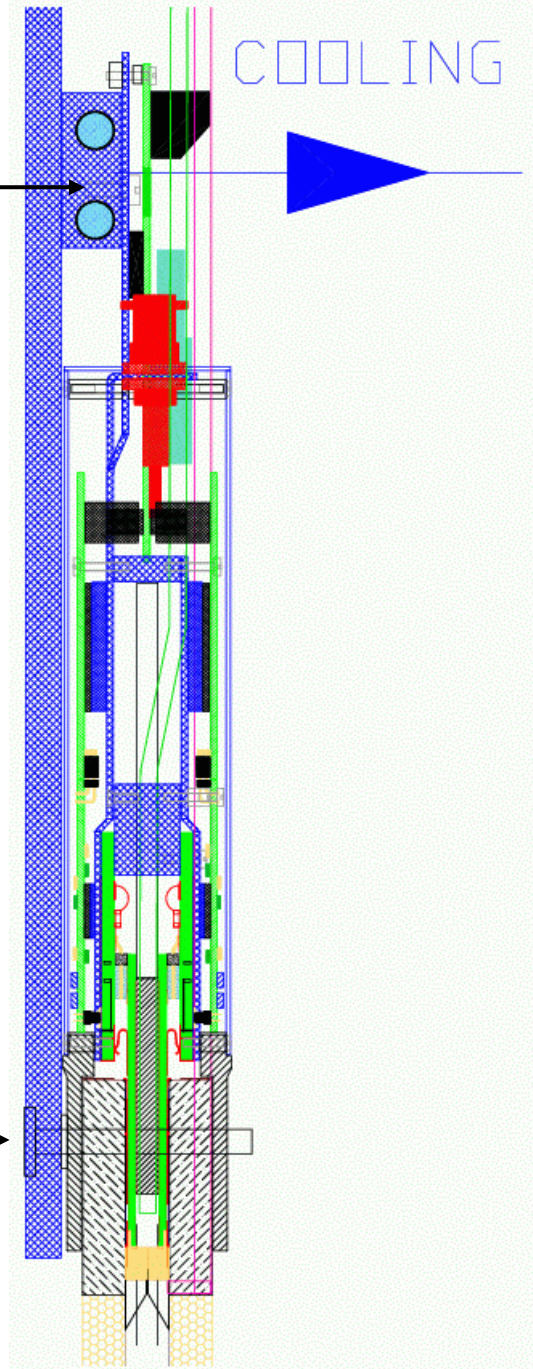


Front-end cards:

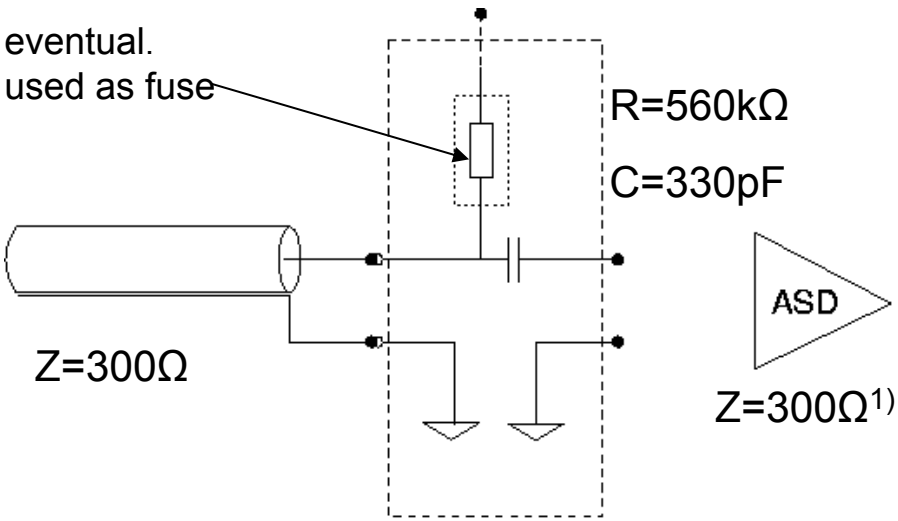
- have to fit inside a closed metal shielding box: 22 x 30 x 4 cm
- excellent ground connection to straw-tubes and module reference ground
- power dissipation of cards is about 22 W / box → water cooling
- easy access should be maintained

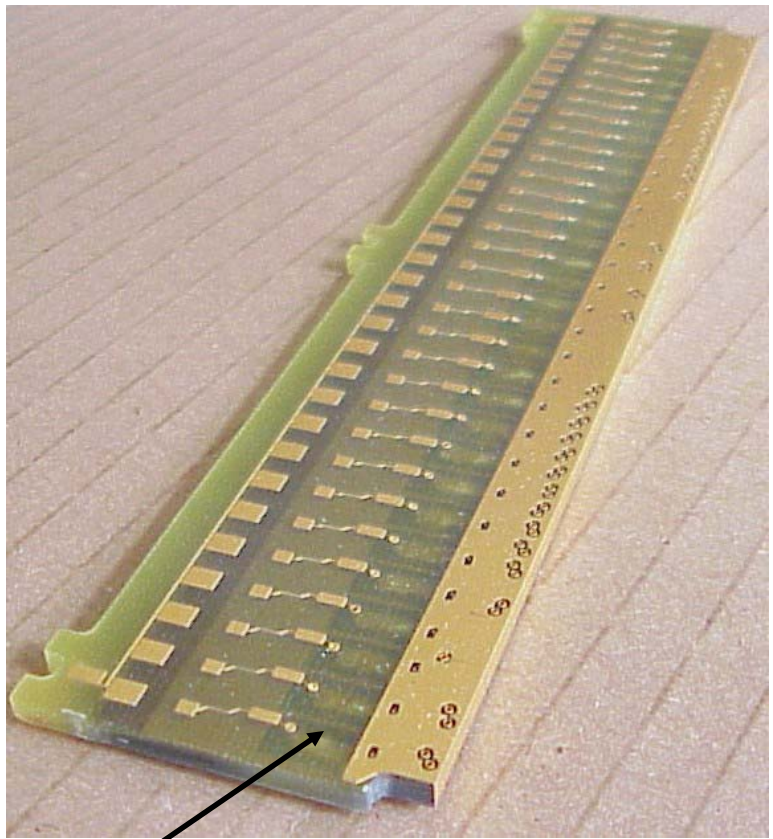
Front-end electronics box: How it fits together





HV Boards



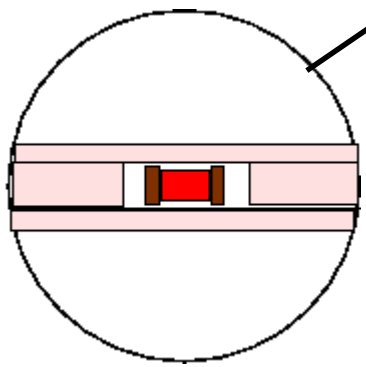


Capacitors:

JOHANSON 302R29W331KV4E

Max. Volt.: 4kV

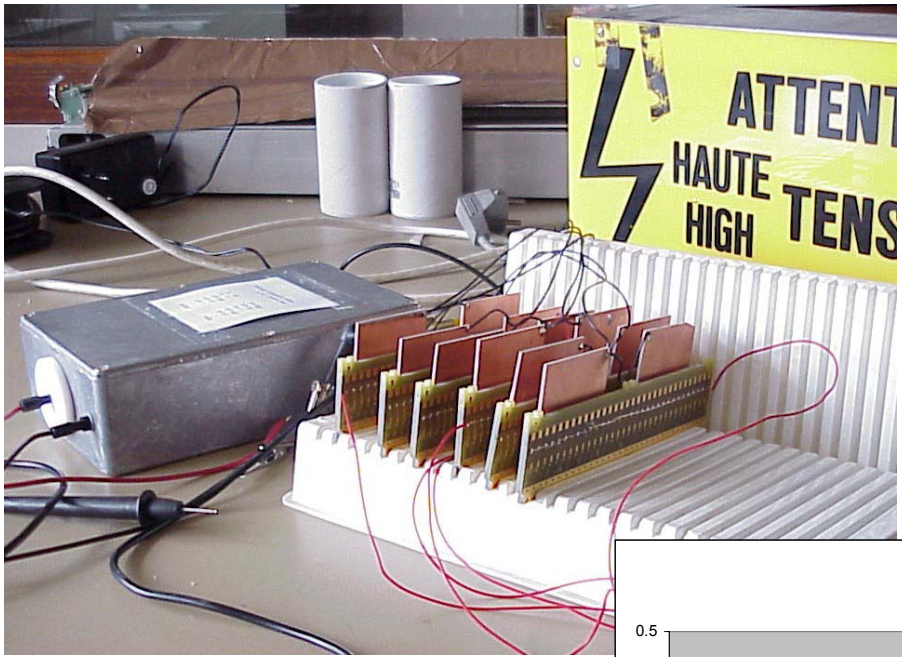
Size: 4.6 x 2 x 1.5 mm^3



32 channels per board

Capacitors embedded in PCB:

1) Z=150Ω at high frequencies + 150Ω in series



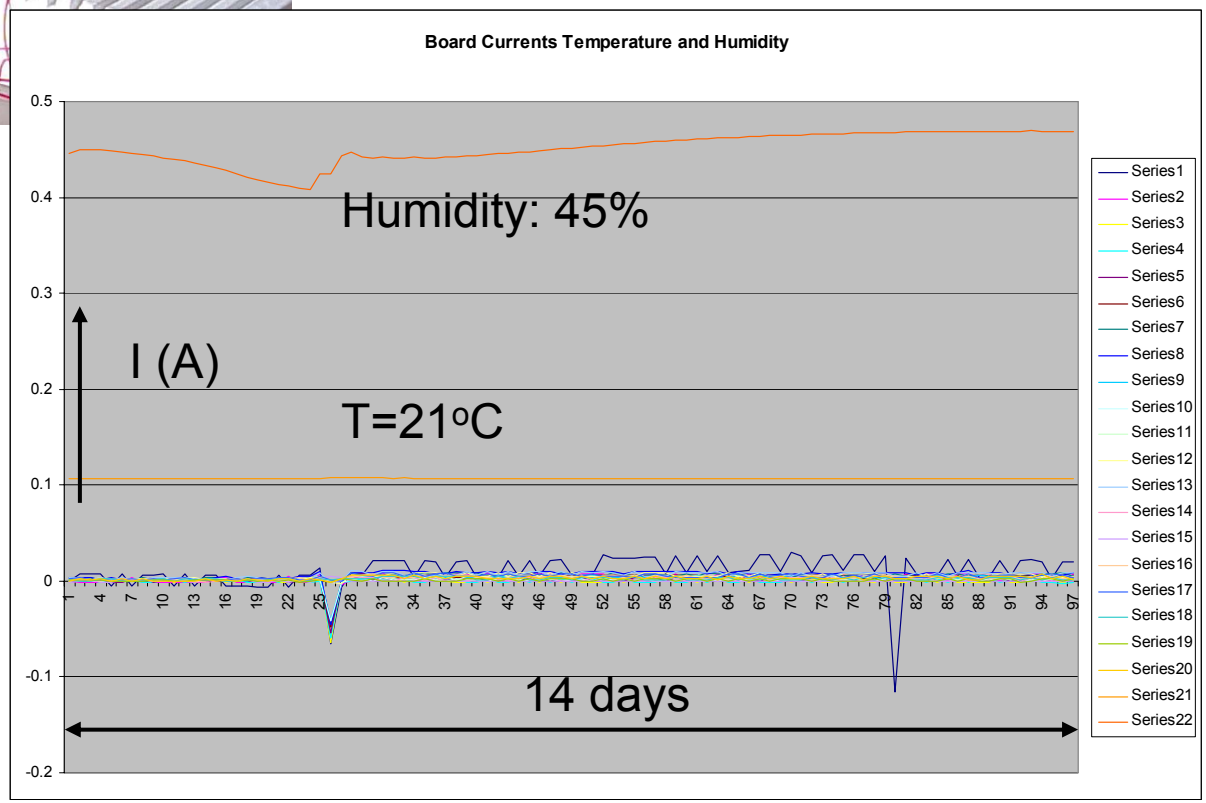
Long term tests:

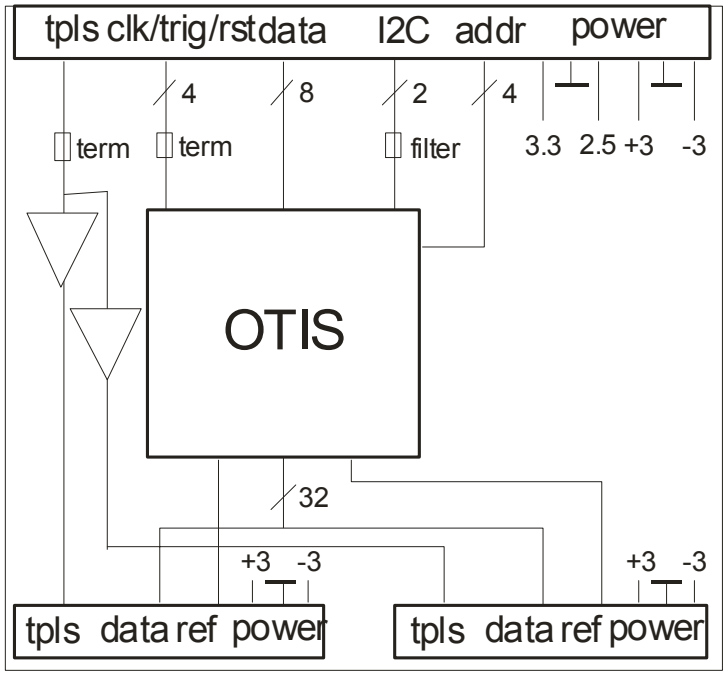
19 boards = 608 channels

1. HV = +2.5 KV, t = 14 days
   → I (32 cha) < 50 nA
   → 1 failing cap

2. Temperature cycling:
   every hour 25-65°C
   HV = +2.5 KV, t = 14 days
   → 1 failing cap

⇨ More studies needed

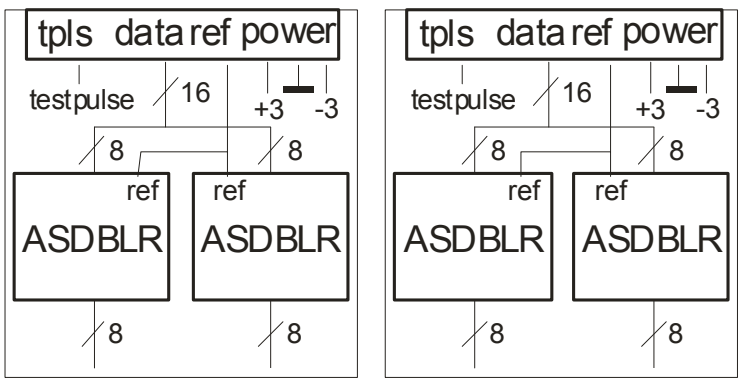




min.
42 pins
connector

TDC board:

- radiation hard OTIS TDC chip
- provides bias voltage for ASD
- power rooting for ASDBLR card
- test pulses for ASDBLR



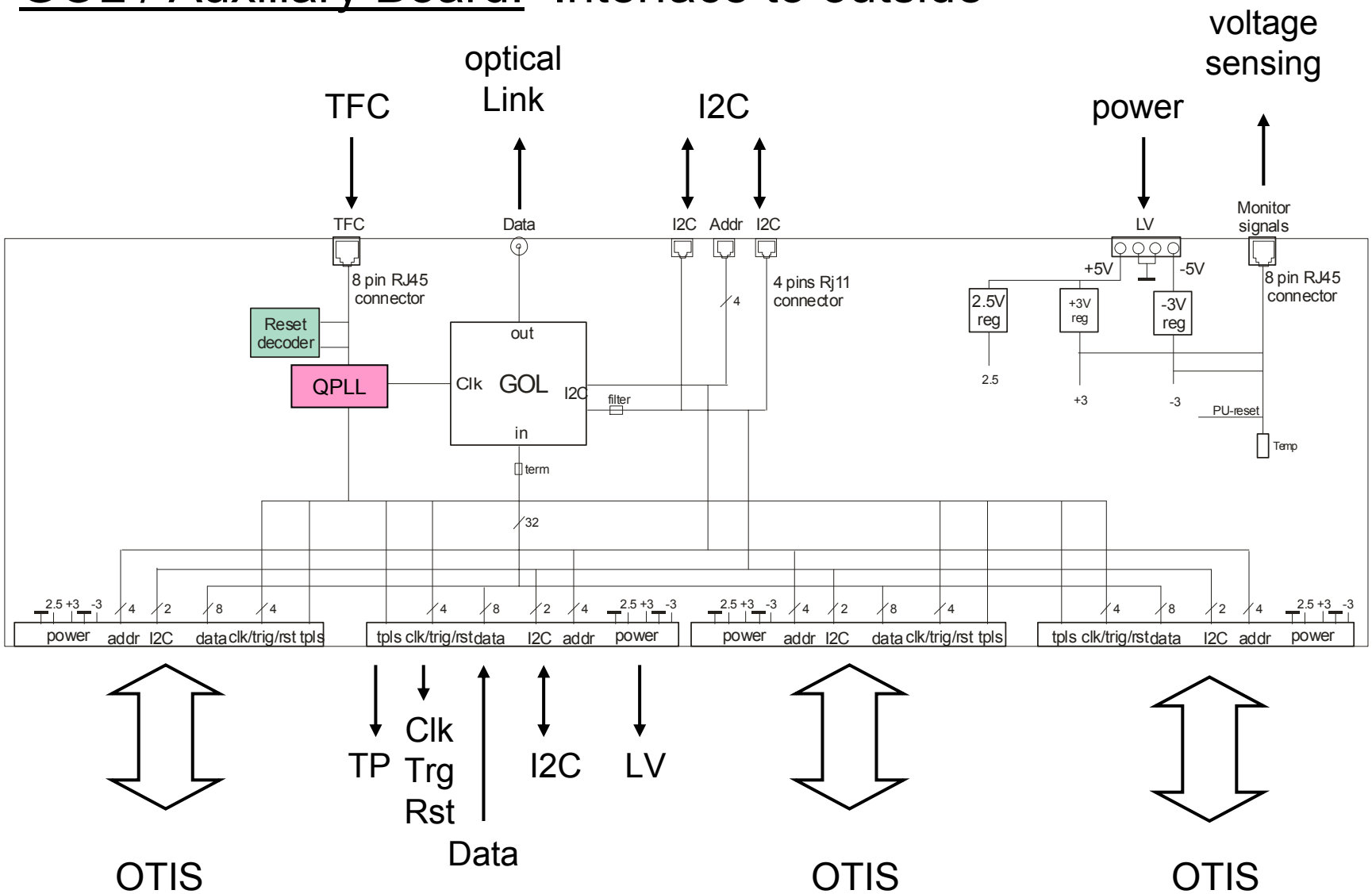
min.
38 pins
connector

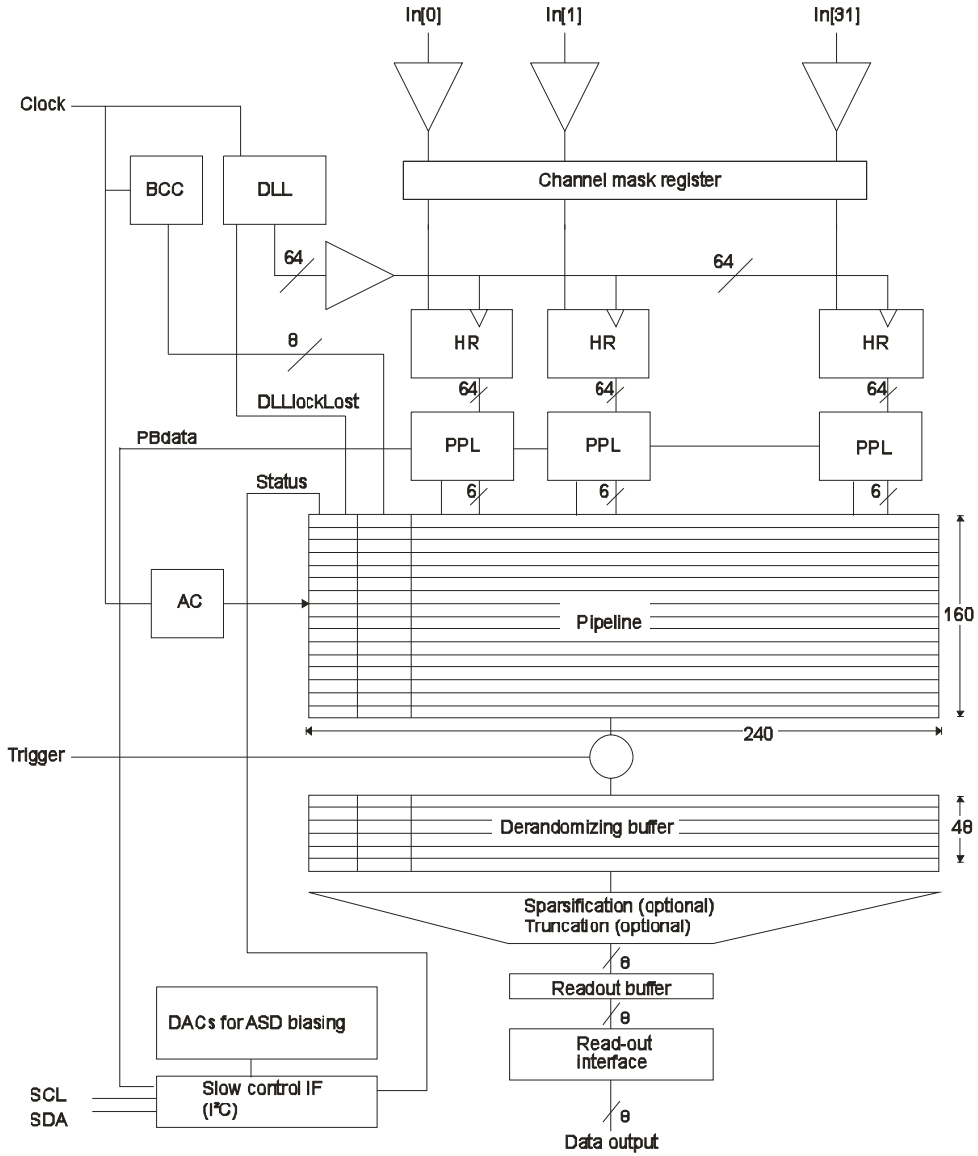
ASDBLR chip:

ATLAS DMILL version 02

⇨ joining ATLAS chip order

GOL / Auxiliary Board: Interface to outside





OTIS TDC Chip

Components:

- **32 maskable channels**
- **DLL, HitRegister, PrePipeline:**
  6 bit drift time encoding:
  1 bit ↔ 0.39 ns (req. resolut. < 1ns)
  playback data feed-in (testing)
- **Pipeline, Derandomizing Buffer:**
  buffer length: 160 evts ↔ 4.0 μs
- **Control Algorithm:**
  Memory and trigger management,
  2 read-out modes: 1, 2, 3 BX/evt
- **I2C Slow Control Interface:**
  Programming, ASD bias setting
- **DAC:** ASD-Chip bias

⇨ **0.25 μm CMOS technology**

OTIS Readout Modes

Problem: max. drift-time 42 ns

→ min. 2 BX / evt

I. All hits of n BX with possible truncation for length > 36 bytes:

→ variable event length

Bit	0..31	32..95	96..101	...	90+(6n)...95+(6n)
Data	Header	2 * Hit-Info	Drift Time 1	...	Drift Time n

II. Single (first) hit mode

→ fixed event length

Bit	0 .. 31	32 .. 39	...	280 .. 287
Data	Header	time 0	...	time 31

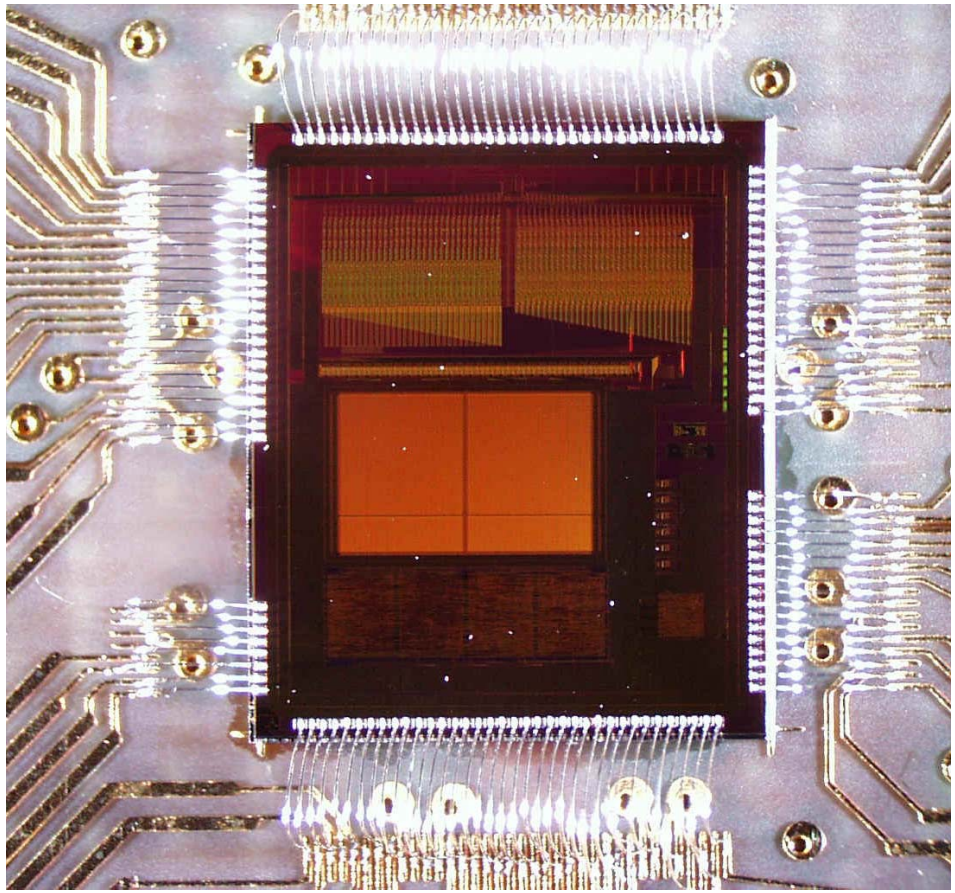
preferred readout mode

⇨ 320 Mbit/s @ 1.1 MHz L0

Hit Position	Data
1. BX	00xxxxxx
2. BX	01xxxxxx
3. BX	10xxxxxx
no Hit	11xxxxxx

OTIS1.0 Prototype

- First prototype with basic functionality
- ~700.000 transistors
- 5100µm x 6000µm
- Submission: 15/04/2002
  Delivery: 29/07/2002
- Small test PCB: possibility to connect ASD and GOL chips



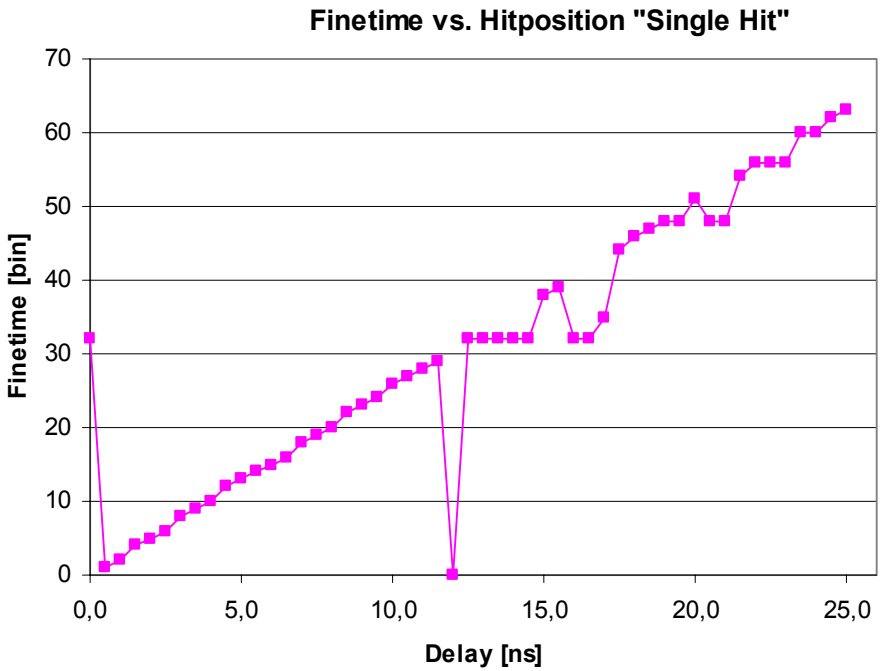
OTIS1.0 Status

DLL Lock Range	29-56 MHz @ 300K 10-90°C @ 40 MHz
DLL Lock Time	≤ 1µs
DLL DNL	0,51 ± 0,03 LSB (≈190ps)

DLL test chip

PowerUp Reset	as expected
Power Consumption	550mW
DLL: Lock Time	≤ 1µs
Lock Lost	not observed
DAC	as expected
Slow Control	as expected
Fast Control: Memory, Data Output, Debug Features	no errors found
Memory Selftest	timing problems
Drift Time Encoding	timing problems

good progress

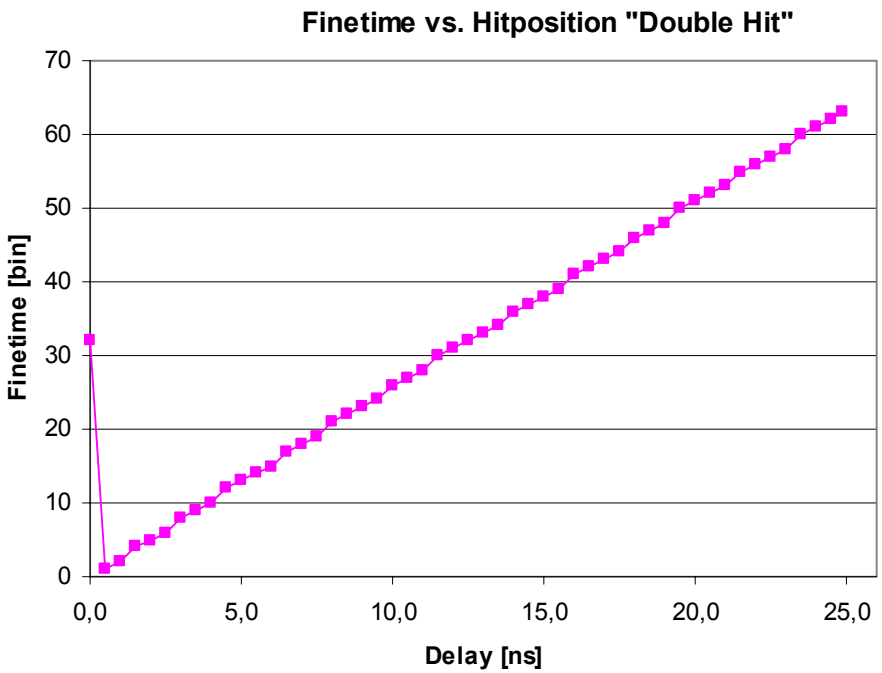


Drift time measurement:

- In 2nd half of BX clock times are not correctly encoded:

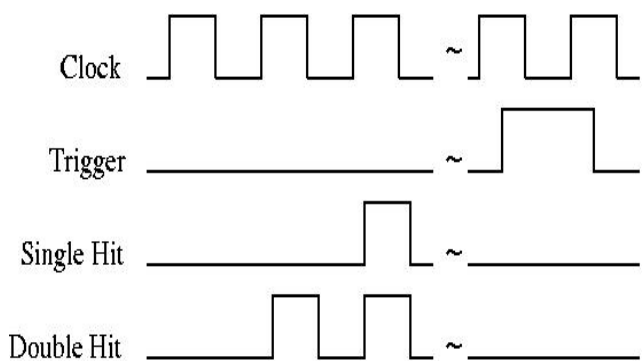
  studies (measurements and simulation) revealed timing problems between data bits and Clk signal at memory input

  reason : parasitic capacities

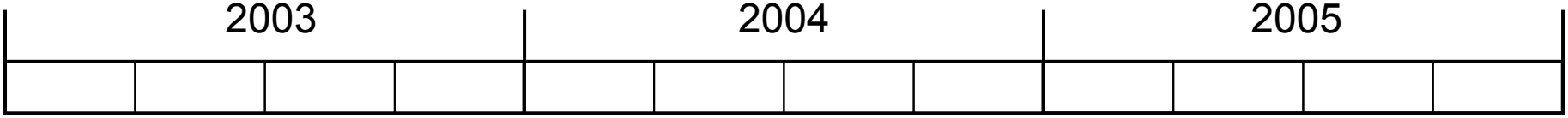


- Double hit measurement:

  1st hit to pre-charge



OTIS Time Schedule



03/03 OTIS chip review

MPW11: Submission OTIS1.1

07/03 Validation of OTIS baseline

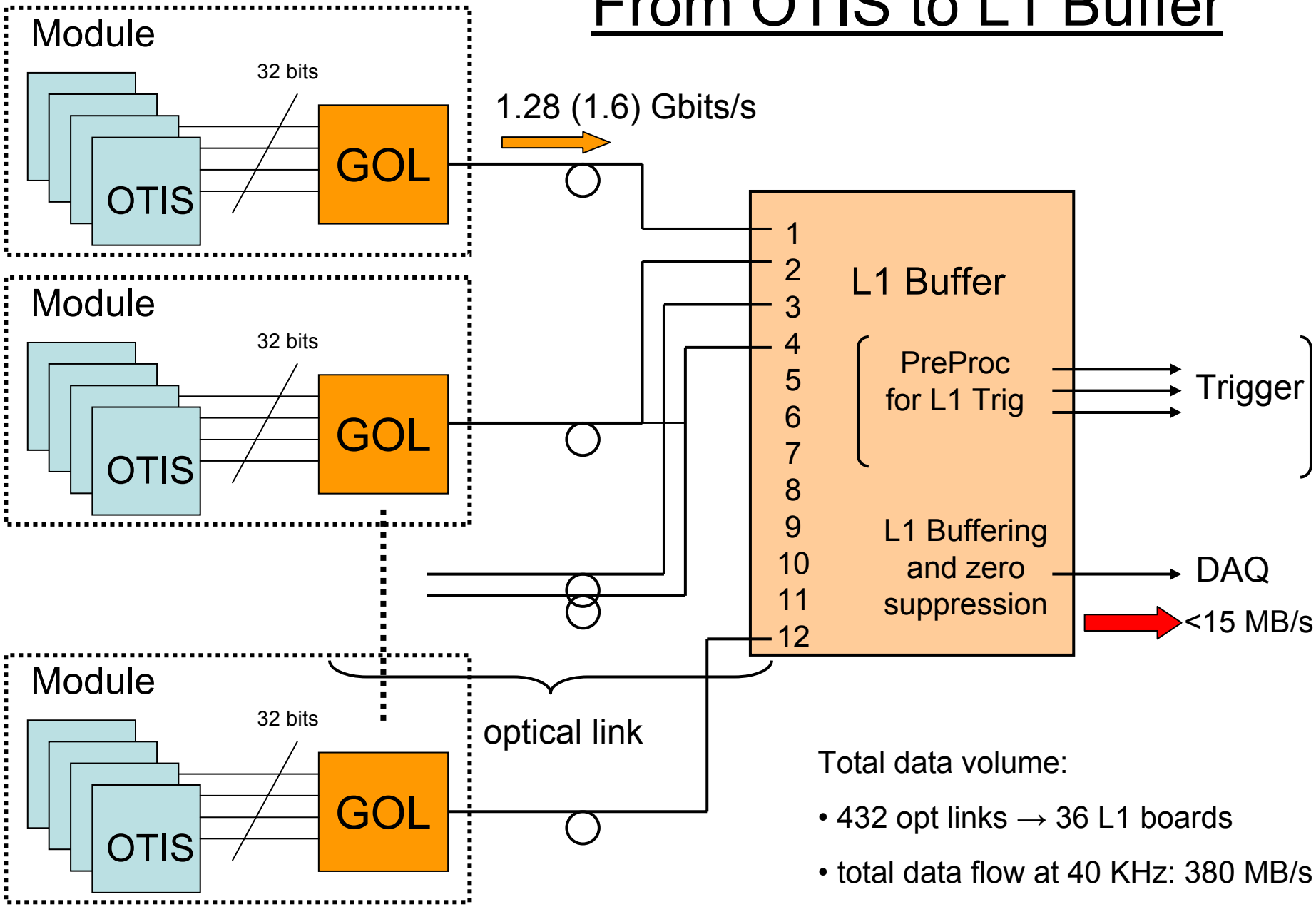
Delivery of OTIS1.1 – Start of test

10/04 OTIS 1.2 Engineering Run

01/05 Delivery of OTIS1.2

03/05 Start Electr Prod

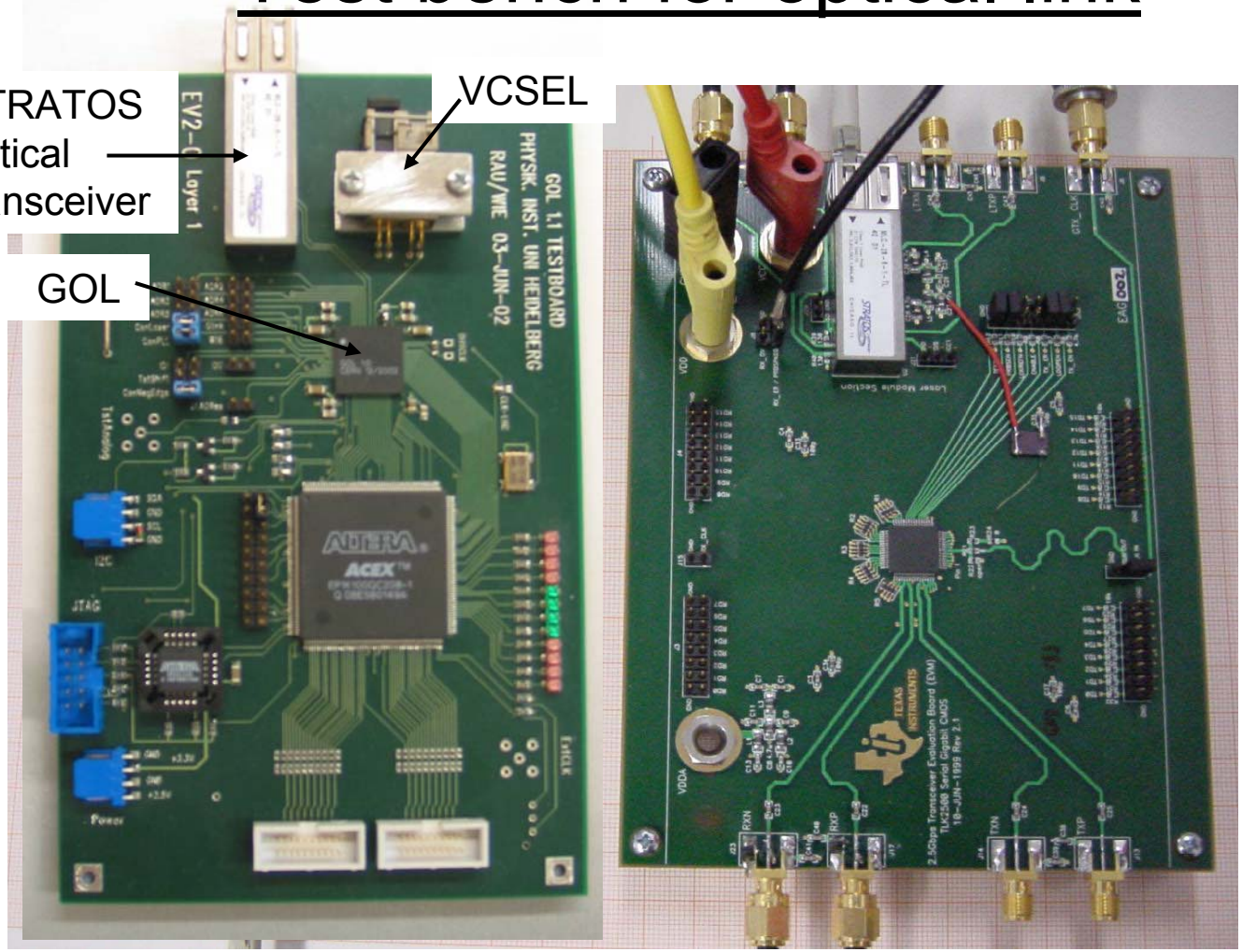
From OTIS to L1 Buffer



Total data volume:

- 432 opt links → 36 L1 boards
- total data flow at 40 KHz: 380 MB/s

Test bench for optical link

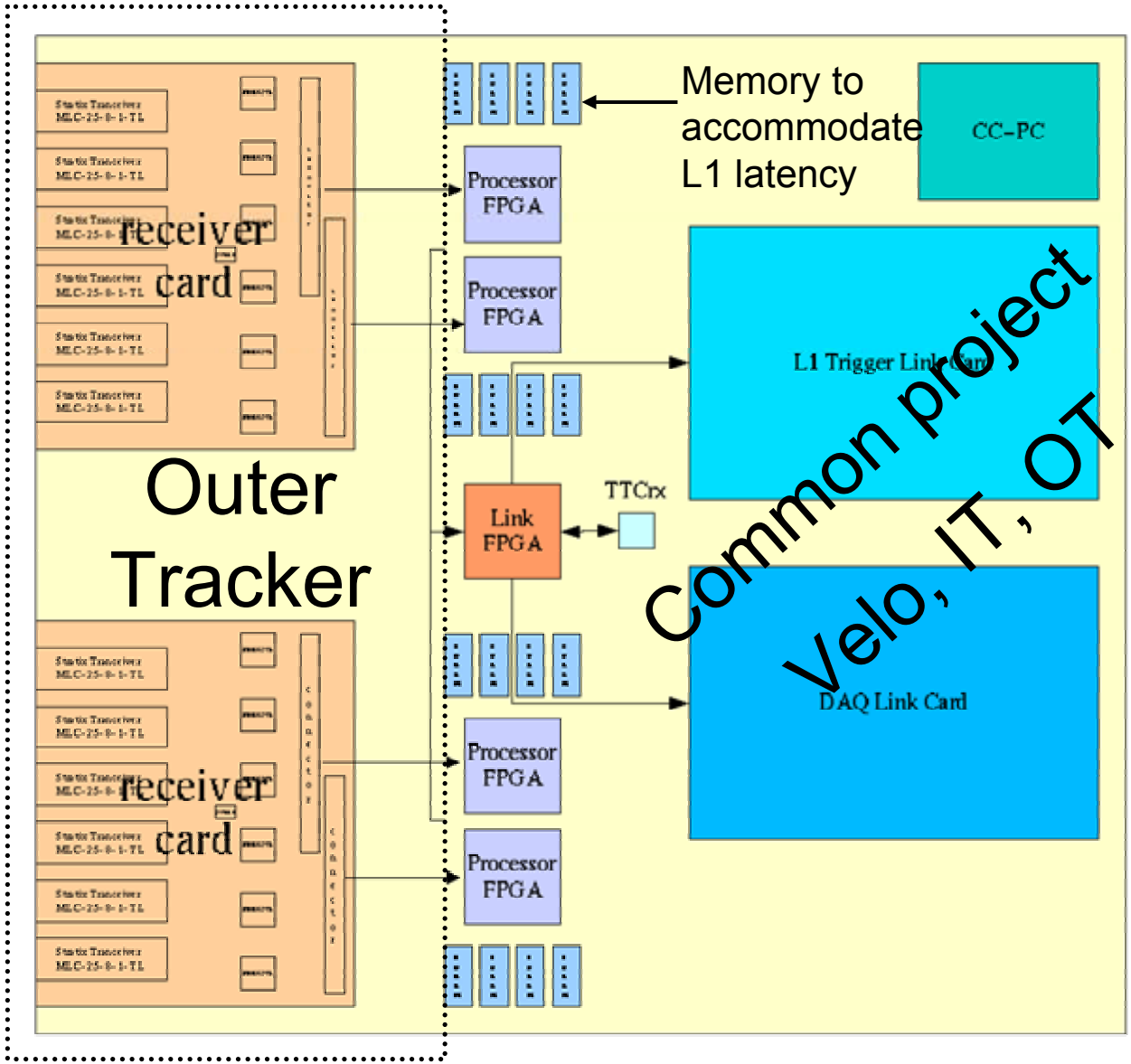


GOL Test board: GOL + VCSEL

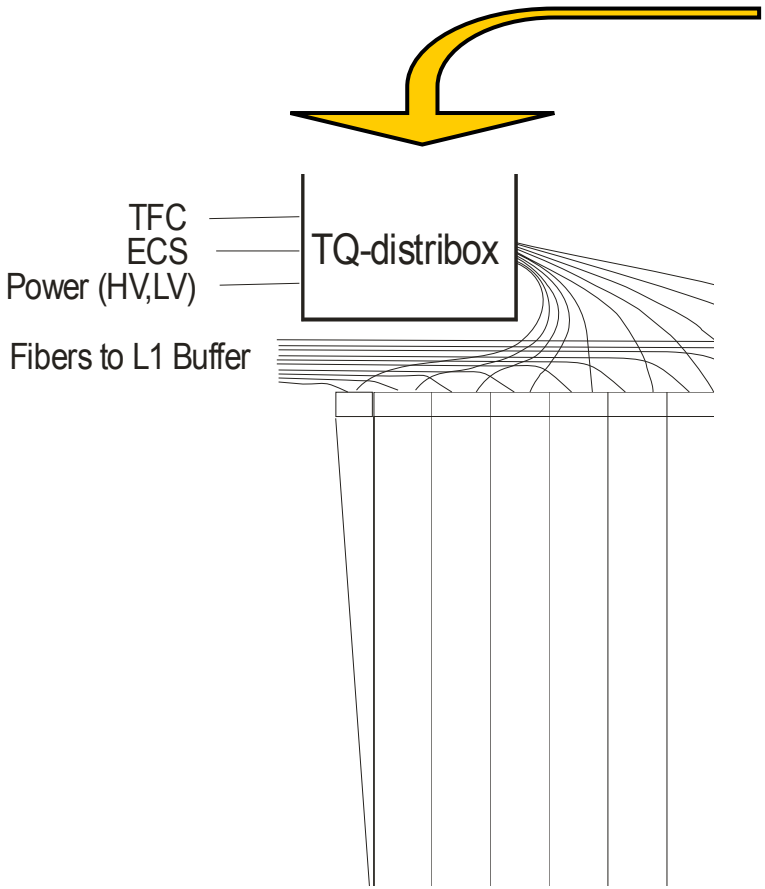
TI TLK2501 evaluation board

⇨ Error rate < 10^{-13}

L1 Buffer Board:



Services:



1 service box / quadrant

Service Box

TFC:

TTCrx + Rst Decoder → LVDS Signals → modules

ECS:

SPECS Slave → I2C bus lines → modules

→ JTAG → ADCs → LV sensing

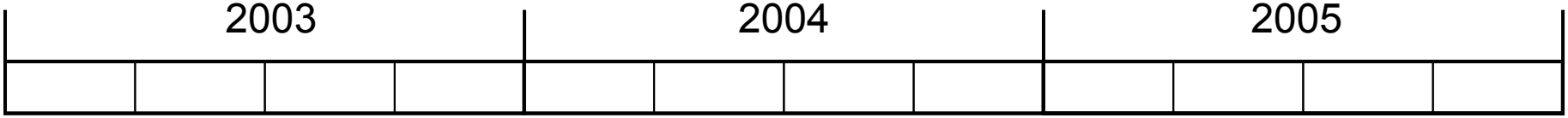
Low Voltage:

passive +/- 5V distribution → modules

High Voltage:

passive distribution → 2 connections/modules

Outer Tracker Electronics: Time Schedule



07/03 Validation of OTIS baseline

10/03 Delivery of OTIS1.1

03/04 Start pre-series production

06/04 Pre-series finished: start mounting

01/05 Delivery of OTIS1.2

03/05 Start Mass Prod