27.05.2002

OTIS1.1 Reset Handling

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Introduction
Throughout the whole LHCb experiment the LHC bunch crossing clock and associated time critical clock synchronous control signals will be distributed through the Timing and Fast Control (TFC) system [1]. The TTCrx chip [2] will be used as an interface between the TFC system and its signal receiving front end users. The following sections describe how the OTIS chip uses the TFC- and other signals to reset and/or to synchronise itself to the LHC bunch crossing clock.

Power Up Reset
The OTIS chips automatically performs a power up reset after each power cycle [3]. After power on, the chip is in reset state for up to 100ms depending on the capacity coupled to the power up reset pad. Without a power cycle, a power up reset can be obtained manually if the power up reset pad is pulled to ground.
Internally the power up reset signal is used to set all configuration registers to zero and to bring the I^2C interface into a state ready to recieve data. As the power up reset affects all configuration registers, it is recommended that latency and read out mode are programmed anew in order to meet LHCb specifications. Without reprogramming the configuration registers after a power up reset the chips default configuration provides a minimum set of functionality. Then, the pipeline read pointer will just follow the write pointer (i.e. latency: 0) and in case of a trigger, the data output would be of fixed length (i.e. read out mode: single hit; search window: 1).

Global L0 Reset
The global L0 reset signal provided by the TFC system is used to start data taking synchronously in all parts of the system. Most probably the TFC system will broadcast the L0 reset signal in regular intervalls (and then at the beginning of a new LHC machine cycle) [4]. The OTIS chip uses the L0 reset signal

- to reset pipeline- and derandomizing buffer pointers,
- to adapt to programmed parameters (e.g. operation mode or latency),
- to bring all finite state machines into a defined state ready for data taking and to
- reset the bunch crossing counter.

The OTIS chip starts acquiring data with the first LHC clock cycle after the L0 reset signal was released. And, depending on the programmed latency, the chip will start accepting trigger signals `latency` clock cycles after the L0 reset.

Bunch Crossing ID Reset
In order to check synchronisation of the complete front-end system, a bunch crossing ID gets assigned to every triggered data sample. The bunch crossing numbers within each data set can be checked against the numbers provided by the TFC system. In addition the TFC system distributes a clock synchronous reset signal to reset and restart the bunch crossing counters within the front-end electronics synchronous to the beginning of an LHC machine cycle. As the bunch crossing numbers are supposed to be attached to triggered data sets as they enter the derandomizing buffer [4], the bunch crossing ID reset signal is applied `latency` clock cycles after the LHC machine cycle started.
In contrast to the supposed scheme, the OTIS chip attaches a bunch crossing number to each acquired data set as soon as data enters the pipeline. Therefore the OTIS chip uses the global L0 reset signal to start its bunch crossing counter. The bunch crossing ID reset signal is used to preload (offset: `latency`) and restart the counter. For both schemes, the data sets read from the derandomizing buffer show no offset in between the two attached bunch crossing numbers.

Since the bunch crossing counter of the OTIS chip is 8bit wide, the allocated numbers are not unique, but it is still possible to set up and maintain synchronisation by comparing eight least significant bits.

Event ID Reset
A second means to provide and check correct synchronisation between all parts of the experiment is to count the number of accepted events. The event counter will be reset by the event ID reset signal distributed through the TFC system. If applied, the event ID reset signals will occur synchronous to the bunch crossing ID reset signals.
Because it is not mandatory for front-end chips to provide an event ID in the data output stream, the event counter of the OTIS chip is only accessible through its I²C interface and is therefore only of limited use for synchronisation purposes.

DLL Reset
All fast control signals distributed by the TFC system should be used in a way that data taking could be resumed within a few clock cycles [4]. Therefore these reset signals cannot be used to reset the Delay Locked Loop (DLL) of the OTIS chip because the DLL needs up to 1µs to reach its lock state which is needed to acquire valid data. So far, the only available signal to reset the DLL is the power up reset signal.

According to the reset scheme of the GOL chip [5] it is proposed to introduce the following:
A chip internal watchdog circuitry is used to observe the DLL lock state for every clock cycle. The lock state information will be attached to the data sets entering the pipeline. If the number of consecutive clock cycles with lost DLL lock exceeds a programmable limit, the DLL gets resetted automatically (making acquired data invalid for approx. 1µs). In addition, a reset of the DLL can be obtained manually via the I²C interface or the DLL reset pad. The latter is only useful while operating the chip at the laboratory and for test purposes. The DLL reset pad will not be accessable in the LHCb experiment.
Four different DLL lock scenarios are possible:

- DLL is locked
- Soft lock lost due to SEE, noise, etc. (number of lost locks below programmable limit)
- Hard lock lost due to internal/automatical reset (number of lost locks above programmable limit)
- Hard lock lost due to external/manual reset
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In principle, one lock lost bit within the header of the data output stream is sufficient to flag a lock lost situation to the subsequent DAQ stage. In some cases, depending on the trigger sequences, it is possible to distinguish between the different lock lost scenarios by examining the number of lock lost bits in successive read out sequences. But by introducing a second lock lost bit and encoding the different reasons for a lost DLL lock to the data output stream one would gain more transparent information (e.g. for test purposes) about the lock state of the DLL. Again – for test purposes – one could think of counting the different lock lost scenarios and making the numbers available via I^2C interface.

References
[1] Timing and Fast Control, R. Jacobsson et al, LHCb Technical Note, LHCb DAQ 2001-16, 15.06.2000
[2] TTCrx Reference Manual, J. Christiansen et al, Version 3.6, June 2002
[3] The OTIS Reference Manual, U. Stange et al, Version 1.0, September 2002
[4] Requirements to the L0 front-end electronics,
J. Christiansen, LHCb technical note, LHCb 2001-014, 03.07.2001
[5] GOL Reference Manual, P. Moreira et al, Version 1.1, January 2002