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OTIS - a TDC chip for the LHCb Outer Tracker

Status Report for the Chip Review on June 5, 2003

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1 Introduction

The OTIS chip is a clock driven TDC chip developed for the readout of the LHCb Outer Tracker straw tubes. A first complete version of the chip, OTIS1.0 was submitted in April 2002. The prototype has undergone intensive tests and is essentially understood by now. A second version of the chip, OTIS1.1 is currently in preparation. OTIS1.1 is supposed to include all features of the final chip.
This document tries to summarize the specifications, the architecture and the current status of the chip in a compact form.

2 A TDC chip for the LHCb Outer Tracker

LHCb Outer Tracker readout electronics

The digitization of the Outer Tracker drift-tube signals is done with the ATLAS (DMIL) version of the amplifier-discriminator chip ASD-BLR. To avoid expensive and voluminous cabling the TDC chips must be mounted next to ASDs. The chip should provide clock synchronous time digitization and data buffering for the fixed latency of the L0 trigger. On an L0 accept signals the digitized hit time events of always 4 OTIS chips are fed to the 32 bit inputs of the GOL serializer chip. The serialized data is optically transmitted (10/8 bit encoding) to the L1 buffer boards. Steering signals such as the 40 MHz bunch crossing clock (BX) which serves as reference for the time measurement, the L0 trigger signal and reset signals are provided by the timing and trigger control (TTC) system. The TDC chip should contain DACs to biasing of the ASD threshold voltages.
An overview of the readout architecture of the LHCb Outer Tracker is shown in Figure 1.

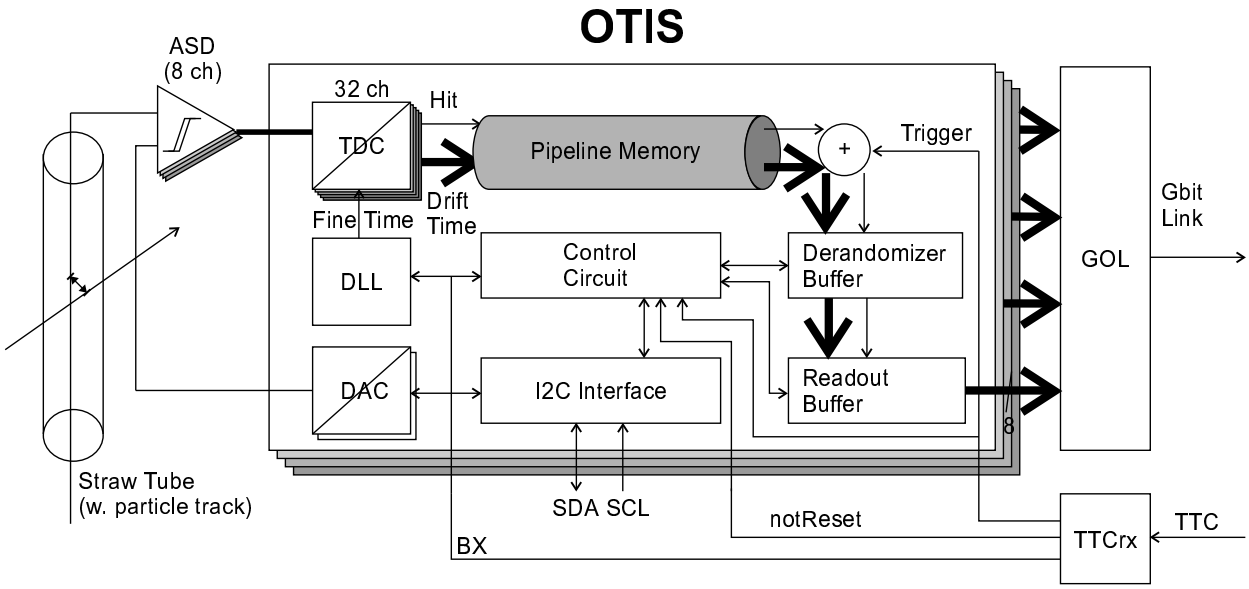


Figure 1: Outer tracker readout schema

Outer Tracker requirements

In the original proposal the OTIS chip was facing high channel occupancies ($> \ 10\%$) and a high radiation level ($>$ 100 krad over the lifetime of LHCb). Therefore, radiation-hard layout techniques together with a commercial 0.25 μm CMOS process are used to guarantee OTIS operations over the lifetime of LHCb. The recent decision not to have any tracking chambers in the area of the dipole magnet has relaxed the demands on the radiation hardness. The expected maximum radiation dose in the area of the TDC chip has now reduced to only 10 krad.

The TDC is clocked with the 40 MHz BX signal of the LHC and should record for every channel only one hit - the first - per bunch crossing. As the double pulse resolution of the ASD-BLR can better than 25μs the correct handling of several hits per single bunch crossing should be enforced.

The maximum drift-time of the straw tubes is larger than 25 μs and therefore demands the readout of several bunch crossings (2 or 3) per trigger. In the case that several bunch crossings are read for every accepted event a channel might have several hits.

To exploit the full spatial resolution of the straw drift-tubes the time resolution of the chip must be better than 1 ns.

For a convenient readout modularity the TDC chip should serve 32 drift-tube channels, i.e. 4 ASD-BLR chips. The TDC chip has to provide 4 threshold voltages for the corresponding ASDs.

Table 1 summarizes the Outer Tracker demands on the TDC chip.

Outer Tracker Requirements	
max. drift-time in $ArCF_4CO_2$ ($ArCO_2$)	37 ns (44 ns)
max. occupancy	10%
double hit sequence	$<$ 20 ns
radiation dose (10 years)	$<$ 10 krad
temp. range	15 ... 70^o C
TDC resolution	$<$ 1 ns

Table 1: Outer Tracker Requirements to the TDC chip

DAQ/L0 requirements

The TDC chip has to fulfill the LHCb L0 specifications summarized in the following table:

DAQ/L0 requirements	
max. L0 rate	1.1 MHz
L0 Latency / Pipeline	4.0 μs / 160 events
BX Counter	12 bit
max. readout time	900 ns
size of Derandomizer	≥ 16

Table 2: L0 Requirements to the TDC chip

Compulsory reset signals and there action:

- BX counter reset:
  Reset bunch counter. Regular reset issued every LHC machine cycle period guarantee correct synchronization of the BX counters.
- Global L0 reset:
  General reset issued at power-up or after parameter reconfiguration. (e.g.: reset state machines).

3 OTIS architecture

The architecture of the OTIS chip is clock driven. The chip operates synchronous to the 40 MHz LHC clock. Main components of the chip are:

- the TDC core, consisting of a DLL, hit register and hit decoder,
- the L0 pipeline buffer together with the derandomizing buffer to cover the L0 latency and to cope with fluctuations of the trigger rate
- the control logic for the trigger and memory management and to prepare the output data
- the I2C interface for setup and slow control

In addition the chip comprises 4 DACs to provide the threshold voltages for the ASD discriminator chips. The block diagram of the OTIS chip is shown in Figure 2.
The chip serves 32 input channels (LVDS) and provides 8 bit wide data output (CMOS differential).

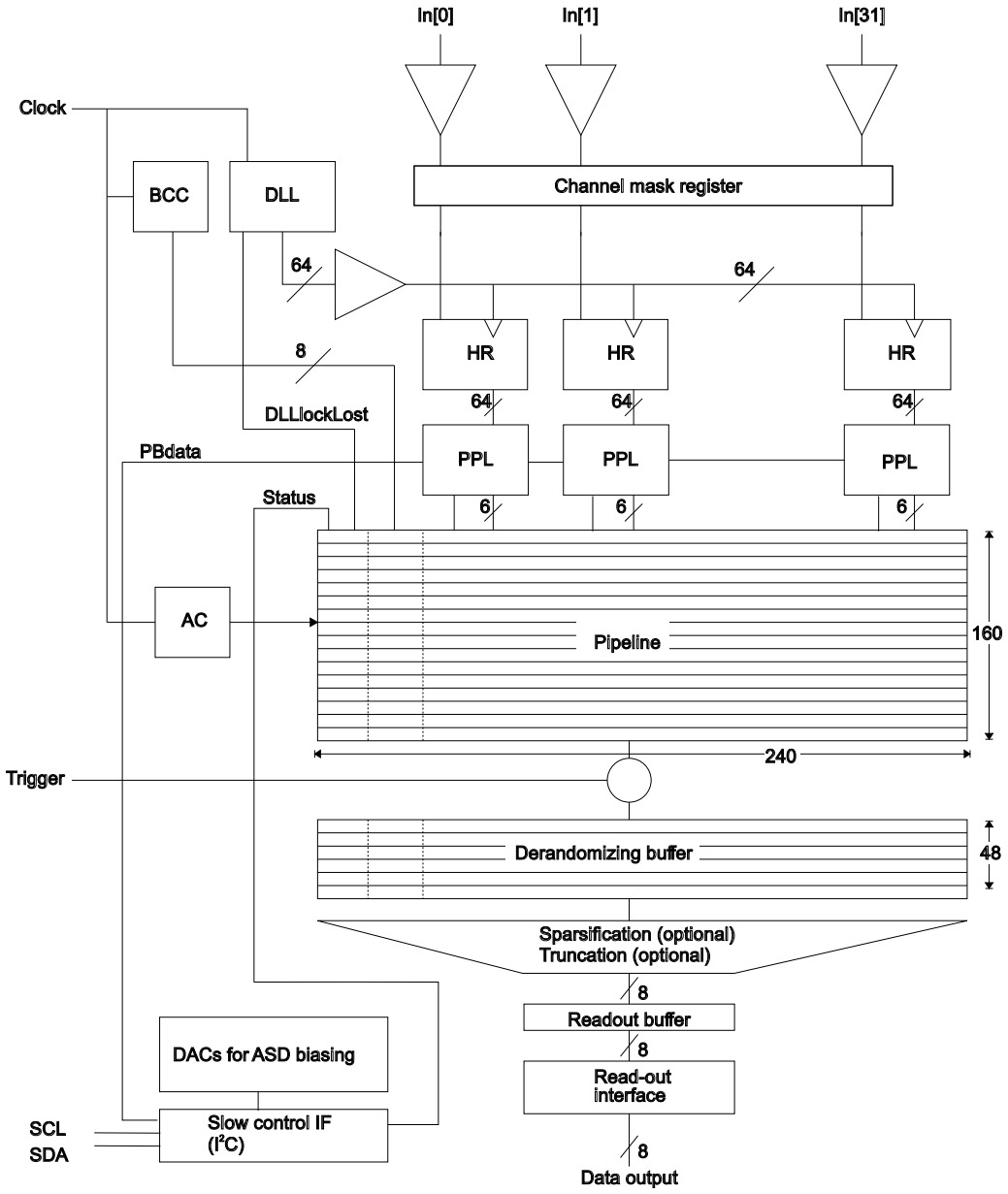

In[0]
In[1]
In[31]
Clock
BCC
DLL
Channel mask register
64
64
8
HR
HR
HR
64
64
64
DLLlockLost
PBdata
PPL
PPL
PPL
Status
6
6
6
AC
Pipeline
160
240
Trigger
Derandomizing buffer
48
Sparsification (optional)
Truncation (optional)
8
Readout buffer
8
DACs for ASD biasing
Read-out
interface
SCL
SDA
Slow control IF
(I²C)
8
Data output

Figure 2:

TDC core

For the time measurement a DLL, consisting of a chain of 32 double staged delay elements, is used. The BX clock propagates through the chain. A phase detector compares the delayed clock with the original one. Depending on the observed phase shift a charge pump adjusts the voltage controlled delay elements until the phase difference vanishes. In this state the DLL is locked and the DLL clock can be used as reference for the time measurements. To decrease the uncertainty of the digitization the number DLL tabs are doubled by using both stages of each of the 32 delay elements. The output of the DLL stages are used to clock 64 hit registers and to latch the the discriminated hit signal. A decoder converts the status of the 64 registers into a 6 bit "fine time".

Pipeline and derandomizing buffer

Pipeline and derandomizing buffer are built as arrays of dual ported SRAM cells. The memory dimensions are 164 events x 240 bits and 48 events x 240 bits respectively. The depths of both buffers are thus larger than required by the L0 specifications.

Control Algorithm

The control algorithm provides trigger and memory management as well as the control of the data output stream. The hardware description language *Verilog* was used to code the algorithm. In addition to simulations the most important parts of the code have been tested on a FPGA.

a) Readout modes:

On a positive L0 trigger the control algorithm can search detector hits in up 3 bunch crossings. In the multi BX modes not all hits can be transmitted within the required 900 ns readout time. Therefore, there are 2 different readout modes to cope with this situation:

1. For every channel hits are searched in the data of up to three bunch crossings. Only the first hit is transmitted. To flag the bunch crossing of the hit, additional two bits are added to the "fine time" value. Channels without valid hits are flagged as "not hit" but are nevertheless transmitted. Table 3 shows the 8 bit coding of the constructed "extended times". In this mode the TDC works as a single-hit TDC for the time span of up to 3 bunch crossings.

Hit position	Data
1st BX	00XXXXXX
2nd BX	01XXXXXX
3rd BX	10XXXXXX
No Hit	11000000

Table 3: Extended time encoding

2. For every bunch crossing a 32 bit hit mask indicates for which channels hits have been found. Fine-times are transmitted only for channels with hits. In case the event data, including the header, is longer than 36 bytes the data is truncated. In this mode the TDC works as multi-hit TDC as long as the channel occupancy is low.

The first readout mode has the advantage of a fixed event length. In addition the time data is byte aligned. It is therefore the preferred readout mode and also the mode implemented in OTIS1.0.

b) Data format

The meaning of the event header bits are summarized in Table 4. The data format of the 2 readout modes are listed in Tables 5 and 6.

Bit	0...11	12, 13	14 ...17	18 ...21	22, 23	24 ...31
Data	ID	0	Status	Readout mode	0	BX counter

Table 4: Event header

Bit	0...31	32...39	...	280...287
Data	Header	Drift time(0)	...	Drift time(31)

Table 5: Data format for the read-out mode (1): single hit, fixed event length

c) Counters and resets

Bunch crossing counter:
The OTIS uses only 8 bits to count the bunch crossings. The counter is thus not

Bit	0...31	32...63	64...69	...
Data	Header	Hit mask (0)	Drift time [1]	...

...	$58+(n\times6)...63+(n\times6)$
...	Drift time[n]

Bit	0...31	32...63	64...95	96...101	...
Data	Header	Hit mask (0)	Hit mask (1)	Drift time [1]	...

...	$90+(n\times6)...95+(n\times6)$
...	Drift time[n]

Bit	0...31	32...127	128 ... 133	...
Data	Header	Hit mask (0) ... Hit mask (2)	Drift time [1]	...

...	$122+(n\times6)...127+(n\times6)$
...	Drift time[n]

Table 6: Data format for the read-out mode (2) - 1, 2 or 3 bunch crossings per event.

unique but will allow nevertheless a synchronization of the detector data. The counter is inserted into the event header and it is set to zero when the `bunch crossing ID reset` is applied for every machine cycle.

L0 event counter:
The L0 event counter of the OTIS will not be added to the data but is accessible via I2C. It is therefore only of limited use. The `event ID reset` signal will reset this counter.

Reset signals:
Beside the mentioned `bunch crossing ID reset` and the `event ID reset` the OTIS foresees the following reset signals:

- `power up reset` (Slow Control)
- `global L0 reset` (Fast Control)
- `DLL reset` (automatic at DLL lock lost or via Slow Control - not implemented in OTIS1.0)

A detailed description of the reset schema can be found in the "Reset Document" available on the web.

d) Implemented debug features:

The chip provides several debug possibilities:

- memory self-test at power-up reset:
  A regular pattern is written to all cells of the memory. After reading the cell information the pattern is verified.
- by-pass the hit registers and write arbitrary data directly into the pipeline (play-back mode).
- readout of the data after the derandomizer using I2C - not implemented in OTIS1.0

4 Evaluation of OTIS1.0 and changes planned for OTIS1.1

Measured chip performance	
Power consumption	550 mW
DLL lock time	$< 1\ \mu s$
DLL lock range	25...60 MHz (10...90^{o}C)*)
DLL lock lost	not observed
DNL**)	0.54 ns
DACs	0...2.5 V***)
Slow Control IF	okay
Fast Control Logic	okay
Memory self test	see below
drift time encoding	see below

**) Temperature range measured with DLL prototype only.
**) DNL measured on the FIB patched chip.
***) No detailed test done.

Table 7: Chip performance as measured with OTIS1.0.

List of known bugs of OTIS 1.0

1. Drift time encoding:
   OTIS1.0 showed a problem for the hit time encoding. Shifting a hit signal

in steps of 100 ps across a complete BX cycle and measuring the 6 bit fine-time one expects a linear behavior. For the first half of the BX cycle (0 ns to $\equiv$ 12 ns) this behavior is found. As shown in the following Figure (page 11) the encoded fine-times are incorrect for the second half of the BX cycle.

The problem is meanwhile understood. It is caused by timing violations - mainly due to parasitics - in the signal path from the pre-pipeline logic to the pre-pipeline register. The problem has been solved for 3 channels with a FIB patch. The Figure on p. 12 shows the result of the above time scan for the FIB patched chip.

To compensate the parasitic capacities the signal routing and the driver strength have to be improved for OTIS1.1. In addition the clock timing for storing the fine-time and the HitBit will be relaxed.

2. HitBit information lost or propagated to the subsequent BX:
   Measuring fine-times in the second half of the bunch clock cycle - as described above - the HitBit for a fraction of the hits is lost. The behavior is strongly correlated with the fine-time encoding problem. The changes described above will also solve this problem. A confirmation are the FIB patched channels for which the HitBit is correctly transmitted.

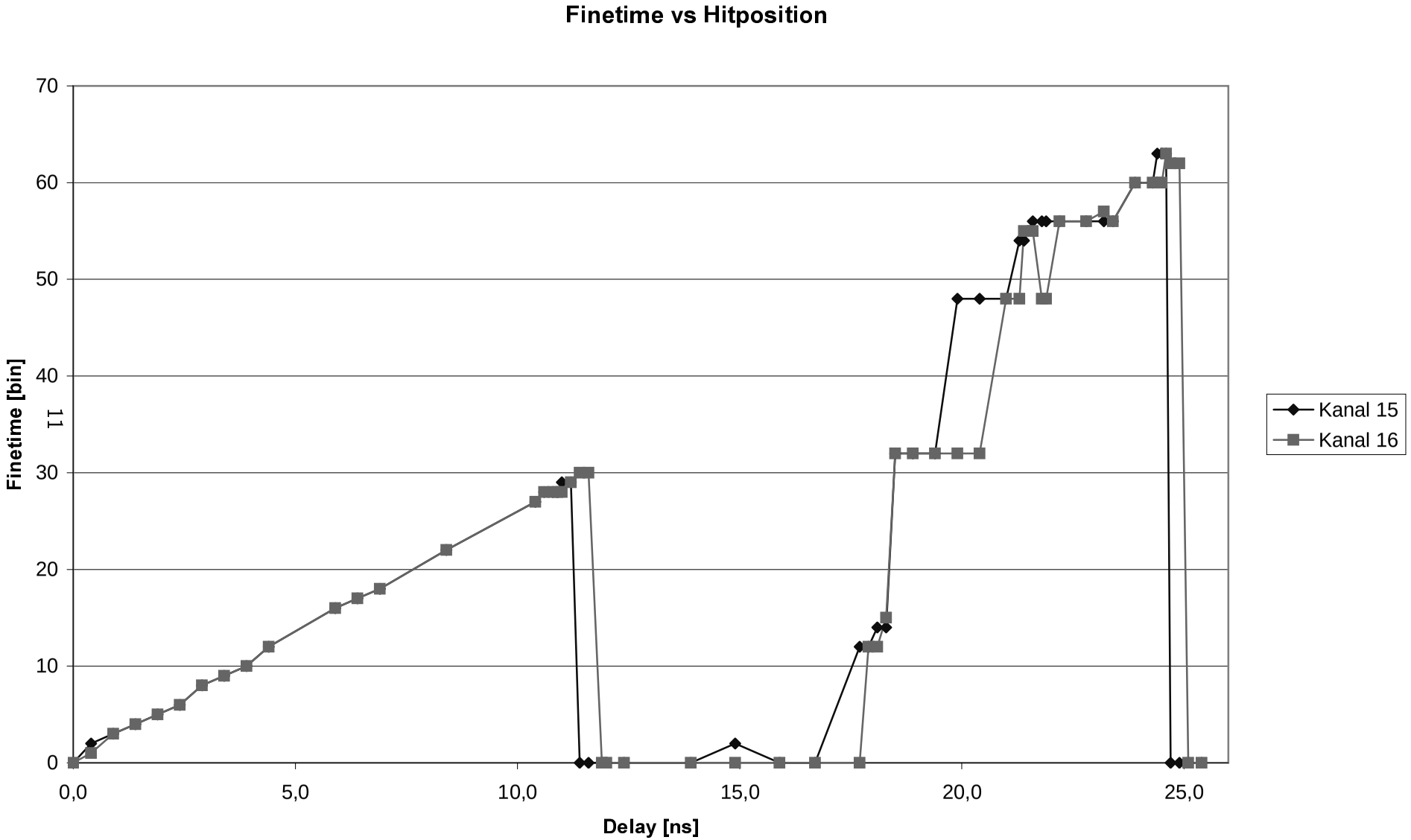
3. Memory self-test: For the memory self-test a dependency on the clock frequency is observed. While the test fails at clock frequencies of 40 MHz already after 100 cycles out of the necessary 5000 cycles the self-test passes all 5000 cycles successfully at 35 MHz. This feature is under study but so far not understood. Due to a understood bug in the `Verilog` code the self-test does not stop if case that no errors appear.

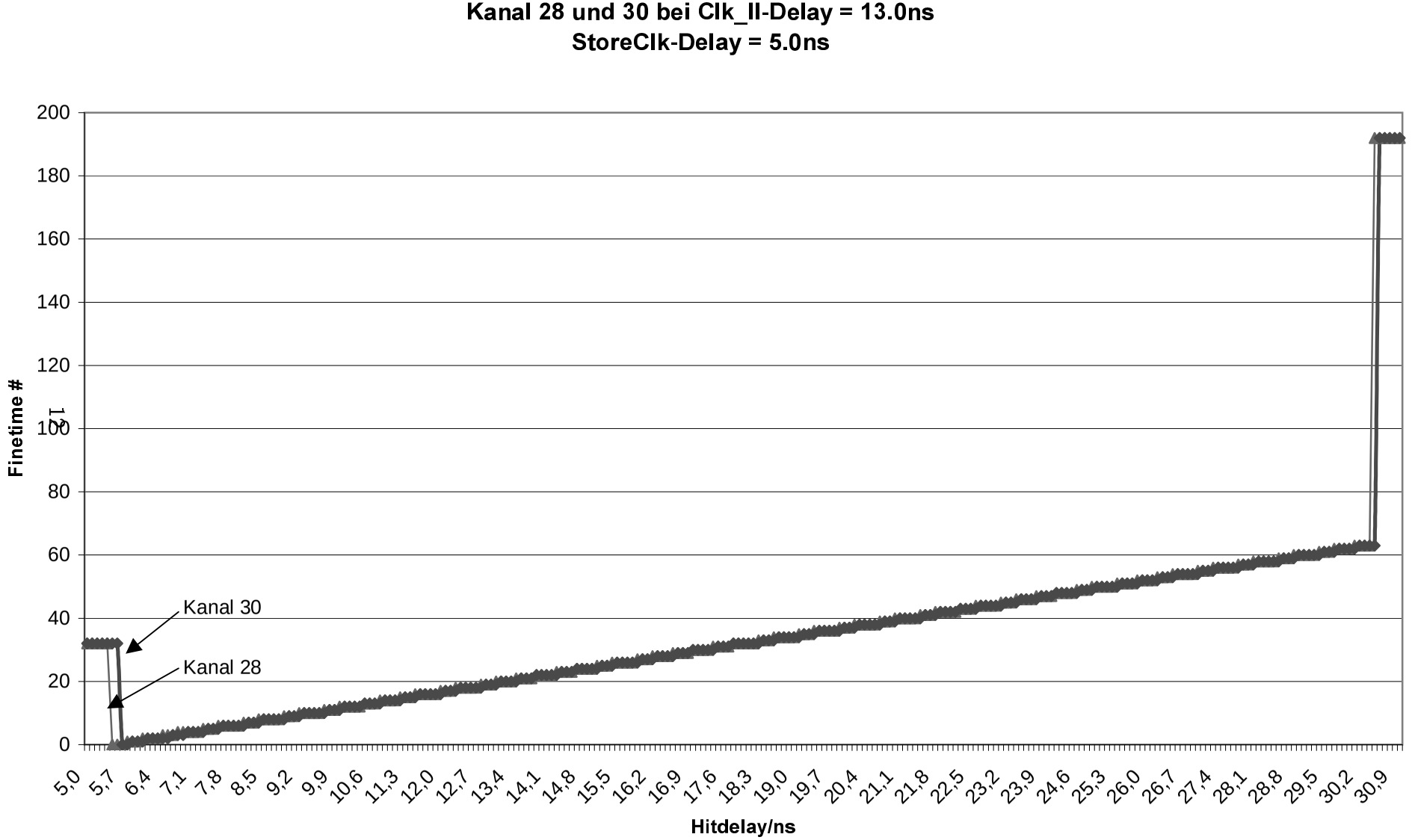
4. BX counter The time behavior of the BX counter for the FIB patched OTIS1.0 does not agree with the simulations. The feature is under study.

New features and changes for OTIS1.1

1. accommodate to new specification for input signals (assumed double pulse resolution now 20 ns - old assumption 40 ns):
   necessary changes in the pre-pipeline-logic and in the MUX to guarantee the correct drift-time of the first hit.

2. check of DLL lock state and implementation of an internal reset mechanism for the DLL (similar to the GOL).


Finetime vs Hitposition
Finetime [bin]
Delay [ns]
0
10
20
30
40
50
60
70
0,0
5,0
10,0
15,0
20,0
25,0
Kanal 15
Kanal 16


Kanal 28 und 30 bei Clk_II-Delay = 13.0ns
StoreClk-Delay = 5.0ns
Finetime #
Hitdelay/ns
Kanal 30
Kanal 28
200
180
160
140
120
100
80
60
40
20
0
5,0
5,7
6,4
7,1
7,8
8,5
9,2
9,9
10,6
11,3
12,0
12,7
13,4
14,1
14,8
15,5
16,2
16,9
17,6
18,3
19,0
19,7
20,4
21,1
21,8
22,5
23,2
23,9
24,6
25,3
26,0
26,7
27,4
28,1
28,8
29,5
30,2
30,9

3. implementation of second readout mode: sending multiple hits per channel with possible data truncation
4. introduce a comma (0xFF) into the output data stream for events of non-consecutive triggers (this helps to synchronize the optical link)
5. I2C ID and chip ID will be decoupled: 8 bit I2C ID, 12 bit chip ID, both as externals pads
6. use 5 V compatible I2C pads
7. fix the fine-time encoding and the HitBit problem: take the parasitic capacities for the timing design of the TDC core into account
8. additional current drivers for the DACs used to bias the ASDs
9. Features for better testability: it is discussed to include a JTAG boundary scan
10. include I2C readout
11. change the 8 bit data output from LVDS to differential CMOS.