LogicBox

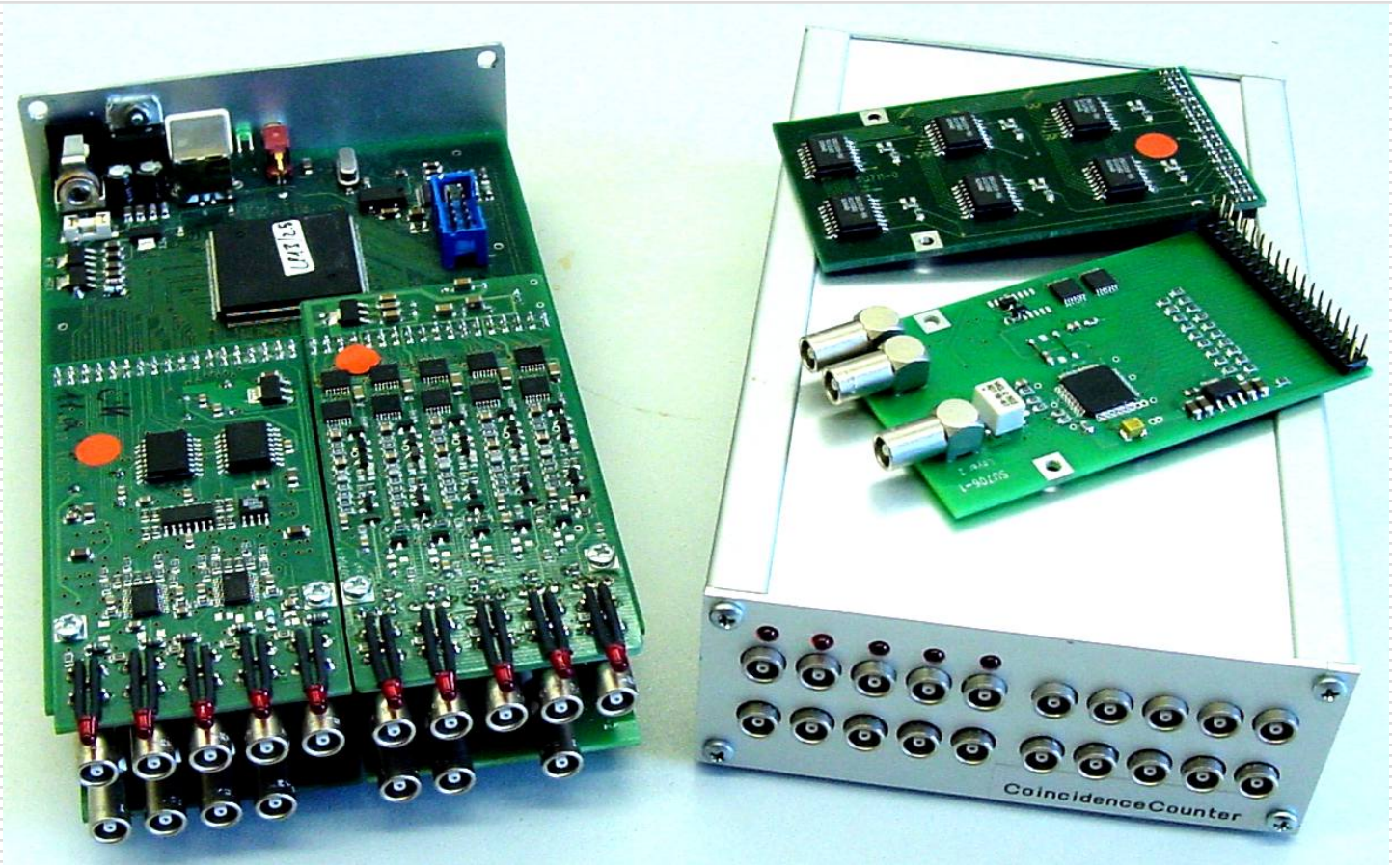
A universal, FPGA-based Control & DAQ System.

- Hardware
  - DL7xx
  - SU7xx
- Firmware (LogicPool)
  - Conception
  - Function Modules
- Future

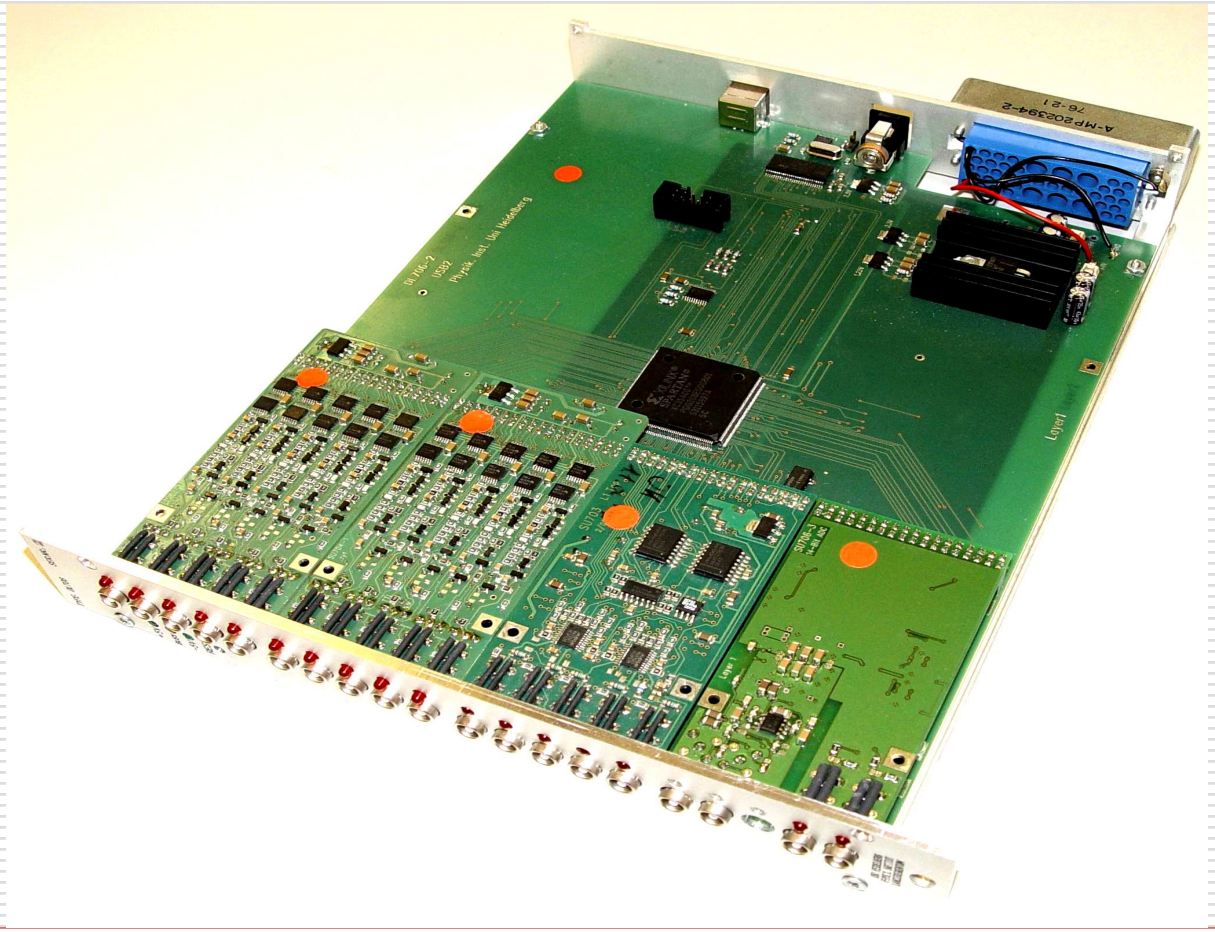
LogicBox: Hardware

- DL7xx: FPGA-Box
  - Digital Logic: FPGA
  - Interface: USB, (Ethernet)
- SU7xx: exchangable Submodule
  - Digital I/O: TTL, TTL^{coax}, NIM, LVDS, ...
  - Analog I/O: Discriminator, ADC, DAC, ...
  - Display: LEDs
  - Internal Extensions: Memory, Delay...
  - Application specific: Controller, IF, ...

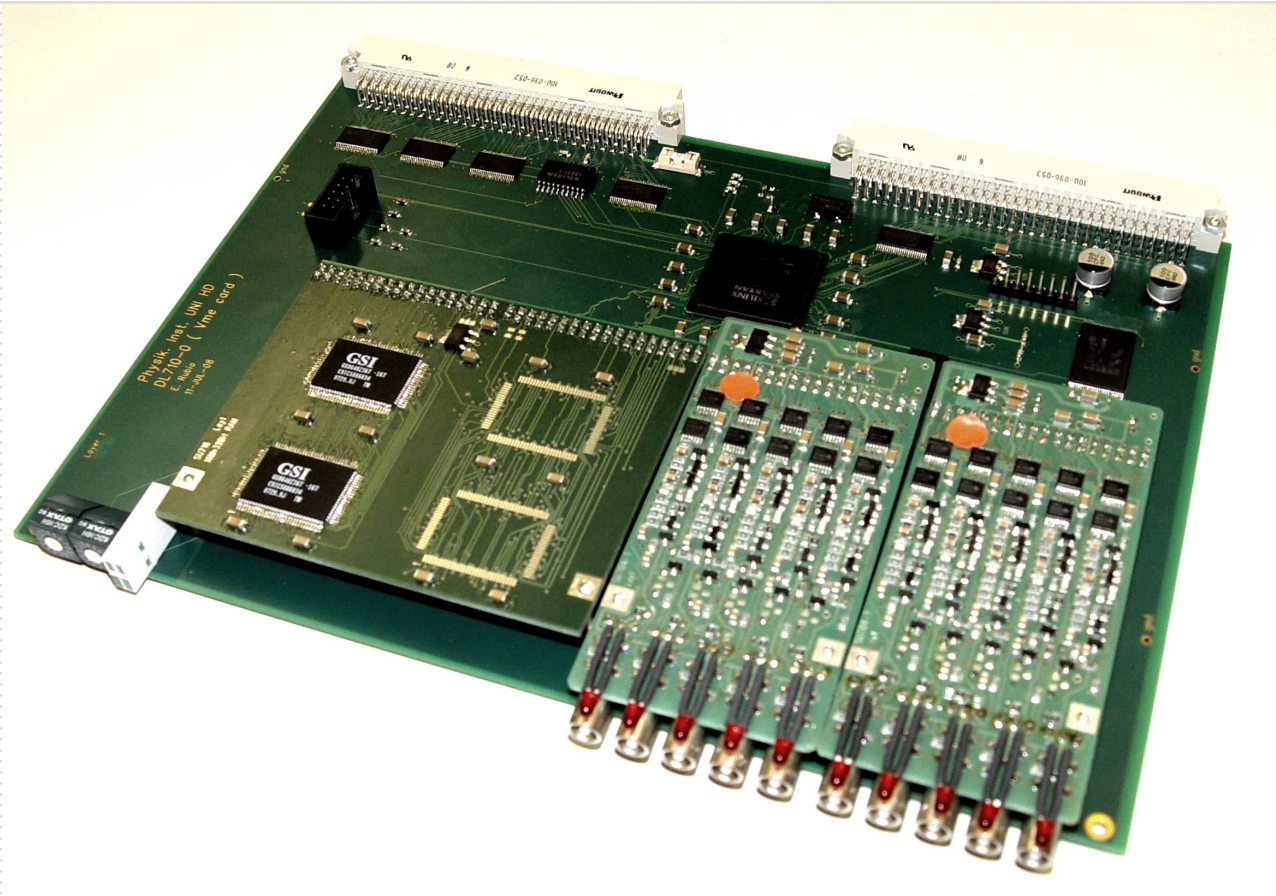
DL701: FPGA Box



DL706: NIM



DL710: VME



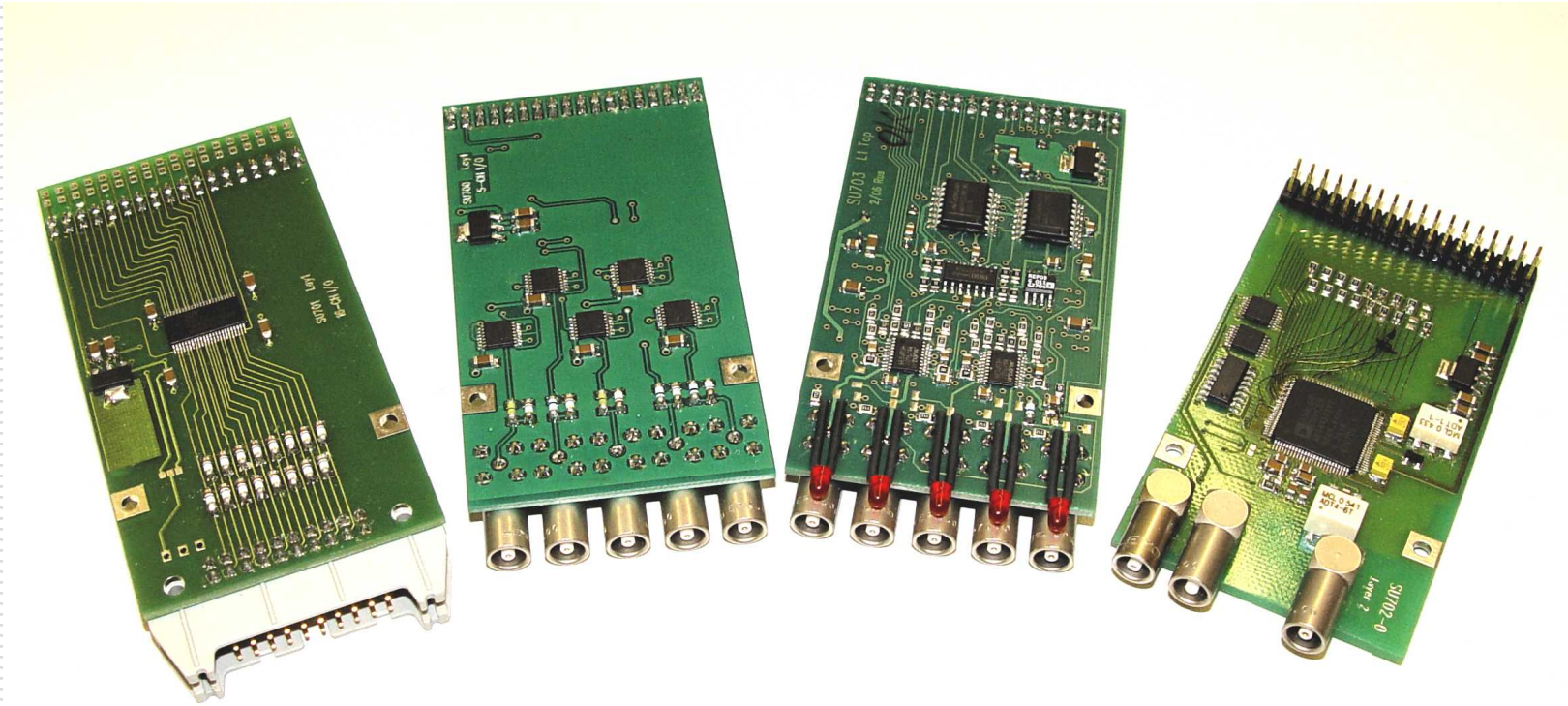
LogicBox: FPGA Boards (DL7xx)

Typ	Form factor	IF	FPGA	Remarks
DL701	3HE/4 SU	USB 1.1	XC3S400	
DL702	6HE/4 SU	VME	Altera	Not compatible!
DL703	3HE/4 SU	Parallel	XC3S400	
DL704	3HE/4 SU	Parallel	-	
DL705	3HE/4 SU	USB 2.0	XC3S400	
DL706	NIM/4 SU	USB 2.0	XC3S400	
DL707	3HE/4 SU	USB 2.0	XC3S4000	
DL708	NIM/4 SU	USB 1.1	XC3S400	
DL709	NIM/8 SU	USB 2.0	XC3S4000	
DL710	6HE/4 SU	VME	XC3S4000	
DL711	NIM/8 SU	SU7xx	XC3S6xx	Memory, SFP

USB 2.0: - Firmware via USB loadable.
- LogicPool Setup in Powerup saved

SU7xx: - Modular Interface (USB, Ethernet, ...)

SU7xx: Sub-Boards



LogicBox: Sub-Boards (SU7xx)

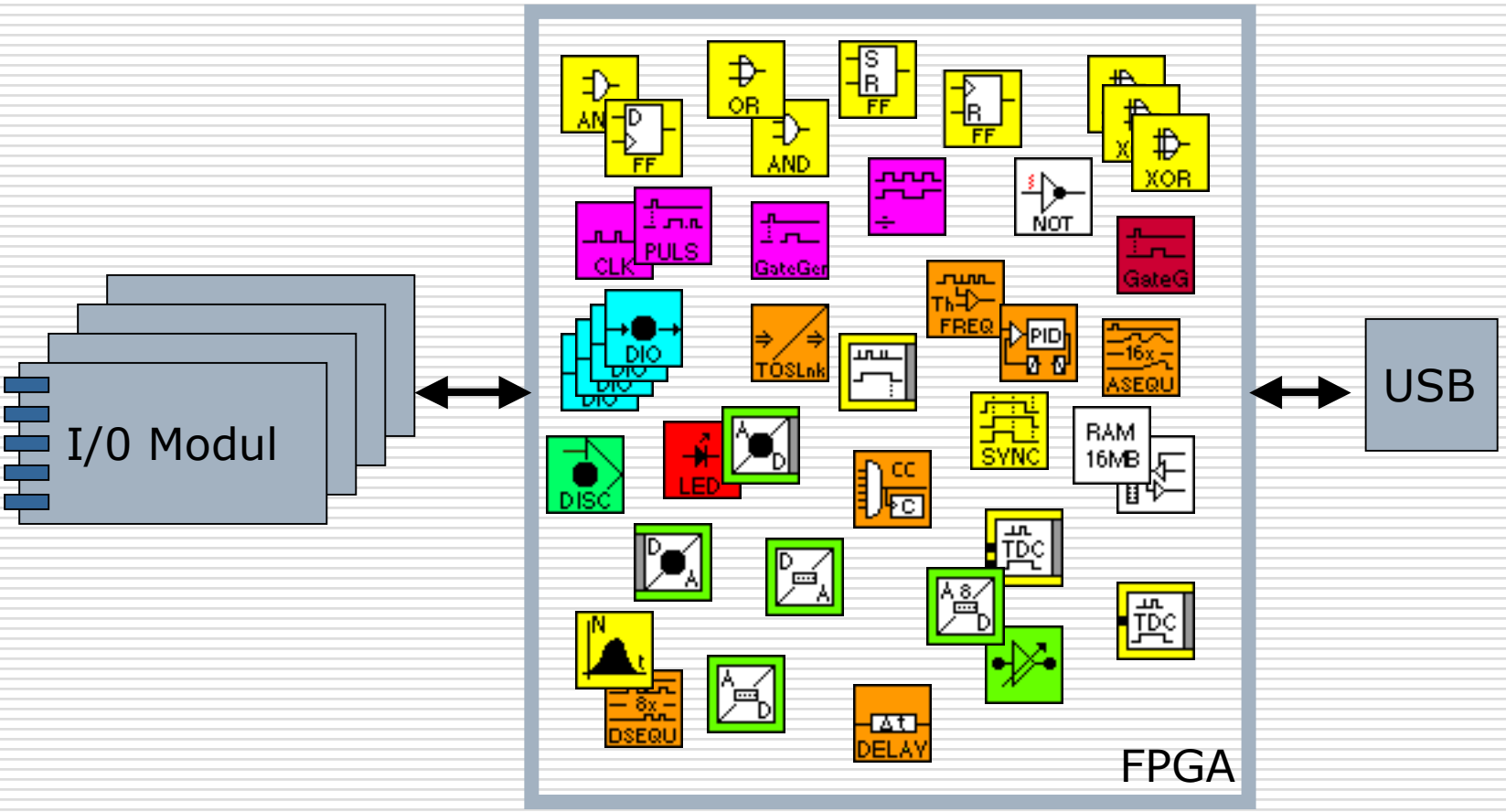
Type	Description
SU700	5x TTL I/O – LEMO coax
SU701	16x TTL I/O - Multiconnector
SU702	8x ADC, Diff, bipolar
SU703	4x Discriminator and 1x TTL I/O –coax, std
SU704	5x NIM/TTL I/O – LEMO coax
SU705	16 MByte RAM (100 MHz statisch)
SU706	1x ADC (100 Mhz) ,2x TTL I/O – LEMO coax
SU707	8x LVDS I/O
SU708	Cascade IF50 Interface
SU709	8x Temperaturesensor
SU710	2x Fast DAC (100 Mhz)
SU711	6x programmable Delayline 0,5ns .. 128 ns
SU712	16x ADC (5 us, 14 Bit)
SU713	16x DAC (14 Bit)
SU714	HAL25 Interface
SU715	NF-Amplifier with prog. Gain
SU716	16M*32b RAM (100 MHz statisch)
SU717	QDC, Ladungsempfindlicher ADC
SU718	8x ECL/TTL
SU719	2x Drucksensor-Interface (für SU712)
SU720	2x 8 ADC (5 us, 14 Bit), ISO (2*16mA)
SU721	2x 8 DAC (14 Bit), ISO
SU722	5x TTL I/O – LEMO coax, ISO
SU723	400 MHz DDS

Type	Description
SU724	TOSLink IF
SU725	8 x ECL Input
SU726	32 x LED Monitor
SU727	3 x TOSLink IF
SU/28	4 Ch. ADC, 1 Ch. DAC, ISO, 1us
SU729	SD-Card IF
SU730	8Mx16b PSRAM

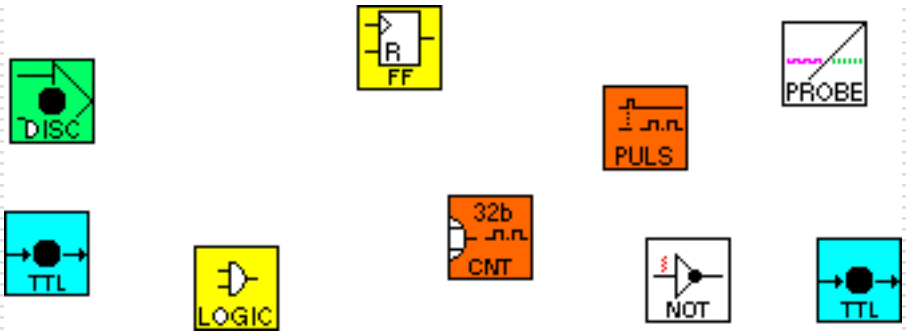
„LogicPool“ (Firmware)

- Preprogrammed Modules (Pool)
  - I/O (Digital, Analog, ADC, DAC, ...)
  - Logic (Gates, Coincidence, FlipFlops, ...)
  - Counter (Clock, Pulser, Scaler, ...)
  - Special (TDC, PID, Histogrammer, ...
  - ...
- User Configurable (LabVIEW, C, ...)
  - Wiring of Modules
  - Dynamic Reconfiguration
  - Read & Write of Parameters

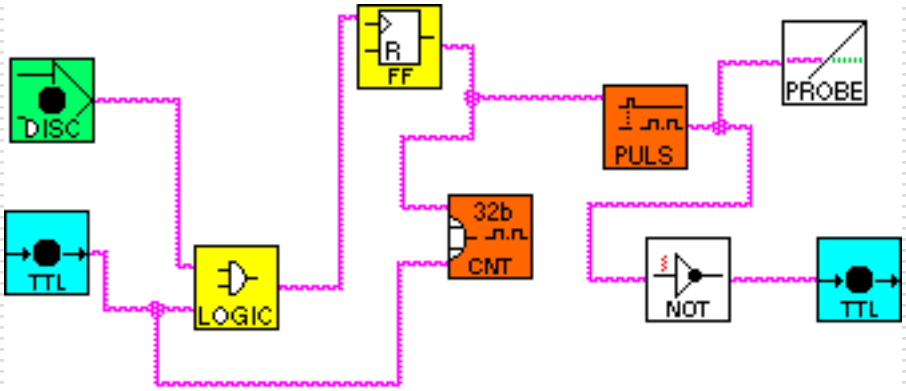
LogicBox: Setup



LogicPool: Modules

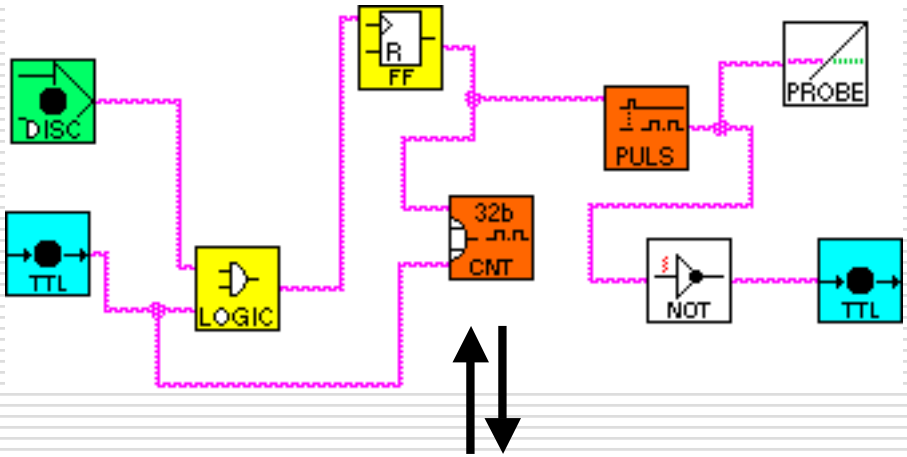


LogicPool: Wiring



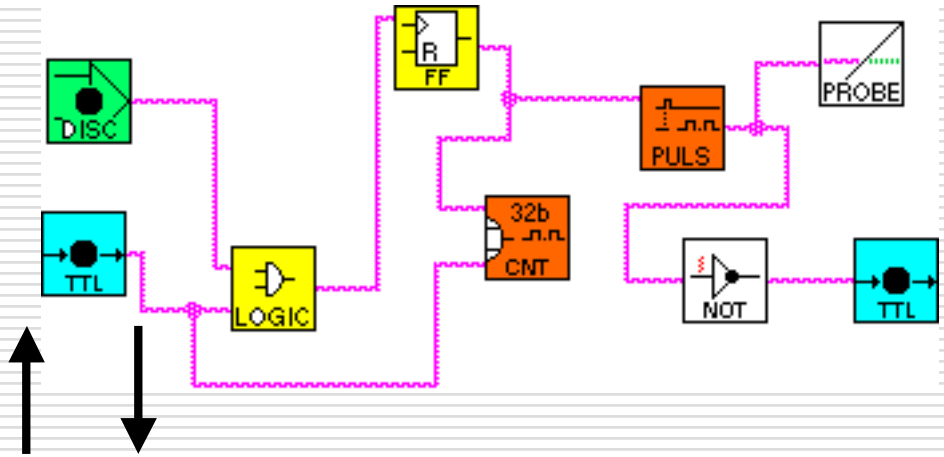
LabVIEW, ...

LogicPool: Parameters & Data



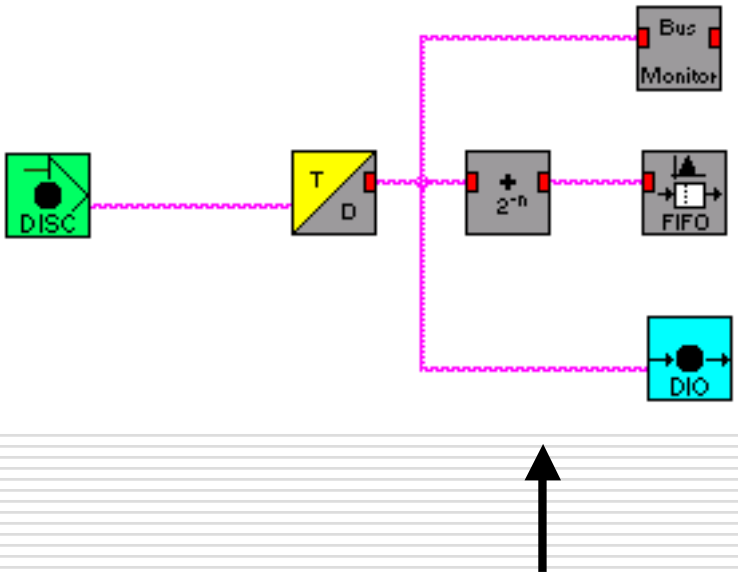
Parameters, Data (READ, WRITE)

LogicPool: Signals



- Inputs can be set LOW, HIGH, OPEN oder CONNECT (SET).
- Outputs (Signal States) can be read (GET).

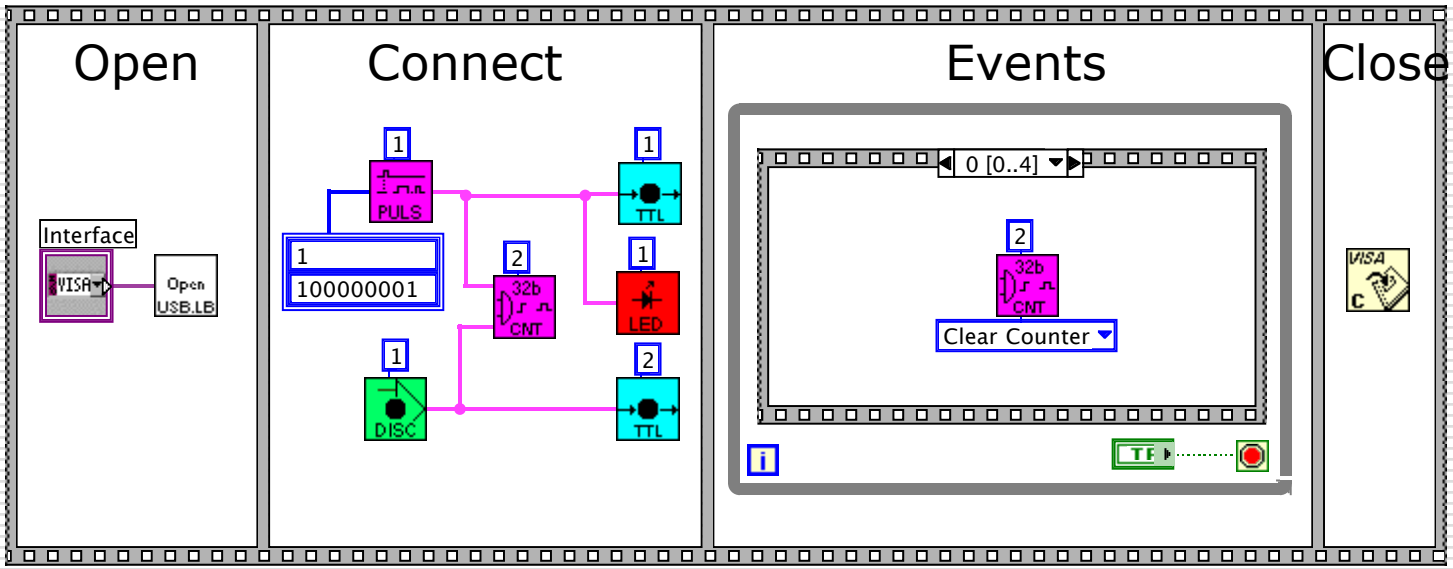
LogicPool: Signals & Data-Bus



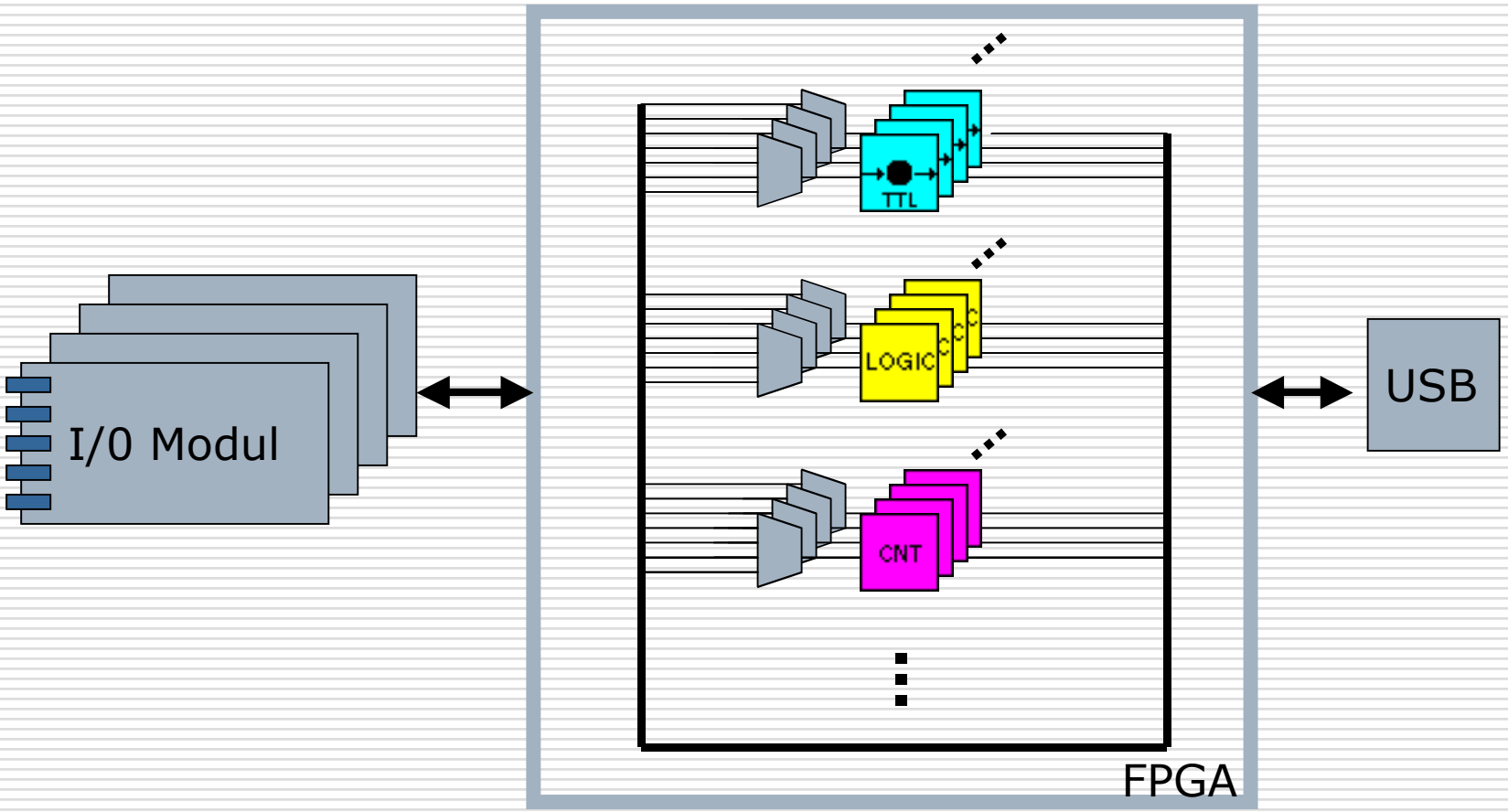
- Specific signales carry Data (typ. 32b)!
- Data is valid on Signal HIGH! (typ. 10ns Strobe)
- Data will be transferred synchronously with system clock!

LabVIEW: Typical Program

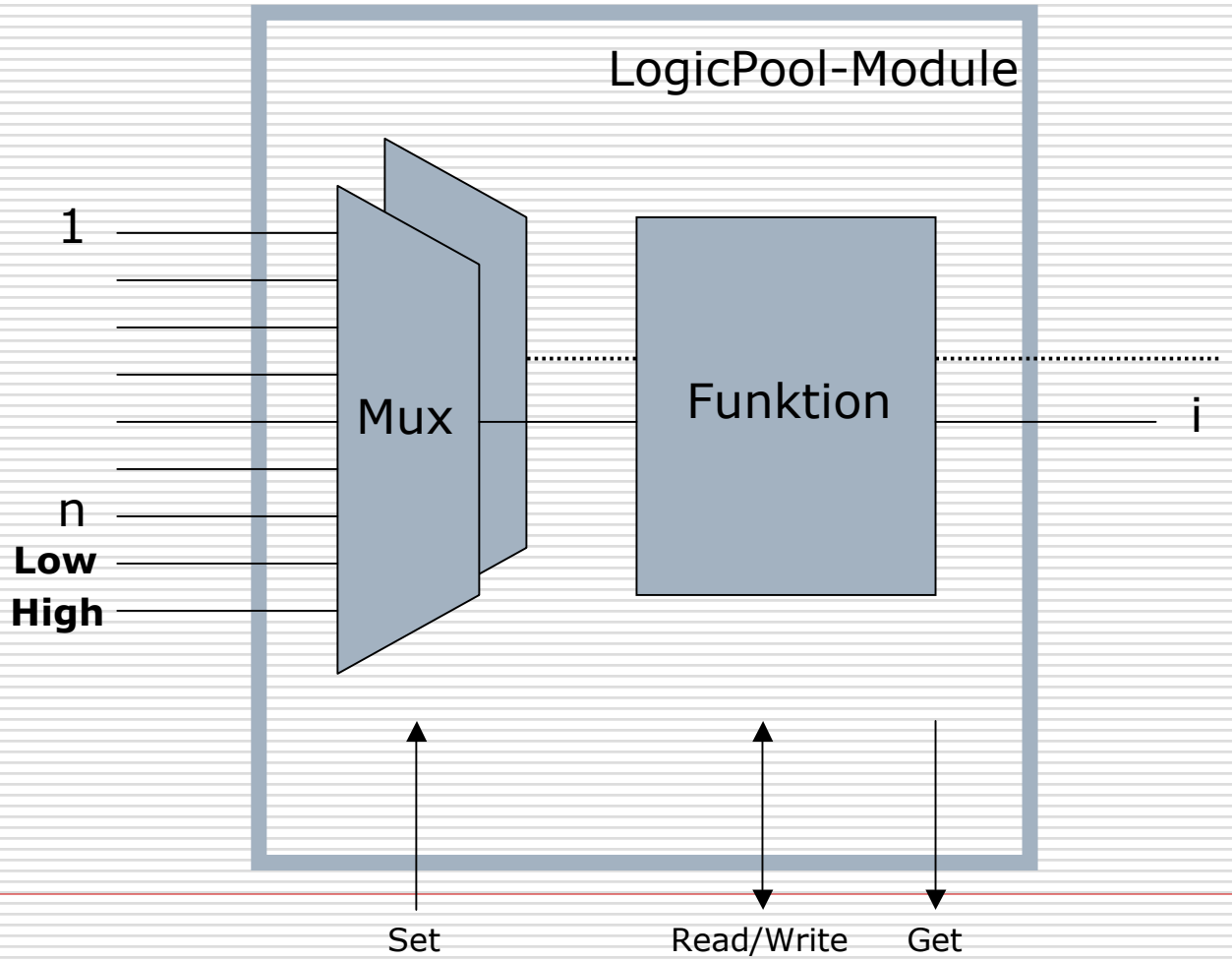
- Open Communication (Open)
- Wiring and Initialisation (Connect)
- Program, Flow Control (Events)
  - Setting of Parameters
  - Readout of Data and Visualisation
- Close Communication (Close)



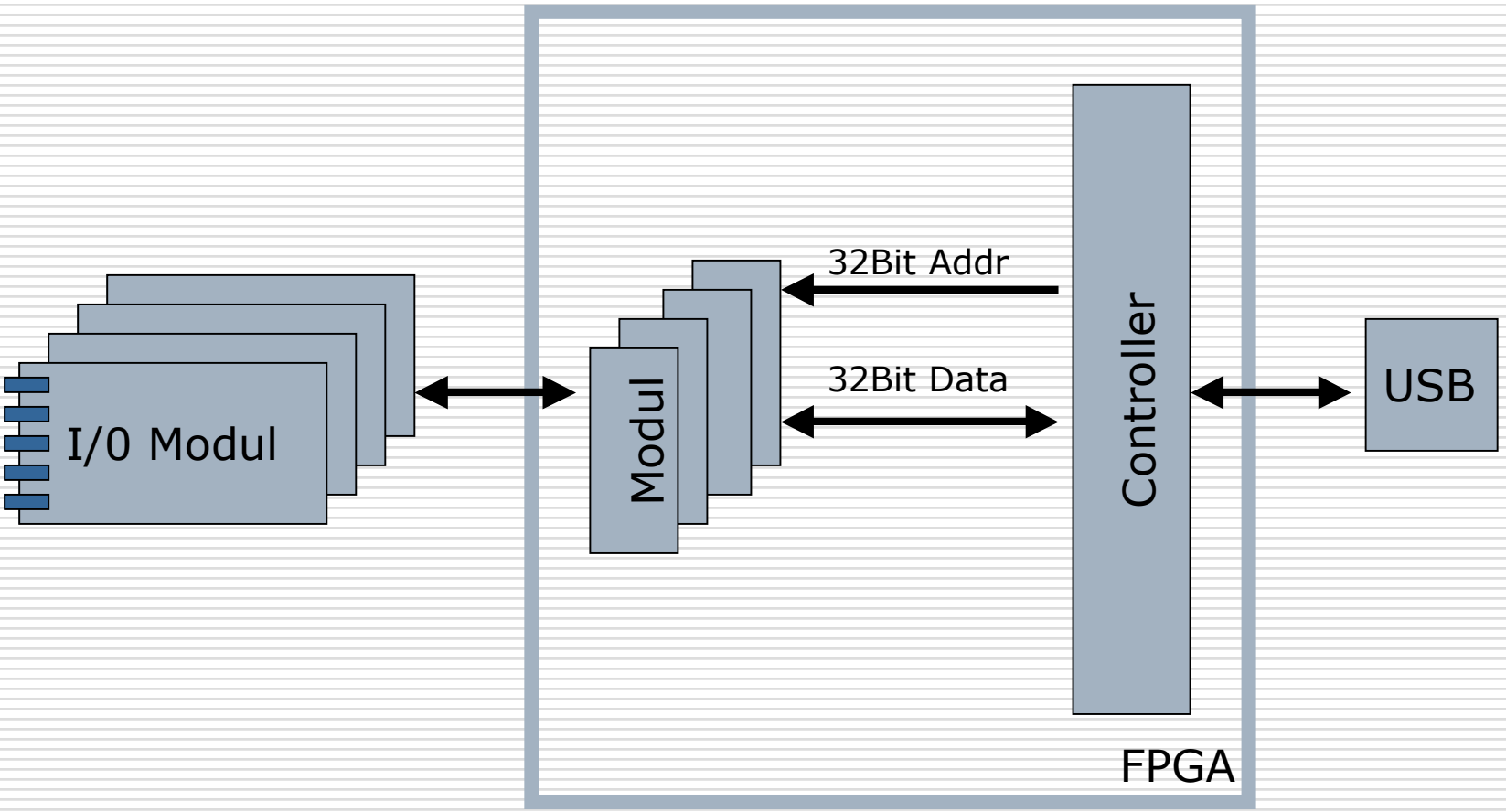
LogicPool: Wiring of Modules



LogicPool: Input Mux



LogicPool: Communication



USB: IF Protocol

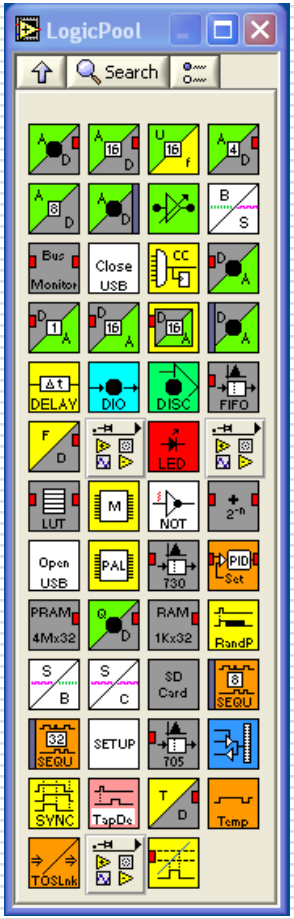
Kommando (ASCII)	Senden	Empfangen	Bedeutung
#		4 Bytes	Sende ID31..0
R			System Reset

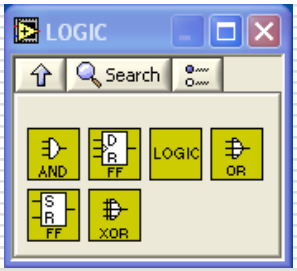
Kommando (ASCII)	Senden	Empfangen	Bedeutung
A	4 Bytes		Setzt Adresspointer A31..0
E	3 Bytes		Setzt Adresspointer A23..0
M	2 Bytes		Setzt Adresspointer A15..0
S	1 Byte		Setzt Adresspointer A7..0
a		4 Bytes	Liest Adresspointer A31..0
+			Erhöht Adresspointer A31..0 um 1
-			Erniedrigt Adresspointer A31..0 um 1
N	2 Bytes		Setzt Zähler N15..0 für Blocktransfer (A autoincr)
F	2 Bytes		Setzt Zähler N15..0 für FIFOtransfer (A)
L	N* 4 Bytes		Schreibt N Langwort(e)(A) (*)
l		N* 4 Bytes	Liest N Langwort(e)(A) (*)
T	N* 3 Bytes		Schreibt N Triple(s)(A) (*)
t		N* 3 Bytes	Liest N Triple(s)(A) (*)
W	N* 2 Bytes		Schreibt N Word(s)(A) (*)
w		N* 2 Bytes	Liest N Word(s)(A) (*)
B	N* 1 Byte		Schreibt N Byte(s)(A) (*)
b		N* 1 Byte	Liest N Byte(s)(A) (*)

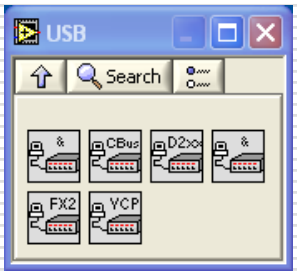
LogicPool: History

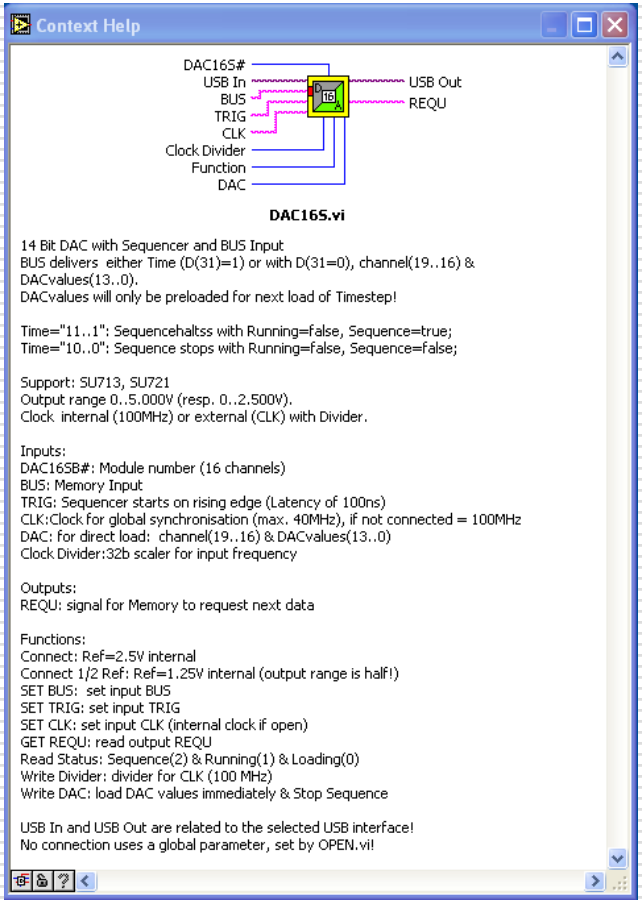
- V1.x
  - First Prototype
  - LOGIC, COUNTER, DIO, DISCR, LED, ..
- V2.x
  - Global Version ID & Date
  - ADCs, DACs (incl. Memory)
  - DELAY, TDC, ..
  - V2.10 Commercial Version!
- V3.x
  - Global Version ID & Date changed
  - SEQUENCER, PID, FREQUENCY, ..
  - Function Modules with Model and Version
- V4.0
  - Modules with Data BUS
  - RAM, FIFO, LUT, ..
  - GATEGEN Modules extended (replace COUNTER Modules)
  - Icons (Picture, Terminals) changed and unified
  - Names partly changed

LogicPool: LabVIEW

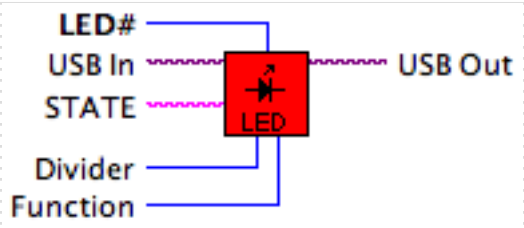




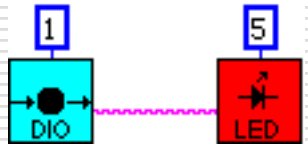




LP: LED



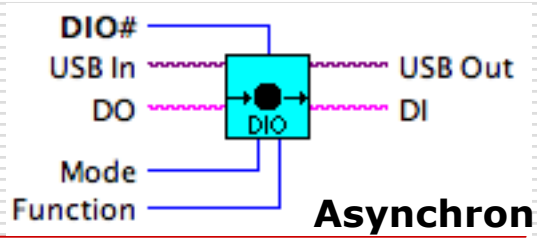
- SU7xx
- Display:
  - Static: ON/OFF (High/Low)
  - Dynamic: edge triggered
    - Pulse: prolonged (10 ms)
    - Rate: Divider



Memory Map for Modul n:

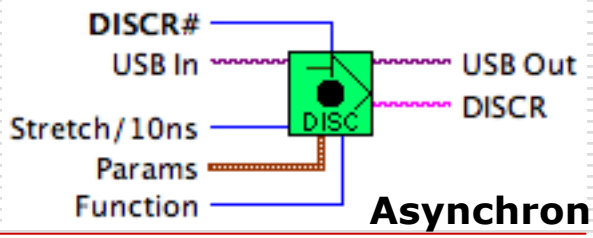
Address	Read	Write
x,“I“,n,0	0	IN_LED (8b)
x,“I“,n,1		Divider (32b)

LP: DIO (Digital I/O)



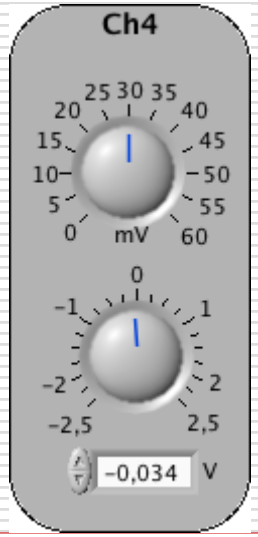
- SU7xx
- Mode: supports TTL, TTL-Coax, NIM, LVDS, ECL, ...
- Input or Output (selectable)
  - Input:
    - High impedance or 50 Ohm, Pull-Up
    - NIM 16mA @ 50 Ohm
  - Output:
    - TTL-Coax: 60 mA=3 V/50 Ohm
    - Risetime: approx. 2 ns

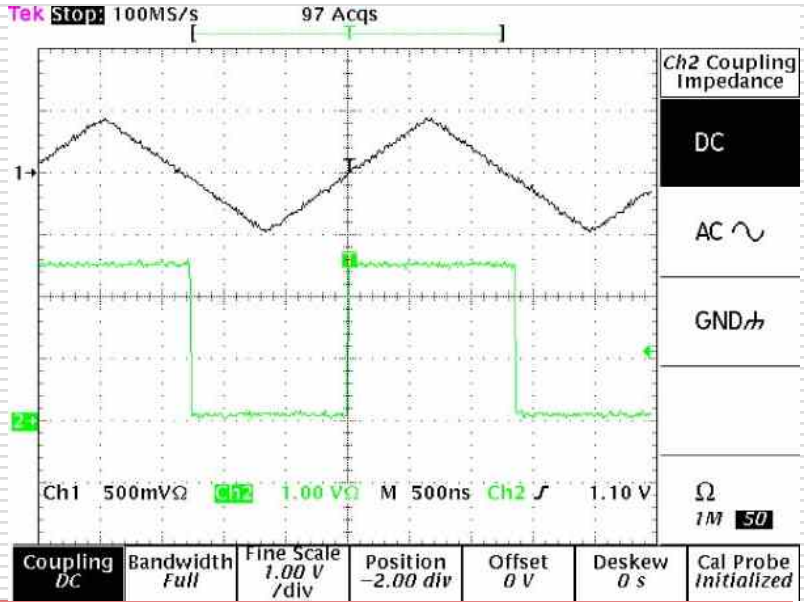
- f.e.: SU722: 5 TTL-Coax Kanäle galvanisch isoliert
- f.e.: SU704 (5 TTL/NIM Kanäle):
  - Mode: TTL/NIM (Jumper!)
  - HighImp/50 Ohm (Relay)

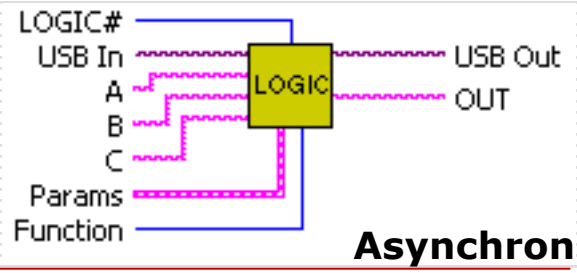


LP: DISCR

- SU703: 4 Discr. Channels, 1 TTL I/O
- Input
  - Threshold: -2.5V .. +2.5V (12 Bit)
  - Hysteresis: 0 .. 60 mV (12 Bit)
- Prop. Delay: 4..5 ns



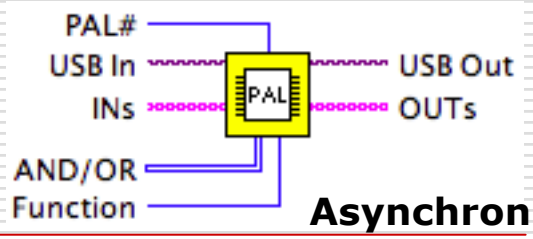




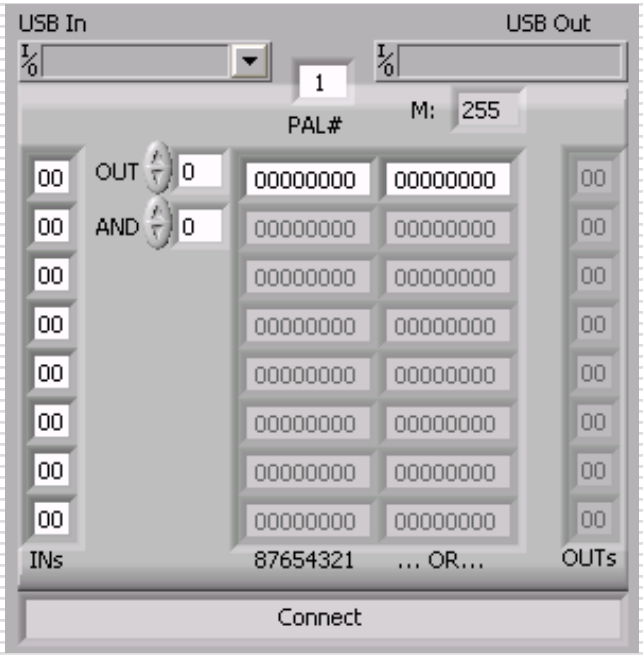
LP: LOGIC

- Passive Logic: 3 Inputs => 1 Output
- Variants (programmable)
  - Boole Logic
    - AND [LOGIC]
    - OR [LOGIC]
    - XOR [LOGIC]
  - FlipFlops
    - RSFF [LOGIC] RS-FlipFlop
    - DFF [LOGIC] D-FlipFlop
- Prop. Delay: approx. 6ns

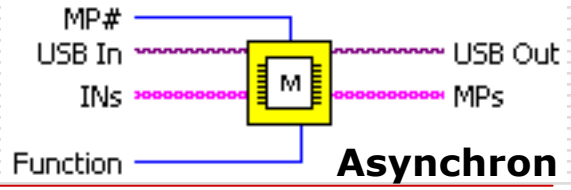
LP: PAL



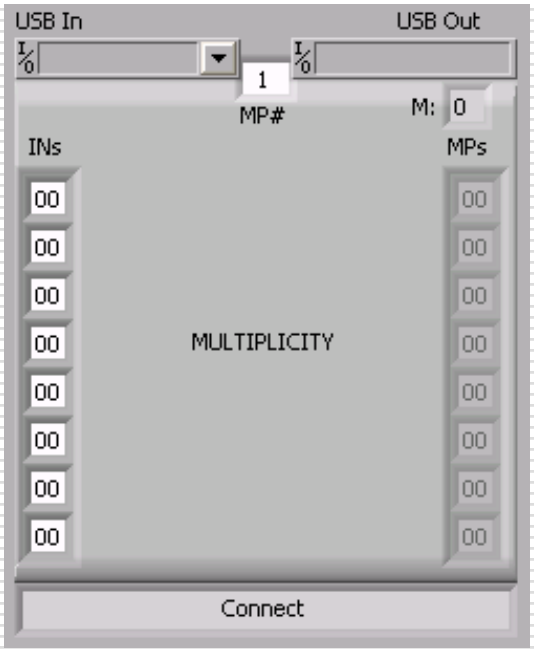
- Universal Logic Module (programmable Array Logic)
  - 8 Inputs => 1..8 Outputs
  - Logic free programmable (AND & OR)
- OUTn = A/BC...+/AB/D...+...
- Prop. Delay: approx. 8 ns



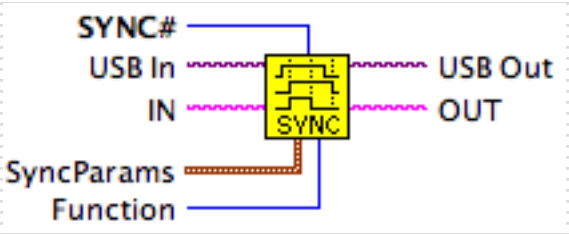
LP: MULTIPLICITY



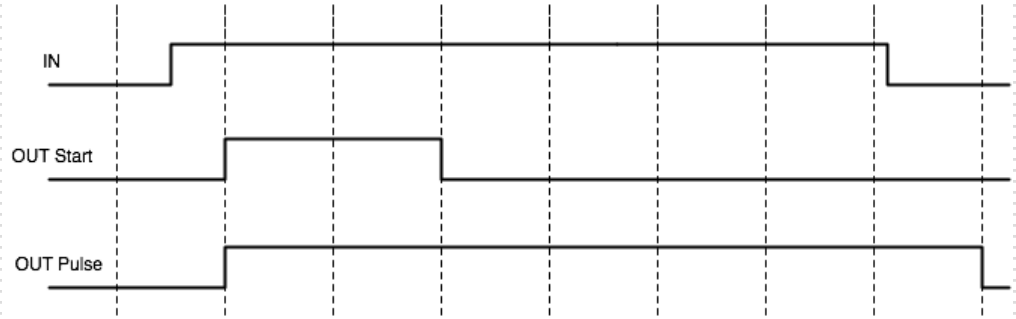
- Passive Logic Modul
  - 4..8 Inputs
  - Outputs for each Multiplicity
- OUTn <= n Inputs=High
- Prop. Delay: approx. 14 ns



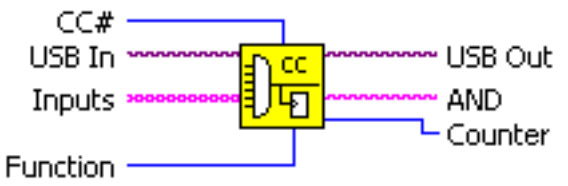
LP: SYNC



- Mode (programmable)
  - Synchroniser
    - Start (20 ns Pulse at rising edge)
    - Pulse (synchronous with system clock=100MHz)
  - Debouncer (Deadtime)
    - 0..255*10 ns
    - 0..255*1 ms



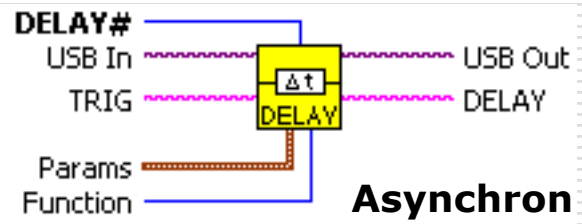
LP: COINCIDENCE



- Coincidence Counter
- 8 Inputs
- AND=High whenever n connected Inputs are High
- 32b Counter (rising edge)

VHDL:

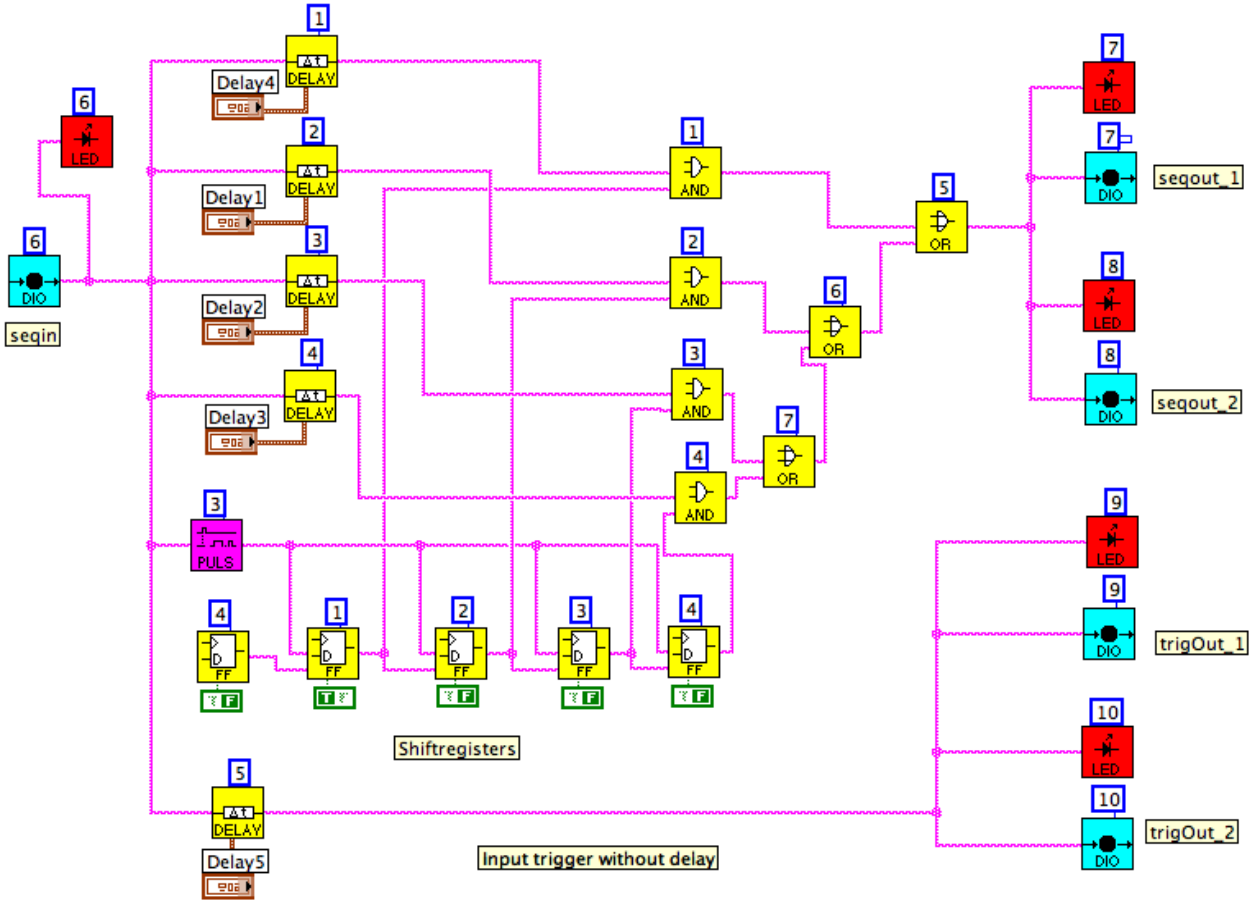
```
Coinzidence: process(In_TIG)
   variable KTerm: integer;
begin
   KTerm := 0;
   for i in 1 to Ins loop
      if In_TIG(i)='1' then KTerm := KTerm +1; end if;
   end loop;
   for i in 1 to Ins loop
      if i=KTerm then Outp_TIG(i) <= '1'; else Outp_TIG(i) <= '0'; end if;
   end loop;
end process;
```

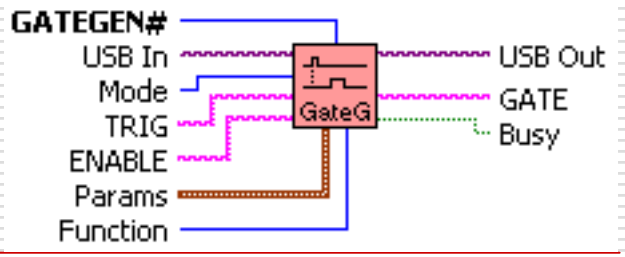


LP: DELAY

- SU711: 6 Channels
- Programmable Propagation Delays
  Independant from system clock (100MHz)
- Delay: typ. 30 ns + n*0.5 ns (n=0..255)
- Mode:
  - Delay: TRIG -> DELAY
  - MonoFlop: Pulse with DELAY after TRIG (rising edge)
- Application:
  - Calibration of Signals
  - Jitter free Pulse Generator

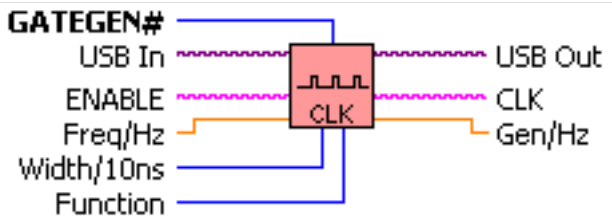
Delay: Jumping Trigger





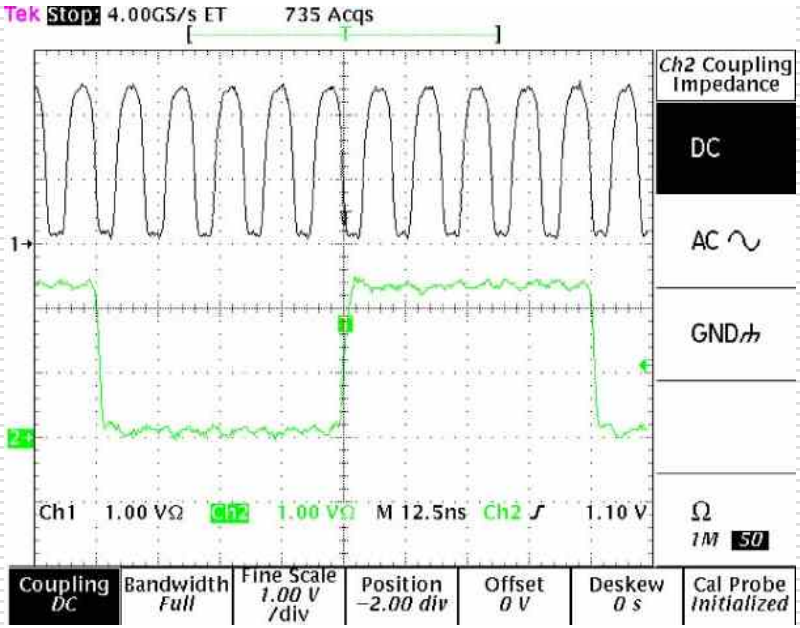
LP: GATEGEN

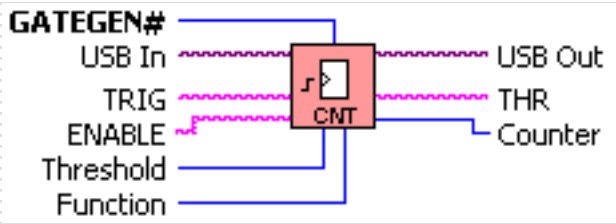
- Parameter: Delay & Duration
- Resolution: .. 32 Bit @ 10 ns (..ca. 40 s)
- Inputs:
  - TRIG: starts Pulse (rising edge)
  - ENABLE: for Trigger
- Modes: Non-/Retrigger
- Outputs:
  - GATE: Pulse (synchronous to system clock!)
- Variants (programmable)
  - GATEGEN (Pulser)
  - CLOCK (Clock generator)
  - COUNTER (Event counter, Time counter)



LP: CLOCK

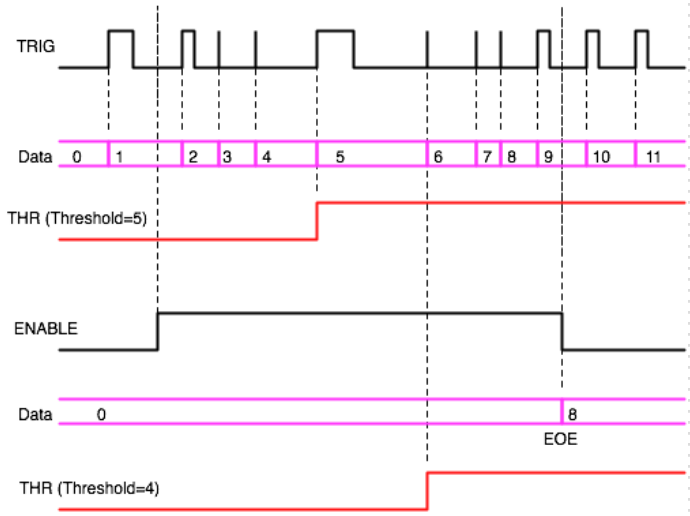
- Clock generator [GATEGEN]
- Divider: 32 bit
- Frequency: 0,02 Hz .. 100 MHz
- Duty Cycle
  - Width=0: 50%
  - Width=n: High n*10ns
- Enable: synchronous

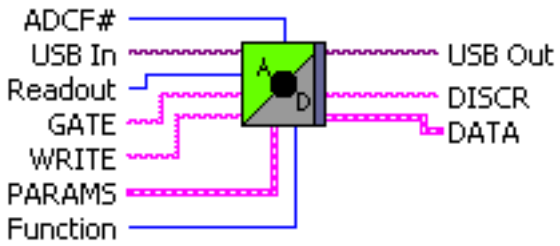




LP: COUNTER

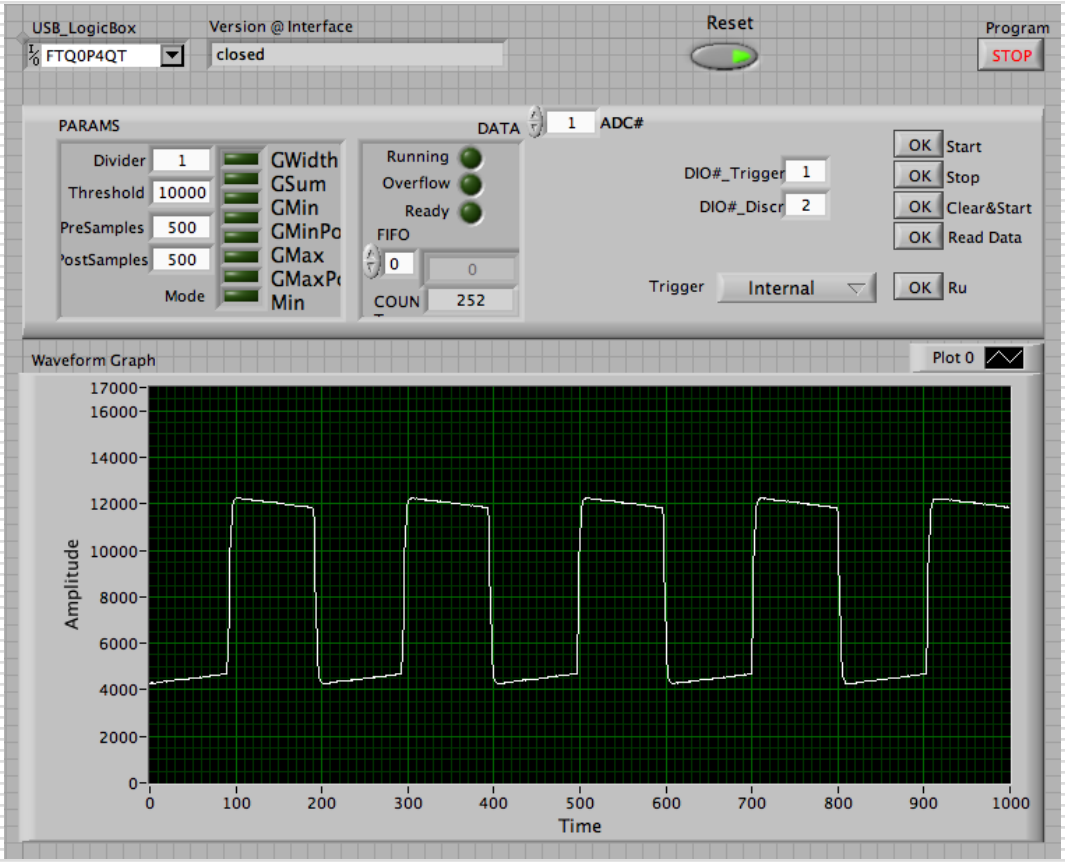
- Event counter, Time counter [GATEGEN]
- Counting rate: max.100 MHz
- Resolution: 32 Bit (modulo)
- Inputs:
  - TRIG:
    - Edge triggered (rising)
    - 100 MHz on open input
  - ENABLE:
    - Storage in register on EOE
    - Cont. counting on open input
- Output:
  - THR: HIGH on Counter ≥ Threshold



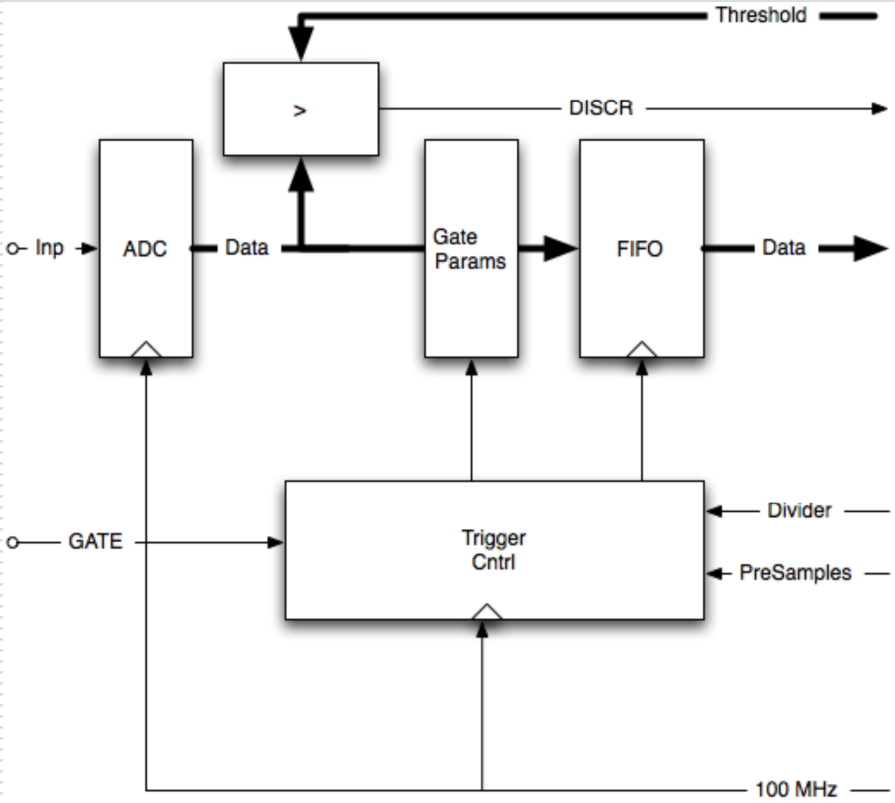


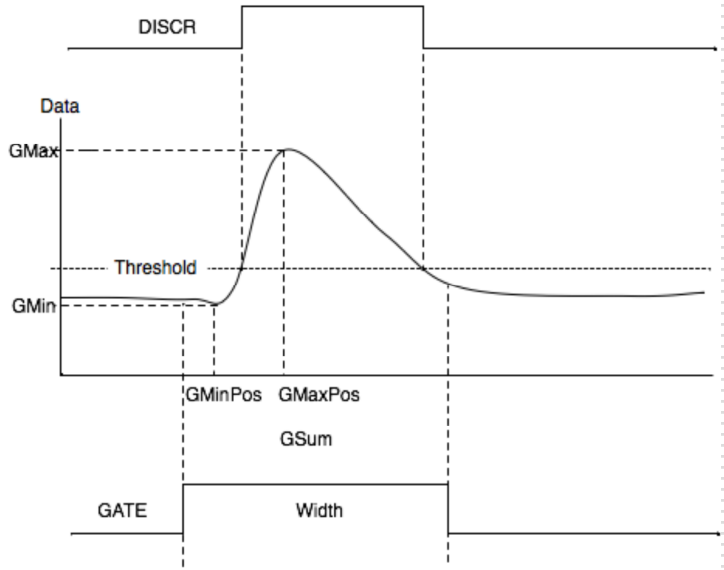
LP: ADCF

- SU706
- Sampling rate:
  100 MHz/n (n=1..2^16)
- Resolution: 14 bit
- FIFO/Histogr.: 1024
- WRITE: Veto
- Wave Mode:
  - GATE=Trigger
  - Raw Data
  - Pre-& Postsamples
- Parameter Mode:
  - Integral
  - Width
  - Max, Min
  - Position

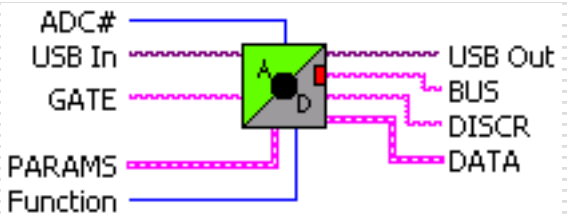


ADCF: Function



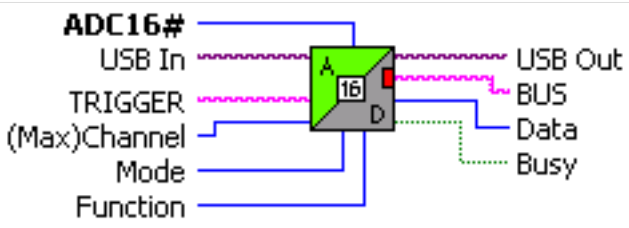


LP: ADC



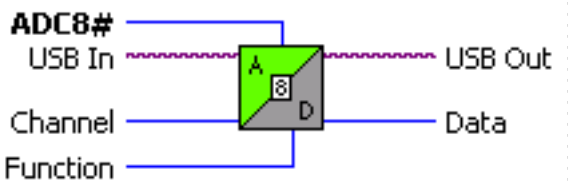
- SU706
- Sampling rate:
  100 MHz/n (n=1..2^16)
- Resolution: 14 bit
- Digital Discriminator
  - Threshold
- Analog Input
  - AC: > 20kHz
  - DC: 2Vpp (0..200MHz)
- Trigger
  - GATE (rising edge)
  - Write
- Output
  - BUS (32b)
  - Read
- Parameters
  - Divider
  - Threshold
  - MinWidth
  - Offset
  - Wave Mode:
    - GATE=Trigger
    - Raw Data
    - Pre-& Postsamples
  - Parameter Mode:
    - Integral
    - Width
    - Max, Min
    - Position

LP: ADC16



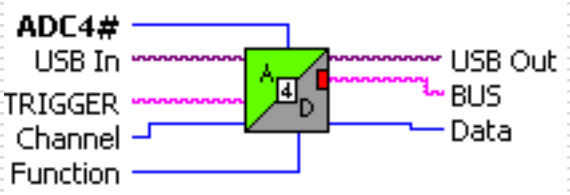
- SU712: 16 channels
- SU720: 2*8 channel (isolated)
- Resolution: 14 bit
- Latency: 5 us
- Analog Input
  - 0..+2,5 V
- Trigger (sequential)
  - Write
- Output
  - BUS
  - Read

LP: ADC8

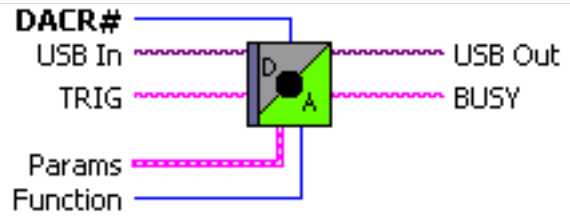


- SU702: 8 channels
- Resolution: 14 bit
- Latency: 5 us
- Analog Input
  - -4..+4V
  - differential
- Trigger
  - Write
- Output
  - Read
  - (BUS)

LP: ADC4



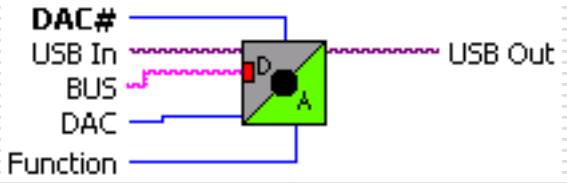
- SU728: 4 channels (isolated)
- Resolution: 16 bit
- Latency: 1 us
- Analog Input
  - -5..+5V
- Trigger
  - TRIGGER
  - Write
- Output
  - BUS
  - Read
- Application
  - PID



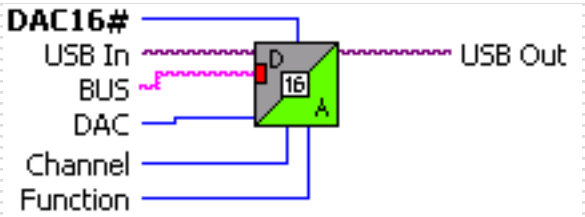
LP: DACR

- SU710: 2 channels
- Clock rate: 100 MHz/n (n=1..2**16)
- Resolution: 14 bit
- Input
  - RAM: 1024*14b (Single & Continous)
  - Write
- Analog Output
  - +-1V @ 50 Ohm
  - differential
- Application
  - Arb. Func. Generator

LP: DAC



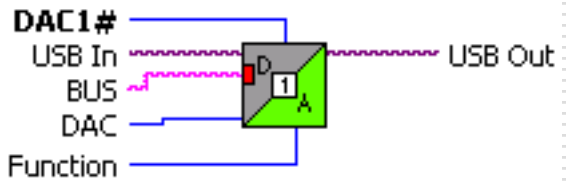
- SU710: 2 channels
- Conversion rate: 10 ns
- Resolution: 14 bit
- Input
  - BUS
  - Write
- Analog Output
  - +-1V @ 50 Ohm
- Application
  - Arb. Func. Generator



LP: DAC16

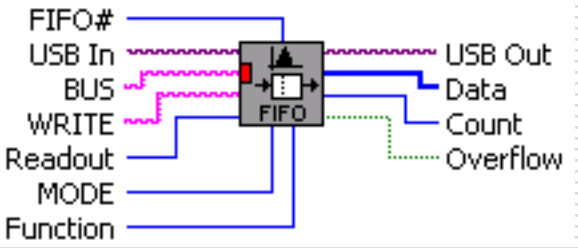
- SU713: 16 channels
- SU721: 2*8 channels (isolated)
- Resolution: 14 bit
- Lateny: 5 us
- Input
  - BUS
  - Write
- Analog Output:
  - 0..2.5V, 0..5V
  - Slewrate=3V/us

LP: DAC1



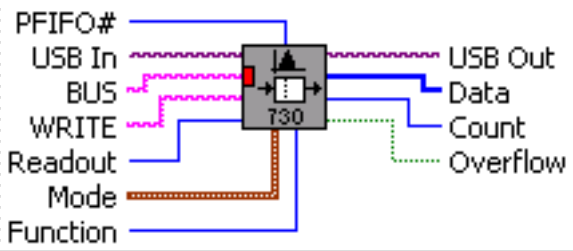
- SU728: 1 channel (isolated)
- Resolution: 16 bit
- Latency: 1 us
- Input
  - BUS
  - Write
- Analog Output
  - -5..+5V
- Application
  - PID

LP: FIFO



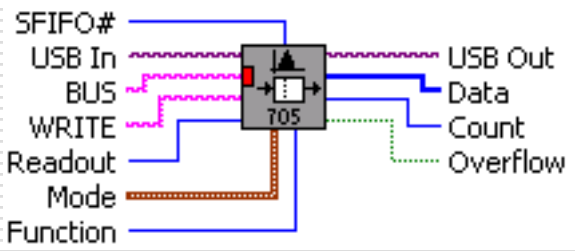
- FPGA Memory: 1024 * 32b
- Mode (programmable)
  - FIFO: 1024 * 32b
  - Histogram: 1024 Bins @ 32b
- Rate: 100 MHz (FIFO)
- Input
  - BUS
  - WRITE (Veto)
- Output
  - Data
  - Count
  - Overflow

LP: PFIFO



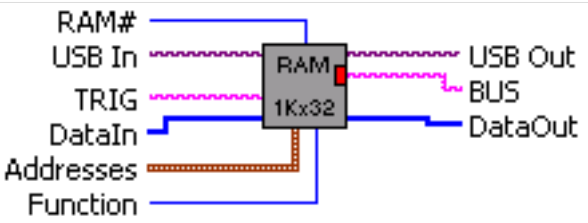
- SU730: Pseudo Static Memory 4M * 32b
- Modus (programmierbar)
  - FIFO: 4M * 32b
  - Histogram:
    - 64 pages with 65536 Bins @ 32b
    - ...
    - 65536 pages with 64 Bins @ 32b
- Rate: 10 MHz
- Input
  - BUS
  - WRITE (Veto)
- Output
  - Data
  - Count
  - Overflow

LP: SFIFO



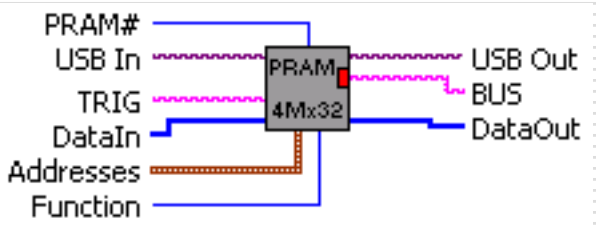
- (SU705) SU716: Static Memory 4M * 32b
- Mode (programmable)
  - FIFO: 16M * 32b
  - Histogram:
    - 4096 pages with 1024 Bins @ 32b
- Rate: 100 MHz
- Input
  - BUS
  - WRITE (Veto)
- Output
  - Data
  - Count
  - Overflow

LP: RAM

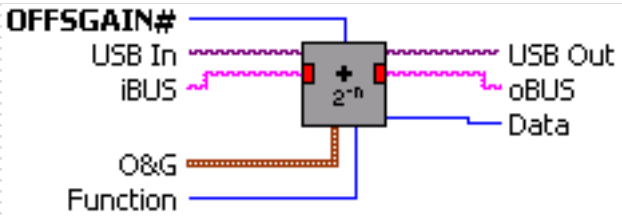


- FPGA Memory: 1K * 32b
- Rate: 100 MHz
- Input
  - Data (Write)
  - TRIG (Request for next word)
- Output
  - BUS
  - Data (Read)

LP: PRAM



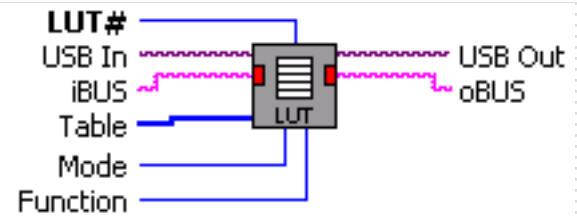
- SU730: Pseudo Static Memory 4M * 32b
- Rate: 10 MHz
- Input
  - Data (Write)
  - TRIG (Request for next word)
- Output
  - Data (Read)
  - BUS



LP: OFFSGAIN

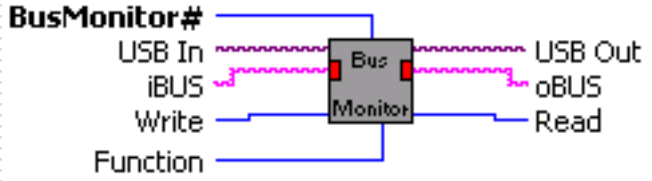
- Data scaling
- Data width: 32b
- oBus = iBus * Gain + Offset
  - Gain: 2^-n (Abschwächung)
  - Offset: 32b signed
- Application:
  - Histogram

LP: LUT

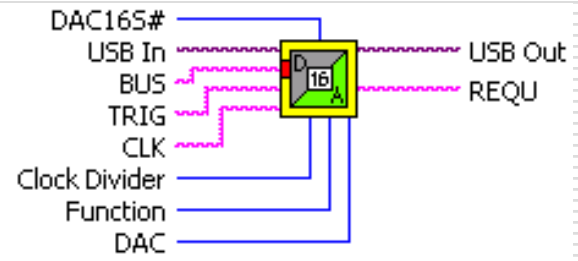


- Data conversion (Linearisation)
- Memory: 1024 * 16b
- Input: iBUS
  - Width: 16b
  - Memory: N=10b (MSB)
  - Interpolation: P=6b (LSB)
- Output: oBus
  - Width: 16b
  - = Value(N) + ((Value(N+1) – Value(N)) * P)/2^6
- Mode
  - BUS: oBUS(iBUS)
  - Counter: Sequential output (iBUS strobe)

LP: BUSMONITOR

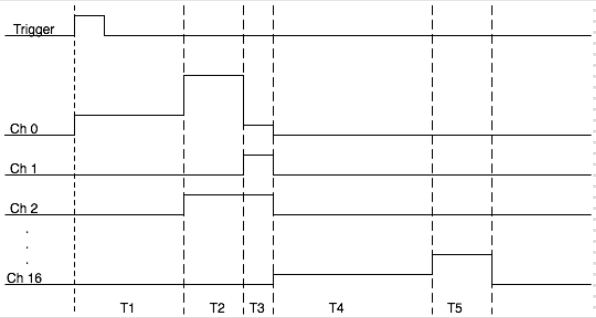


- Data I/O via BUS
- Write
  - 32b
  - Data => oBUS (Register)
- Read:
  - 32b
  - iBUS => Data (Register)
- Application
  - Test



LP: DAC16S

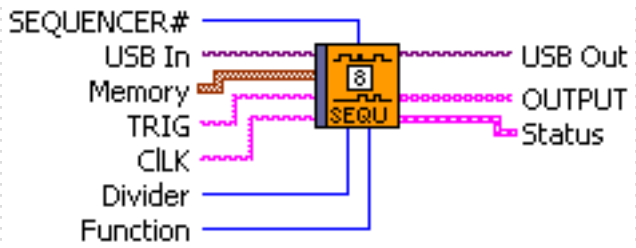
- SU713: 16 Channels
- SU721: 2*8 Channels (isolated)
- Analog Sequencer
- Resolution: 14 bit
- Analog Output:
  - 0..2,5V; 0..5V (Slewrate=3V/us)
- Input
  - BUS
  - Write
- Sequencer
  - Int.Clock=100MHz / Ext. Clock
  - Start (TRIG)
  - Time
    - Resolution (Divider 32b): 10 ns.. 40 sec
    - Range: 23 bits = 80 ms (10 ns) .. 10**8 s
    - Preload: 1us
  - REQU

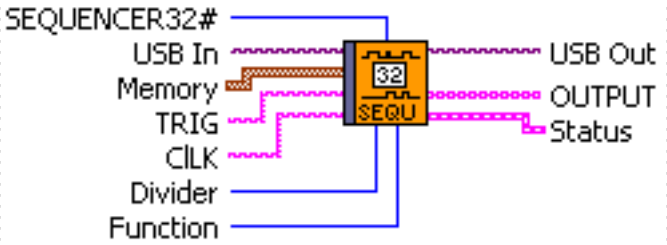


Beispiel:

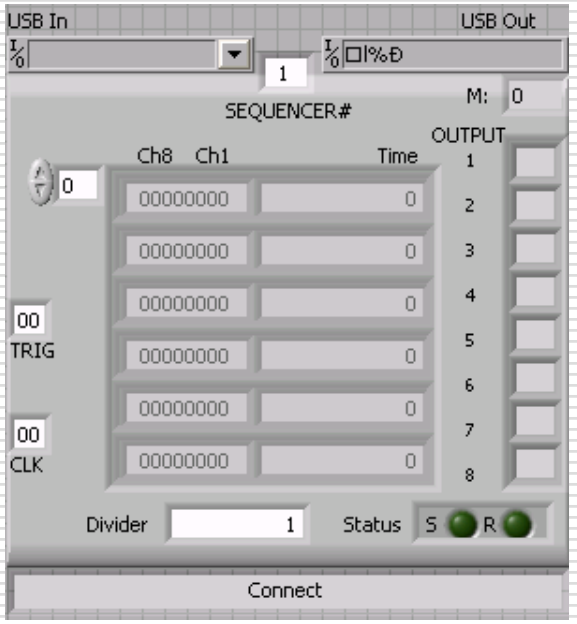
Ch 0 & Value
Time T1
Ch 0 & Value
Ch 2 & Value
Time T2
Ch 0 & Value
Ch 1 & Value
...
...

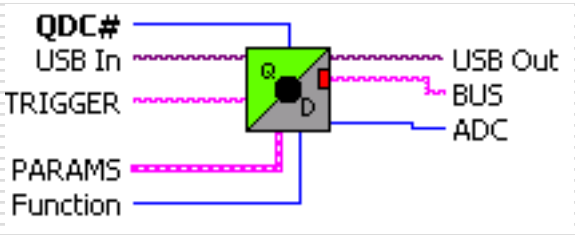
LP: SEQUENCER/32





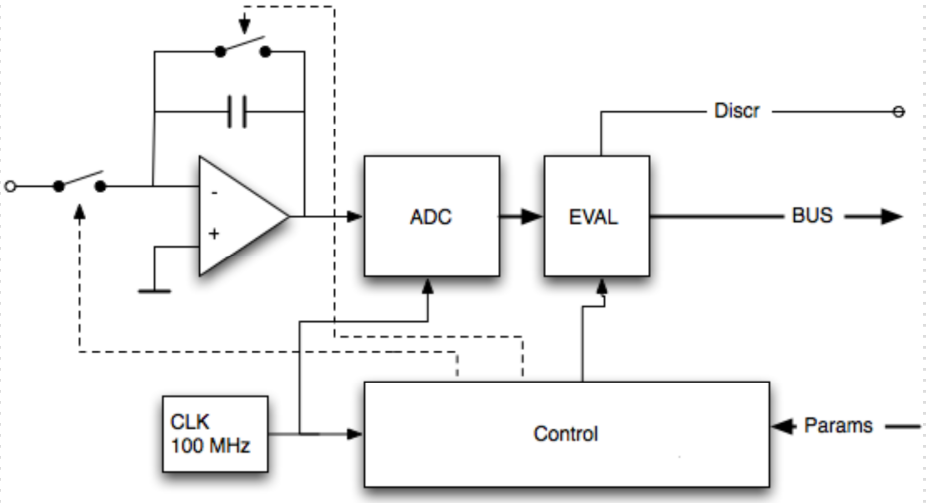
- Digital Sequencer
- Channels: 8, 32
- FPGA Memory: 1K..8K*8b,32b
- Time:
  - Int.Clock=100MHz/Ext. Clock
  - Divider 32b
  - Resolution: 32b
- Input
  - Data
  - TRIG (rising edge)
- Output
  - Digital





LP: QDC

- SU717: 1 Channel Charge Integration-ADC
- Resolution: 14 bit
- Input:
  - TRIGGER: start measurement (rising edge)
- Output:
  - BUS
  - Read
- Parameter:
  - Integration time (Gate)
  - Time of Sampling
- Multi Measurement!
  - Baseline
  - Integral
  - Integral - Baseline

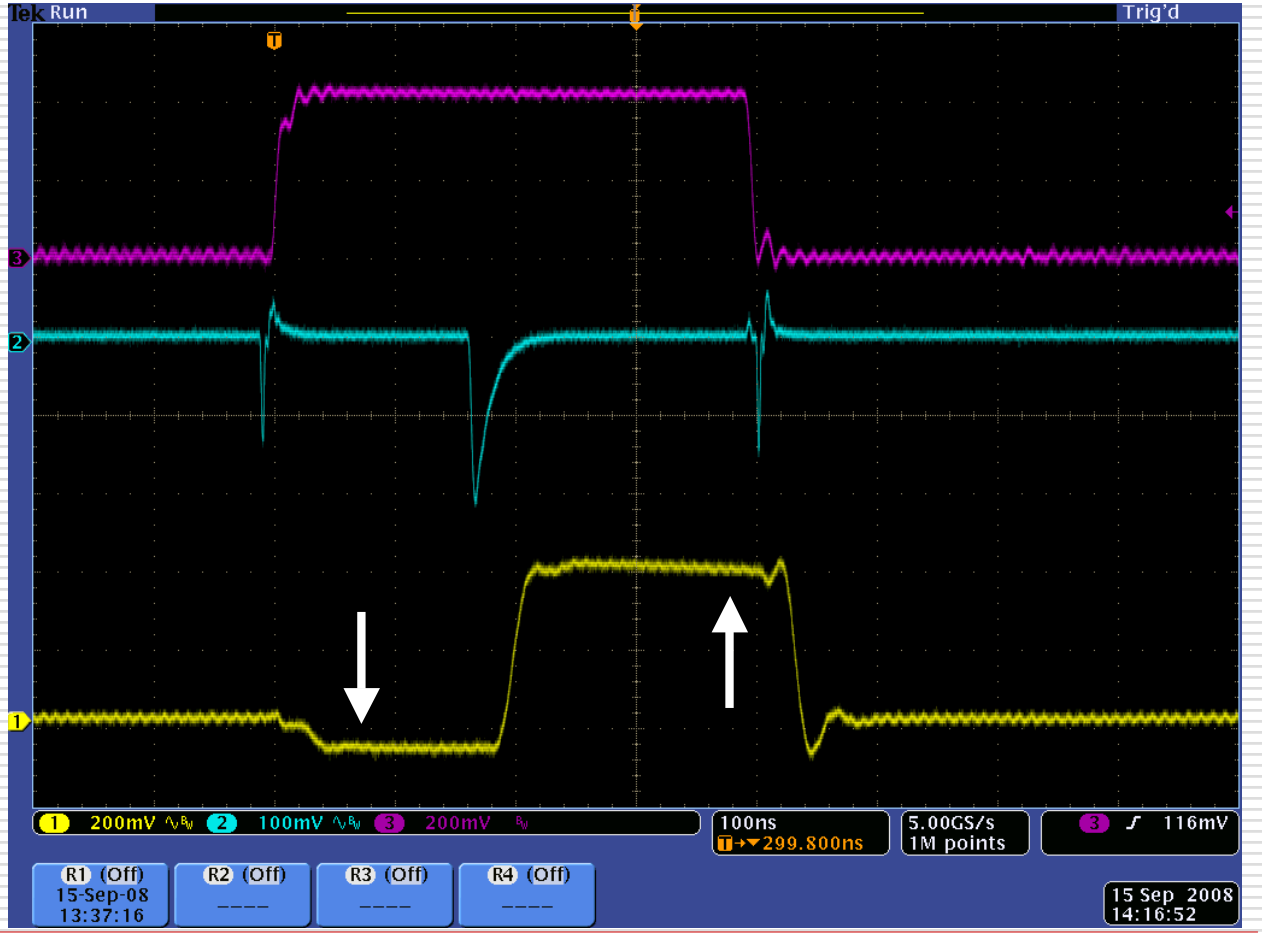


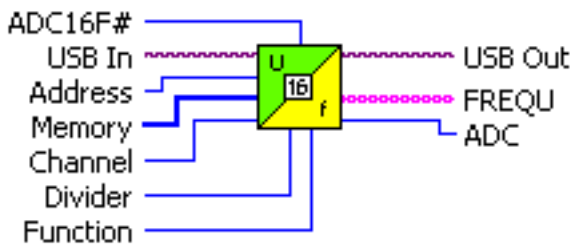
QDC: Signals

Gate

Input

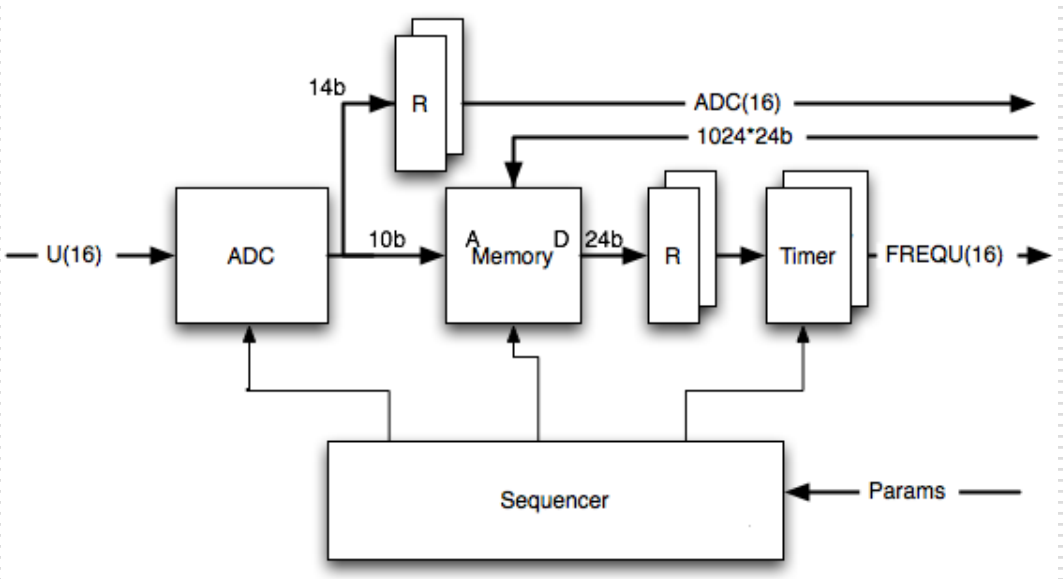
Integral



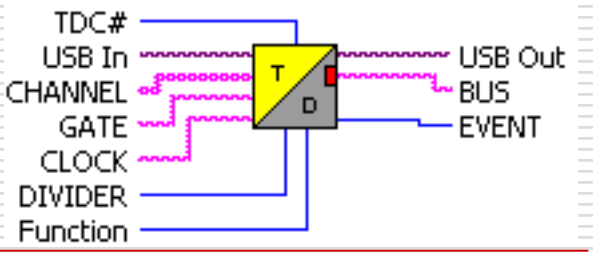


LP: ADC16F

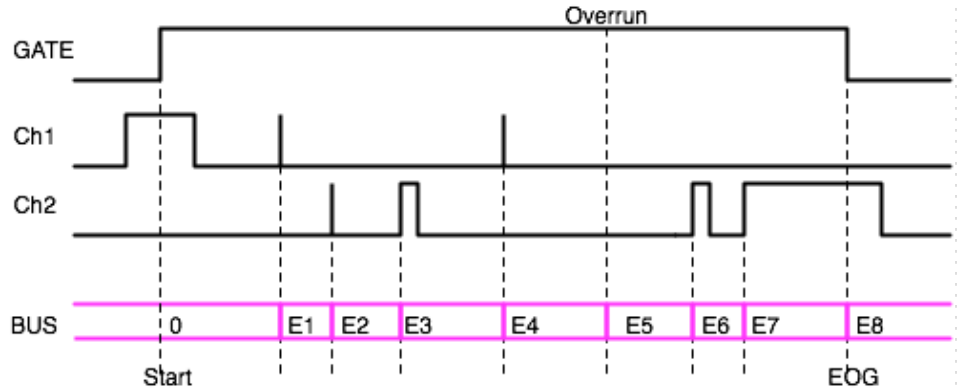
- SU712, 720
- Voltage/Frequency Converter
- 16 Channels (sequential)
- Conv. Rate: Divider * 10ns
- Analog Input
  - 0..2,5 V
- LUT (1024*24)
- Output:
  - Frequency
  - Readout

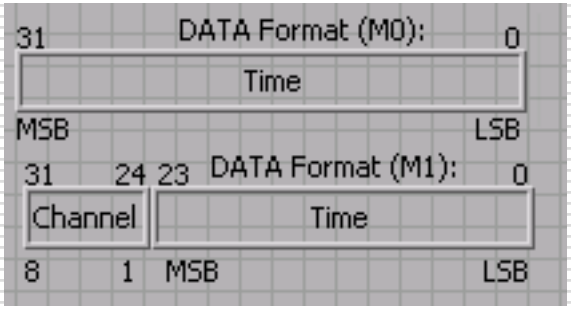


LP: TDC

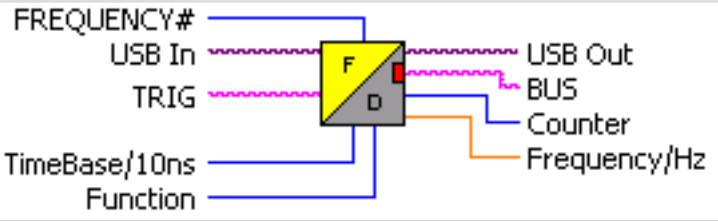


- 1..8 Channels
- Multi Hit
- Timer (Range): 32b
- Resolution:
  - 10 ns
  - Ext. Clock
  - Divider: 32b
- Marker:
  - Timer Overrun
  - EOG
- Data
  - BUS
  - Readout (Register,Last Event)





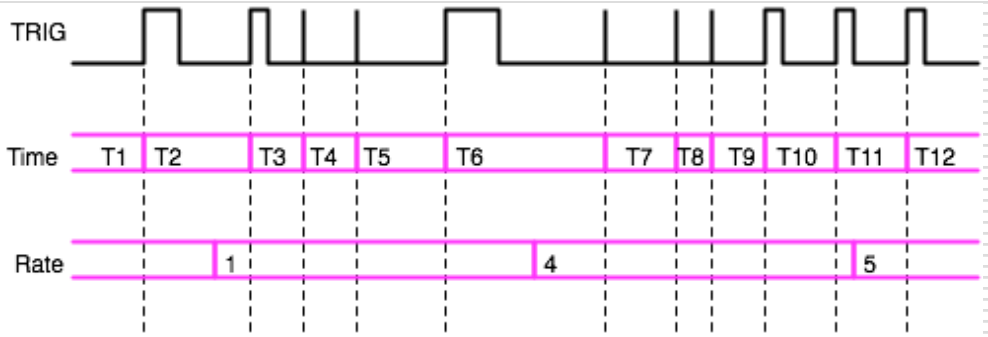
LP: FREQUENCY

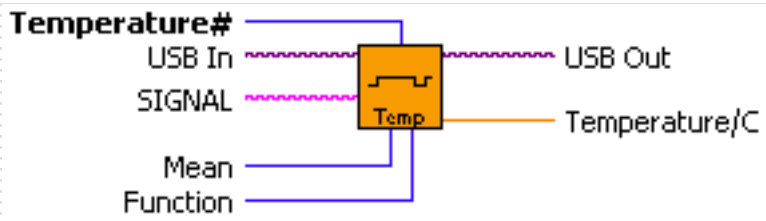


- Frequency / Rate Meter (FDC)
- Resolution: 10 ns
- Time Base (Range): 32b
- Mode
  - Time: Time Base=0

    cont. Time measurement between two consecutive TRIG-Pulses (rising edge)
  - Rate: Time Base=n

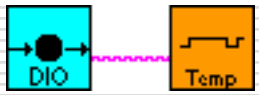
    cont. Rate measurement over time range = n*10ns
- Data
  - BUS
  - Readout (Register)



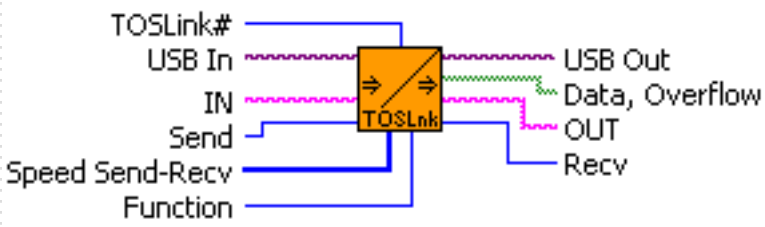


LP: TEMPERATURE

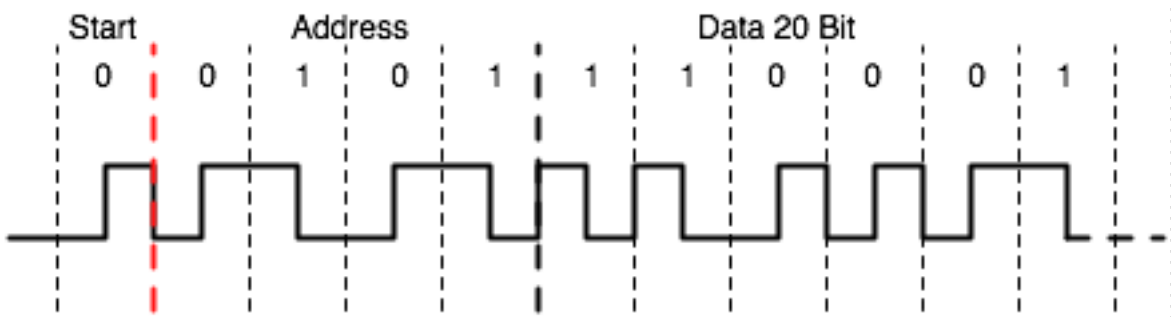
- Duty cycle meter (HIGH/LOW)
- Resolution: 10 ns
- Time Base (Range): 32b
- Accuracy: 0,7°C
- INPUT:
  - Digital sensor signal (SMT16030)
- Data:
  - Readout (Register)
  - High/Low => °C
- Application:
  - Multichannel (64) temperature

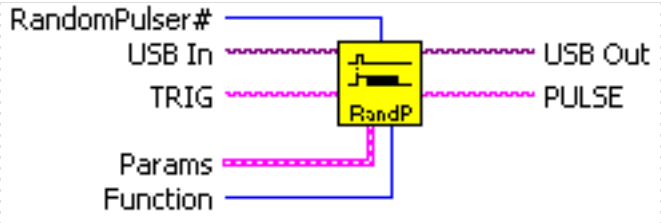


LP: TOSLink



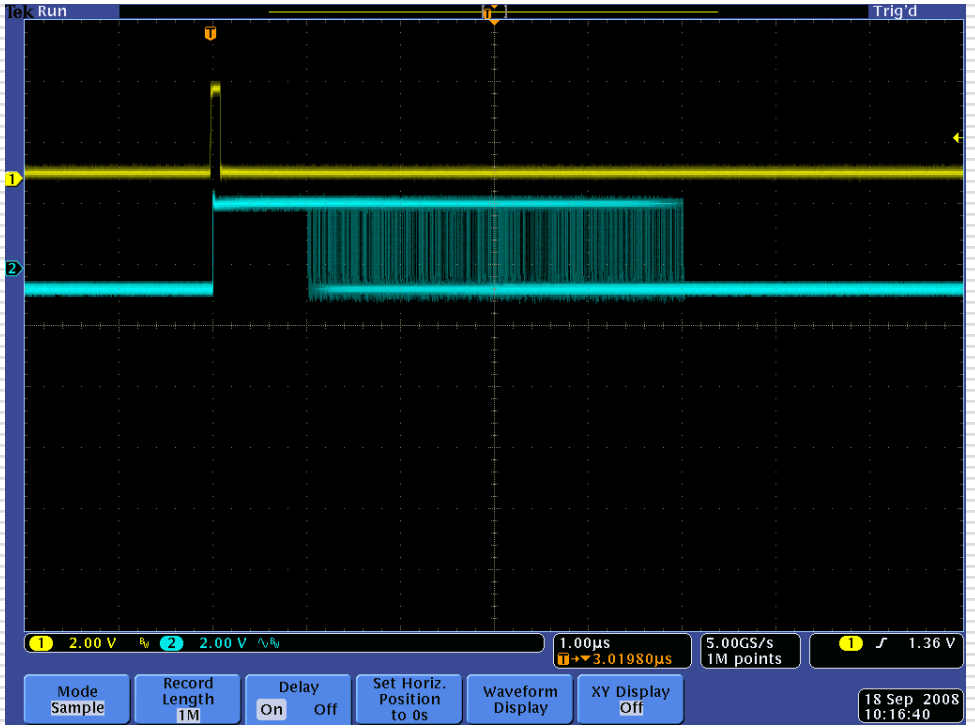
- SU724, SU727, DIO, ...
- Coder/Decoder for optical data communication
- BiPhase (0=rising edge; 1=falling edge)
- 24b Data
- Speed: typ 5 MHz



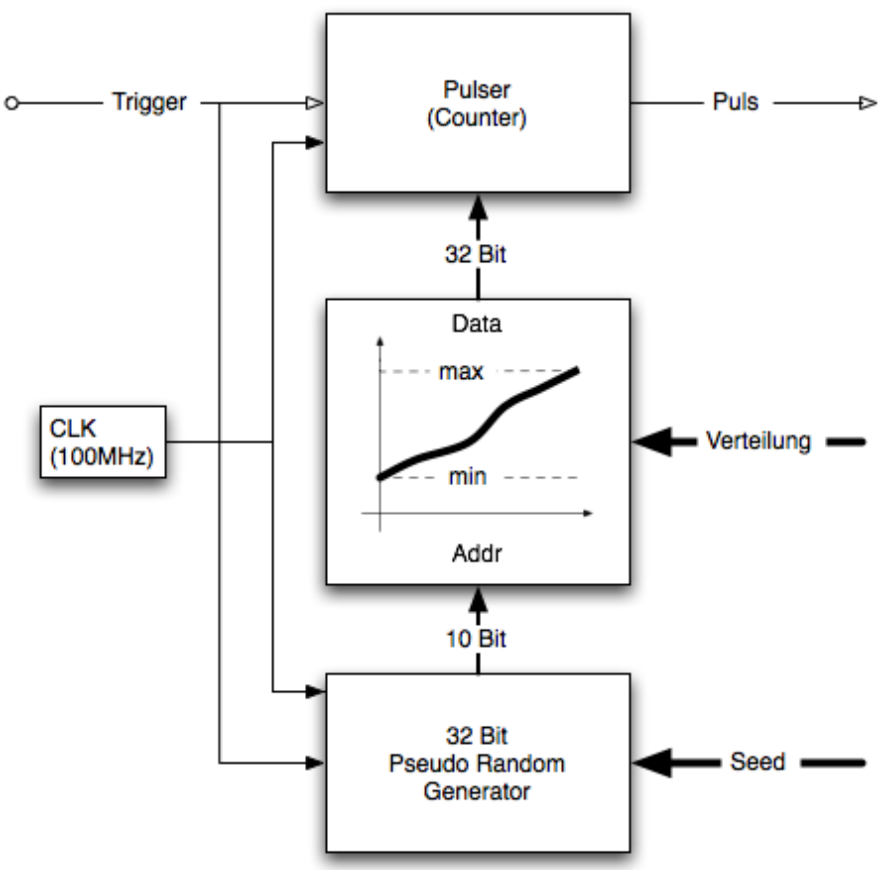


LP: RandomPulser

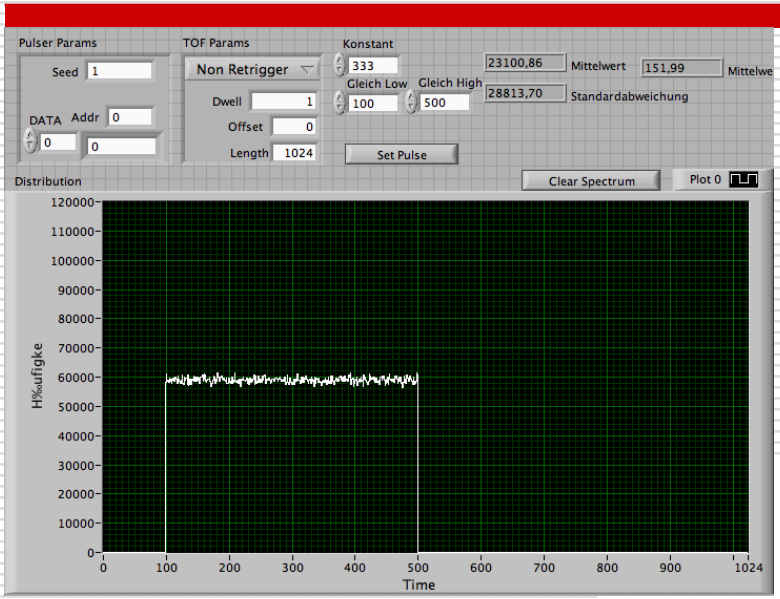
- Duration (32 bit): 10 ns .. 43 s
- (Pseudo) Random Generator (32 bit)
- Distribution table (1K * 32 bit)
- Mode
  - Trigger
  - Free run

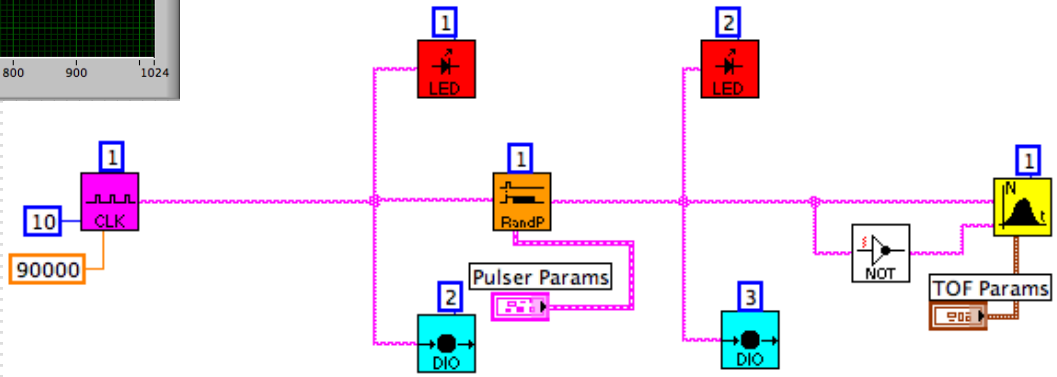


RandomPulser: Funktion

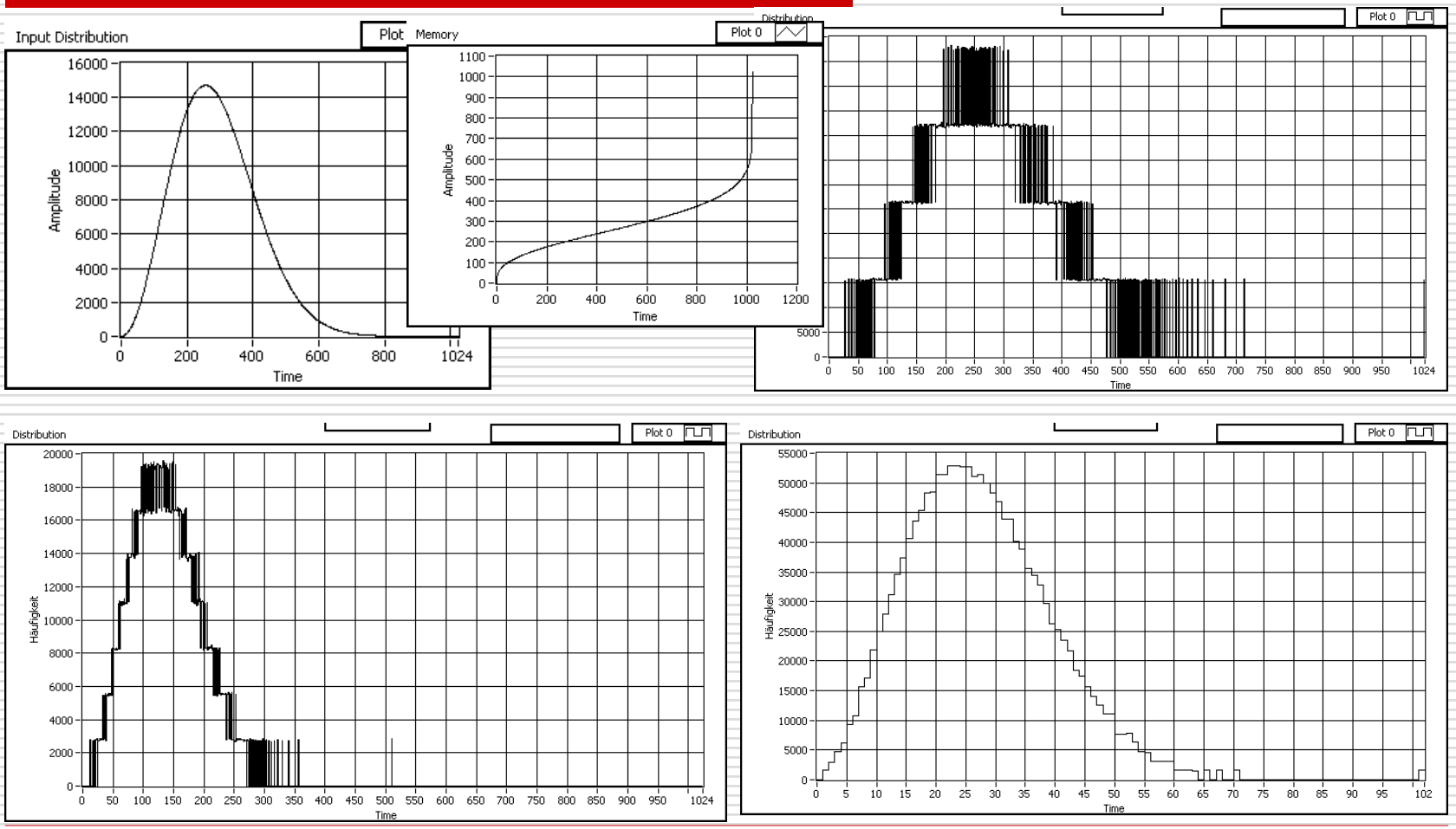


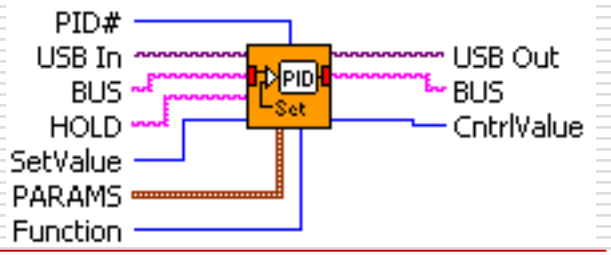
RandomPulser: Messaufbau





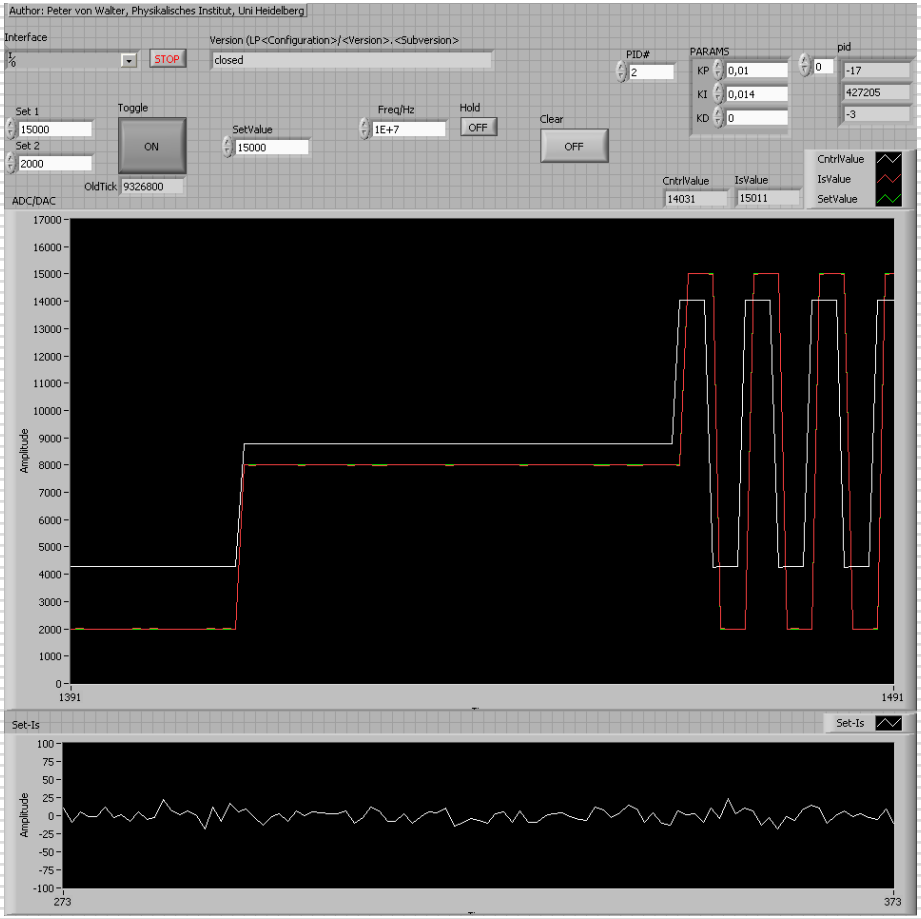
RandomPulser: Boltzman-Verteilung



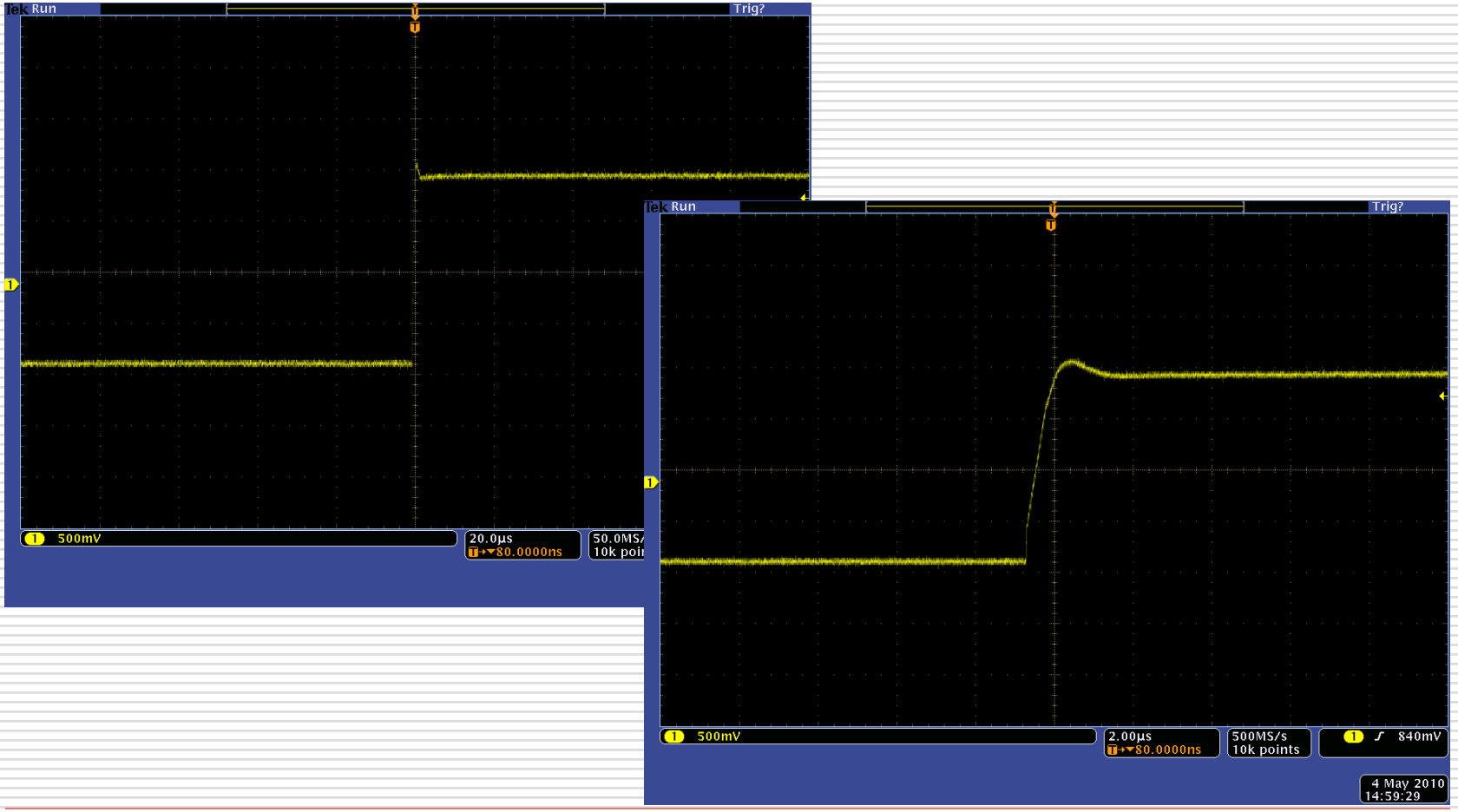


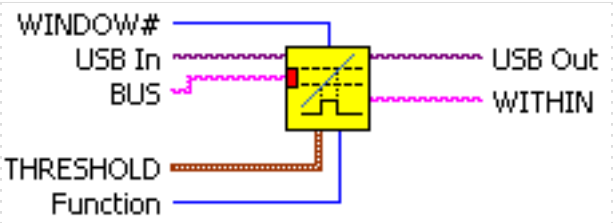
LP: PID

- Digital Controller
- Resolution: 16 bit
- Sampling: 100 MHz
- Latency: 30 ns
- PID-Parameters: 0,1%
- HOLD Function



PID: Performance

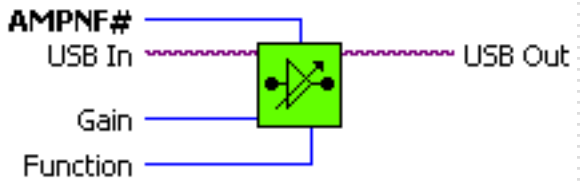




LP: WINDOW

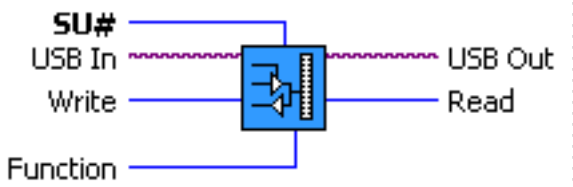
- Digital Comparator
- 2 THRESHOLDs:
  - Lower
  - Upper
- WITHIN:
  - HIGH: Lower <= BUS Data < Upper
  - LOW: Lower < BUS Data > Upper

LP: AMPNF



- SU715: 2 Channel Audio Amplifier
- GAIN programmable: 1 .. 100

LP: SU

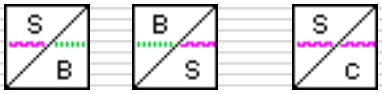


- SUxxx: 32 pins
- Free programmable
  - Write
  - Enable
  - Read
- Application:
  - Tests

LP: NOT

- Inverter
- No extra FPGA resources used!
- Prop. Delay: 0 ns

LP: Converter



- Adaption to LabVIEW
  - B_S: Boolean to Signal (Set)
  - S_B: Signal to Boolean (Get)
  - (S_C: mask MSB for Signal connection number)
- No FPGA resources used!

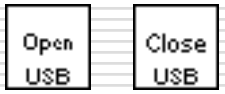
LP: SETUP

SETUP

- System Infos
  - Firmware Configuration/Version
  - LogicBox (DL7xx, Interface, FPGA)
  - SubModules (SU7xx)
    - Type
    - Model
  - LogicPool (FW-Module)
    - Type
    - Model _
    - Number
    - Version ()
    - Connection number

```
LP 255 / V3.3;  30.8.11  15:55:7
------------ LogicBox
DL701: Compact  USB 1.1 XC3S400; 338
------------ SubModules
0: SU706_0: ADC (A0), 14b, 100 Mhz; Digital IO TTL_Coax (2T0); SU706-1,2; 62mA; 520
1: SU700_1: TTL_Coax  (5T0); LED (5I0); 13mA; 153
------------ LogicPool
A0_1(1.0)3: Analog Digital Converter, 100MHz, 14 Bit, BUS; (ADC)
B0_1(1.2)1: Time To Digital Converter,  1 Ch., 10ns, 32b Time, Multihit, BUS;  (TDC); 168
F1_1(1.0)0: FIFO/Histogrammer, 1024x32b, BUS (FIFO); 187
G2_1(1.0)6: Gate Generator, 32b (GATEGEN,GGCOUNTER/GGCLOCK,GGTIME)
G2_2(1.0)7: Gate Generator, 32b (GATEGEN,GGCOUNTER/GGCLOCK,GGTIME)
I0_1(1.0)0: Light Emitting Diode Indicator (LED)
I0_2(1.0)0: Light Emitting Diode Indicator (LED)
I0_3(1.0)0: Light Emitting Diode Indicator (LED)
I0_4(1.0)0: Light Emitting Diode Indicator (LED)
I0_5(1.0)0: Light Emitting Diode Indicator (LED)
L0_1(1.0)4: Logic  (LOGIC,AND/OR/XOR/FF)
L0_2(1.0)5: Logic  (LOGIC,AND/OR/XOR/FF)
M0_1(1.0)2: BusMonitor, BUS; (BUSMONITOR)
T0_1(1.0)8: Digital IO (DIO)
T0_2(1.0)9: Digital IO (DIO)
T0_3(1.0)11: Digital IO (DIO)
T0_4(1.0)12: Digital IO (DIO)
T0_5(1.0)13: Digital IO (DIO)
T0_6(1.0)14: Digital IO (DIO)
T0_7(1.0)15: Digital IO (DIO)
```

LP: OPEN/CLOSE



- OPEN
  - Open data communication
  - global RESET (optional)
  - Read ID and check FW-Version
  - Read Setup (LogicPool modules)
- CLOSE
  - Store Setup (DL706) (optional)
  - Close data communication

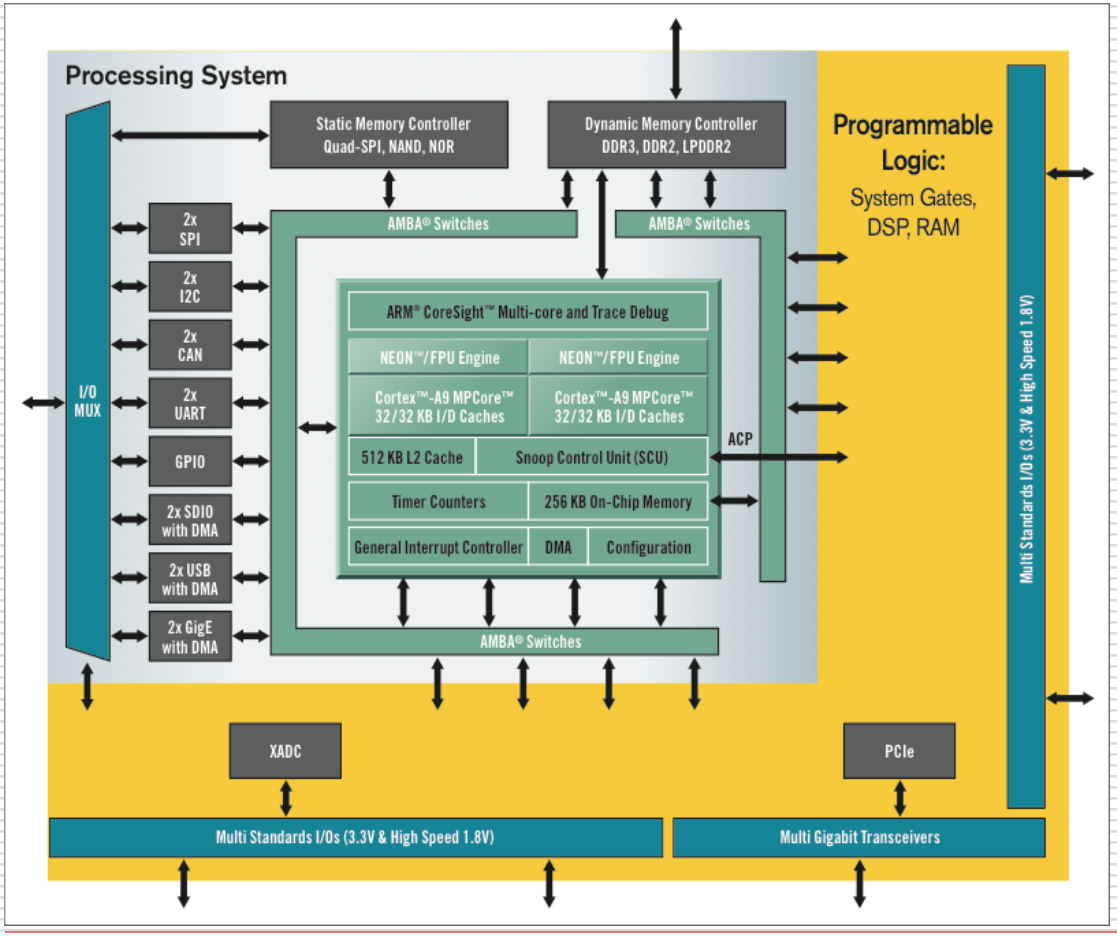
LogicBox: Future

- Bigger & faster FPGAs, Memory, Interfaces
  - Spartan 6, ...
  - DDR2, DDR3, ...
  - Ethernet, Optical, ...
- User Specific Submodules
  - AD-Converter, DA-Converter
    - Multichannel, Resolution, Speed, ...
    - Isolated
  - Memory (Static, Pseudo Static, Flash)
  - Interfaces (Detector spec.)
  - ...
- User specific Firmware
  - ...

Xilinx: FPGA Families

	DL701 DL706 **XC3S400**	DL709, DL710 **XC3S4000**	DL711 **XC6SLX150T**	Advance Product Specification (maximum capability!) **Artix-7**	**Kintex-7**	**Virtex-7**
Logic Cells	8K	62K	147K	348K	478K	2M
Block RAM	36KB	216KB	603KB	2,4MB	4,25MB	12,5MB
DSP Slices	-	-	180	1040	1920	5280
GTPs	-	-	8	16	32	96
Peak Serial BW				211Gbps	800Gbps	2784Gbps
GEthernet	-	-	+	+	+	+
PCIe	-	-	PCI	x4 (2)	x8 (2)	x8 (3)
Memory IF	-	-	4	1066Mbps	1866Mbps	1866Mbps
I/O Pins	116	712	576	600	500	1200
Package	PQ208	BGA	BGA	BGA,FC	FC,HPFC	HPFC

ZYNQ-7000: Features



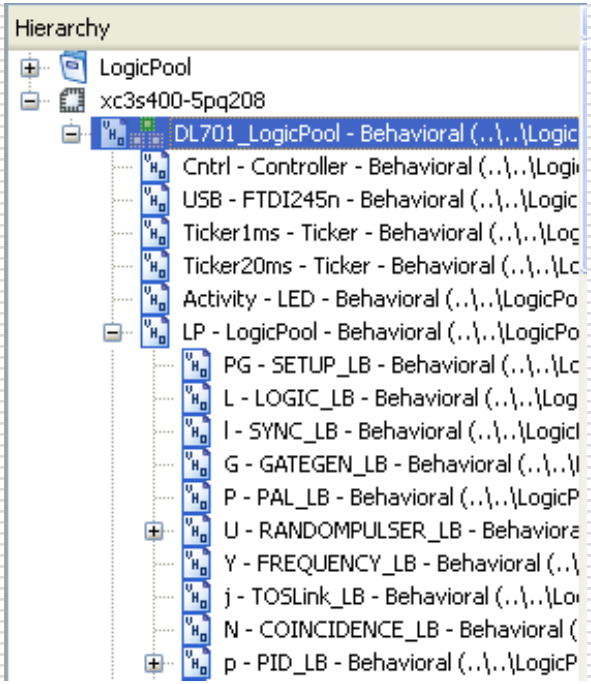
- Dual ARM Cortex-A9 MPCore
  - Up to 800MHz
  - NEON Extension, Single, Double FPU
  - 32kB Instr. & 32kB Data L1 Cache
- Unified 512kB L2 Cache
- 256kB on-chip Memory
- DDR3, DDR2,LPDDR2 Dyn. Memory Controller
- 2x QSPI, NAND Flash & NOR Flash Controller
- 2x USB2.0 (OTG), 2x GbE, 2x CAN2,0B 2x SD/SDIO, 2x UART, 2x SPI, 2x I2C, 4x 32b GPIO
- AES & SHA 256b encryption engine
- Dual 12bit 1Msps Analog-to-Digital converter
  - Up to 17 Differential Inputs
- Advanced Low Power 28nm Progr. Logic:
  - .. 235k Logic Cells (.. 3.5M of equivalent ASIC Gates)
  - .. 1.86MB Extensible Block RAM
  - .. 760 18x25 DSP Slices (58 to 912 GMACS peak DSP performance)
- PCI ExpressÆ Gen2x8 (in largest devices)
- 154..404 User IOs (Multiplexed + SelectIO)
- 4..12 12.5Gbps Transceivers

ZYNQ-7000 : Family

		Zynq-7000 Product Table (Software View)			
	Device Name	Z-7010	Z-7020	Z-7030	Z-7040
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z040
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ and Single/Double Precision Floating Point			
	Maximum Frequency	800 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support	DDR3, DDR2, LPDDR2			
	External Static Memory Support	2x QSPI-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Security	AES and SHA 256b for secure boot			
	Peripherals and Static Memory Multiplexed I/O[1]	54			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	235K Logic Cells (~3.5M)
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	1,860KB (465)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	760
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	912 GMACS
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for secure configuration			
	Multi-Standards 3.3V I/O[2]	100	200	250	350
	Serial Transceivers[2]	—	—	4	12

LogicPool: Open Source

- Modular
  - Common interface
  - Hierarchic setup
  - VHDL (ISE)
    - Modify
    - Extend
    - Exchange
- Setup
  - Constants package
  - UCFs




```
package LogicPool_Setup is
   constant LB            : LB_Setup  := (DL701,255);
   constant SU_s          : SU_Setup  := ((SU728,0),(SU700,1),(SUempty,0),(SUempty,0));
   constant PID_s         : LP_Setup  := (1,2);
   constant GateGen_s     : LP_Setup  := (2,0,0);
   constant LUT_s         : LP_Setup  := (1,0);
   constant BusMonitor_s  : LP_Setup  := (2,0,0);
end LogicPool_Setup;
```

DL711: Blockdiagram