

# Status of the OT readout electronics in Heidelberg

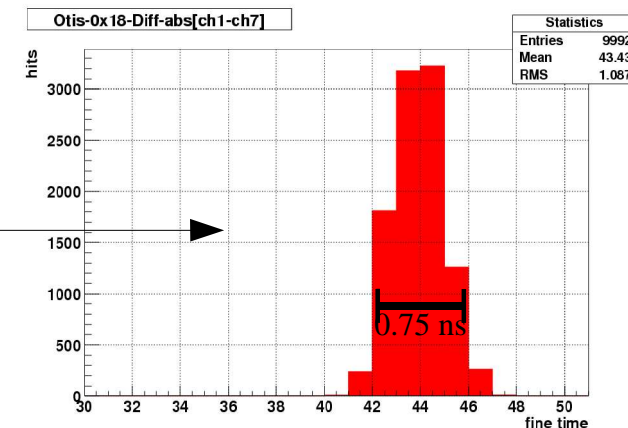
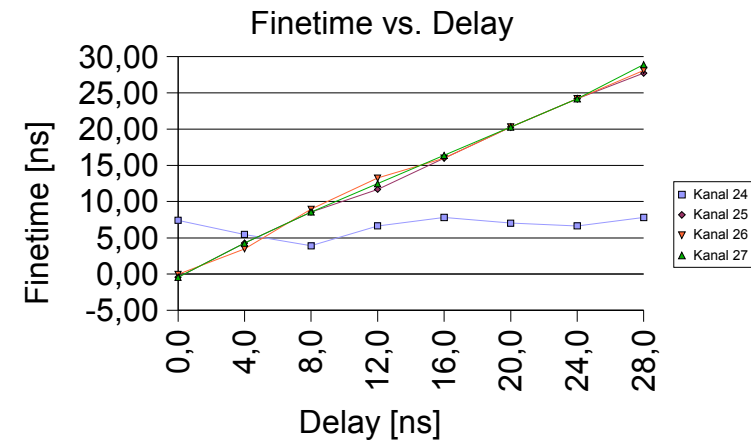
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# Progress since the electronics review

- ASDBLR used with Straw module + FE-box + OTIS 1.1
- OTIS 1.0 and OTIS 1.1 tested in readout chain
- GOL-AUX modifications for preproduction under way
- FE-Box tested with optical link, on module tests started
- O-RxCard: readout tests, BERT, samples for preproduction ready
- TELL1 emulation used for data acquisition

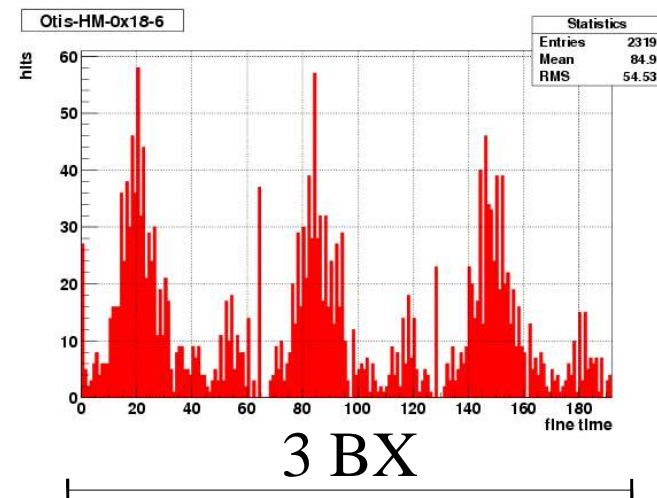
# ASDBLR

- System test with with full FE-box (OTIS 1.0):
  - Coupling clock synch. Pulses into ASDBLR via delay
- System with ASDBLR on FE-box, OTIS 1.1 on test board
  - Delayed Pulser signal in ASDBLR rel. Pulser signal on OTIS 1.1



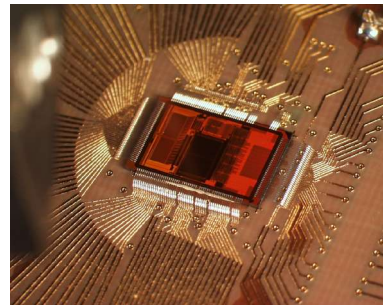
# ASDBLR noise

- Noise observed at 600 mV  
3 fC threshold, bad grounding
  - Data shows 12.5 ns  
„harmonics“
- ASDBLR on Module
- OTIS 1.1 for fine time measurement

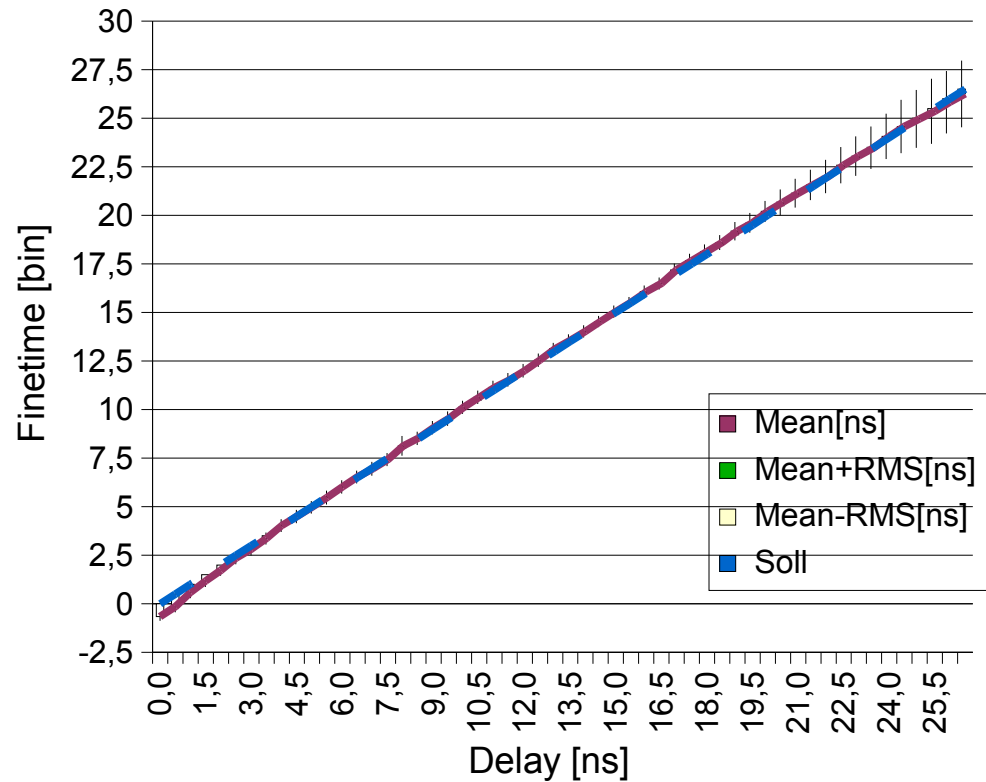


# OTIS

- OTIS 1.0 tested in full FE box
- OTIS 1.1 on test board
  - Integrated non linearity good: max. 0.7 ns off
  - ASDBLR thresholds within 8 mV of programmed level
  - First data with cosmic set up taken

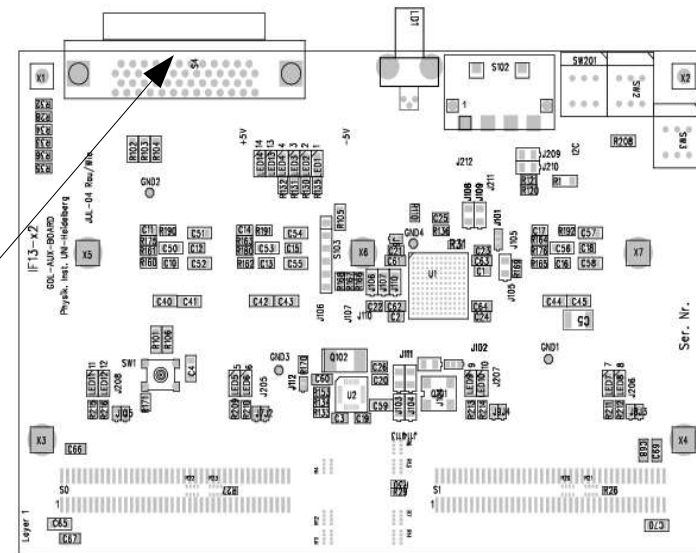


Finetime vs. Delay



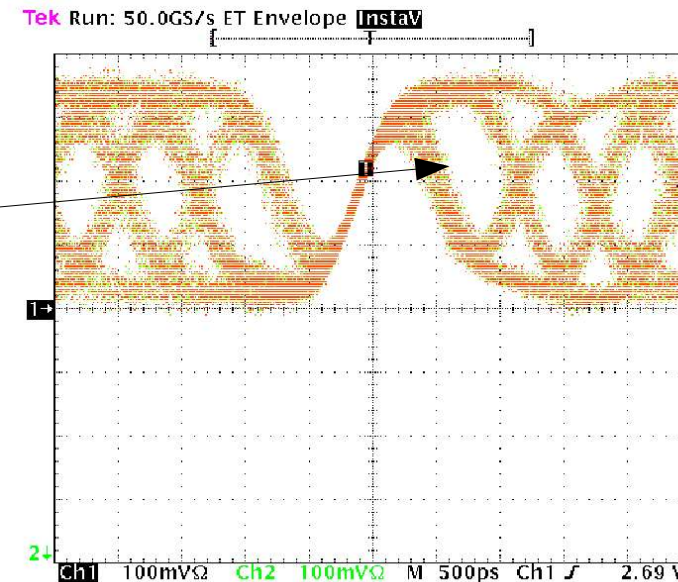
# GOL-Aux Board

- First version works but needs modifications:
  - QPLL locking range too small – better results for smaller board capacity? - TTCrq now in HD
  - Monitor for QPLL/GOL + Clock sel.
  - Termination for OTIS Data
  - Passive distribution of TFC signals
  - Negative power regulator demands tantalum or ceramic+series R
  - Now SCSI2 50-pin for TFC
  - LVDS I2C



# O-RxCard

- O-RxCard fully tested
  - BERT: error rate (one channel)  
 $< 2.6 * 10^{-15}$
  - Eye diagrams good
  - Series termination examined 30  
– 50 Ohm optimum
  - Test with new Emcore receiver
- First 3 Preproduction samples
  - Very good optical impression
  - Fast turnaround
    - 13 days for PCB
    - 11 days for mounting

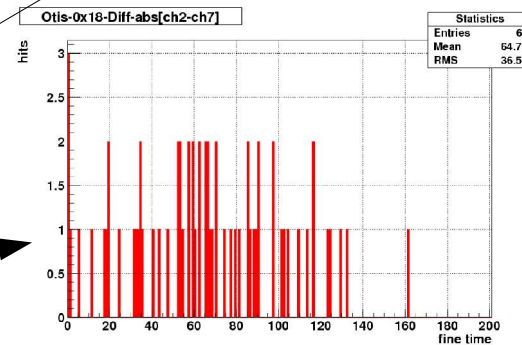


# TELL1 emulation

- All data taking for tests now with STRATX PCI card
- High data throughput 115s for 1 million events
- TTL or LVDS transmission from O-RxCard (4 links)
- Text menu control
- ROOT diagrams
- 2 systems in use

## SHIPPO\_STRATIX main menu

1. Write Config Registers
  2. Read Config Registers
  - 3.
  4. Send Command
  5. Write Events to File
  6. Print Events on Screen
  7. Read LED Status
  8. Set Dummy Readout Event Rate
  9. Access SHIPPO\_STRATIX registers by name
  10. Access SHIPPO\_STRATIX memory and IO ranges
  11. TURN non\_zero mode ON
  12. TURN reset, start & stop before reading OFF
  13. TURN reset fifo while print on screen ON
  99. Exit
- Enter option:





# Summary and outlook

- System tests for ASDBLR + OTIS + GOL + O-RxCard + PC
- Biggest drawback QPLL operation / locking range
- System tests with full readout plus Module has started
- Szintillator Trigger plus time reference works
- Preproduction for O-RxCard in good shape
- To do:
  - GOL AUX board redesign
  - Testing of LVDS I2C
  - Testing of 4-12 optical link readout