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Development and Test of a Radiation Hard Dual Port Static-RAM with 2.2GByte/sec Data Rate for the LHCb Outer Tracker Readout Electronics

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Abstract

In this thesis a dual port Static Random Access Memory (SRAM) in radiation hard CMOS technology has been developed. It will be integrated on the OTIS TDC chip which is a key element in the readout chain of the LHCb outer tracker. The memory is characterized by its extreme word length of 240bit which enables data rates of 1.1GBytes/sec on each port at the nominal frequency of 40MHz. Therefore, special care has been taken of low-power design, in order to keep cross-talk to analog devices on the TDC low.
A test-chip has been designed to study the performance of the SRAM under realtime conditions. Simulation results and measurements are presented and compared.

Zusammenfassung

Entwicklung und Test eines strahlenharten Dual Port Static-RAMs mit 2.2GByte/sec Datenrate für die LHCb Outer Tracker Auslese-Elektronik:
In dieser Diplomarbeit wurde ein Dual Port Static Random Access Memory (SRAM) in strahlenharter CMOS Technologie entwickelt. Es soll im OTIS TDC Chip integriert werden, einem Schlüsselelement in der Auslesekette des LHCb Outer Tracker. Das Memory wird durch seine extreme Wortlänge von 240bit charakterisiert, wodurch pro Port Datenraten von 1.1GByte/sec bei der nominellen Frequenz von 40MHz ermöglicht werden. Besonderer Wert wurde auf niedrige Leistungsaufnahme gelegt, um das Übersprechen auf analoge Komponenten des TDCs gering zu halten.
Ein Testchip wurde entworfen, um die Funktionalität des SRAMs im Echtzeitbetrieb zu untersuchen. Simulationsergebnisse und Messungen werden präsentiert und verglichen.

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Chapter 1

Introduction

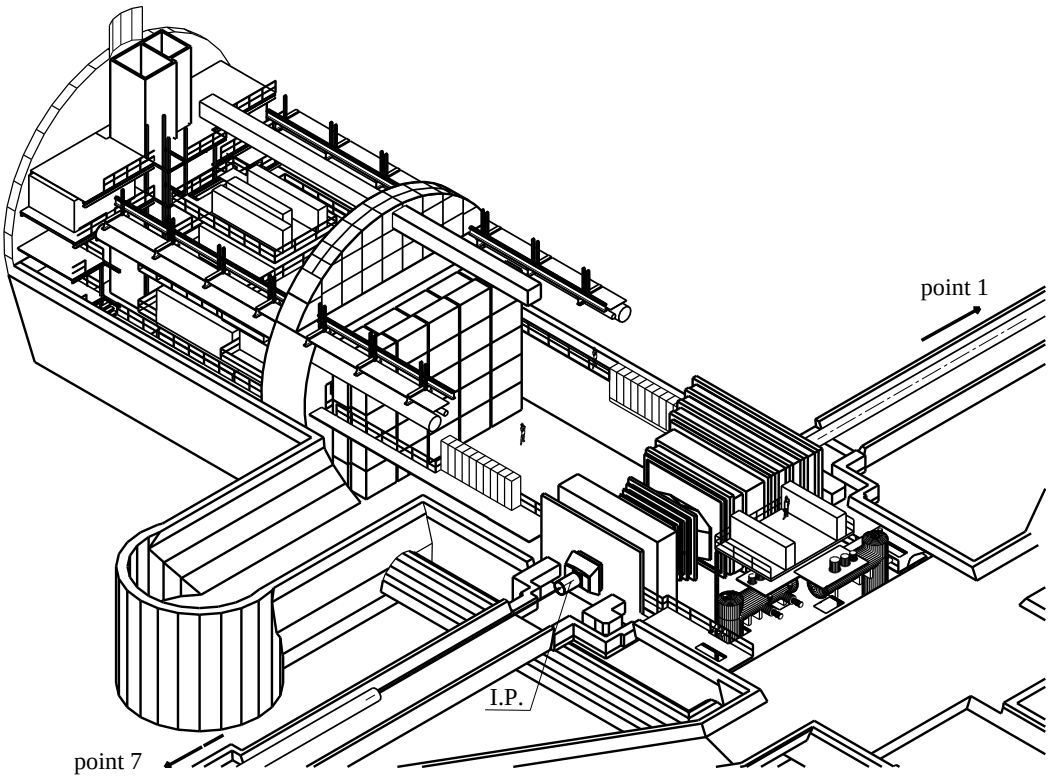

Figure 1.1: Experimental zone of the LHCb experiment

1.1 LHCb experiment

The idea that matter is assembled by particles that cannot be split is old. Demokrit (460 BC) stated this thought for the first time and called those particles atoms. Today it is known that atoms consist of electrons, protons and neutrons. Only the electron is believed to be

elementary, but protons and neutrons are compositions of quarks. The analysis of matter on a sub-nucleon level is made possible by large colliders which produce either head on collisions of two bunches of particles or collisions of one bunch with a fixed target. The Large Hadron Collider (LHC) at CERN (Switzerland) is of the first type and will provide collision energies of 14TeV. The magnitude of the collision energy is the key factor for the physics that can be performed at a collider. The Large Hadron Collider beauty (LHCb) experiment is supposed to start in 2006 and plans to operate with an average luminosity of 2×10^{32} cm^{-2} s^{-1}. The LHCb detector is designed to exploit the large number of b-hadrons produced at the LHC in order to make precision studies of CP-asymmetries and of rare decays in the B-meson systems. Figure 1.1 shows the experimental zone of the LHCb experiment.

1.1.1 CP-violation in the B-meson system

Symmetries are always of great importance for the understanding of physics. Long time it was believed, that the laws of nature are invariant to symmetry operations like parity P and charge conjugation C. In 1960 weak decays of pions and muons showed that C- and P-symmetry is not conserved. CP violation was first discovered in neutral kaon decays in 1964 [1]. CP in the weak interaction is generated by the complex three-by-three unitary matrix, known as the CKM matrix, introduced by Kobayashi and Maskawa [2]:

$$V_{\mathrm{CKM}} = \begin{pmatrix} V_{\mathrm{ud}} & V_{\mathrm{us}} & V_{\mathrm{ub}} \\ V_{\mathrm{cd}} & V_{\mathrm{cs}} & V_{\mathrm{cb}} \\ V_{\mathrm{td}} & V_{\mathrm{ts}} & V_{\mathrm{tb}} \end{pmatrix}.$$

V_{ij} describe the relative strengths of the transition of down-type quarks (j = d, s, b) to up-type quarks (i= u, c, t). Since V_{CKM} is unitary, it is defined by four parameters. The most convenient parameterization was proposed by Wolfenstein [3] and gives an expansion up to third order in λ, where λ is the sine of the Cabibbo angle [4], measured to be 0.221 ± 0.002 [5] from decays involving s-quarks:

$$V_{\mathrm{CKM}} \approx V^{(3)}_{\mathrm{CKM}} + \delta V_{\mathrm{CKM}}$$

$$V^{(3)}_{\mathrm{CKM}} = \begin{pmatrix} 1-\lambda^2/2 & \lambda & A\lambda^3(\rho - i\,\eta) \\ -\lambda & 1-\lambda^2/2 & A\lambda^2 \\ A\lambda^3(1-\rho-i\,\eta) & -A\lambda^2 & 1 \end{pmatrix}.$$

$$\delta V_{\mathrm{CKM}} = \begin{pmatrix} 0 & 0 & 0 \\ -i\,A^2\lambda^5\eta & 0 & 0 \\ A(\rho + i\,\eta)\,\lambda^5/2 & (1/2-\rho)\,A\lambda^4 - i\,A\lambda^4\eta & 0 \end{pmatrix},$$

For a qualitative discussion of CP violation in B-meson systems, $V^{(3)}_{\mathrm{CKM}}$ is sufficient and the second term δV_{CKM} can be ignored.

In the Wolfenstein's parametrization V_{CKM} can be described by two unitarity triangles (figure 1.2). The asymmetry in the B and $\overline{\mathrm{B}}$ decays determines the angles of the unitary triangles. They can be measured by the following decays:

1. $\beta + \gamma$ from $\mathrm{B^0_d} \to \pi^+\pi^-$
2. β from $\mathrm{B^0_d} \to \mathrm{J/\psi K_S}$

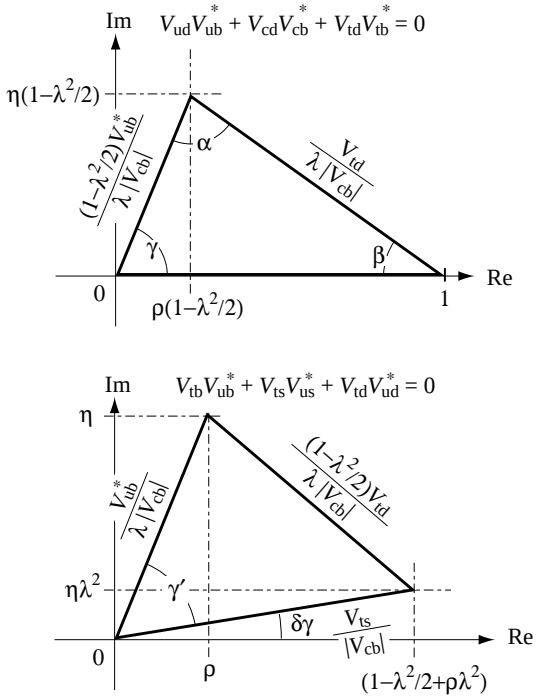

Figure 1.2: Two unitarity triangles in the Wolfenstein's parameterization with an approximation valid up to $\mathcal{O}(\lambda^5)$.

3. $\gamma - 2\delta\gamma$ from $B_s^0 \to D_s^{\pm}K^{\mp}$
4. $\delta\gamma$ from $B_s^0 \to J/\psi\phi$
5. γ from $B_d^0 \to \overline{D}^0K^{*0}, D^0K^{*0}, D_1K^{*0}$,

1.1.2 Experimental setup

The LHC reuses the accelerator tunnel of the LEP experiment. The detector for the LHCb experiment is currently under construction and will be located at the interaction point where the DELPHI experiment was performed. It is a single-arm spectrometer with a forward coverage of 10 to 300mrad [6]. This geometry is motivated by the fact that due to their high energies both the b- and the $\overline{b}$-hadrons are emitted in a narrow forward cone. The general layout is shown in figure 1.3. The detector is assembled by a vertex detector system, a tracking system, RICH counters, an electromagnetic calorimeter, a hadron calorimeter and a muon detector. A spectrometer dipole magnet is placed close to the interaction region. It changes the direction of charged particles whose momentum can so be measured precisely by the tracking system. There are two tracking system units, the inner and the outer tracker.

The last consists of drift cells with strawtube geometry. Correlated signals from many straws in the tracker enable reconstruction of the particle's track. High voltage is applied between the conducting straw and a sense wire which runs along the center of the straw. The straw is filled with $Ar/CO_2/CF_4$ 75/10/15. When a particle crosses the device, ionization of the drift gas takes place. The electrical field causes an avalanche of electrons drifting towards

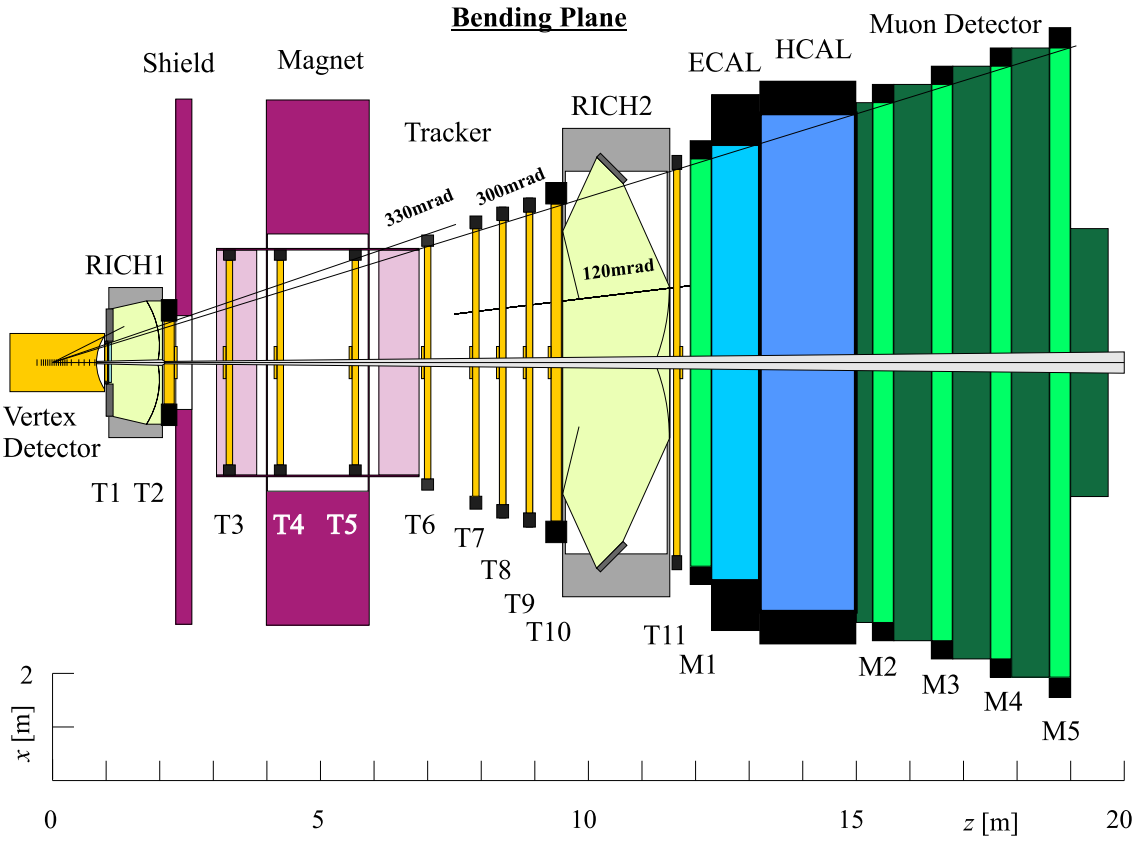

Figure 1.3: The LHCb detector seen from above

the sense wire. Typical drift times are expected to be below 50ns. The drift time information is important, since it allows to measure the radial distance of the track from the sense wire with a resolution of 200μm . The signals from 110,000 channels of the outer tracker are pre-amplified by ASD chips (Amplifier Shaper Discriminator) and then digitized and selected by TDCs (Time to Digital Converter).

1.1.3 TDC

The TDC (Time to Digital Converter) is a key element in the readout chain of the Outer Tracker. Different solutions have been suggested that fit the specification more or less. The HPTDC by Jörgen Christiansen could be used although its specifications are not ideal for this purpose. It is considered as a backup solution. The preferred chip is the OTIS TDC [7], since it is designed to fit the LHCb requirements. The preferable readout scheme in the LHCb environment is a synchronous clock driven scheme, due to high trigger rates and occupancies and short drift times. If that scheme is supported by the TDC, a high internal data rate has to be handled, since data is taken every cycle, even when no hit has been detected. The benefit of this approach is that no intrinsic dependency on occupancy is introduced.

Figure 1.4 shows the block diagram of the OTIS TDC. It is clocked with the LHC bunch crossing frequency of 40MHz. A DLL (delay locked loop) resolves a clock cycle in 64 time bins. This gives a resolution of 0.39ns. If a hit occurs the DLL's state is latched into the

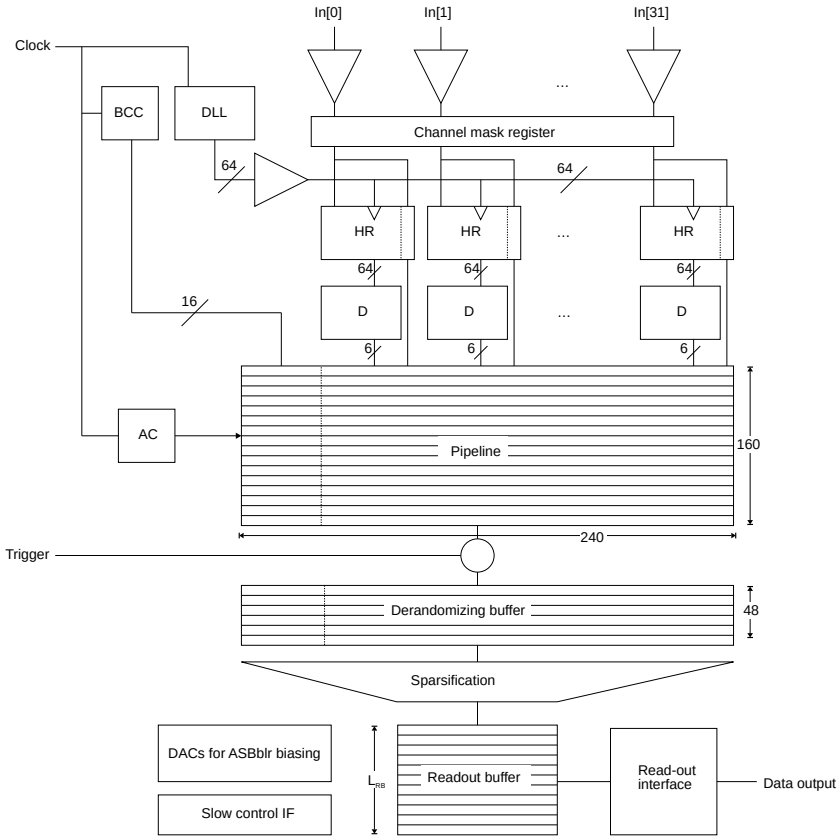

Figure 1.4: OTIS TDC

hit register and a hit flag is set indicating that the hit register's data is valid. The location of the 0-1 transition in the hit register is encoded into a 6bit drift time code. The content of all hit registers and the content of the bunch crossing counter (BCC) is transferred into the pipeline every clock cycle. The write pointer is forwarded every bunch crossing so the pipeline actually acts as a ring buffer. The level 0 trigger of the LHCb experiment triggers the transfer of data from the pipeline into the derandomizing buffer.

1.2 CMOS technology

Complementary Metal Oxide on Semiconductor (CMOS) technology is the state of the art of today's electronics development. Its characteristics are low power, good linearity and simple processing. Detailed information can be found in [8].

1.2.1 CMOS principles

The MOSFET (Metal Oxide on Semiconductor Field Effect Transistor) is one of the most important devices in microelectronics. A distinction is drawn between a n-channel MOSFET and a p-channel MOSFET. A n-channel MOSFET is defined by two highly n-doped regions, source and drain. They are separated by the gate, a conducting layer insulated from the

p-substrate (bulk) by a very thin oxide layer. The p-channel MOSFET is placed in a n-substrate. Its source and drain are highly p-doped regions. Both devices can be implemented on the same chip. Therefore, one of them has to be placed in a well doped opposite to the substrate. The TDC is implemented in an n-well process. A summary of the MOSFET model for both n-channel and p-channel devices in the low frequency approximation is shown in table 1.1. Figure 1.5 visualizes the characteristics of the MOSFET.

n-channel MOSFET

$$I_G = 0$$

$$I_D = \begin{cases} 0 & V_{GS} < V_T \text{ (cutoff)}, V_{DS} \geq 0 \\ \frac{K'W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} & V_{GS} > V_T,\ 0 < V_{DS} < V_{GS} - V_T \text{ (ohmic)} \\ \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) & V_{GS} > V_T, V_{DS} > V_{GS} - V_T \text{ (saturation)} \end{cases}$$

p-channel MOSFET

$$I_G = 0$$

$$I_D = \begin{cases} 0 & V_{GS} > V_T \text{ (cutoff)}, V_{DS} \leq 0 \\ -\frac{K'W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} & V_{GS} < V_T,\ 0 > V_{DS} > V_{GS} - V_T \text{ (ohmic)} \\ -\frac{K'W}{2L}(V_{GS} - V_T)^2(1 - \lambda V_{DS}) & V_{GS} < V_T, V_{DS} < V_{GS} - V_T \text{ (saturation)} \end{cases}$$

Design parameters:	W	=	channel with
	L	=	channel length
Process parameters:	K'	=	transconductance parameter
	λ	=	channel length modulation parameter

Table 1.1: Low-frequency MOSFET model

1.2.2 Radiation hardness [9, 10]

The TDC will be exposed to ionizing radiation up to 1Mrad total dose in 10 years. Conventional electronics shows some severe effects at such exposure. It can be distinguished between total ionizing dose effects and single event effects. In the LHCb environment both are caused by electrons and charged hadrons. Neutral particles such as neutrons and γ-particles can cause ionization secondarily by energy deposition.

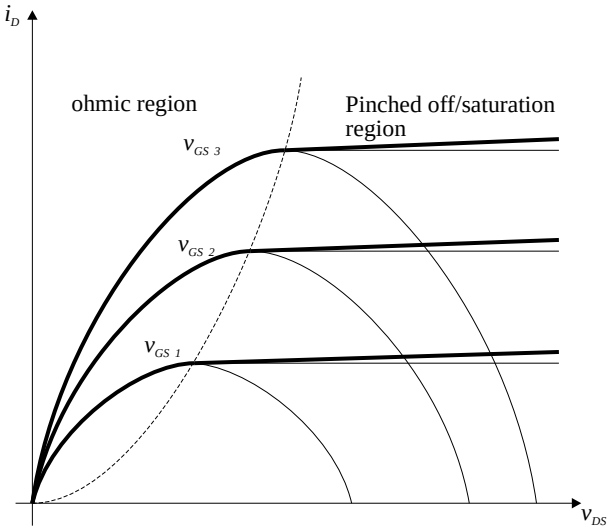

Figure 1.5: MOSFET characteristics

Total ionizing dose effects

Cumulative radiation effects occur during the complete time an electronic device is exposed to radiation. The most sensitive part of a MOS transistor is the gate oxide. If an electron-hole pair is created by ionization in the gate oxide when no gate voltage is applied, it will recombine after a short time. Once the transistor is turned on, the electric field in the gate oxide will separate the electron from the hole. Due to its much higher mobility the electron will leave the oxide within the order of a picosecond and recombination becomes very unlikely. The hole travels much slower along the electrical field and eventually gets captured in deep trapping sites [11]. These arise from interface states which are energy levels between the conduction and the valence band. They are caused by lattice mismatch at the interface, disconnected atomic bonds or impurities. The electrical effect of those trapped holes is a positive offset in the effective gate voltage. This is reflected by a shift in the transistor's threshold voltage V_{T} (figure 1.6). The lifetime of trapped holes is determined by recombination processes with electrons injected into the gate oxide. Under constant exposure to radiation the threshold voltage shift will find an equilibrium. If the thickness of the gate oxide is significantly smaller than 20nm tunneling becomes the most efficient process determining the lifetime of trapped holes. Today's deep sub-micron technologies are therefore very suitable for applications in irradiated environment.

Another part that is sensitive to trapped charges is the field oxide in an n-MOS transistor. The field oxide is much thicker than the gate oxide, so tunneling is not effective. Accumulated holes in the field oxide produce a parasitic channel in the adjacent substrate which forms a leakage path from source to drain (figure 1.7). This effect can be handled by an edgeless transistor layout. Therefore, the gate has to be designed ring shaped, enclosing the source and so eliminating field oxide paths from source to drain. Figure 1.8 shows the different layouts of a linear and an enclosed transistor. The price that has to be paid for this method is a limitation in the design parameters. The minimum width of the enclosed type is about four times bigger than of the linear one. Therefore, radiation hard layouts are principally

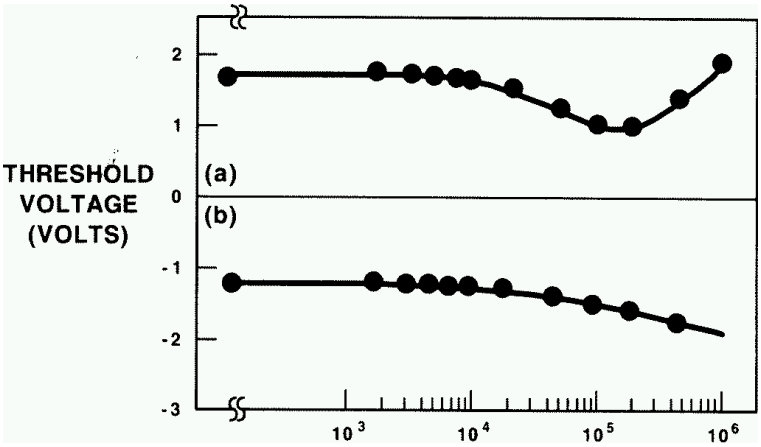

Figure 1.6: Threshold voltage shift of n-MOS (a) and p-MOS (b) transistor [9]

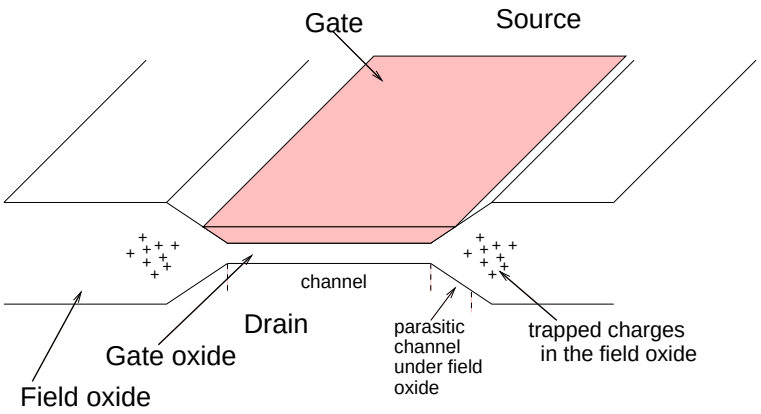

Figure 1.7: Parasitic leakage current. Due to trapped charges in the field oxide a channel is created which forms a leakage path from source to drain.

larger than conventional designs.

Single event effects

Single event effects are triggered by single particles that cross the device. Sub-micron processes are more sensitive to those effects due to their smaller diffusion nodes (source and drain).

Single event upset (SEU) is the effect of flipping memory states in an electronic device. If ionization takes place within a pn-junction of a transistor, a current spike is generated originating from the electron-hole pairs created by this event. The linear energy transfer (LET) is dependent on the mass of the ionizing particle and is a measure for the amount of charge set free. Especially, the heavy B-mesons in the LHCb experiment are expected to be a source for SEU. The minimum LET needed to cause a SEU is called critical LET. It is strongly dependent on the fabrication process.

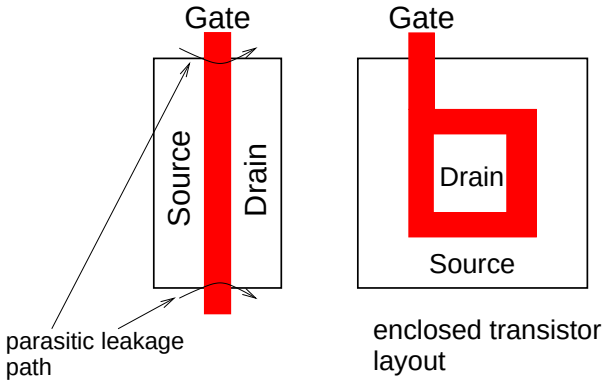

Figure 1.8: Linear and enclosed transistor layout

Single event latchup (SEL) may occur due to high temperature, large transients on the power supply or ionizing particles. Inherently present bipolar transistors in a CMOS device can be completely turned on and so cause short circuits. This event is usually destructive. The presence of these parasitic npn and pnp structures is presented in figure 1.9. The collector of the npn transistor is connected to the base of the pnp transistor. In case of an increasing collector current in the pnp transistor base current and collector current of the npn transistor are also increasing. This positive feedback leads to a short circuit between the power supplies. Special layout techniques help to reduce the sensitivity for SEL. The systematic use of guardrings around the wells of transistors ensures a low-ohmic connection of the bipolar transistors.

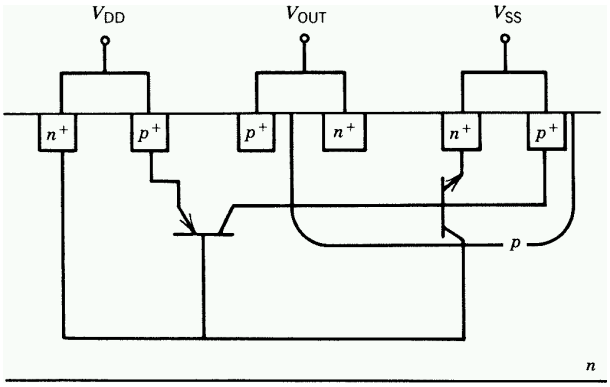

Figure 1.9: Parasitic npn and pnp bipolar structures in a CMOS device

Chapter 2

Design and Simulation of Radiation Hard Static-RAM

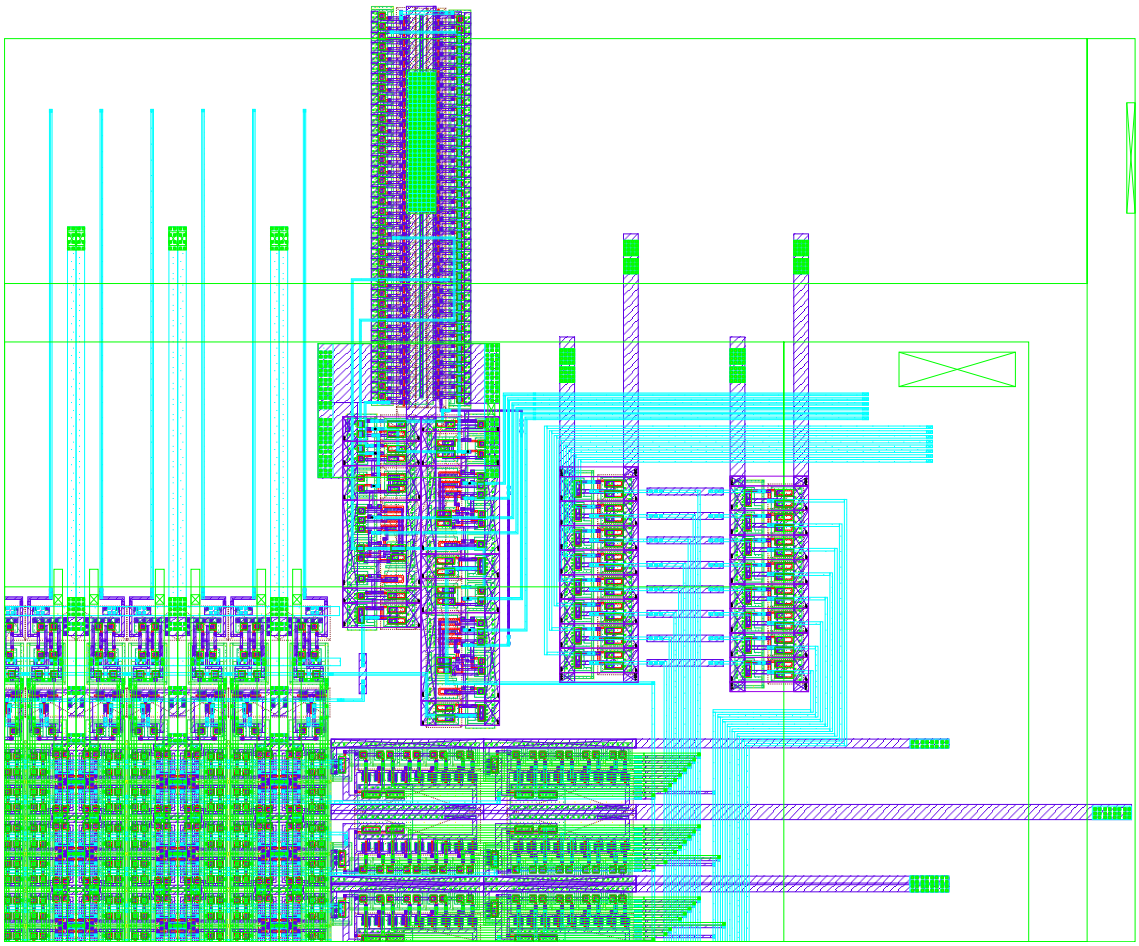

Figure 2.1: Partial view of the layout of the OTIS pipeline

2.1 Design specifications

A full custom design dual port Static-RAM in radiation hard layout technology has been developed for the OTIS TDC. The pipeline and the derandomizing buffer are planned to be implemented this way. The memory is characterized by its extreme width, since each TDC receives data from the ASD chips on 32 channels. The time information of each channel is converted by the TDC to a 6bit time code. Additionally, there is a hit bit for every channel indicating if a hit has occurred. Besides this, a 16bit bunch crossing code has to be stored each clock cycle giving a total pipeline width of 240bit. This results in massive parallel switching actions which have to be considered carefully to obtain current limits.

The maximum latency of the level 0 trigger in the LHCb experiment is specified to be 4μs. According to the 40MHz bunch crossing clock this means a pipeline length of 160 entries. The prototype has been designed with a length of 186. The data flow of the LHCb experiment requires simultaneous readout while new data is written into the pipeline. Thus, for the SRAM solution of the pipeline two address ports are required.

2.2 SRAM basics

The major part of a static RAM is an array of memory cells each storing one bit of digital information. A cell's state can be read out or set via a pair of bit-lines. In case of readout, the memory cell becomes the driver for the bit-lines and an output amplifier senses the state and eventually latches it until the next bit is read out. During a write process the bit-lines are driven by the input amplifiers. Fundamentals of memory design can be found in [12]. Table 2.1 summarizes the nets of the OTIS pipeline.

Signal	Name	Description
W	write enable	controls write process
AdrW(7:0)	write address	defines the write pointer
$\overline{\text{WPrS}}$	not write-precharge select	switches the write prechargers
IE	in enable	connects the input amplifier to the bit-lines
DE	decoder enable	enables the write decoder
WS(x)	write select	selects word #x for write
DI, $\overline{\text{DI}}$	data in, not data in	write bit-lines
R	read enable	controls read process
AdrR(7:0)	read address	defines the read pointer
$\overline{\text{PrS}}$	not read-precharge select	switches the read prechargers
RS(x)	read select	selects word #x for read
OE	out enable	triggers the data output
DO, $\overline{\text{DO}}$	data out, not data out	read bit-lines

Table 2.1: Nets of the memory

2.2.1 Memory cell

The standard solution for a Static RAM cell are two inverters which are mutually fed back. This forms a system with two stable and one unstable equilibrium. The stable ones define the digital state the cell is in. The cell can be switched from one state to the other by forcing the two nets in the feedback circuit to opposite logic. This requires that the impedance of the driver performing the flip is sufficiently low, since the memory cell works against the driver. The memory cell is addressed by a select-line, which connects the cell via two pass transistors to the bit-lines. In case of a dual port memory, this means that there are two select-lines and four bit-lines. Figure 2.2 shows the schematic and layout of the memory cell.

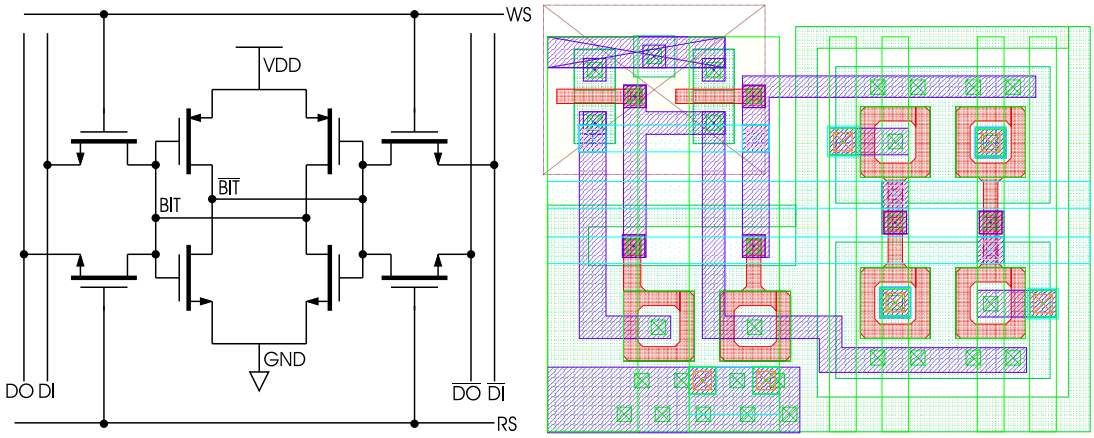

Figure 2.2: Memory cell - schematic and layout

The size of the memory is mainly determined by the size of the cell. Thus, the cell ought to be designed for minimum size. The radiation hard technology requiring edgeless n-channel transistors puts a limit to the minimization. The minimum size edgeless transistor width in the 0.25μm process used is 3.19μm and therefore 4 times bigger then a linear minimum size transistor with a width of 800nm. Considering the two inverters of the cell this is not of a big disadvantage. The reason is, that during a read process the memory cell itself has to act as a driver for the bit-lines. It is convenient to precharge the bit-lines to an initial voltage of about 1.6V. This means that only the n-channel transistors of the cell acting as pull-down device drive the bit-lines while the p-channel transistors can be minimum size linear transistors. Only the pass transistors forming the ports are negatively influenced in size by the radiation hard design.

The memory cells are connected via their word- and bit-lines and so form the memory array. The bit-lines run vertically and are connected to the sources of all port transistors of a channel (column). Therefore, the bit-lines form a capacitive load that has to be driven either by the input amplifier or a cell that reads out its state. But also the word-lines which run horizontally and are driven by the decoders have a high capacitance, which is determined mainly by the gate capacitance of the port transistors. The simulation shows that the word-lines have to be divided into two blocks and connected via a buffer in order to maintain current limits.

2.2.2 I/O amplifiers

The input and output amplifiers are connected to the bit-lines at the end of the memory array. Since the two ports of the OTIS pipeline are specialized for either writing or reading, there is a pair of bit-lines connected to the input amplifier at one end and the other pair to the write amplifier at the other end.

Input amplifier

For writing information into the memory, the bit-lines have to be charged to opposite levels by the input amplifier. After that, a select-line addresses one of the cells in each channel and, in case the cell's state is different from the bit-lines, it is forced to flip. The fact that the bit-lines are connected to each cell in a channel by a pass transistor causes them to be a high capacitive load. Thus, during a write process the input driver has to charge the bit-lines first and when the select-line is pulled, the capacity of the bit-lines provides the driving force for the bit-flip. This has a major advantage in this specific design. Since there are 240 channels switching parallel, the peak currents add up to a level where cross-talk of the RAM

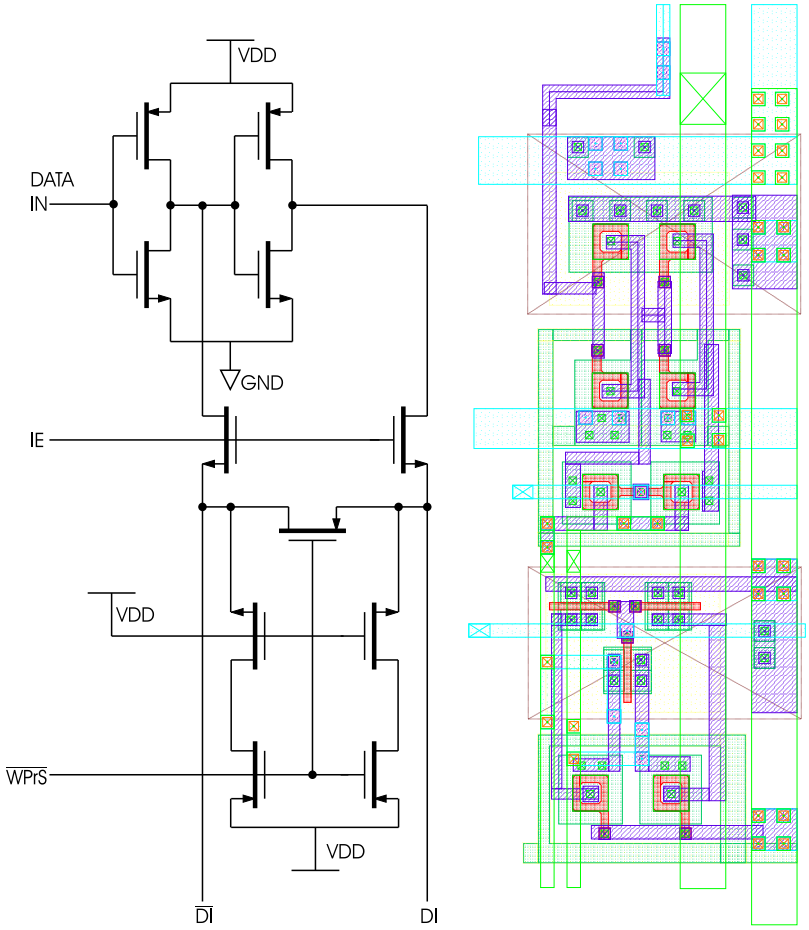

Figure 2.3: Input amplifier - schematic and layout

with other, analogue parts on the chip have to be considered. The driving force of charged bit-lines is exactly the reason why the input drivers can be designed rather small. Therefore, the current peaks can be kept on an acceptable level. This advantage is obsolete when the depth of the RAM is reasonably smaller. Then the capacitance of the bit-line is not large enough to perform a bit-flip, so the input drivers had to be stronger. Figure 2.3 shows the schematic and layout of the input amplifier.

Output amplifier

The output amplifiers task is to read the information from the read bit-lines and to provide a defined output signal. Even when data is not valid during the read cycle the output of the amplifier has to be in either of the two digital states, since devices connected to the RAM might be sensitive to a non-digital state. In any case, preceding drivers would show an increased power consumption due to counter performing pull-up and pull-down devices. In this output amplifier, a single port memory cell has been integrated, which latches the data

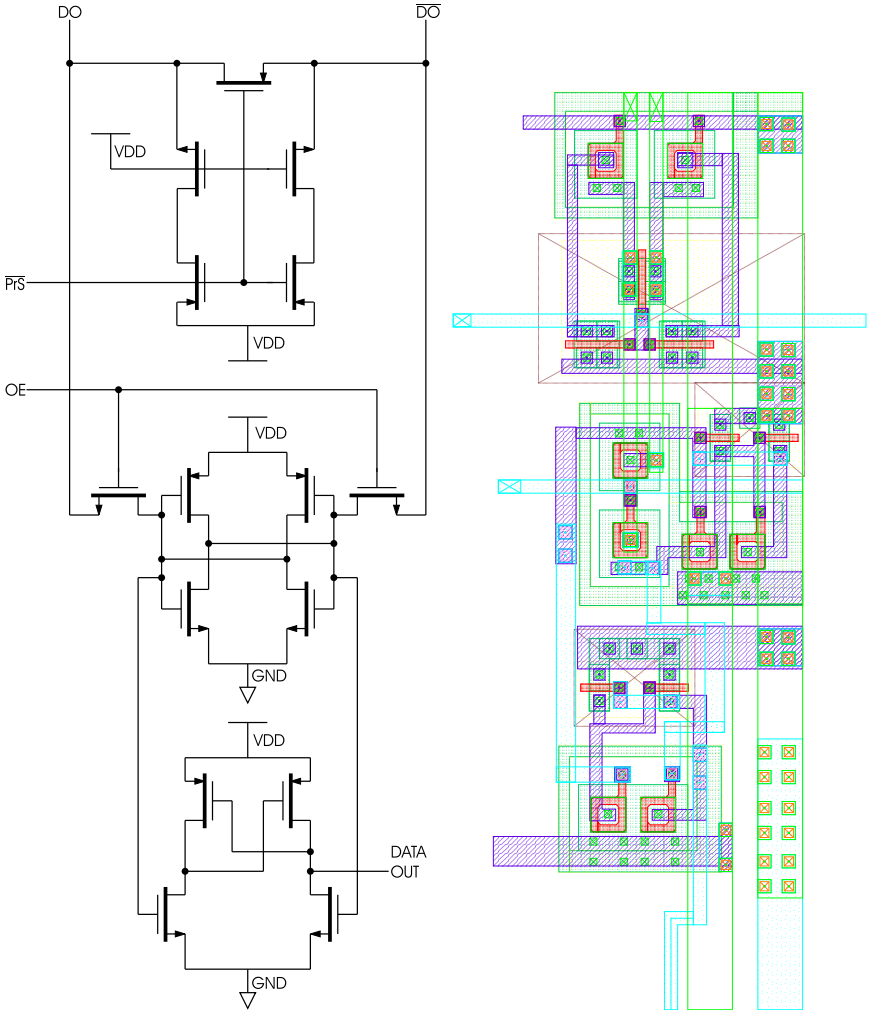

Figure 2.4: Output amplifier - schematic and layout

until the next readout occurs. This assures a digital state at the output.

Also, the output stage has to bring back the bit-lines to their initial conditions. This process is called precharging and is a known technique in memory design. If the bit-lines were kept on different potentials the next read cycle could turn out to be an unwanted write process. Therefore, the bit-lines are connected together during precharging to eliminate any differential voltage that might influence the cell's state. From this point of view, the absolute precharge level could be anything between 0 and VDD. As mentioned before, the memory cell is strongly asymmetric regarding pull-up and pull-down capability due to radiation-hard minimum size design. By choosing the precharge level to be one threshold voltage below the power supply, in this case about 1.6V, the cell's task turns out to pull-down one of the bit-lines while the other is kept on its precharge level. This enables a much faster readout than if the weaker p-channel transistors in the cell had to charge a bit-line too. Figure 2.4 shows the schematic and layout of the output amplifier.

2.2.3 Address decoder

The address circuitry has to control where data is written into the RAM and which data has to be read out. Since the OTIS pipeline is a dual port RAM, two decoders are required. An 8-bit address information is required to select one row out of 186 (or any number between 129 and 256). The decoder outputs also need sufficient driving strength since the select-lines are connected to each memory channel by two pass-transistors. This causes a high capacity, especially, because those transistors have an enclosed geometry. In order to provide fast switching while keeping current peaks low, it is of advantage to split the select-lines in the middle of the memory array and insert a buffer. This way, the overall propagation delay is

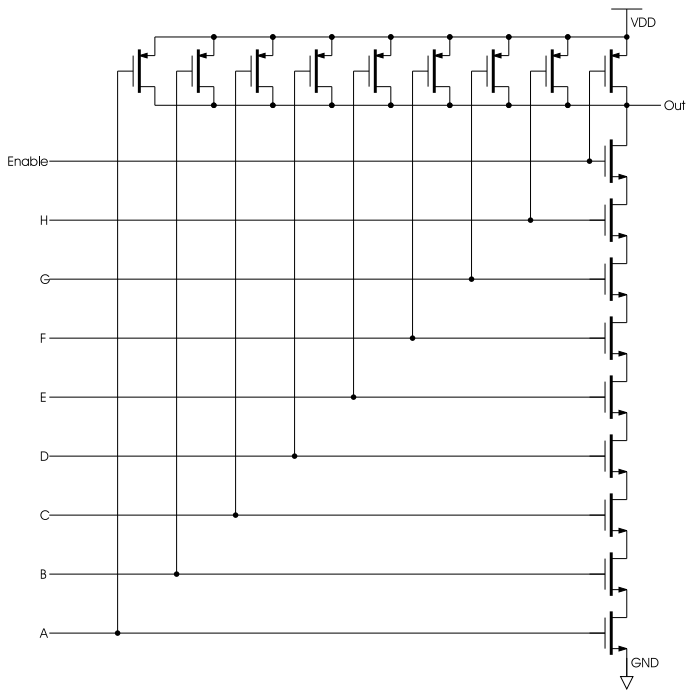

Figure 2.5: Decoder element - 9-input NAND for 8bit address plus enable signal

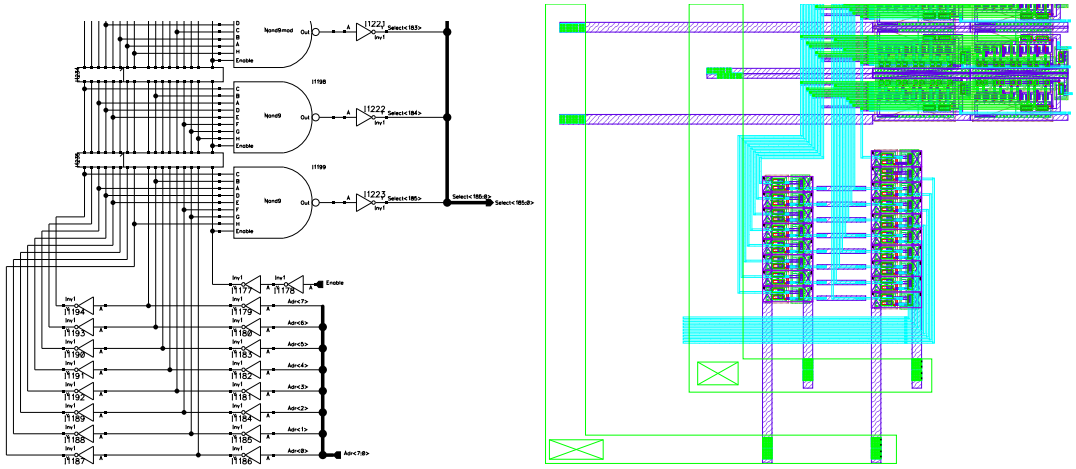

Figure 2.6: Decoder. 16 decoder bit-lines and an enable line drive 186 NAND gates, which are connected to the select-lines via inverters.

even shorter and the currents can be kept below critical values.

The key element in an address decoder is a logical NAND-gate (figure 2.5). For 8bit address information plus an enable signal a 9-input NAND is required. The enable line is needed since there are moments in a read or write when no cells are selected, for example during precharge. Also, during the address transition the decoder's enable signal has to be low, so spikes appearing during switching are not propagated to the select-lines. Therefore, the enable signal has to switch the last stage in the decoder. Since the decoders of the OTIS pipeline have only one stage (the 9-input NAND), this condition is fulfilled. Figure 2.6 shows the schematic and layout of the decoder.

2.2.4 Coordinators

Coordination of the signal-lines turns out to be the most tricky part of the memory design. Especially, at high data rates the available time during one cycle has to be scheduled carefully to achieve proper performance.

Consecutive switching actions introduce propagation delays which have to be considered. Delays have to be integrated to adjust timing and shape of signals. The simplest delay element are two standard inverters in series. Unfortunately, their propagation delay is not very large so many elements would have to be used. Nevertheless, the delay element can be slowed down and reduced in size at the same time. If the edgeless p-mos transistor is replaced by a minimum size linear one, the delay increases dramatically. This is of course due to the by a factor of 8 diminished driving power of the pull-up device.

The RAM's activity is controlled externally by the read enable R and the write enable W signal. These have to trigger the decoders, the prechargers and the I/O amplifiers. The coordinators derive those trigger signals from the read and write enable signals according to the required schedule. This is done by inverter chains acting as delays and logical gates which combine original and delayed signals in order to form new ones. Figure 2.7 shows the schematic of the coordinators.

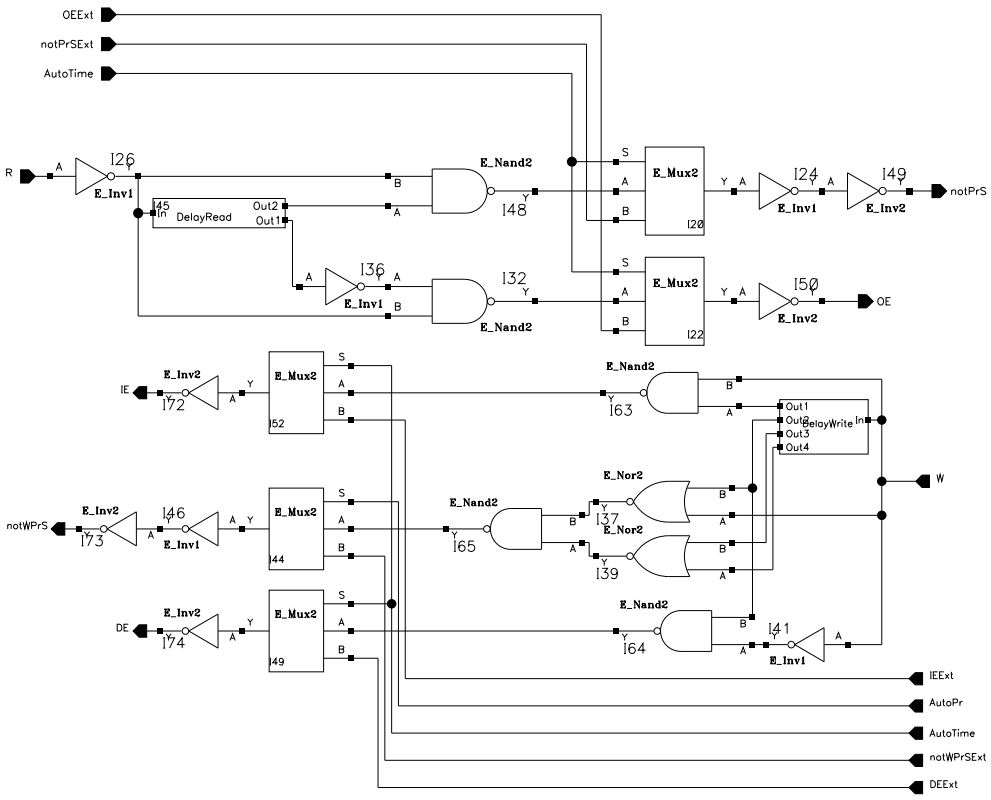

Figure 2.7: Coordinators. The multiplexers have been added to enable external control of the internal signals on the test chip.

Read cycle

The read cycle starts when the address is valid. After the address setup time read enable can be switched to high, which simultaneously turns off the prechargers and enables the decoder. The decoder has a propagation delay long enough to make sure that the prechargers are turned off when one of the select-lines connects the memory cells to the bit-lines. This is important, as otherwise prechargers and memory cells would compete in pulling the bit-lines to different levels. That would cause an increased power consumption which could be critical, concerning that 240 channels are doing so in parallel.

Once the bit-lines reached their levels, the memory cells can be disconnected from the bit-lines. Then, the data can be latched by the output amplifier. The out enable line of the output amplifier is pulsed in order to latch the bit-line's state for readout. After that, the bit-lines can be precharged again to their initial level and the cycle begins anew. Latching and precharging are triggered by the falling edge of read enable.

Write cycle

Also the write cycle requires proper coordination. After the address setup the write enable line can be switched. This must first lead to switching off the write prechargers and then to connecting the bit lines to the input amplifier. Once the bit-lines reach their levels, write

enable has to be switched off in order to pulse the decoder enable line. This leads to the selection of a select-line and writing the state of the bit-lines into the cell. The decoder has a propagation delay of about 3ns (worst case) and the precharger has to wait until write select is low again before it switches back on. Therefore, the delays of the write coordinator are reasonably longer than of the read coordinator.

2.3 Simulation and results

The behaviour of CMOS transistors can be precisely determined using standard MOS-transistor models. Nevertheless, simulation of VLSI designs requires, that propagation delays and overall timing are precisely determined. Therefore, one has to regard capacitance and resistance of all elements in the signal path. The transistor capacitances are considered in the transistor model, but the parasitics of metal connections and lines have to be extracted from the layout. Especially, when the capacitance of a long metal line has to be driven, the signal propagation is strongly dependent on the power of the driver. Some design kits offer an automated extraction of the parasitics. Unfortunately, this feature is not supported by the design kit used

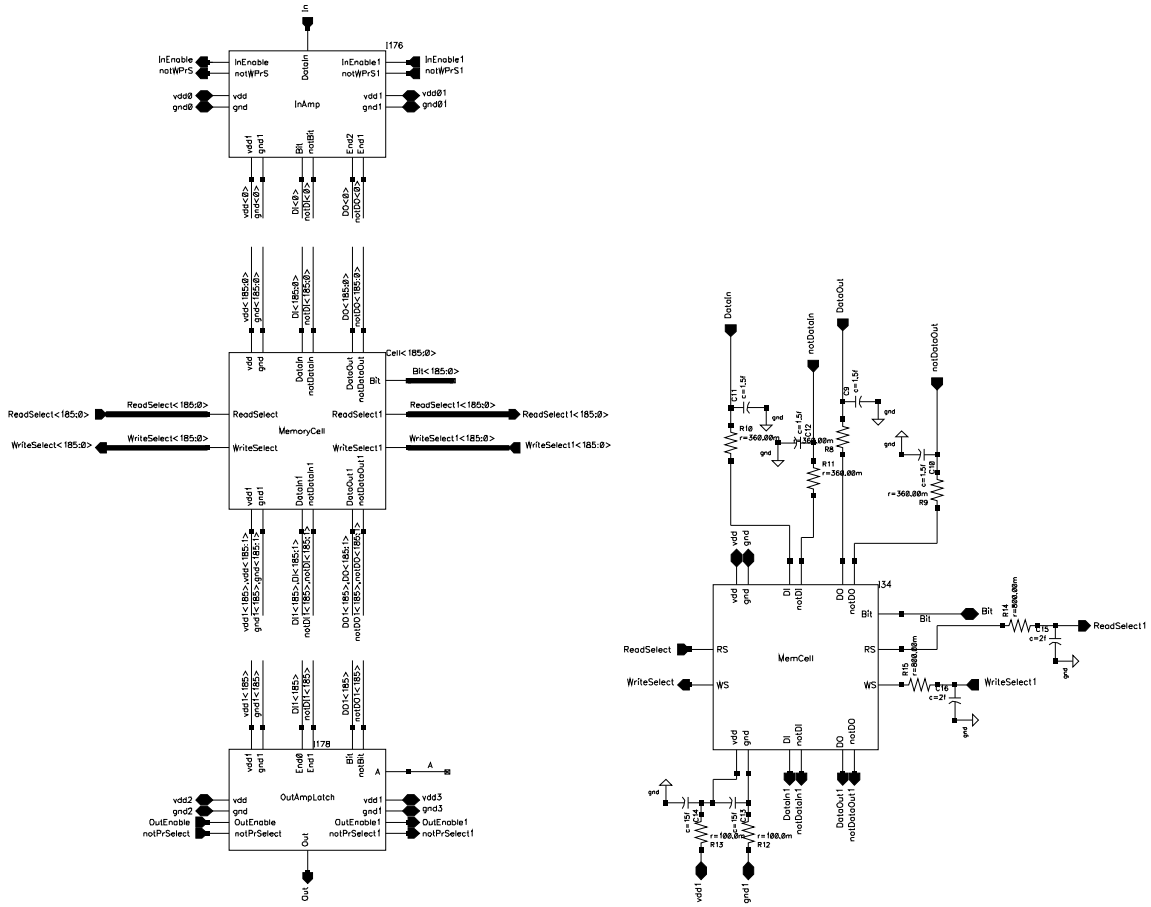

Figure 2.8: Memory channel and realistic memory cell. All nets in the memory cell are low-passes due to parasitics transistor capacities. They determine the propagation delay.

for the TDC, so it is up to the designer to include important parasitics in the simulation.

The behaviour of a RAM is majorly influenced by the capacitances of its select-lines and bit-lines. They limit the data setup and hold times and require the use of buffers in case of large memories. Figure 2.8 shows the implementation of a memory channel with the network of low-passes for a realistic simulation.

A simulation of a complete RAM would not only take a long time but is also unnecessary. The reason is that the majority of nets in a RAM is passive during a read or write process and thus doesn't have to be simulated. Further, other nets behave identical, so it is sufficient to regard only one of those nets. So the task is to predict the behavior of one memory cell in its network of select- and bit-lines. Those are only 6 nets plus the cell itself. Of course, this unit itself has to be regarded in the environment of decoders and I/O amplifiers.

2.3.1 Simplified simulation

Figure 2.9 shows the environment for a simplified simulation of a simultaneous read and write cycle. This simulation gives a pretty good insight of how the signal lines of the memory have to be controlled in order to achieve proper performance. This environment is ideal for the dimensioning of the coordinators. The simulation regards only one memory channel. Since the missing channels would influence the propagation through all horizontal lines (select-lines and amplifier control lines), capacitances have been added to those nets and matched to cause equivalent propagation delays. The decoders have been replaced by delay chains with comparable propagation delay and identical driving power. Those delay chains are connected to a specific cell in the channel. This environment enables simultaneous writing into cell #185 and reading from cell #0. The simulation results are displayed in figure 2.10. It demonstrates

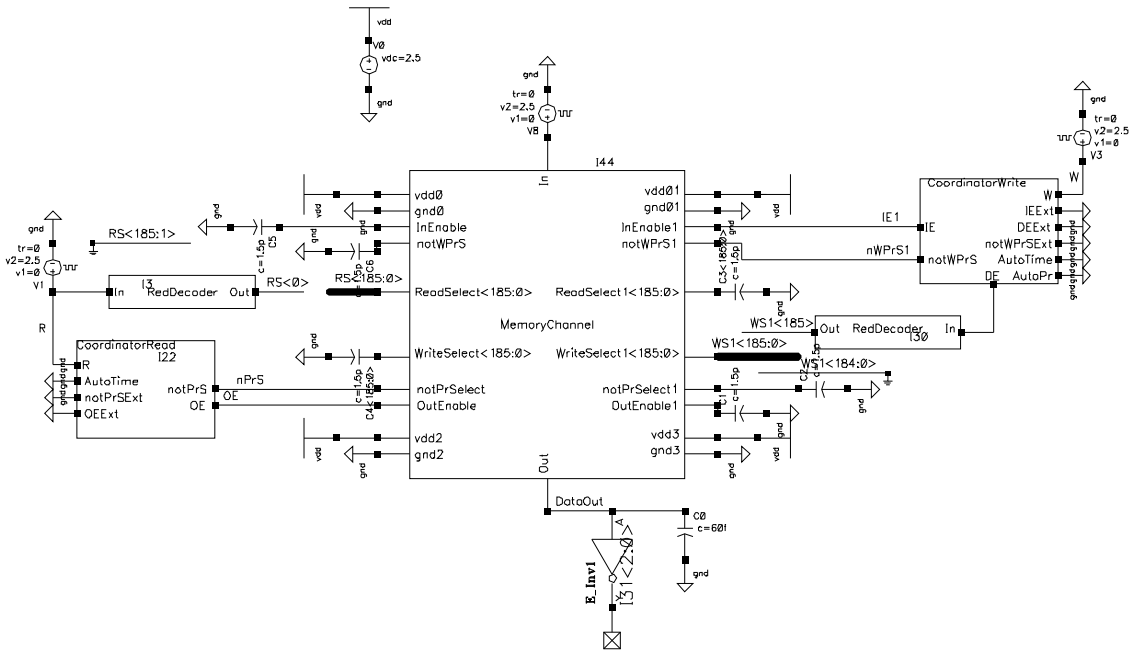

Figure 2.9: Test environment for simultaneous read and write cycle

how the signals $\overline{\text{WPrS}}$, IE, DE, $\overline{\text{PrS}}$ and OE are derived from the external signals W and R. It also gives a realistic impression of the bit-line behavior since no simplification has been applied to those. During a read or write process data is transferred through the bit-lines. In fact, the bit-line's capacitance turns out to be an intermediate storage for the data and provides the driving force for a bit-flip. This is the reason why a short memory (meaning a small number of words) is not a trivial thing. If the capacitance of the bit-lines was much smaller, this would have to be compensated by stronger amplifiers. In this specific design a big effort has been put in low power design due to the extreme length of data words. This is why the capacitance of the bit-lines have a positive effect on low power design.

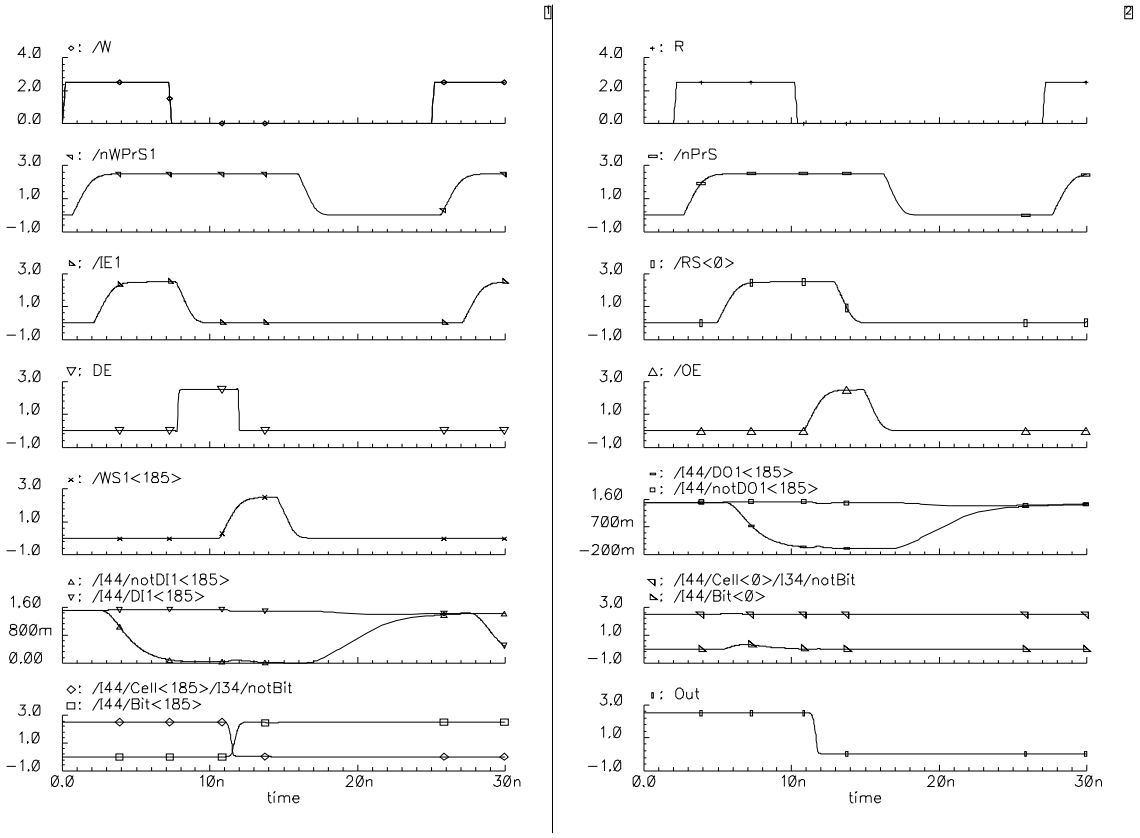

Figure 2.10: Simulation of simultaneous read and write cycle. The write enable rising edge first switches off the write precharger and then connects the input amplifier to the data-in bit-lines. This leads to pulling one of the bit-lines to ground. After that, the write enable falling edge pulses the decoder enable net, which leads to the selection of a write select line. This causes the memory cell to flip. Finally, the write precharger pulls the write bit-lines back to their initial levels.
The read enable rising edge switches off the read precharger and enables the decoder, which leads to selection of a read select line. The selected cell pulls one of the data-out bit-lines to ground. The read enable falling edge pulses the out enable net, which leads to latching the data by the output amplifier. At the end, the read precharger pulls the read bit-lines back to their initial levels.

2.3.2 Overall simulation

The best compromise between time consumption during simulation and accuracy in the results is achieved when passive nets are not implemented in the simulation environment. In this simulation, read and write processes take place for words #0 and #185. All other words are never selected so their select-lines don't have to be simulated. Further, it is sufficient to regard only channel #0 and #239, since timing constraints will be dictated by the edges of the memory array. Therefore, instead of simulating the complete array two columns and two rows of memory cells are sufficient to describe the behaviour of the RAM at its corner cells. These of course are implemented in their real environment of select- and bit-lines. High order effects like capacitive coupling to passive nets are neglected in this approach, but they are not expected to have a significant impact on the performance. The reduced array in the simulation environment completes words #0 and #185 and connects the select lines of the passive words so they are not floating. Also, the I/O amplifiers for all channels and the buffers for the signals IE, $\overline{\text{WPRS}}$, $\overline{\text{PrS}}$, OE and the select-lines of words #0 and #185 are integrated in order to simulate the correct propagation delay of those nets.

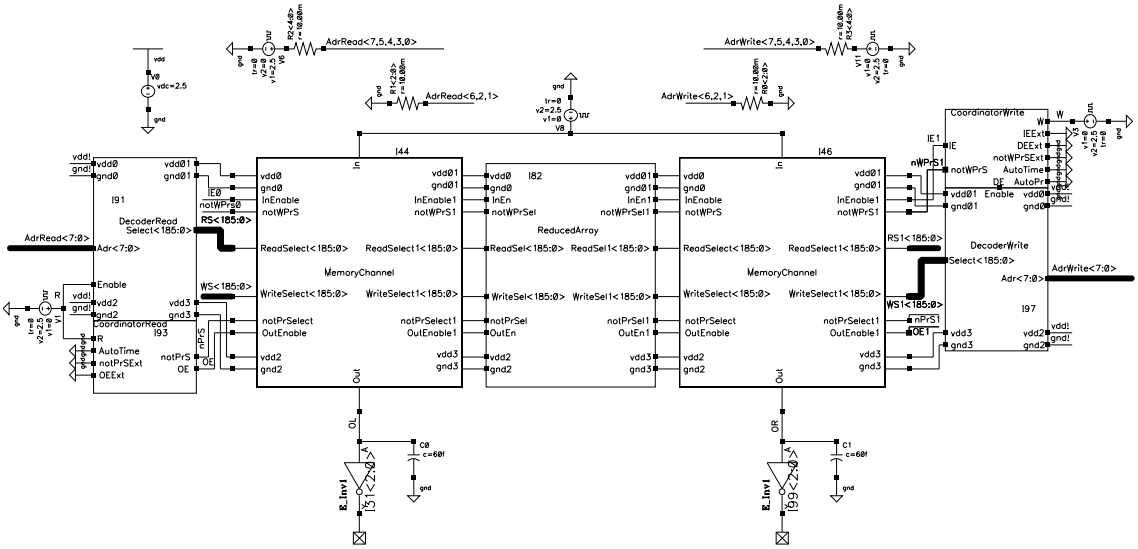

Figure 2.11: Overall simulation environment

The new insights gained from this simulation are rather small. The propagation delay introduced by the buffers is about the same for all horizontal lines and ranges from 0.5ns to 1ns depending on the corner parameters. This only has an effect on data related timing constraints, since data is propagating in vertical direction. The fact that the two memory blocks switch consecutively requires that the data input is valid about 1ns longer and causes the data out valid time to be 1ns shorter. Other than that, the results of this simulation are identical with those of the simplified simulation. Figure 2.11 shows the simulation environment. The results for the overall simulation are presented in figure 2.12. Figure 2.13 demonstrates the importance of the prechargers. If the precharge time is too short to bring back the bit-lines to their initial level, this results in an unwanted write process.

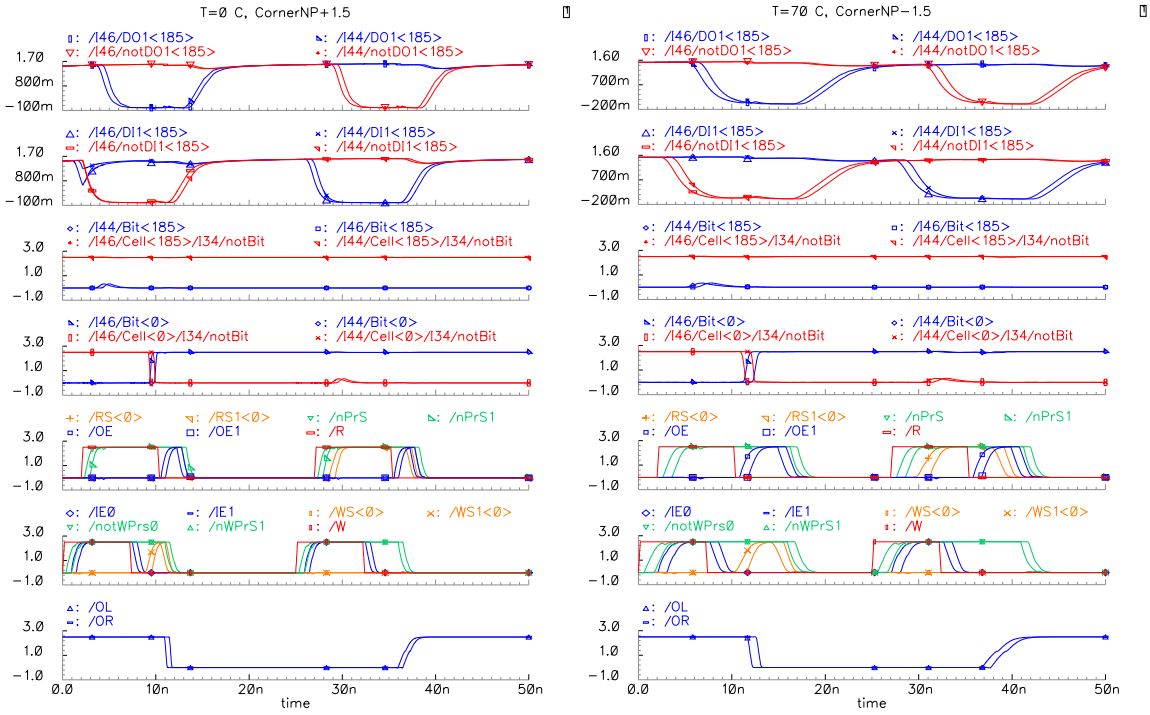

Figure 2.12: Overall simulation. This cycle is identical with the one presented in figure 2.10. Every signal appears as double line, since a propagation delay is introduced by the buffers in the memory array. Best case (left) and worst case (right) are presented. OL and OR represent outputs of the left and the right memory block.

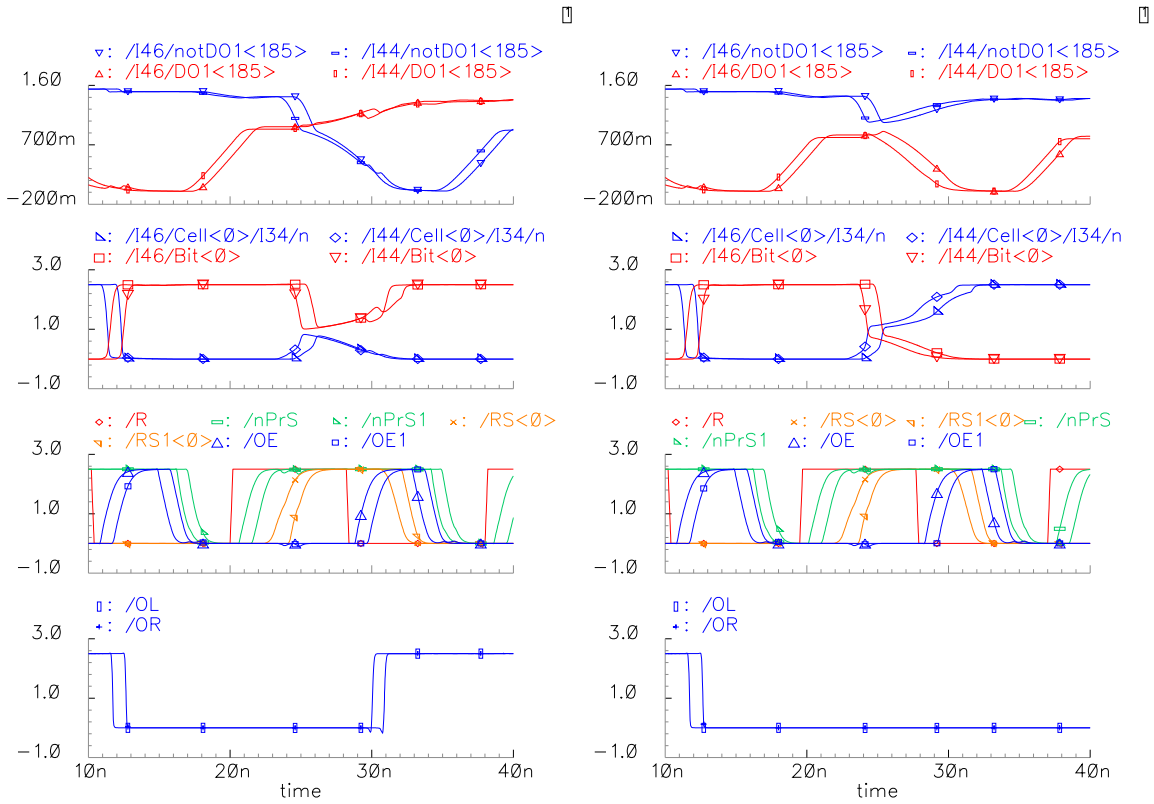

Figure 2.13: Timing limits. If the read enable low phase drops below 9ns (considering the worst case simulation), precharging is not completed. The voltage difference between the bit-lines leads to flipping the memory cell that is supposed to be read out next (right). If the precharge time is just long enough, the cell's state almost collapses (left).

2.4 Timing

The timing can be extracted from the simulation results presented in the last chapter. The simulation shows that the memory still functions to a certain extent with improper precharging. Nevertheless, the ideal timing has been derived such that level changes of the bit-lines are completed. This leads to a tight schedule within the 25ns cycle, but slight deviations from those limits won't lead to malfunction. t_{WHDV} is not an obligatory constraint, but if obeyed it reduces the power consumption. The timing diagram is presented in figure 2.14 The corresponding constraints are found in table 2.2.

Symbol	Parameter	Best	Worst	Unit
t_{AVRH}	address valid to read enable high	≥ 1.5	≥ 3	ns
t_{RLAX}	read enable low to address transition	≥ 2.5	≥ 5	ns
t_{RHRL}	read enable high to read enable low	≥ 4	≥ 8	ns
t_{RLRH}	read enable low to read enable high	≥ 8	≥ 15	ns
t_{RLDX}	read enable low to data transition	$= 1$	$= 2$	ns
t_{RLDV}	read enable low to data valid	$= 3.5$	$= 7$	ns
t_{WHDV}	write enable high to data valid	≤ 1	≤ 2	ns
t_{DVWL}	data valid to write enable low	≥ 1.5	≥ 3	ns
t_{WLDX}	write enable low to data transition	≥ 1.5	≥ 3	ns
t_{AVWL}	address valid to write enable low	≥ 1.5	≥ 3	ns
t_{WLAX}	write enable low to address transition	≥ 4.5	≥ 9	ns
t_{WHWL}	write enable high to write enable low	≥ 4	≥ 7	ns
t_{WLWH}	write enable low to write enable high	≥ 8	≥ 16	ns

Table 2.2: AC characteristics

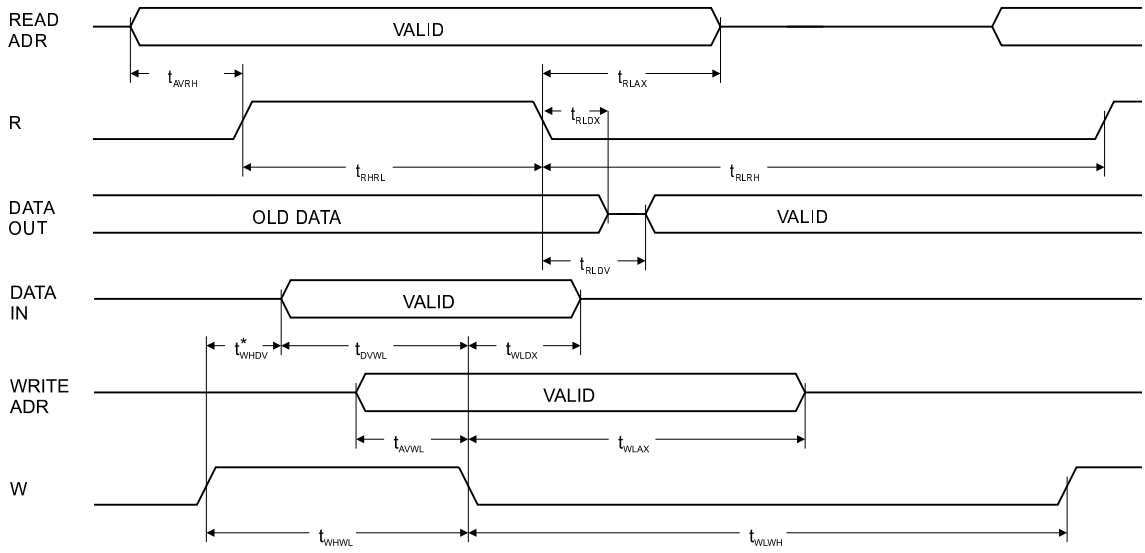

Figure 2.14: Timing diagram

Chapter 3

Design of OTISMem1.0 Test-Chip

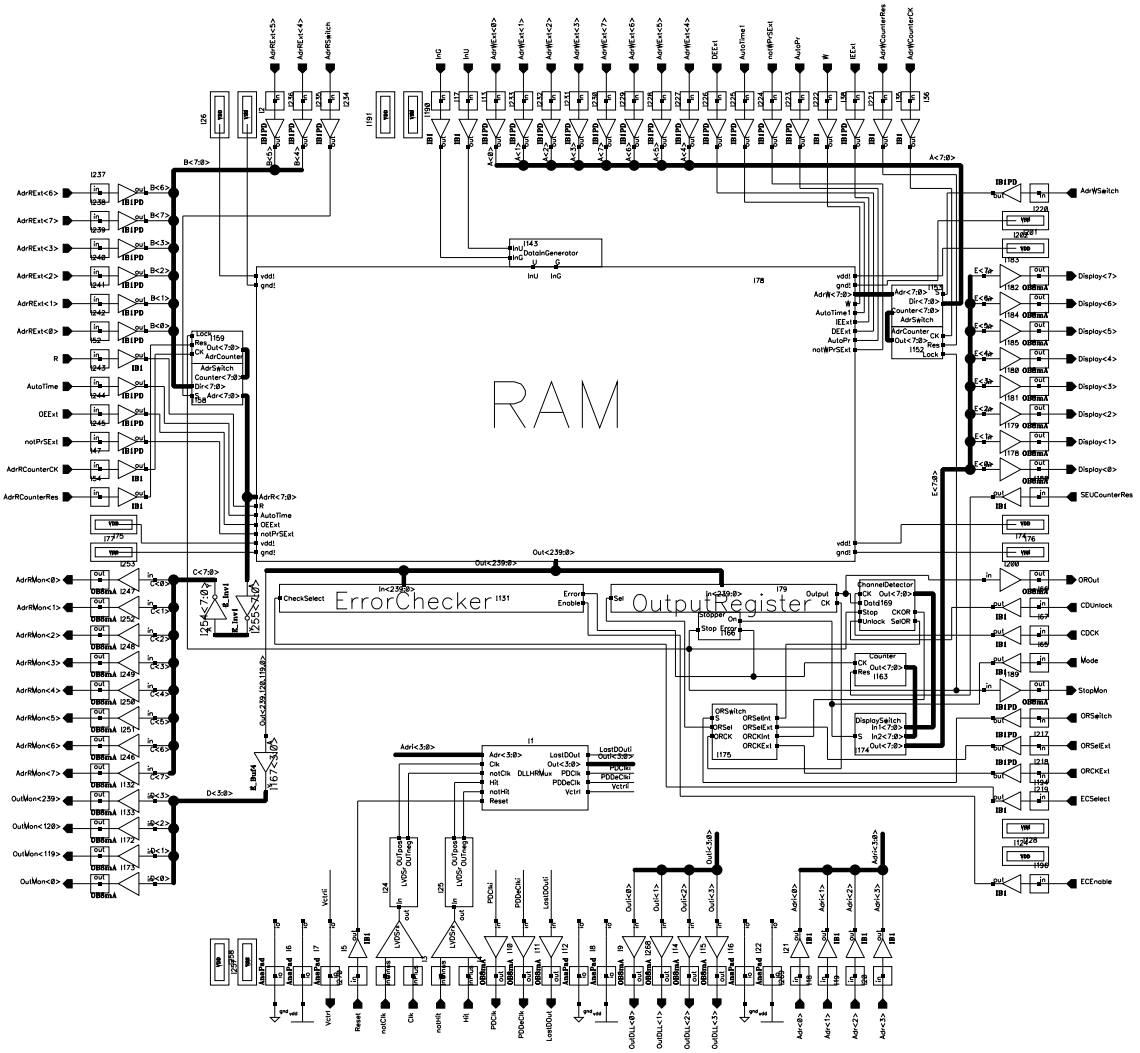

Figure 3.1: OTISMem1.0

3.1 General concept

The OTISMem1.0 is a chip designed for testing the OTIS pipeline. Therefore, a test environment is developed, which enables performance in real-time and simple access to the RAM's controls. The test structure is designed synchronous. It requires different clock signals which generate a constant bi-directional data flow. Two pointers determine the addresses for read and write independently. The test structure enables writing of four different patterns: 1010..., 0101..., 0000... and 1111..., which is achieved by two data inputs, one for all even and one for all odd channels. Direct access to four data outputs of the RAM enable visualization of the read out data word. For detailed analysis there are two modes of real-time testing: Locating bit flips (mode 1) and SEU-counting (mode 0). Both require that the RAM's output is checked for valid patterns. This is done by the error checker. If the read out pattern differs from both of the patterns 1010... and 0101... an error signal is created. In mode 0 the SEU counter counts the invalid data words and the test cycle continues. This way the performance of the RAM can be tested over a long period of time. In mode 1 the error signal stops the address counters and triggers the channel detector. Thus, the read-address monitor shows the row in which the flip occurred. The channel detector detects in which channel a bit is flipped. Therefore, once triggered by the error signal it latches the RAM's output into the output register and reads it out until there are two consecutive equal bits. The channel detector displays the channel number of the first flip it finds and waits for an unlock signal that causes the channel detector to resume and check for the next flip. This mode is suitable for identifying chips with malfunctioning SRAM cells. Once a chip is shown to work properly, it can be tested for SEU in mode 0. Figure 3.1 shows the block diagram of the OTISMem1.0.

3.2 Components

3.2.1 Data-in generator

It would be a challenging task to provide 1.1 GByte/sec of external data to feed the RAM. Anyway, it is not of major interest to be able to write an arbitrary pattern into a test-structure. It is more important to be able to provide defined patterns within a precise and variable time window in order to examine timing constraints. So the 240 channel RAM is operated as a 2 channel test-RAM with 120-fold redundancy. In other words, there are two data inputs, one for all even and one for all odd channels. Two buffers provide the power for driving a total of 240 data inputs of the RAM. That is the data-in generator.

3.2.2 Address counters

The OTIS pipeline has two address decoders requiring 16 address lines all together. Those can be accessed externally, although this would cause a serious occupancy of the available pattern generators and thus should be avoided. For simplification, the address information can be provided by two asynchronous 8bit-counters on chip. Those need only a clock and a reset signal. A read and a write pointer with different offset can so be generated by two clocks. The offset is needed, since valid data has to be written into the RAM before it can be read out at the beginning of a test run.

The address pointers are supposed to run cyclically, since the memory is planned to be used as a ring buffer. This requires an automatic reset at 186 (10111010). This is achieved

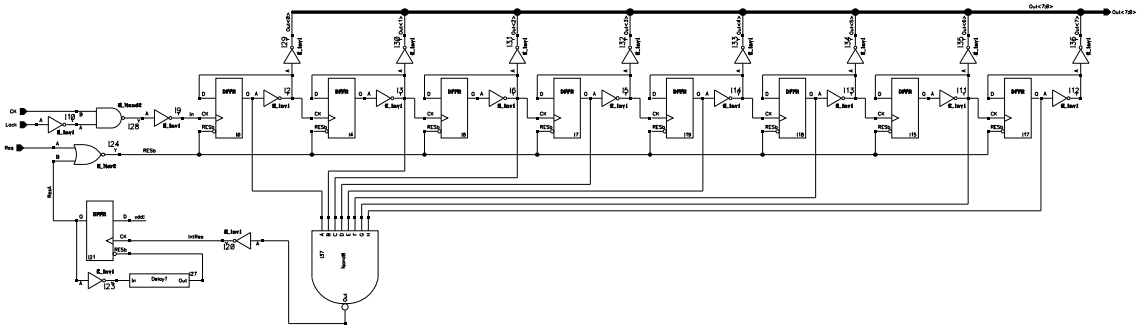

Figure 3.2: Address counter

by an AND gate, which detects the digital pattern for line 185 and then pulls the reset line of the counter flip-flops. Unfortunately, a design error has occurred in the reset circuit, namely that the reset happens one count too early. Therefore, the address counter will not consider the last line of the memory. This is not a problem for the real time test modes. Anyway, the last line could be addressed via the external address port. Figure 3.2 shows the schematic of the address counter.

3.2.3 Error checker

The error checker is hardwired with the RAM's data output. Its task is to detect deviations from the valid patterns 1010... and 0101... Also, it has to signalize an error within the same cycle it has occurred. This is required for mode 1, since the read address counter is supposed to point to the row where the error appeared. This is not a problem, if it is implemented as a parallel structure. 120 XNORs are required to check the data output of the RAM for the valid patterns (1010... and 0101..). Therefore, an even and an odd numbered channel have to be connected with one XNOR. In case of a valid pattern the XNORs would see two opposite input signals and put out a 0. If all XNORS show a 0 then the pattern is considered valid by the error checker. This structure would not realize if two bits, which are compared by the same XNOR gate have flipped. For non-correlated flips the probability for such an event is $p^2/239$ where p is the probability for a single bit flip. Obviously, this can be neglected, since p is expected to be extremely small. The only thing to take care of is that there is no correlation between the data lines compared by one XNOR, when testing radiation hardness. The horizontal distance of two memory cells is only about 5μm. The probability that one ionizing particle causes two neighboring cells two flip simultaneously is of course bigger than if the cells had a larger separation. For this reason, the data output of the RAM is logically grouped into octets of consecutive channels. The error checker then compares channel 1 with channel 8, 2 with 5, 3 with 6 and 4 with 7 of each octet in order to physically separate channels that are compared by an XNOR.

The following stage in the error checker is an OR gate which connects all XNOR outputs. In case of an error the output of the OR will go high. The last stage contains an enable signal, which is required for filtering the glitches that might appear during the switching of the error checker. Those glitches could trigger a stop although no error has been detected. Therefore, the enable signal has to be send after the checkers state becomes static.

One task of the OTISMem1.0 is to check the RAM's influence on the OTIS DLL. Since

the error checker is located in between the RAM and the DLL and its current peaks are comparable with the RAM's, rather the error checkers influence on the DLL would be measured, if it couldn't be switched off. Therefore, there is a transmission gate at each input of the error checker and a pull-down transistor for a defined state at the input in case the gate is closed. The power consumption of the error checker is reduced by a factor of about 10 when check select is low.

3.2.4 Output register

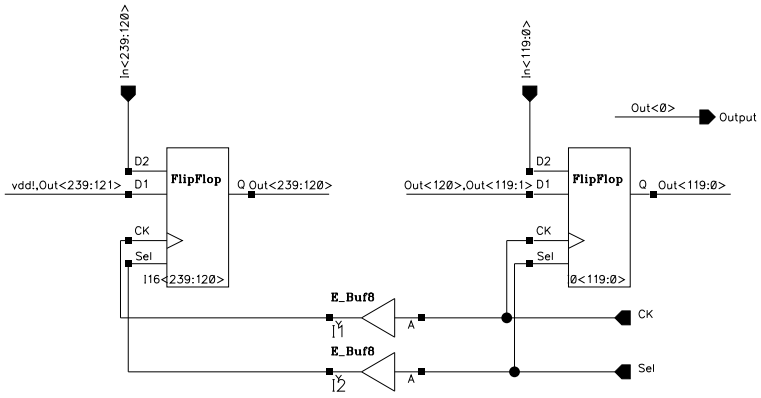

Figure 3.3: Output register

Besides the error checker the output register reads the complete data output of the RAM. It is used to serially read out a pattern from the RAM. Its output is monitored for external access and its control can be switched between internal and external. External control enables serial readout of the RAM off chip and has also been integrated in case the internal testing unit doesn't work properly. (If one could be sure everything is working, there would be no need for a test chip.) In the expected case the output register will be controlled internally by the channel detector and its only use is to determine the horizontal location of a bit flip.

The design of the Output-Register is straight forward and is known from CCD-readout structures. One element of the register is assembled by a multiplexer with two inputs and a D-flip-flop, which latches the multiplexer's output. One of the multiplexer's inputs is connected to a memory channel, the other to the output of the previous flip-flop. The multiplexer switches between latch and queue mode. The first is used to copy the RAM's output into the register, the second to read it out.

In order to avoid racing conditions, the register has to be clocked from the end where it is read out. This makes sure that an entry is copied before it is overwritten. If the clock would propagate in the direction of data flow and its propagation delay was longer than the flip-flop's clock-to-Q delay, data would be overwritten before copied and thus be lost. This can happen easily at clock buffers, since those introduce reasonable propagation delays.

A look at the currents in the clock and select lines justifies the need for a buffer for the same reason as in the RAM. Figure 3.3 shows the schematic of the output register.

3.2.5 Channel detector

The channel detector is probably the most complicated instance on the OtisMem1.0 although it is only good for one task: determining the horizontal location of a flipped bit. Obviously, this could be done externally by looking at the output registers output. Nevertheless, testing becomes much more convenient if any calculation and detection is done on chip. This way, all one has to do is to drive the test environment with an input pattern and look at its outputs for the result.

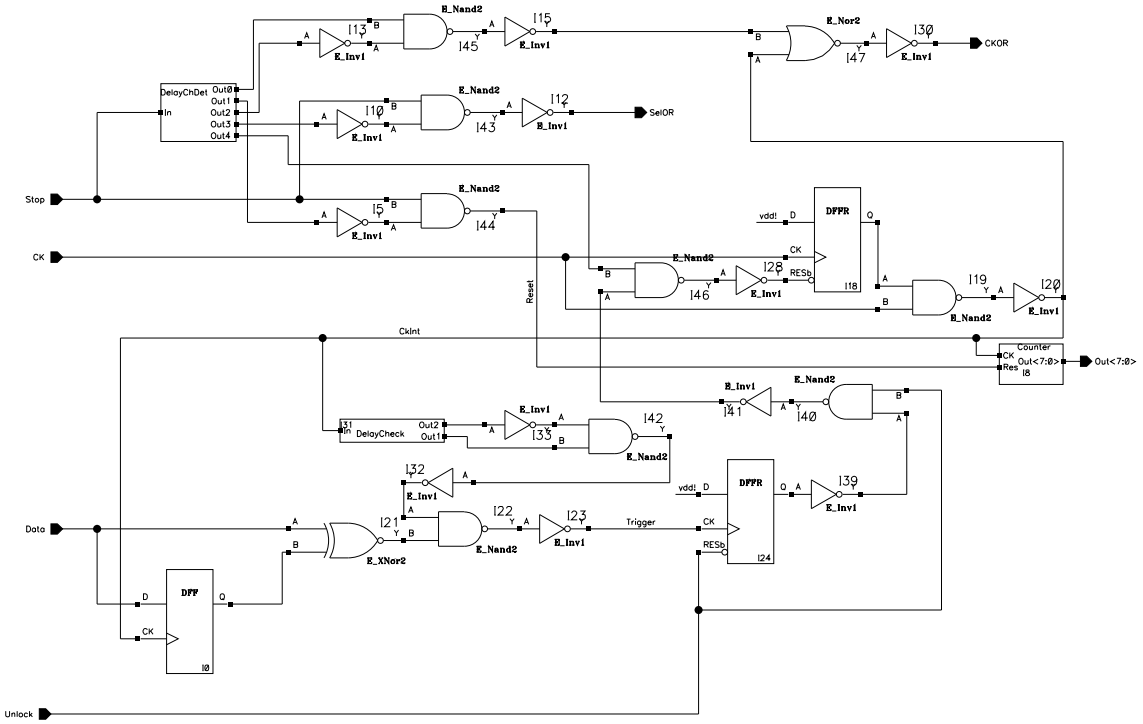

Figure 3.4: Channel detector

The channel detector reads the output of the output register. Therefore, it has to control the output register's clock and its select line, which switches the input source. Those signals have to be coordinated within the given timing constraints. Once the RAM is copied into the output register, one bit after the other is latched in the channel detector and compared with its following. An internal clock provides the control of the register's clock and the internal latch. It also drives a counter, which displays the number of the channel of the checked bit. In case both bits match, the internal clock is stopped immediately. The counter is monitored via the display switch and shows the horizontal position of the flip. The channel detector can be resumed by the unlock signal and it will look for the next match of consecutive bits. A single bit flip should cause the channel detector to stop twice, since it causes two deviations from a valid pattern in a row. The only exception is if the first bit (channel #0) is flipped. Then the internal clock would stop only once and display 1, which means that bit #0 is flipped. Whenever the counter stops twice in a row, the first number is the location of the flipped bit counting from 0. Figure 3.4 shows the schematic of the channel detector.

After a detection is completed the process has to be reset by switching the mode. Also,

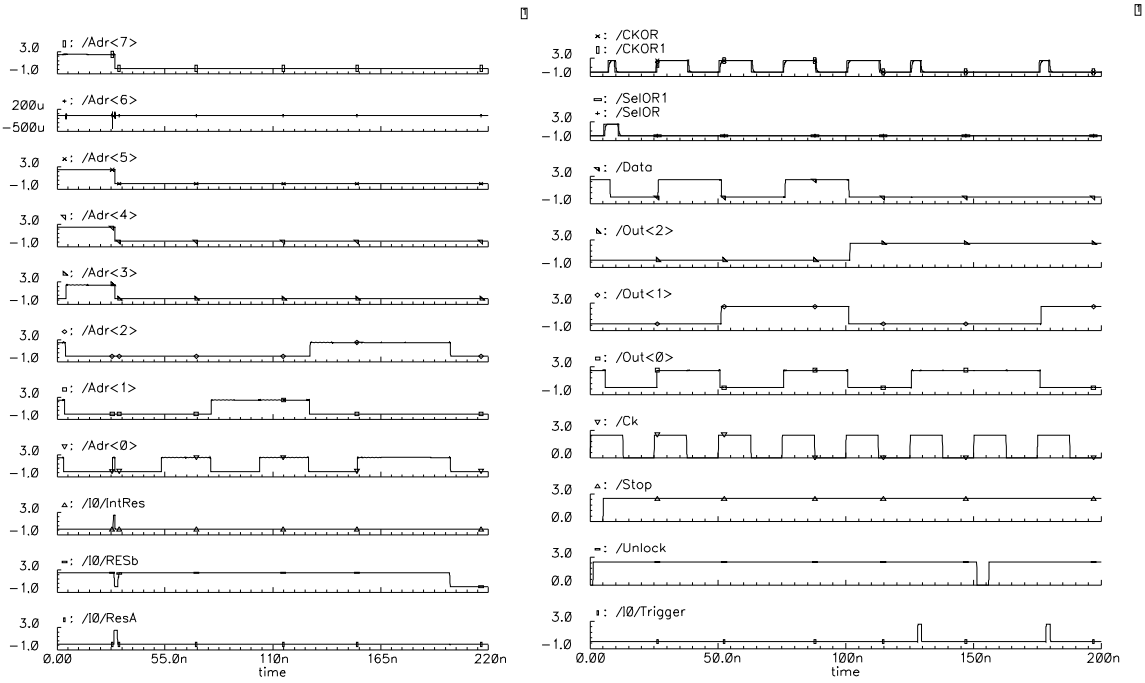

Figure 3.5: Simulation results for adress counter (left) and channel detector (right). The adress counter performs an automatic reset at position 185 (10111001). The channel detector reads out the output register. It detects a flipped bit in the 5th channel and pauses its internal clock. The channel number can be monitored via the display switch

an unlock signal has to be given in order to resume the channel detector. Figure 3.5 shows the simulation results for the address counter and the channel detector.

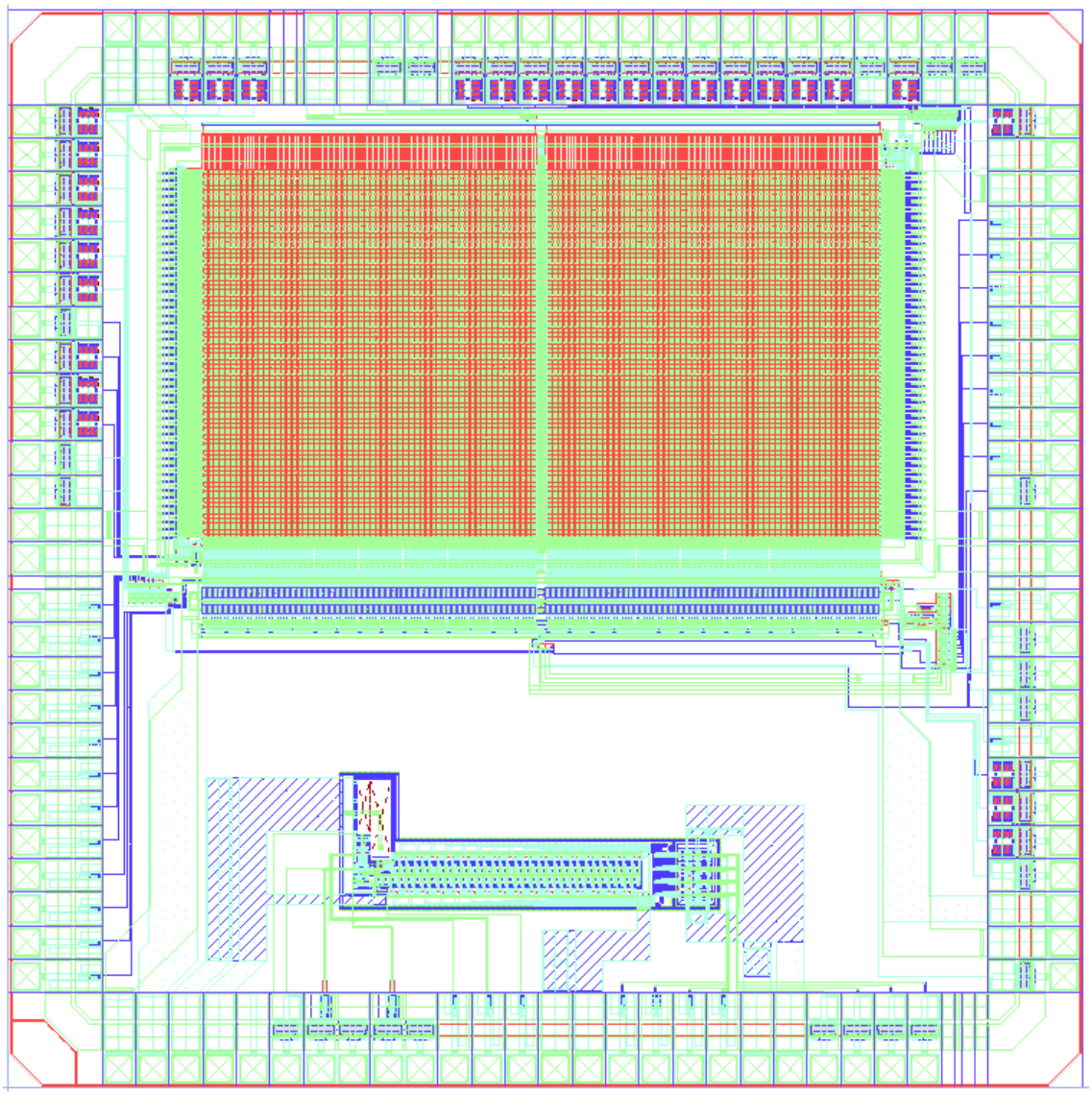

Figure 3.6: Layout of OTISMem1.0. The large block in the upper half is the OTIS pipeline prototype. The OTIS DLL (bottom) is included for studies of cross-talk.

Chapter 4

Mesurements of OTISMem1.0

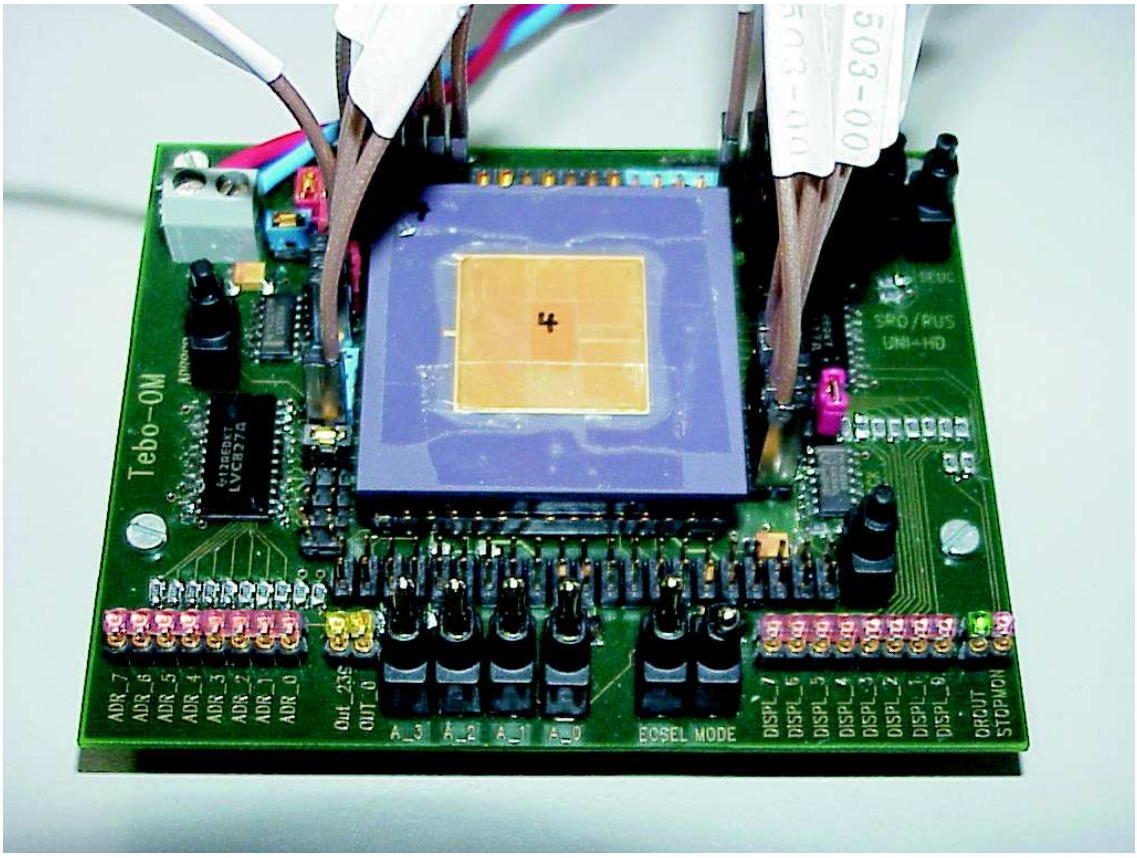

Figure 4.1: Test board for OtisMem1.0

4.1 Test environment

The test structures of the OTISMem1.0 are designed to simplify functional testing and measuring of the exact timing constraints. A special test-board (figure 4.1) has been developed

that provides the OTISMem1.0 with the correct input patterns and displays its outputs. A pattern generator (Tektronix DG2020) is used to create the required clock patterns for the test environment and the control signals for the RAM. Since pulse widths of this pattern generator can only be adjusted in minimum steps of 5ns, logic AND gates on the board generate pulses with adjustable rising and falling edge. This is necessary for precise timing control.

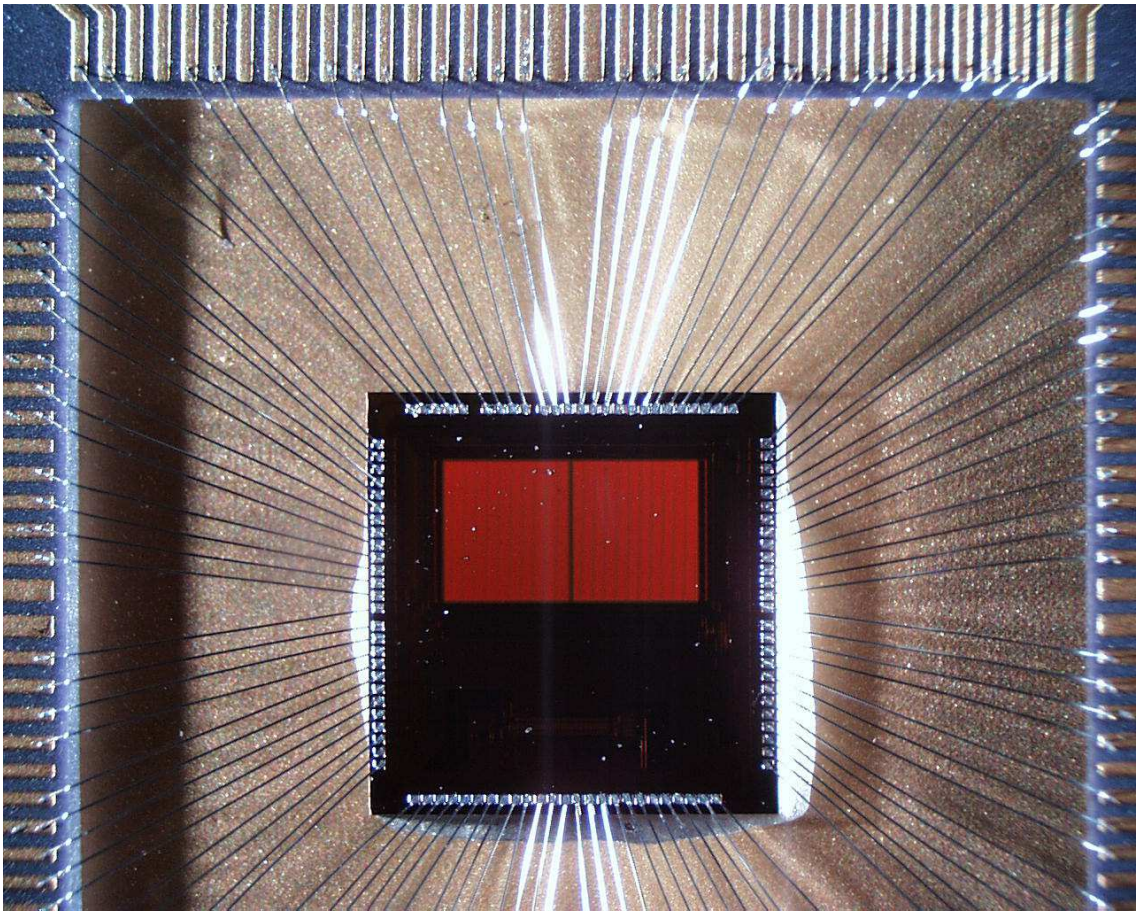

Figure 4.2: OTISMem1.0 bonded to PGA-144 package. The memory array appears bright orange, because the bit-lines on the top metal layer act as diffraction grating.

4.1.1 Input signal processing

The required pattern for driving the memory with its ideal timing can be derived regarding propagation delays introduced by the AND gates on the board and by the test structure on the chip. Figure 4.3 shows the generation of the write enable signal W using two delayable outputs W1 and W2 of the pattern generator. The AND gates introduce a delay of 1.7ns which have to be considered for timing adjustments.

Figure 4.4 shows the relation between the memory pattern and the input pattern. The corresponding timing constraints for the nominal timing at 40MHz are presented in table 4.1.

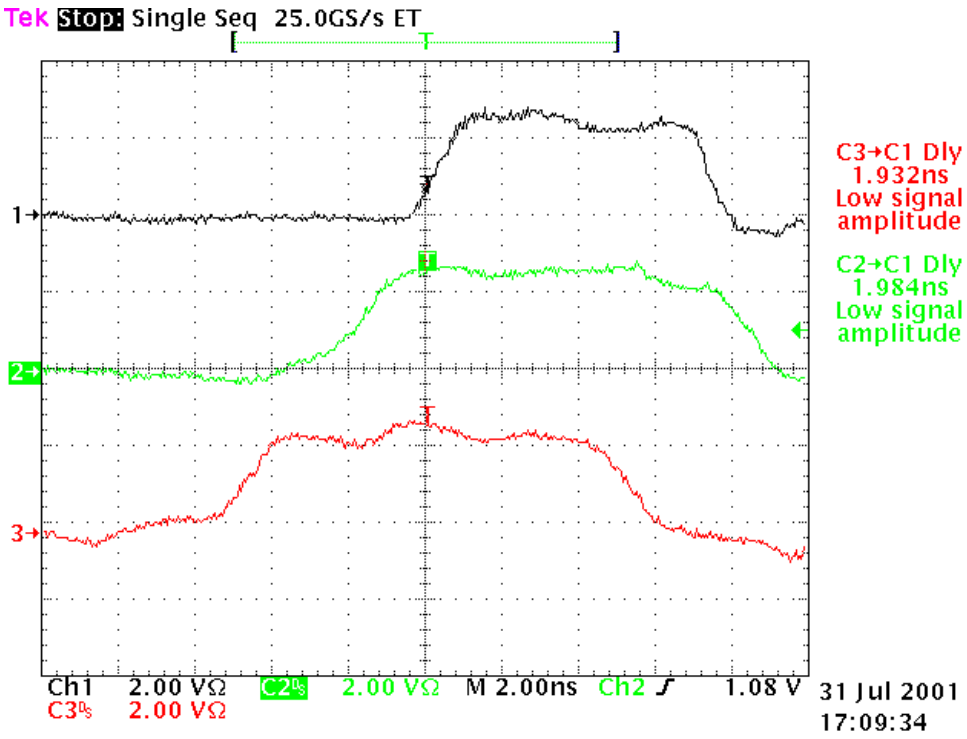

Figure 4.3: Write enable signal (1) generated by two signals W1 (3) and W2 (2) and an AND gate on board. The AND gate introduces a propagation delay of 1.7ns. This measurement actually shows a delay of 1.9ns, but 0.2ns are introduced by the probe.

Symbol	Parameter	Value	Unit
t_1	write enable falling edge delay	0	ns
t_2	write enable rising edge delay	3	ns
t_3	read enable falling edge delay	3	ns
t_4	read enable rising edge delay	5	ns
t_5	InU valid delay	2	ns
t_6	InU transition delay	4	ns
t_7	InG valid delay	2	ns
t_8	InG transition delay	4	ns
t_{WH}	write enable high	4.7	ns
t_{WL}	write enable low	11.7	ns
t_{RH}	read enable high	6.7	ns
t_{RL}	read enable low	14.7	ns
t_{DV}	data valid	6.7	ns
t_{DX}	data transition	13.7	ns

Table 4.1: Nominal timing for OTISMem1.0 at 40MHz

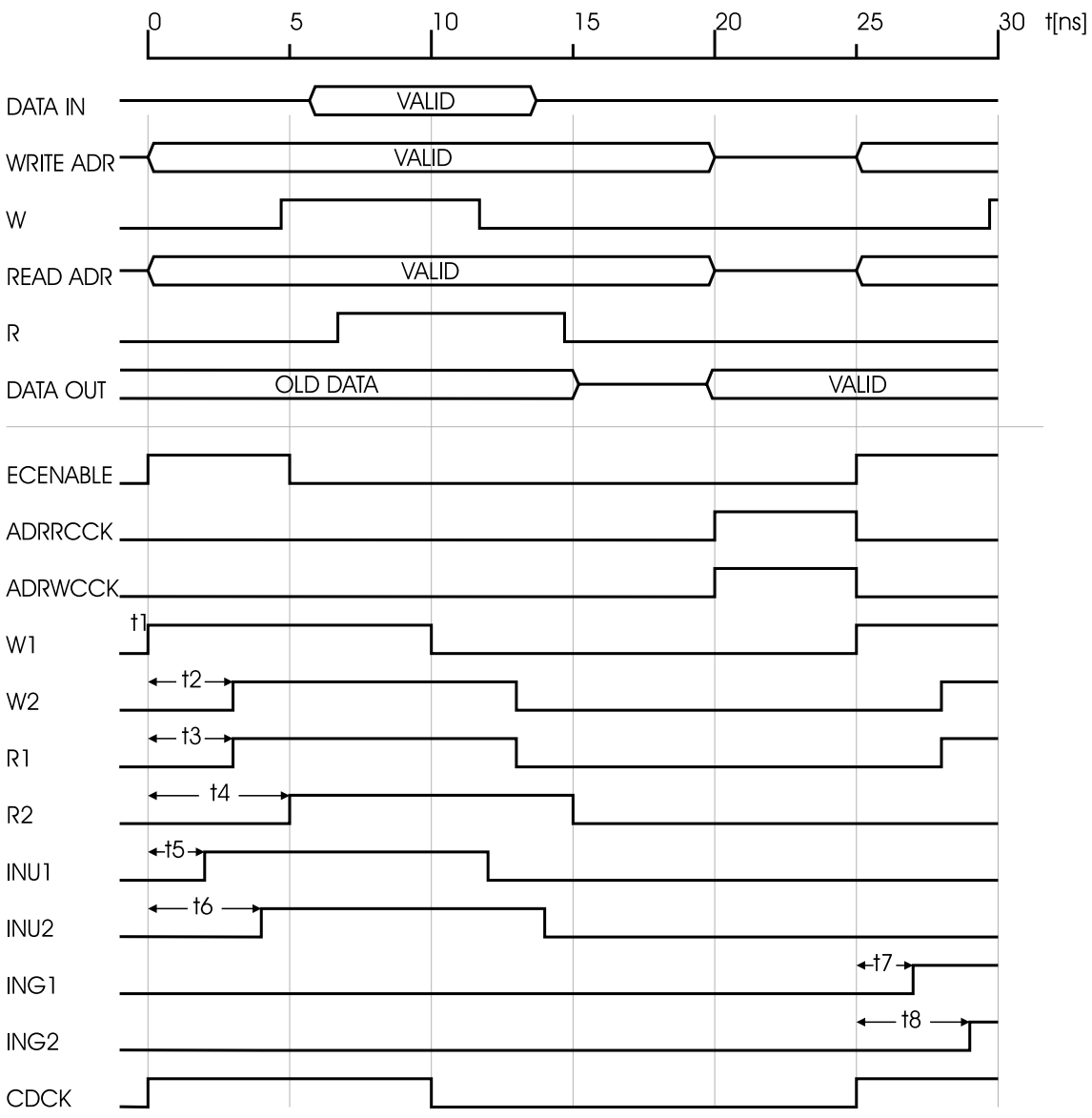

Figure 4.4: Pattern for ideal timing at 40MHz. t1 through t8 are adjustable delays of the pattern generator.

4.1.2 Output display

The read address is displayed as binary 8bit code. Also, two outputs of the RAM, namely Out(239) and Out(0) are monitored which enable the determination of the data word at the given read address. A second 8bit monitor displays the state of the memory test environment on chip. In mode 0 the SEU counter is displayed. In case of a functioning chip and adequate timing this display should stay off as long no error occurs. In mode 1 the channel detector is displayed. The 8bit number gives the horizontal location of a detected bit flip. With the CDUnlock button multiple bit-flips within one data word can be determined. The STOPMON indicates if the memory cycle has been stopped after an error was detected. The OROUT LED shows the output of the output register. If the channel detector displays a flip the polarity of the flipped bit can be read from this LED. The monitors of the test board are shown in figure 4.5.

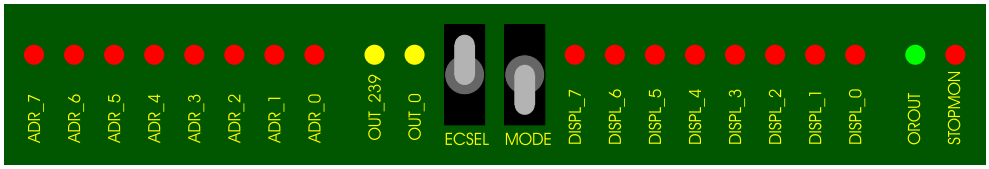

Figure 4.5: Display of the test board

4.1.3 Test modes

In order to run mode 0 reset signals have to be sent to the address counters and to the SEU counter. These can be performed manually by pressing the corresponding reset buttons on board. After that, at least one data word has to be written and the write pointer has to be forwarded before the first read cycle can be performed. An arbitrary offset between read and write pointer can so be achieved. Both counters can now be clocked with the cycle frequency and data can be written and read out simultaneously.

If the memory is operated correctly the SEU counter will stay at 0. The functionality of the error checker can be verified by changing the delay of an input signal, e.g. the data input, so much that timing constraints are no longer obeyed. This will lead to apparently turning all 8 LEDs of the display on. Thus, the exact timing limits can be measured by watching the SEU counter and varying the delays which determine the input pattern. A resolution of 100ps can be achieved this way.

Mode 1 can be performed with the same input pattern as mode 0. Before the pattern starts the CDUnlock button has to be pressed in order to activate the channel detector. Since the mode signal is also the reset for the stopper it is necessary to switch the mode before the start of every test run. In this mode malfunctioning memory cells can be located. Also, the influence of the buffer in the memory array at timing limits can be examined. For example, timing limits could only be observed for one block of the memory.

4.2 Memory testing

4.2.1 Functional test

Eight chips have been packaged for testing so far. Chips #1 and #5 don't show any sign of life at all. The displays of the board turn on when putting the finger on the package what indicates that the outputs of the chips are floating. Measurements of the resistance between different power pads show that the metal power bars on the chip are not connected to the pads. It is believed that those chips came from the edge of a waver were a mask problem has occured during processing. Most likely the metal 2 to metal 3 vias are not existent. The other six chips behave more or less identical. When driven with the pattern derived in figure 4.4 the displays show the expected behavior. After power up in mode 0 the read address counter and the SEU counter are in an arbitrary state. Both can be reset and then display 0. When the pattern is started all LEDs of the read address display turn on. This indicates that the read pointer is running cyclically through the memory. The SEU counter stays at 0 which means that no errors are detected. Obviously, it has to be proven next that the error checker is working at all. By changing the delay of one of the data input patterns so much, that the generated data in pulse doesn't obey the timing rules any more, invalid data words are written into the RAM and the SEU counter should register an error every cycle. Indeed, this effect is observed with a data input pulse width of less than 1.6ns. When readjusting the timing, the counter stops at its present state and then can be reset again during the test run.

The next step is to check the performance of mode 1. After the pattern is started an error can be induced by changing the timing as mentioned above. Once the timing limits are exceeded, the stop monitor switches on and the address pointers automatically stop. The read address display now shows the address of the word read out last. The second display shows the horizontal location of the first two equal bits serially read out. By toggling to the next equal bits in a row it turns out that the channel detector always stops at least at two consecutive columns which was expected, since one flipped bit causes three equal bits in a row.

4.2.2 Timing measurement

The timing applied to the memory so far is ideal according to its simulated behavior. Now the timing limits of the memory have to be examined and compared with the expected ones. The error checker is of great help for this job and can be used as memory self-test unit together with the SEU counter. By changing the timing of the delayable input patterns and considering all propagation delays on chip and on board one can successively determine the absolute maximum ratings of the timing constraints. Table 4.1 presents the nominal values for the delays t1 through t8. The pulse width of all delayable signals is 10ns. The resulting timing constraints are also shown. After the timing for OTISMem1.0 is measured, corrections have to be applied considering the propagation delays on chip, in order to find the timing of the memory itself.

t_{WHWL} and t_{RHRL}

The minimum widths of read and write enable can easily be determined by increasing t_{WH} and t_{RH} until the error checker indicates false timing. It is important to assure that no other timing limit is exceeded than the one measured when changing the timing of an event.

Symbol	Chip 2	Chip 3	Chip 4	Chip 6	Chip 7	Chip 8	Unit
t_{WH}	8.7	8.6	8.5	8.9	8.5	8.6	ns
t_{WL}	11.7						ns
t_{RH}	12.8	12.7	12.6	13.1	12.6	12.7	ns
t_{RL}	14.7						ns
t_{WHWL}	3.0	3.1	3.2	2.8	3.2	3.1	ns
t_{RHRL}	1.9	2.0	2.1	1.6	2.1	2.0	ns

Table 4.2: Measurements of t_{WHWL} and t_{RHRL}

t_{DVWL} and t_{WLDX}

These times are related to the write enable low transition which is kept constant for this measurement.

Symbol	Chip 2	Chip 3	Chip 4	Chip 6	Chip 7	Chip 8	Unit
t_{DV}	10.8	10.8	10.7	10.8	10.7	10.7	ns
t_{WL}	11.7						ns
t_{DX}	12.1	12.2	12.2	12.1	12.2	12.2	ns
t_{DVWL}	0.9	0.9	1.0	0.9	1.0	1.0	ns
t_{WLDX}	0.4	0.5	0.5	0.4	0.5	0.5	ns

Table 4.3: Measurements of t_{DVWL} and t_{WLDX}

t_{WLWH} and t_{RLRH}

For the measurement of the minimum read and write enable low phases the patterns have to be altered. The minimum width for a low phase of a logic AND is determined by the low phases of its inputs. These can be set to a minimum of 5ns with the DG2020. Therefore, the pulse widths of W1, W2 ,R1, R2 have to be set to 20ns. The memory cycle was still working properly for t_{WLWH}=5ns. The limit might be quite shorter, but it could not be determined with the available means. Anyway, it is not neccessary to set this time to even smaller values.

Symbol	Chip 2	Chip 3	Chip 4	Chip 6	Chip 7	Chip 8	Unit
t_{WL}	9.7						ns
t_{WH}	14.7						ns
t_{RL}	16.2						ns
t_{RH}	22.5	22.6	22.7	22.1	22.9	22.7	ns
t_{WLWH}	5.0						ns
t_{RLRH}	6.3	6.4	6.5	5.9	6.7	6.5	ns

Table 4.4: Measurements of t_{WLWH} and t_{RLRH}

t_{AVWL}, t_{WLAX}, t_{AVRH} and t_{RLAX}

For the measurement of address related times it is recommendable to supply a direct address rather than using the asynchronous address counter. The actual timing of the memory can be better controlled that way. Further, it is neccessary to adjust the timing of the address. Therefore, two of the delayable outputs of the DG2020 are used to switch the AdrREext(0) and the AdrWExt(0), while the other address lines are kept on 0. This switches the read and write pointers between word #0 and #1.

Symbol	Chip 2	Chip 3	Chip 4	Chip 6	Chip 7	Chip 8	Unit
t_{AV}	13.1	13.2	13.2	13.0	13.1	13.1	ns
t_{WL}	11.7						ns
t_{AX}	14.5	14.6	14.7	14.4	14.6	14.6	ns
t_{AV}	9.0	9.0	9.0	9.0	9.0	9.0	ns
t_{RH}	8.7						ns
t_{RL}	11.7						ns
t_{AX}	11.3	11.3	11.3	11.4	11.2	11.2	ns
t_{AVWL}	-1.4	-1.5	-1.5	-1.3	-1.4	-1.4	ns
t_{WLAX}	2.8	2.9	3.0	2.7	2.9	2.9	ns
t_{AVRH}	-0.3	-0.3	-0.3	-0.3	-0.3	-0.3	ns
t_{RLAX}	-0.4	-0.4	-0.4	-0.3	-0.6	-0.5	ns

Table 4.5: Measurements of t_{AVWL}, t_{WLAX}, t_{AVRH} and t_{RLAX}

t_{RLDX} and t_{RLDV}

The data out transition is triggered by the read enable falling edge. To determine the timing for this event it is suitable to monitor the direct data outputs on an oscilloscope. The two times are expected to differ a little bit, since the output drivers of the memory are asymmetric with respect to pull-up and pull-down speed. This means that t_{RLDX} is determined by the faster data transition 1-0 and t_{RLDV} by the slower transition 1-0. Also, the buffer between the two memory arrays causes a further gap between data out transition and valid time. The out enable signal is propagating from left to right (channel 239 to 0). Thus, the fastest transitions are 1-0 transitions in the left block (channel 239..120) and the slowest 0-1 transitions in the right block (channel 119..0). Figure 4.6 shows the data output transitions of channel 119 and 120 and the read enable signal.

Symbol	Chip 2	Chip 3	Chip 4	Chip 6	Chip 7	Chip 8	Unit
t_{RLDX}	1.5	1.5	1.5	1.3	1.6	1.5	ns
t_{RLDV}	4.7	4.9	5.1	4.4	5.1	4.9	ns

Table 4.6: Measurements of t_{RLDX} and t_{RLDV}

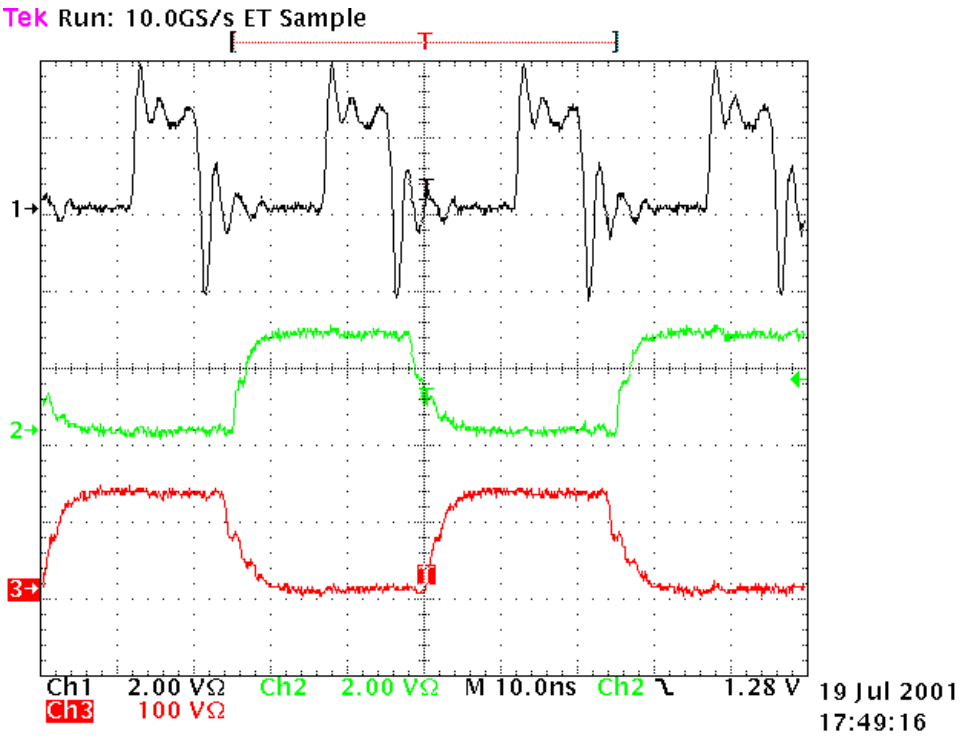

Figure 4.6: Data output transitions of channel 119 (3) and 120 (2) and the read enable signal (1)

4.2.3 Corrections

So far, all measurements refer to the timing of the OTISMem1.0 test chip. The goal is to determine the timing of the memory itself, since this is the information needed for proper control of the OTIS pipeline. The timing of the memory differs slightly from the measurements, because the test environment introduces small propagation delays to the control signals. Unfortunately, there is no way of measuring those delays, so estimates have to be made by simulation. The unknown parameters for this estimate are the process variations of the tested chips. Therefore, a small uncertainty is introduced by this correction. The simulation shows that the only propagation delay reasonably larger than the precision of measurements is the one of the data-in generator. It is estimated to be 0.8ns± 0.3ns. Therefore, 0.5ns are subtracted from t_{DVWL} and 1.1ns are added to t_{WLDX} in order to perform a worst case correction within the uncertainty. The corrected measurements are summarized in the following section.

4.3 Measurements vs. simulation

In general, the measurement results are positive. The average speed of the chips is higher than expected. Table 4.7 presents the measurement results in comparison with the simulation of chapter 2.

It has to be pointed out, that the numbers cannot be compared directly. The measure-

Symbol	Parameter	Simulation		Measurements		Unit
		Best	Worst	Best	Worst	
t_{AVRH}	address valid to read enable high	≥ 1.5	≥ 3	≥ -0.3	≥ -0.3	ns
t_{RLAX}	read enable low to address transition	≥ 2.5	≥ 5	≥ -0.6	≥ -0.3	ns
t_{RHRL}	read enable high to read enable low	≥ 4	≥ 8	≥ 1.6	≥ 2.1	ns
t_{RLRH}	read enable low to read enable high	≥ 8	≥ 15	≥ 5.9	≥ 6.7	ns
t_{RLDX}	read enable low to data transition	$= 1$	$= 2$	$= 1.3$	$= 1.6$	ns
t_{RLDV}	read enable low to data valid	$= 3.5$	$= 7$	$= 4.7$	$= 5.1$	ns
t_{DVWL}	data valid to write enable low	≥ 1.5	≥ 3	≥ 0.4	≥ 0.5	ns
t_{WLDX}	write enable low to data transition	≥ 1.5	≥ 3	≥ 1.5	≥ 1.6	ns
t_{AVWL}	address valid to write enable low	≥ 1.5	≥ 3	≥ -1.5	≥ -1.3	ns
t_{WLAX}	write enable low to address transition	≥ 4.5	≥ 9	≥ 2.7	≥ 3.0	ns
t_{WHWL}	write enable high to write enable low	≥ 4	≥ 7	≥ 2.8	≥ 3.2	ns
t_{WLWH}	write enable low to write enable high	≥ 8	≥ 16	$\geq x < 5$		ns

Table 4.7: Measurement results vs. simulation

ments describe the absolute maximum ratings of the timing constraints, whereas the predicted timing is a conservative estimate. For example, the nominal timing allows complete level changes of the bit-lines of 1.6V. Shorter enable times do not neccessarily cause malfunction, although this would lead to reasonably smaller level changes. One absolute maximum rating simulation for t_{RLRH} was presented in figure 2.13 and can directly be compared with the measurement. In the worst case simulation, t_{RLRH} turned out to be 9ns. The best case can be estimated to be 4.5ns. The measurements fit well in this range, so it is assumed that the tested chips have no serious deviations from their nominal characteristics. Other constraints that can be compared are t_{RLDX} and t_{RLDV}. The reason is, that no conservative estimate has been made for those, because they describe a delay that could precisely be determined by the simulation. Again, the measurements are well in the middle of worst case and best case. These results underline the accuracy of the simulation model. All other constraints are measured to be much less critical than expected. Therefore, performance at 40MHz should not even be problematic for a worst case chip.

4.4 Performance at 100MHz

The measured timing allows to design a cycle at 100MHz. For two ports and 240bit word length this results in a data rate of 5.5GByte/sec. Of course, this has to be seen in relation to the size of the RAM, but anyway it is a pretty impressive number. Figure 4.7 shows the data outputs of channel 0, 119, 120 and 239.

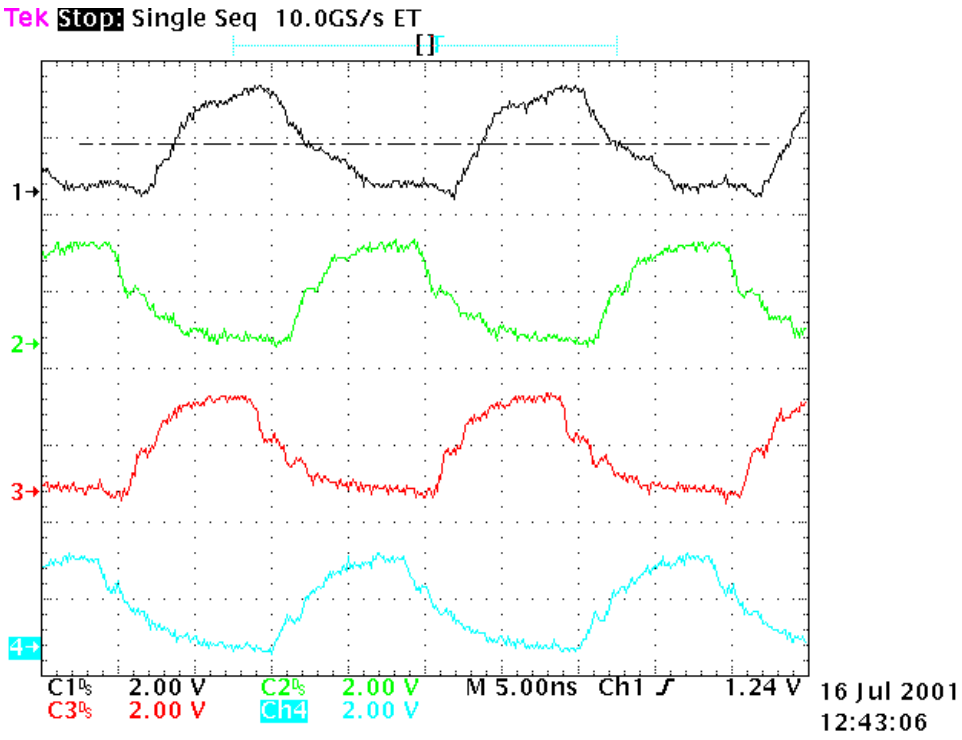

Figure 4.7: Data output of channels 0, 119, 120 and 239 (from top to bottom) at 100MHz

Chapter 5

Integration of Derandomizing Buffer

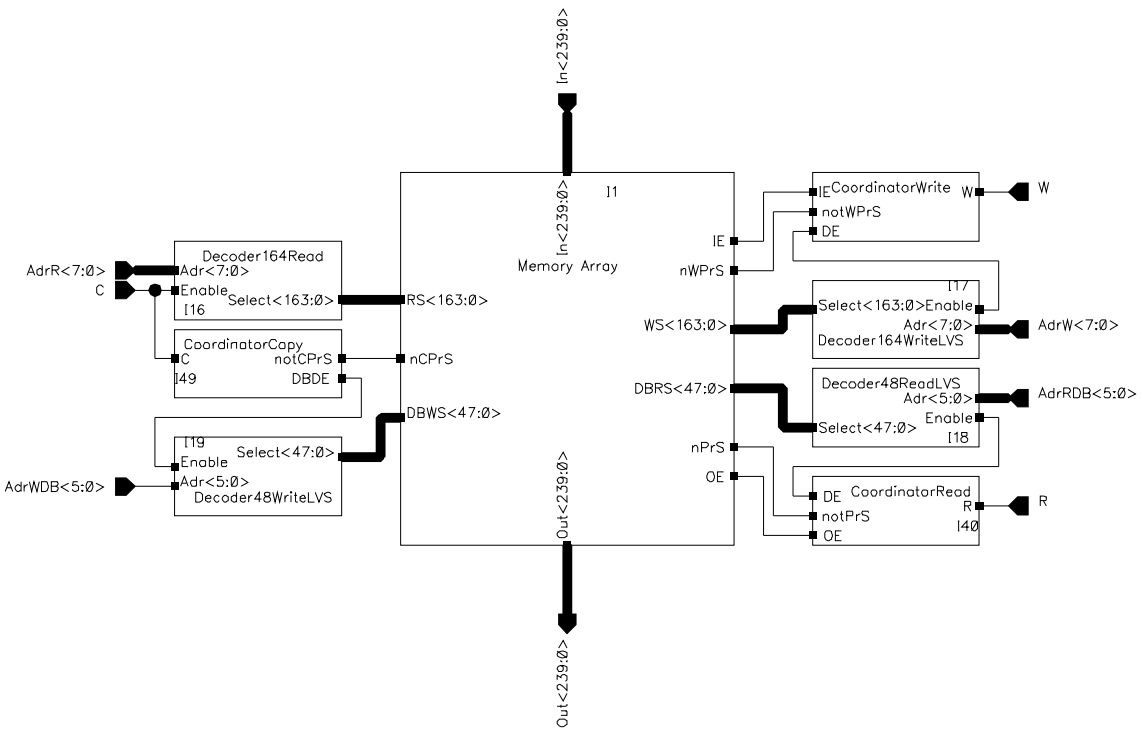

Figure 5.1: Block diagram of memory and derandomizing buffer unit

5.1 Implementation

The succeeding instance after the pipeline on the OTIS TDC is the derandomizing buffer. Selected events are buffered here after readout from the pipeline. Different solutions are possible for the implementation of the derandomizing buffer. One way known from the Helix chip [13] is to design one large memory that is logically separated into pipeline and derandomizing

buffer. This requires a certain overhead of memory and a rather complicated control algorithm that highlights and write protects the derandomizing buffer entries. A simple solution would be the implementation of two independent RAMs. The disadvantage of this approach is that space is wasted for extra I/O amplifiers and power bars between the two RAMs. The optimum in size and simplicity in control is achieved by hard wiring two arrays of memory cells such that the read bit-lines of the first drive the write bit-lines of the second array. The two consecutive blocks can be provided with independent address circuitry, so transfer of events between arbitrary addresses is possible. This copy cycle may run simultaneous to the read and write actions. Writing data into the pipeline is identical with the write cycle of the OTISMem1.0. Readout now occurs only from the derandomizing buffer. The unit consisting of two dual port RAMs can be considered as triple port RAM with three specialized ports: a write port, a copy port and a read port. Figure 5.1 shows the block diagram of the pipeline and derandomizing buffer unit. Table 2.1 summarizes its nets.

Signal	Name	Description
W	write enable	controls write process
AdrW(7:0)	pipeline write address	defines the write pointer
$\overline{\text{WPrS}}$	not write-precharge select	switches the write prechargers
IE	in enable	connects the input amplifier to the bit-lines
WDE	write decoder enable	enables the write decoder
WS(x)	write select	selects word #x of pipeline for write
DI, $\overline{\text{DI}}$	data in, not data in	write bit-lines
C	copy enable	controls copy process
AdrR(7:0)	pipeline read address	points on data to be copied
AdrWDB(5:0)	DB write address	defines the copy pointer
$\overline{\text{CPrS}}$	not copy-precharge select	switches the copy prechargers
CDE	copy decoder enable	enables the DB write decoder
DBWS(x)	DB write select	selects word #x of DB for write
DC, $\overline{\text{DC}}$	data copy, not data copy	copy bit-lines
R	read enable	controls read process
AdrRDB(5:0)	DB read address	defines the read pointer
$\overline{\text{PrS}}$	not read-precharge select	switches the read prechargers
RDE	read decoder enable	enables the DB read decoder
DBRS(x)	DB read select	selects word #x of DB for read
OE	out enable	triggers the data output
DO, $\overline{\text{DO}}$	data out, not data out	read bit-lines

Table 5.1: Nets of the pipeline including derandomizing buffer (DB)

5.2 Simulation and results

The simulation of this building block is completely equivalent with the simulation of the test memory. The simplified simulation environment was already proven to be accurate enough to predict the real behavior of the memory. Small corrections have to be applied to the data

related timings due to the propagation delays introduced by the buffers. Also, it is very important that the propagation delays of the decoders are determined precisely, so they can be replaced by delay chains for the simulation. Figure 5.2 shows the simulation of the reduced decoder (a delay chain) versus the real decoder. The simulation environment (figure 5.3 is set up the same way as the one in chapter 2. The delays of the coordinators have been modified and the multiplexers for the external control have been removed. The simulation results for worst case are presented in figure 5.4.

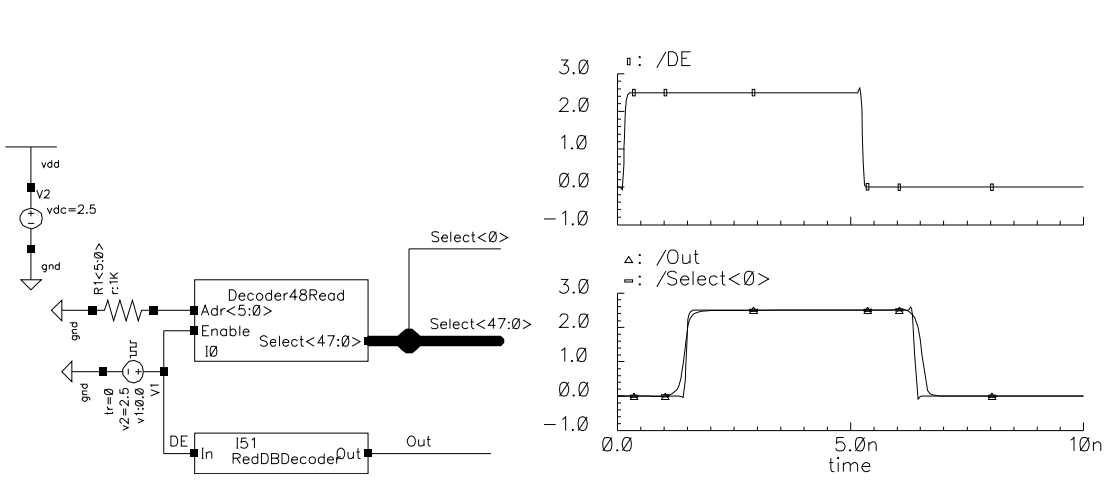

Figure 5.2: Simulation of reduced decoder versus real decoder

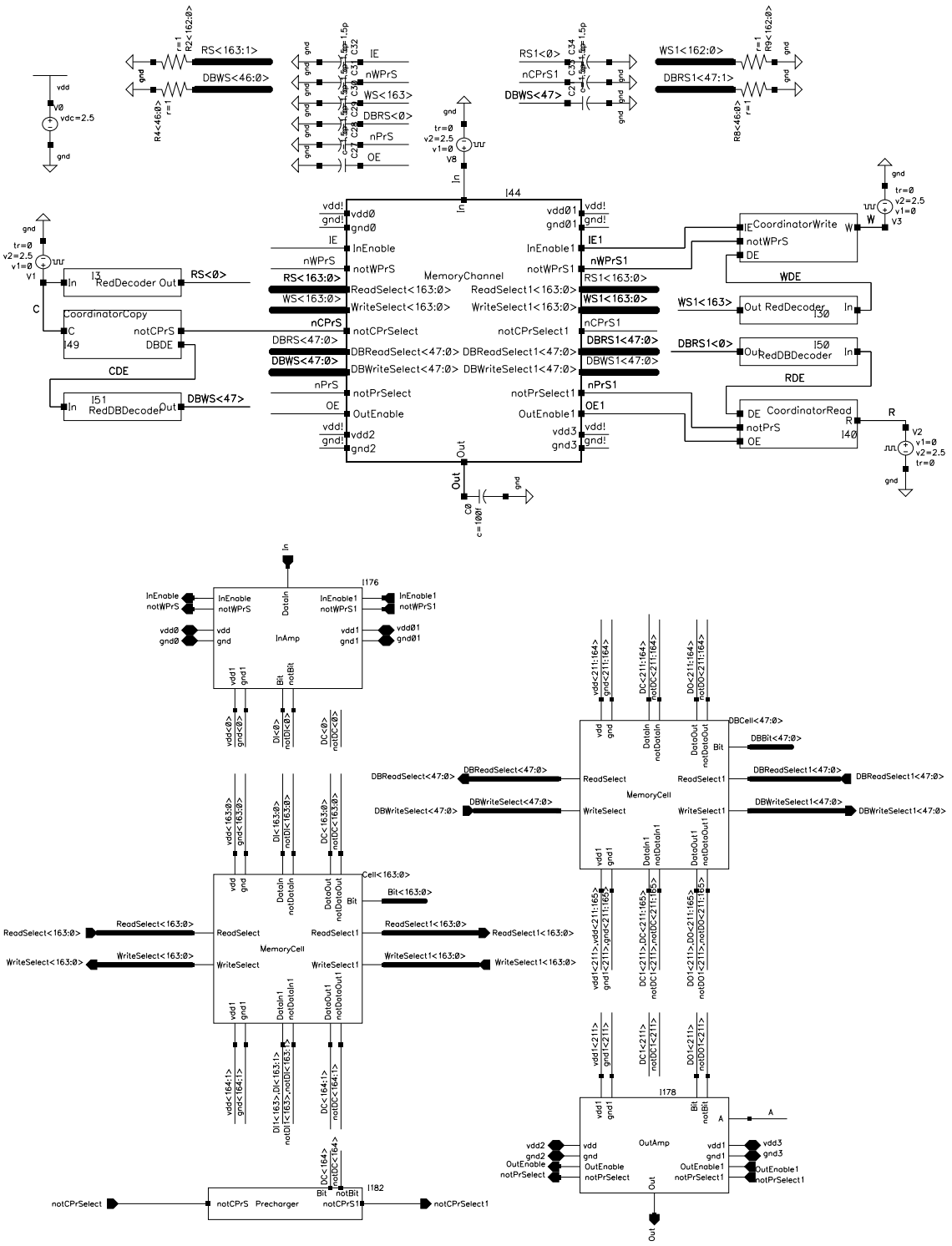

Figure 5.3: Simulation environment of pipeline and derandomizing buffer

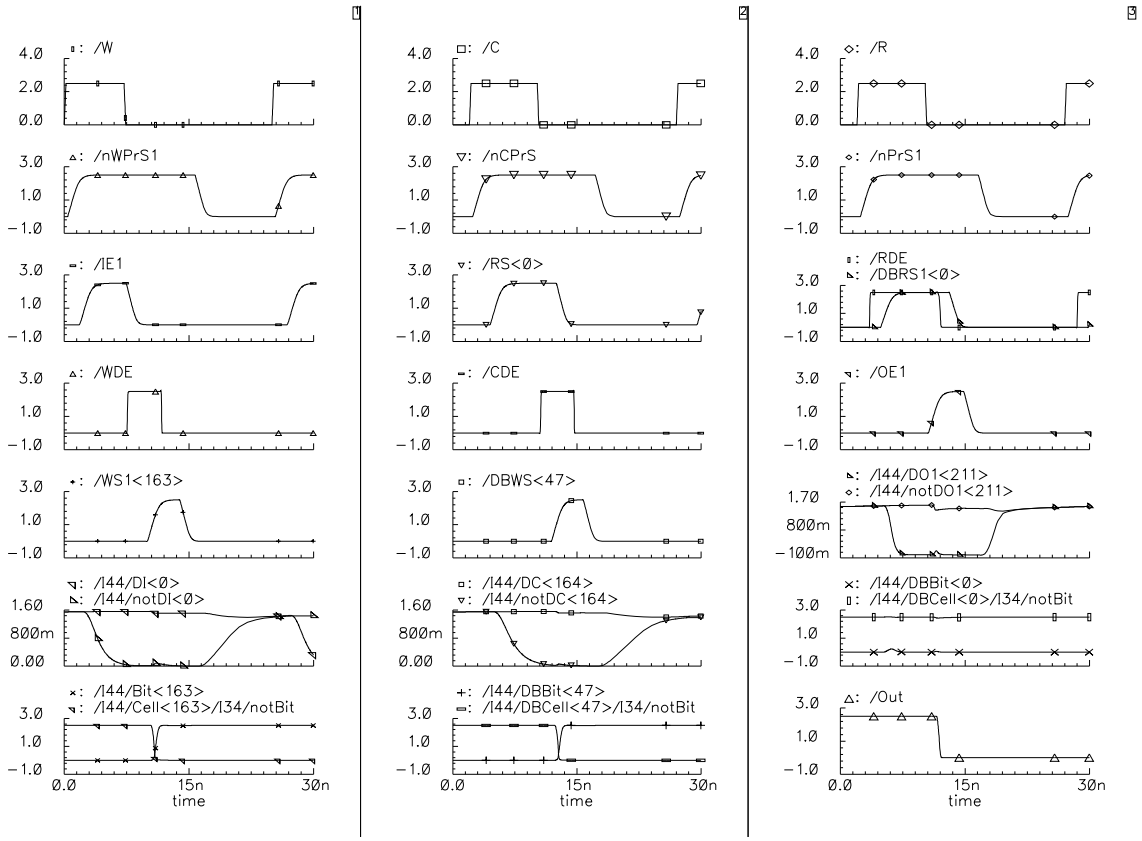

Figure 5.4: Worst case simulation results for pipeline and derandomizing buffer. Read and write was described in figure 2.10. The only difference is, that reading occurs from the derandomizing buffer with slightly different timing. The copy enable rising edge switches off the copy precharger and enables the read decoder of the pipeline. This leads to pulling one of the copy bit-lines to ground. The copy enable falling edge pulses the derandomizing buffer write decoder, which leads to the selection of a write select-line in the derandomizing buffer and to flipping the addressed cell. At the end of the cycle, the precharger brings back the copy bit-lines to their initial level.

5.3 Timing

The timing is derived from the worst case simulation. The best case constraints are better by a factor of two as seen in chapter 2. Data related constraints have to be corrected by the buffer delay of the horizontal control lines, since the simplified simulation considers only one block of the memory array. The propagation delay in the worst case was simulated to be 1ns. The timing diagram is presented in figure 5.5. The corresponding constraints are found in table 5.2.

Symbol	Parameter	Best	Worst	Unit
t_{WHDV}	write enable high to data valid	≤ 1	≤ 2	ns
t_{DVWL}	data valid to write enable low	$\geq$1.5	$\geq$3	ns
t_{WLDX}	write enable low to data transition	≥ 1.5	≥ 3	ns
t_{AVWL}	address valid to write enable low	≥ 1.5	≥ 3	ns
t_{WLAX}	write enable low to address transition	≥ 4	≥ 8	ns
t_{WHWL}	write enable high to write enable low	≥ 3.5	≥ 7	ns
t_{WLWH}	write enable low to write enable high	≥ 7.5	≥ 15	ns
t_{AVCH}	address valid to copy enable high	≥ 1.5	≥ 3	ns
t_{CLAX}	copy enable to address transition	$\geq$2	$\geq$4	ns
t_{DBAVCL}	DB address valid to copy enable low	≥ 1	≥ 2	ns
t_{CLDBAX}	copy enable low to DB address transition	≥ 3.5	≥ 7	ns
t_{CHCL}	copy enable high to copy enable low	≥ 3	≥ 6	ns
t_{CLCH}	copy enable low to copy enable high	≥ 8	≥ 16	ns
t_{DBAVRH}	DB address valid to read enable high	≥ 1	≥ 2	ns
t_{RLDBAX}	read enable low to DB address transition	≥ 1.5	≥ 3	ns
t_{RHRL}	read enable high to read enable low	≥ 2.5	≥ 5	ns
t_{RLRH}	read enable low to read enable high	≥ 5	≥ 10	ns
t_{RLDX}	read enable low to data transition	$= 1$	$= 2$	ns
t_{RLDV}	read enable low to data valid	$= 3.5$	$= 7$	ns

Table 5.2: AC characteristics of pipeline and derandomizing buffer

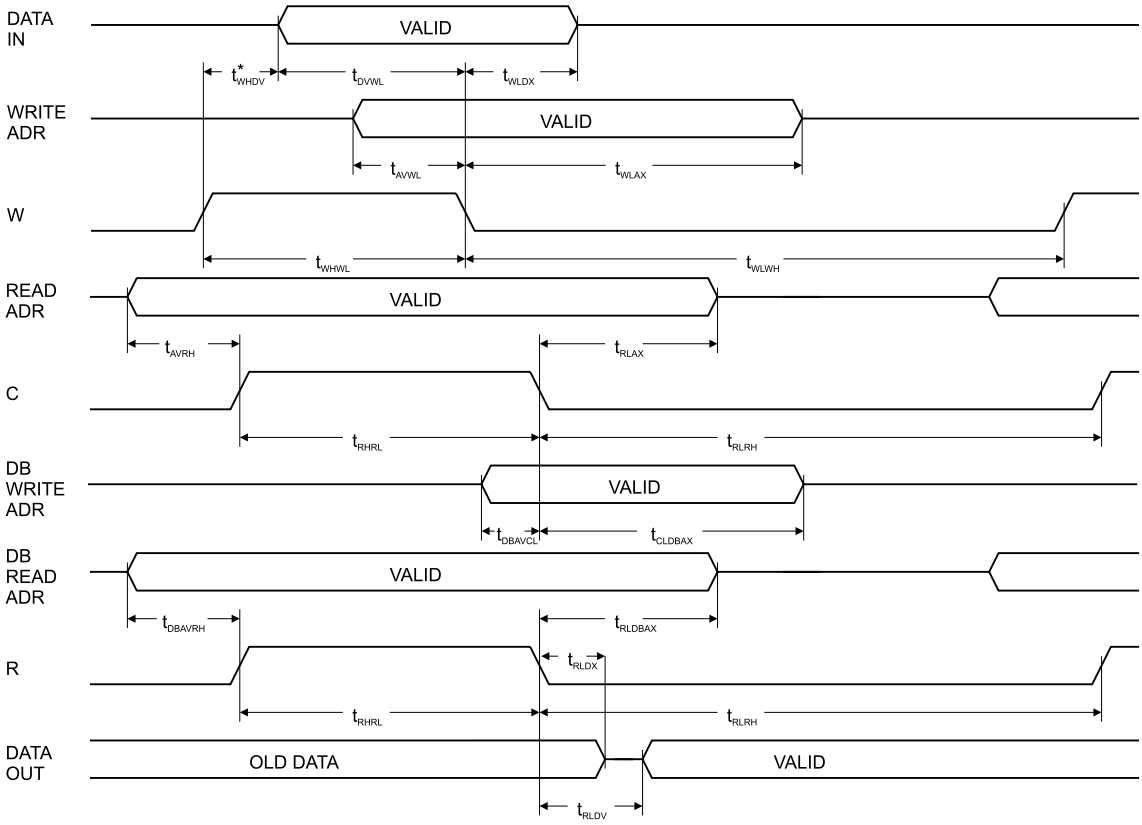

Figure 5.5: Timing diagram for pipeline and derandomizing buffer

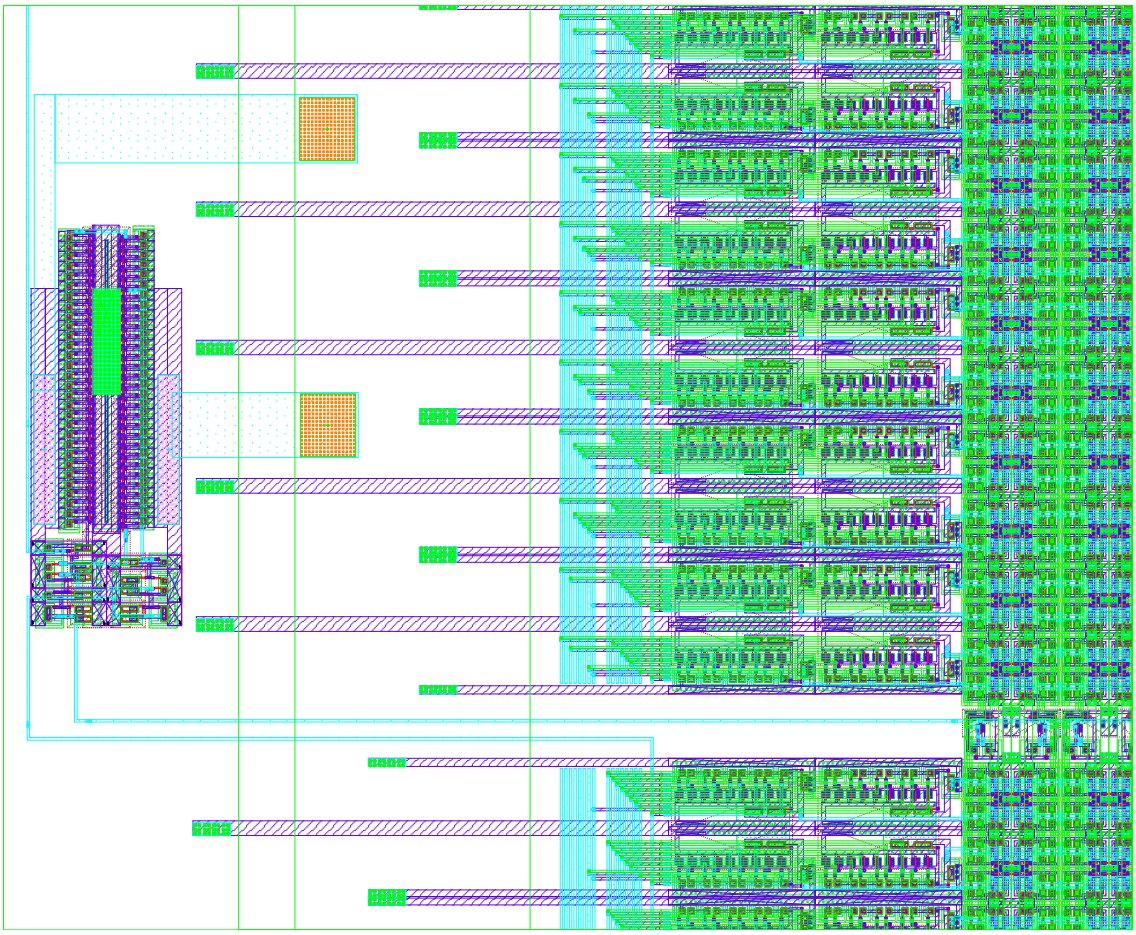

Figure 5.6: Layout of the copy coordinator (left) and the two memory blocks. The pipeline (top) is separated from the derandomizing buffer (bottom) by the copy prechargers.

Chapter 6

Conclusion and Outlook

In this thesis the development of a radiation hard dual port Static-RAM for the OTIS TDC is presented. The OTIS pipeline and derandomizing buffer are planned to be implemented in this structure. The test chip OTISMem1.0 was designed and build for testing the prototype of the pipeline. A test environment on chip enabled to demonstrate the functionality of this RAM at real-time performance. Precise timing measurements could be taken that prove the accuracy of the simulation model. Further, performance at 100MHz was demonstrated, which results in a data rate of 5.5GByte/sec. Therefore, even chips reasonably slower due to process variations are expected to operate at the LHCb bunch crossing frequency of 40MHz.

A building block including pipeline and derandomizing buffer has been designed and simulated based on the experience of the tested chip. Therefore, proper function is strongly expected. In order to examine the behavior of the derandomizing buffer, a derandomizing buffer memory channel has been submitted, which is still to be tested. If this structure shows the expected performance, the building block can be used for the OTIS without any changes. A specialized port enables to copy data from the pipeline to the derandomizing buffer using only the copy enable signal. This simplifies the required control logic and also results in the smallest size possible, since no I/O amplifiers are needed for the copy process.

Based on the measurements, a behavioral model of the pipeline and derandomizing buffer is currently being developed, which will allow to design a control logic for the OTIS TDC. When the LHCb detector will start to exploit the b-hadrons for CP-asymmetry in 2006, hopefully it will be with a little help from OTIS.

Appendix A

OTISMem1.0 Pad List

Pad	Signal	type	Description
1	AdrRExt(6)	input	external read address
2	AdrRExt(7)	input	external read address
3	AdrRExt(3)	input	external read address
4	AdrRExt(2)	input	external read address
5	AdrRExt(1)	input	external read address
6	AdrRExt(0)	input	external read address
7	R	input	read enable
8	AutoTime	input	switches read coordination between internal and external
9	OEExt	input	external out enable
10	notPrSExt	input	external precharge select
11	AdrRCounterCK	input	read pointer clock
12	AdrRCounterRes	input	read pointer reset
13	VDDI	input	power
14	GNDI	input	power
15	AdrRMon(0)	output	read pointer monitor
16	AdrRMon(1)	output	read pointer monitor
17	AdrRMon(2)	output	read pointer monitor
18	AdrRMon(3)	output	read pointer monitor
19	AdrRMon(4)	output	read pointer monitor
20	AdrRMon(5)	output	read pointer monitor
21	AdrRMon(6)	output	read pointer monitor
22	AdrRMon(7)	output	read pointer monitor
23	OutMon(239)	output	read pointer monitor
24	OutRMon(120)	output	read pointer monitor
25	OutRMon(119)	output	read pointer monitor
26	OutRMon(0)	output	read pointer monitor
27	VDDI	input	power
28	GNDI	input	power
29	GNDA	input	DLL power
30	VDDA	input	DLL power

31	Vctrl	analog	DLL control voltage
32	Reset	input	DLL reset
33	notClk	input	DLL not clock
34	Clk	input	DLL clock
35	notHit	input	not hit
36	Hit	input	hit
37	PDClk	output	phase detector clock
38	PDDeClk	output	phase detector delayed clock
39	LastDOut	output	monitor
40	GNDA	input	DLL power
41	VDDA	input	DLL power
42	OutDLL(0)	output	DLL output
43	OutDLL(1)	output	DLL output
44	OutDLL(2)	output	DLL output
45	OutDLL(3)	output	DLL output
46	GNDB	input	DLL power
47	VDDB	input	DLL power
48	Adr(0)	input	MUX adress
49	Adr(1)	input	MUX adress
50	Adr(2)	input	MUX adress
51	Adr(3)	input	MUX adress
52	ECEnable	input	error checker enable
53	VDDI	input	power
54	GNDI	input	power
55	ECSelect	input	switches error checker on and off
56	ORCKExt	input	external output register clock
57	ORSelExt	input	external output register select
58	ORSwitch	input	switches output register between internal and external
59	StopMon	output	monitors the stop signal
60	Mode	input	switches between mode 0 and 1
61	CDCK	input	channel detector clock
62	CDUnlock	input	unlocks the channel detector (active low)
63	OROut	output	monitors the output register's output
64	GNDI	input	power
65	VDDI	input	power
66	SEUCounterRes	input	resets the SEU counter (active low)
67	Display(0)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
68	Display(1)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
69	Display(2)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
70	Display(3)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
71	Display(4)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
72	Display(5)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
73	Display(6)	output	monitors SEU counter (mode 0) or channel detector (mode 1)
74	Display(7)	output	monitors SEU counter (mode 0) or channel detector (mode 1)

75	VDDI	input	power
76	GNDI	input	power
77	AdrWSwitch	input	switches write address between internal and external
78	AdrWCounterCK	input	read pointer clock
79	AdrWCounterRes	input	read pointer reset
80	IEExt	input	external in enable
81	W	input	write enable
82	AutoPr	input	switches write precharger between internal and external
83	notWPrSExt	input	external write precharge select
84	AutoTime1	input	switches write coordination between internal and external
85	DEExt	input	external write decoder enable
86	AdrWExt(4)	input	external write address
87	AdrWExt(5)	input	external write address
88	AdrWExt(6)	input	external write address
89	AdrWExt(7)	input	external write address
90	AdrWExt(3)	input	external write address
91	AdrWExt(2)	input	external write address
92	AdrWExt(1)	input	external write address
93	AdrWExt(0)	input	external write address
94	InU	input	odd channel data input
95	InG	input	even channel data input
96	GNDI	input	power
97	VDDI	input	power
98	AdrRSwitch	input	switches read address between internal and external
99	AdrRExt(4)	input	external read address
100	AdrRExt(5)	input	external read address
101	GNDI	input	power
102	VDDI	input	power

Table A.1: OTISMem1.0 pad list

Appendix B

OTISMem1.0 Test Board

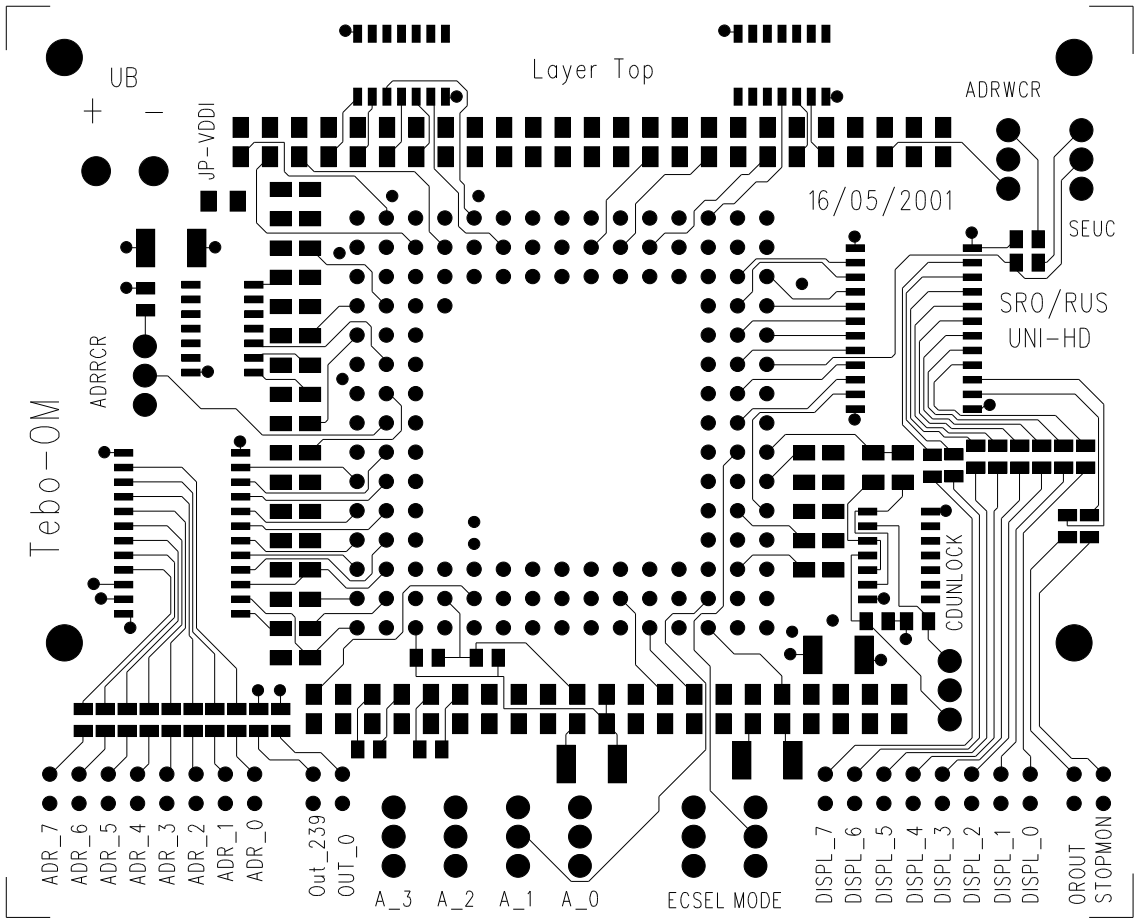

Figure B.1: Test board - layout

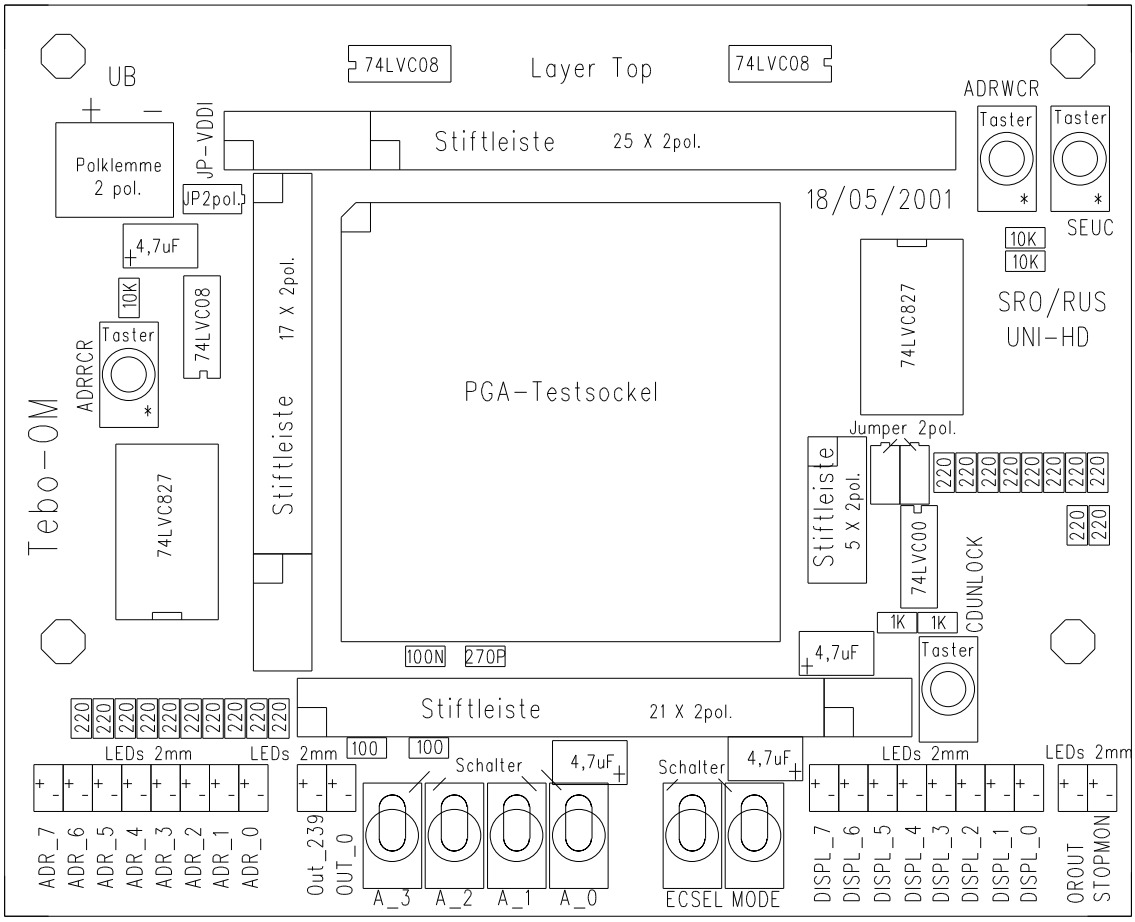

Figure B.2: Test board - devices

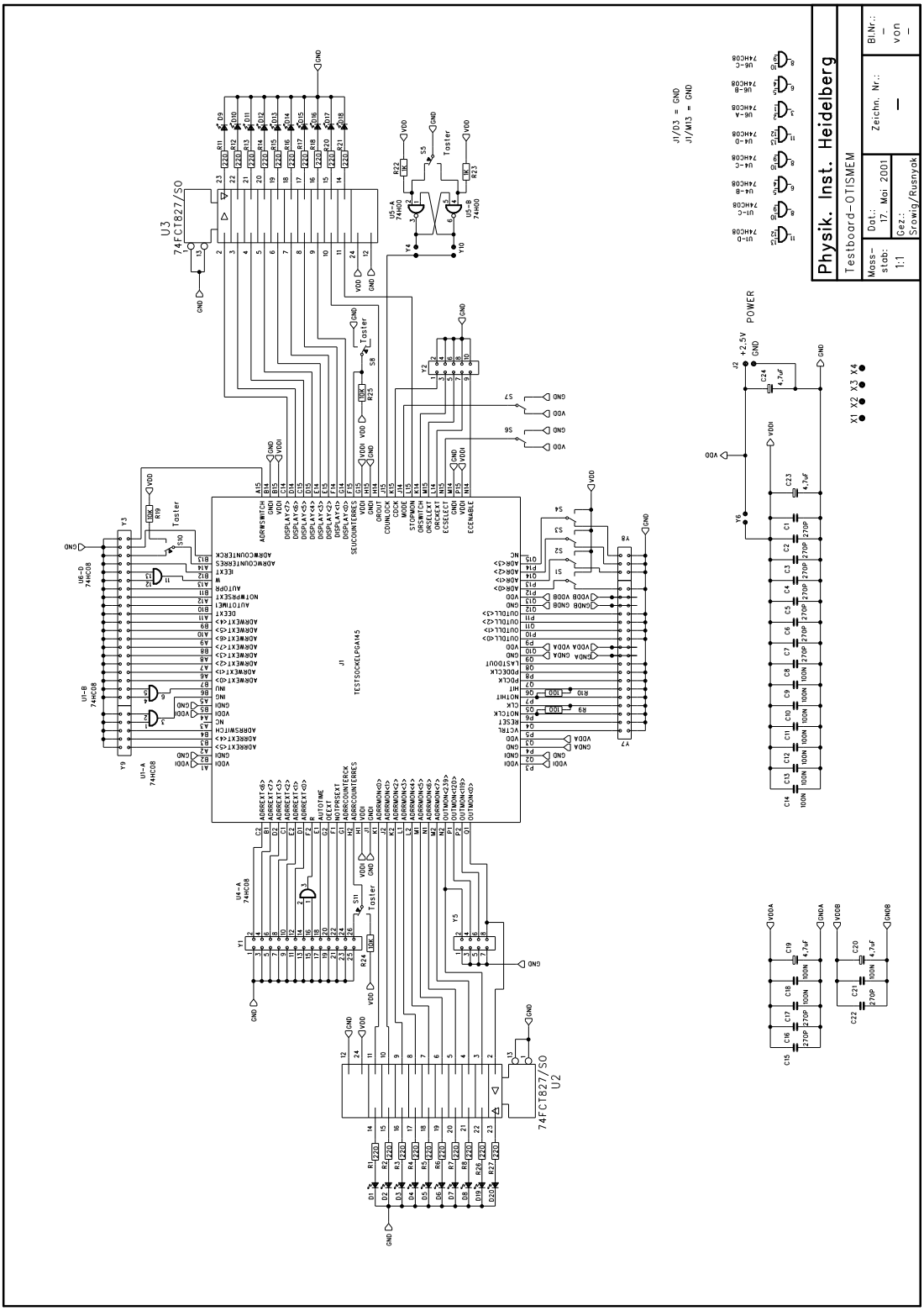

Figure B.3: Test board - schematic

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Erklärung:

Ich versichere, daß ich diese Arbeit selbständig verfaßt und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den ....

Unterschrift