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Prototypes of monolithic pixel sensors based on a 65nm imaging process for high energy physics

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Abstract

The field of silicon imaging technology is advancing steadily. While consumer electronics will be its main driving factor, the vast applicability of silicon offers high energy physics a variety of highly efficient, high precision detector concepts. At CERN, the ALICE experiment is developing a new type of monolithic active pixel sensor, based on the Tower Partners Semiconductor Co., Ltd. (TPSCo) 65nm CMOS imaging process. This technology is foreseen to provide sensors to replace the innermost part of the currently installed Inner Tracking System 2 (ITS2) of the ALICE detector during the third Long Shutdown period 2026-2028 (LS3) of CERN's Large Hadron Collider (LHC).
To achieve a reduction in material budget, and limit power consumption, the innermost three layers of the Inner Tracking System 3 (ITS3) will be composed of wafer-scale stitched particle detectors. The development of this sensor started with the submission of a Multi Layer Reticle (MLR1) in 2021, and will soon conclude its second phase, the evaluation of the Engineering run 1 (ER1), in 2025. This thesis is concerned with test procedure of the first prototypes of this new sensor technology, namely the Analog Pixel Test Structure (APTS), and the Monolithic Stitched Sensor (MOSS). The basic readout and calibration procedure of the APTS is investigated, as well as the effect of electronic noise on the performance of the sensor. For MOSS, studies have been performed investigating single-event effects during two testbeam campaigns in March and April of 2024 at the heavy ion facility (HIF) at UCLouvain in Louvain-la-Neuve, and the cyclotron U-120M at the Nuclear Physics Institute (NIP) of the Czech Academy of Science. Additionally, the overall efficiency and operational margins of the first batch of MOSS has been studied at a third testbeam campaign at the Proton Synchrotron (PS) at CERN in July. These results are discussed with respect to the efficiency of MOSS sensors from the second batch. The results of this study contribute to a better understanding of the operational margin of the sensors, as well as their radiation hardness and the influence of design parameters on the performance of the sensor, and will be considered in the development of the next sensor generation.

Zusammenfassung

Das Feld der Silizium-Bildgebungstechnologie entwickelt sich stetig weiter. Doch nicht nur die Unterhaltungselektronik, die zum größten Teil für besagte Entwicklung verantwortlich ist, profitiert von den vielfältigen Anwendungsmöglichkeiten von Silizium. Auch in der Hochenergiephysik wird von hochpräzisen und effizienten Detektorkonzepten basierend auf Siliziumsensoren Gebrauch gemacht. Am CERN entwickelt das ALICE-Experiment einen neuen Typ von monolithischen aktiven Pixel-Sensoren, basierend auf dem TPSCo 65nm CMOS-Prozess. Diese Technologie soll während der dritten Long Shutdown Phase 2026-2028 (LS3) des Large Hadron Collider (LHC) den inneren Teil des derzeitigen Inner Tracking System 2 (ITS2) des ALICE-Detektors ersetzen.
Im neuen Inner Tracking System 3 (ITS3) werden die innersten Schichten des derzeitig verbauten ALPIDE-Sensors durch Wafer-große Sensoren ersetzt, die zylindrisch um den Strahl herumgebogen sind. Vorteile dieses Entwurfs sind unter Anderem eine Reduktion des vorhan-

denen Materials (durch die intrinsische Stabilität der gebogenen Sensoren sind keine Trägermaterialien notwendig) und eine geringere Leistungsaufnahme im Vergleich zum ITS2. Die Entwicklung dieser Sensoren begann mit der MLR1 Testphase im Jahr 2021 und die zweite Phase wird voraussichtlich mit der Auswertung des Engineering Run 1 (ER1) im Jahr 2025 enden. In dieser Arbeit wird im Rahmen des ER1 über die Testprozedur der ersten Prototypen dieser neuen Sensortechnologie, dem APTS und dem MOSS, berichtet. Die grundlegende Auslese- und Kalibrierungsprozedur des APTS wird untersucht, sowie der Einfluss von elektronischen Störquellen auf die Leistung des Sensors charakterisiert. In zwei Testbeam-Kampagnen im März und April 2024 am Heavy Ion Facility (HIF) der UCLouvain in Louvain-la-Neuve und am Zyklotron U-120M des Nuclear Physics Institute (NIP) der Czech Academy of Science wurden Single-Event-Effekte des MOSS Sensors untersucht, welche in dieser Arbeit präsentiert und diskutiert werden. Zusätzlich wurde die Detektoreffizienz des MOSS in einer weiteren Testbeam-Kampagne am Proton Synchrotron (PS) des CERN im Juli untersucht. Anhand dieser Studien wird die Betriebsmarge des MOSS Sensors bestimmt und zwischen verschiedenen Versionen des MOSS Sensors verglichen. Die Ergebnisse dieser Studie werden in die Entwicklung der nächsten Sensorgeneration einfließen und tragen zu einem besseren Verständnis der Strahlenhärte und des Einflusses von Designparametern auf die Leistung des Sensors bei.

Contents

1 Introduction

In July 2022 at CERN, the four big experiments at the Large Hadron Collider (LHC), A Large Ion Collider Experiment (ALICE), A Toroidal LHC Apparatus (ATLAS), Compact Muon Solenoid (CMS) and LHC-beauty (LHCb) entered a new period of data taking with Run 3. All of them previously performed upgrades to their detection and data selection systems, some of which consisted of the complete replacement of subsystems, to keep up with the high information density resulting from both the proton-proton and lead-lead collisions at a center-of-mass energy of up to 6.8 ATeV and with a heavy-ion collision rate more than ten times higher than in previous runs [1].

The ALICE experiment is dedicated to probing the physics of strongly interacting matter, in particular the properties of the Quark-gluon plasma (QGP). The QGP is a state of matter with such a high energy density, that quarks and gluons are no longer confined into hadrons, but instead form a collective medium that expands and flows like a relativistic fluid. In this plasma, the quarks and gluons that make up all nuclei are strongly coupled to- and interacting with another, while the hydrodynamic expansion accelerates them outwards, cooling the plasma in the process. It is theorised, that this state of matter is very similar to the contents of the universe only 10 µs after the Big Bang [2]. In laboratory conditions, the LHC achieves this state by colliding heavy lead ions with an energy of up to $\sqrt{s_{NN}} = 5.36\,\text{TeV}$ per nucleon pair. By studying the production and decay of outgoing particles from the QGP, ALICE contributes to the understanding of the fundamental interaction of subatomic matter and complex phenomena such as color confinement and chiral symmetry restoration. The experiment attempts to shed light on how matter is organized, with specific investigation of the strong nuclear force and its role in generating a big portion of the mass of ordinary matter.

The current innermost component of the ALICE detector, the Inner Tracking System (ITS)2, is made of seven layers of silicon-based Monolithic Active Pixel Sensor (MAPS), amounting to a total active area of $10\,\text{m}^2$. The implemented sensor is the thoroughly researched and tested ALICE Pixel Detector (ALPIDE) sensor, which employs a 180 nm CMOS Imaging Process from TPSCo[1]. The current material budget (i.e. the detector thickness in terms of radiation length) of one layer of the ITS2 amounts to $0.262\%X_0$ for the inner three layers and $0.813\%X_0$ for the outer four layers [4], which has already been a huge milestone in high precision particle tracking. Following the path towards even higher spatial resolution and improved tracking performance, the material budget is one of the most important and difficult to overcome limitations, since it is directly related to the mean angular deflection of charged particles on their way through the different detector layers by multiple Coulomb scattering. It remains one of the main goals of many high-energy physics experiments to reduce the material budget of their detector systems built for particle tracking purposes.

[1]Formerly: TowerJazz Panasonic Semiconductor Co., Ltd. (TPSCo) [3].

2 Semiconductors

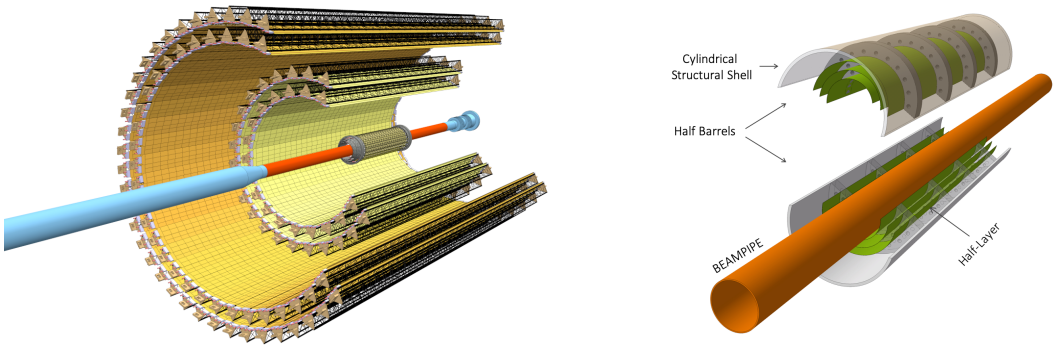
Semiconductor-based detector technology dates all the way back to 1962 with the detection of a gamma-ray spectrum via a lithium-drifted p-i-n junction in Germanium [5]. In 1969, the first Charge-Coupled Device (CCD) was invented [6], solidifying a foundation for silicon as a material in particle detection. However, these devices were still difficult to manufacture, integrate with on-chip electronics and read out at high rates [7], making it simply too expensive to replace the large-area covering gas detectors. In the late 1980s the CMOS process became well-established, replacing the previously used NMOS logic as the dominant fabrication process, as well as the earlier transistor-transistor-logic (TTL). It uses complementary and symmetrical pairs of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) (see section 2.2), to construct integrated circuit chips, including microprocessors, microcontrollers, memory chips and other digital logic circuits. Profiting from the cheaper and more accessible technology, active-pixel sensors began making their way into high-energy particle physics applications. These devices had the special advantage of in-pixel amplification and reduced noise compared to earlier passive designs [8]. As demands for high resolution, high detection rate, and low material thickness devices in particle detection applications steadily rises, active-pixel sensors become more and more attractive as a replacement for previous detectors based on gas-chambers, or silicon strips. With new developments in commercially available silicon imaging technology (especially for consumer applications like photography), it is possible to build these devices with smaller and smaller features – and therefore with increasingly tight spacing. Each new generation semiconductor process receives its name by its minimum feature size in nanometers, either of the process's transistor *gate length*[2], or its transistor density[3]. The currently installed ALPIDE in the ALICE ITS2 (Figure 2.1 (a)), is based on the TPSCo 180 nm imaging process [9], while the new generation of pixel sensors (foreseen to be installed in the ITS3 in 2026 [10]) is based on the TPSCo 65 nm technology node. The smaller feature size of this generation of silicon pixel sensors directly results in several advantages, such as smaller pixel sizes and the availability of large-scale silicon wafers, making it possible to fabricate pixel sensors with unprecedented spatial resolution, that cover a larger area than what was ever possible before. Within the ITS3, they will be thinned down to below 50 µm, and bend around the beam pipe, getting as close as 19 mm to the interaction point (compared to the previous 23 mm in the ITS2) [11].

2.1 A truly cylindrical silicon pixel sensor

The layout of the ITS3 is shown in Figure 2.1 (b). In order to achieve a truly cylindrical layout, the ITS3 is foreseen to make use of a relatively recent technology in the CMOS imaging process called *stitching*. It describes the process of merging multiple design structures on a wafer together, creating a single CMOS image sensor. Its size is not bound by current manufacturing limitations, such as the maximum reticle field size of wafer steppers, but instead only by the wafer size, which in commercial applications can become as large as $300 \times 300\,\mathrm{mm}^2$. Due to the intrinsic stability of their cylindrical geometry, the new ITS3

[2] The distance between the transistor's source and drain electrodes

[3] The exact naming of a process node is decided by the manufacturer, not an exact measurement of feature size.



(a) (b)

Figure 2.1: **(a)** Layout of the ITS2 detector [4] **(b)** Layout of the ITS3 Inner Barrel [12]

layers do not have to be supported by a conventional aluminum frame, but are foreseen to be held in place by ultra-lightweight spacers made from carbon foam. The entire design is going to feature a very low power density across the pixels, which means all water cooling inside the detection volume of the ITS2 will be replaced by air cooling in ITS3. This will decrease the material budget down to $0.07\% X_0$ per layer [11]. This is a crucial step forward, as the current ITS2 material budget is the main limiting factor for the study of low transverse-momentum particles. Monte Carlo simulations have shown [12], that going from the ITS2 to the ITS3 will increase the capability of the detector to separate secondary vertices of heavy-flavour decays from the interaction point, by improving the reconstruction of their decay topologies and those of dileptons. This will all be crucial to provide a better understanding about the properties of the QGP formed in heavy-ion collisions. The general requirements for the ITS3 sensors are listed in Table 1. Current prototypes of $1.4\,\text{cm} \times 25.9\,\text{cm}$ long pixel sensor strips have already been manufactured and are currently being tested at the European Organization for Nuclear Research (CERN). This prototype is called the MOSS, and will be discussed in Section 2.4.

2.2 Working principle of semiconductors

The semiconductors used in electronic devices are crystalline solids – highly ordered structures forming a crystal lattice extending in all directions. This lattice is made up of the nuclei of the crystal atoms (in this case: Si) and tightly bound *valence electrons*. Pauli's exclusion principle states, that the same energy state can not be occupied by more than one electron at a time, and there is only a limited number of energy states that fulfill the periodic boundary conditions of the crystal lattice. Together, these conditions determine, whether the crystal is electrically conductive or not. Valence electrons reside in the so-called *valence band*, while energetically higher electrons take up a spot in the *conduction band* (see Figure 2.2).
The latter is directly responsible for the electrical conductivity of the material. Since the kinetic energy of the electrons in the conduction band is higher than the potential energy of the free states in the valence band, the electrons in the conduction band are delocalised, and act as quasi-free charge carriers. Intrinsically, silicon is an insulator, i.e. there is a gap

Particle Rate	
Pb-Pb average interaction rate	50 kHz
Pb-Pb peak interaction rate	164 kHz
Total particle flux (peak flux, Layer 0)	5.75 MHz cm^{-2}
Detection performance	
Single point resolution	$\lesssim 5$ µm
Pixel pitch	< 25 µm
Detection efficiency	> 99 %
Fake-hit occupancy (10 µs Frame Duration)	$< 1 \times 10^{-6}$ $pixel^{-1}frame^{-1}$
Readout efficiency	
Fraction of Pb-Pb interactions fully recorded, Layer 0	> 99.9 %
Fraction of incomplete Pb-Pb interactions, Layer 0	$< 1 \times 10^{-3}$
Power budget	
Power Dissipation Density, Active Region	< 40 mW cm^{-2}
Power Dissipation Density, Peripheral Region	< 1000 mW cm^{-2}
Material parameters	
Material Budget	0.07 % X_0 $layer^{-1}$
Silicon thickness	≤ 50 µm $layer^{-1}$
Radiation Load	
NIEL	1×10^{13} 1MeV n_{eq} cm^{-2}
TID	10 kGy
Environmental Conditions	
Target Operating Temperature	15 °C to 30 °C

Table 1: General requirements for the ITS3 sensor [11].

in between the valence and conduction band (called band gap), where no energy states are available. At 0 K, all electrons reside in the valence band. By thermal excitation electrons can overcome this barrier and enter the conduction band. In this band, electrons move freely within the material, making it electrically conductive. Since the phenomenon of electrical conductivity of semiconductors is strongly dependent on the band gap, to control a material's electrical properties, one has to control and modify its band gap structure. This can be done by choosing different semiconductor alloys, or introducing impurities to the crystal (referred to as *doping*). In this way, additional energy states are created by introducing a dopant into the lattice. A dopant is typically an element with either one more or one less electron in its outermost electron shell than silicon. Atoms with excess electrons are called *donors*, while atoms with an electron deficit are called *acceptors*. Donors create energy states close to the conduction band, where electrons can easily be excited and delocalized. Acceptors cre-

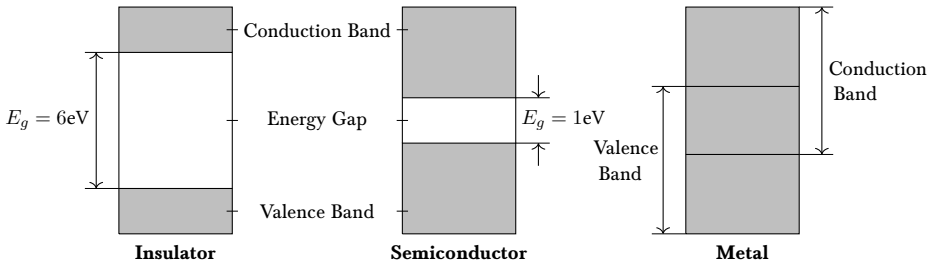


Figure 2.2: Energy band structure of different types of solids

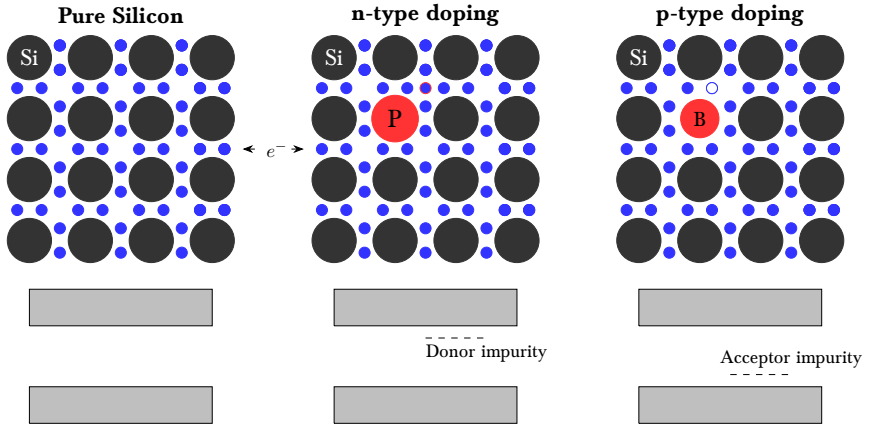


Figure 2.3: Silicon doping example with phosphorus (n-type) and boron (p-type)

ate extra states close to the valence band, attracting electrons from the neighboring valence bonds. Silicon doped with these elements forms what is called *n-type* and *p-type* semiconductors, respectively (See Figure 2.3). Equivalent to the movement of electrons in the conduction band, the vacancies left by excited electrons inside of the valence band can also propagate through the material – they appear to be moving and acting as positive charge carriers. This principle is why in semiconductor detectors, instead of electrons and ions, the free charge carriers are considered to be electrons and holes.

2.2.1 The p-n junction

One important application of doping, which turns a regular semiconductor into an electronic device, is to bring differently doped materials into electrical contact, forming a *p-n junction*. The donor and acceptor doping concentrations N_D and N_A play an important role. When two semiconductors of different type (typically one p-type and one n-type, or an alternating combination thereof) are in contact, the difference in concentration of acceptors and donors will lead to a charge carrier diffusion against the concentration gradient. Electrons and holes recombine, creating what is called a *depletion region* around the junction. In this region, there are no free charge carriers. The recombination of electrons and holes results in the formation of an electric field E, arising from the positively charged donor ions and negatively charged

acceptor ions, which remain in the lattice. Any charge carrier in this region will experience the electric potential and be accelerated along the elecric field lines towards either the p- or the n-side, counteracting the diffusion until an equilibrium is reached. The potential barrier, also called ***junction potential*** is given by [13]:

$$\Delta V = \frac{k_B T}{e} \ln\left(\frac{N_D N_A}{n_i^2}\right) \tag{2.1}$$

k_B : Boltzmann constant $= 1.38 \times 10^{-23}$ J/K
T : medium temperature
e : elementary charge $= 1.60 \times 10^{-19}$ C
n_i : intrinsic charge carrier concentration

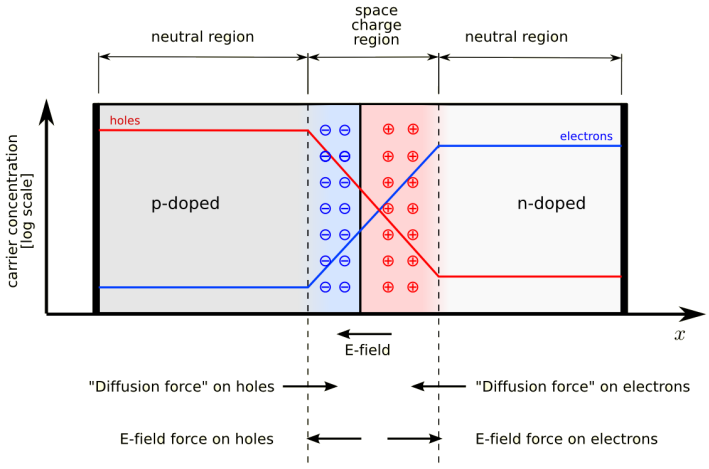


Figure 2.4: P-n junction of two semiconducters with opposite doping profiles [14]

Figure 2.4 illustrates this concept. By applying a voltage across the junction, this depletion region can be modified. For particle detection a *reverse-bias* voltage is typically applied, attracting even more electrons into the p-type and more holes into the n-type volume, effectively enlargening the depletion region. The reason for this, is that the depletion region represents the active detector volume – it is here, where incoming ionising radiation will leave traces of charge carriers, that will be accelerated by the electric field and ultimately collected and processed, resulting in the identification of a particle *hit*. Enlarging the depletion region means increasing the sensitive detection area of the sensor, since the depletion region will cover a larger fraction of the silicon volume. Furthermore, this increases the electric field strength, and therefore improves collection speed of the mobile charge carriers, leading to an increased time resolution.
If the reverse-bias voltage is too high, the junction will break down, and a current will start flowing. This is a result from the high electric fields liberating electrons out of the valence, and into the conduction band by quantum tunneling. These currents are usually tiny due to the relatively low probability of the tunneling process. However, if the electric field strength is high enough, these charge carriers are accelerated up to a point, where they themselves can free electron-hole pairs by colliding into them, creating an avalanche breakdown, potentially

causing permanent damage to the lattice. The voltage applied to thin, monolithic silicon pixel detectors therefore usually does not exceed around 5 V [15].

2.2.2 Particle detection

Semiconductor detectors work on the principle of detection by ionisation. In the context of particle detection, ionisation is a process, in which a formerly neutral atom loses at least one electron, which will leave the atom electrically charged. When ionising radiation (such as X-rays, cosmic muons or some of the collision products at particle accelerators) enters matter, particles will electromagnetically interact and exchange momentum. As long as this momentum exchange is sufficiently high to overcome the specific ionisation threshold, it will cause the atoms to ionise. The reaction products of this interaction (usually a positively charged ion and a negatively charged electron) can be collected by applying an electric field across the traversed medium. This process can be used to measure the incident particles' energy loss and reconstruct its trajectory. To model the average energy loss by ionisation per unit path length of a traversing charged particle, the Bethe-Bloch equation [16] is used:

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi}{m_e c^2} \frac{N_A}{M_u} \left(\frac{e^2}{4\pi\varepsilon_0} \right)^2 \rho \frac{Z}{A} \frac{z^2}{\beta^2} \left[\ln\left(\frac{2m_e c^2 \beta^2}{I\,(1-\beta^2)} \right) - \beta^2 \right] \tag{2.2}$$

with $\frac{4\pi}{m_e c^2} \frac{N_A}{M_u} \left(\frac{e^2}{4\pi\varepsilon_0} \right)^2 = 0.3071\,\mathrm{MeVcm^2/g}$

m_e : electron mass $= 9.109 \times 10^{-31}\,\mathrm{kg}$
N_A : Avogadro's number $= 6.022 \times 10^{23}/\mathrm{mol}$
M_u : Molar mass constant $= 1\,\mathrm{g/mol}$
e : elementary charge $= 1.609 \times 10^{-19}\,\mathrm{C}$
ε_0 : vacuum permittivity $= 8.854 \times 10^{-12}\,\mathrm{C\ s^2/kg\ m^3}$
ρ : density of the absorbing material
Z : atomic number of the absorbing material
A : atomic weight of the absorbing material
z : charge of the incident particle in units of e
I : mean excitation potential
$\beta := v/c$ of the incident particle
$\gamma := 1/\sqrt{1-\beta^2}$

The mean excitation energy describes the traversed material. It is usually inserted from accurate tables of I as a function of Z [17], however a very simplified approximation of the mean excitation energy has been given by Felix Bloch in 1933:

$$I \approx (10\,\mathrm{eV}) \cdot Z. \tag{2.3}$$

With the atomic number $Z_{\mathrm{Si}} = 14$ of silicon, this yields a mean excitation energy of 140 eV for silicon based semiconductor detectors. By modeling the energy loss of a traversing charged particle, it is possible to make assumptions about the number of liberated charge carriers, which is imperative for making design decisions before building a new detector. For example, according to Equation 2.2, a proton with 10 GeV momentum ($\beta\gamma \approx 10$ loses about 550 eV/µm in silicon. For a 10 µm thick sensor, this results in a mean energy loss of 5.5 keV. Considering a separation energy of 3.61 eV [18] for electron-hole pairs, this energy deposit corresponds to the liberation of approximately 1500 electron-hole pairs.

Typical MAPS are built from a highly doped p^{++}[4], a p^- epitaxial layer, which functions as the active volume. They house p-type and n-type implants on top of the epitaxial layer, called PWELL and NWELL, respectively. The n-type implant acts as a collection diode, while the PWELLs shield the epitaxial layer from the on-chip circuitry, housed on top of the PWELLs (see Figure 2.5). When an ionizing particle traverses the depleted volume of the epitaxial

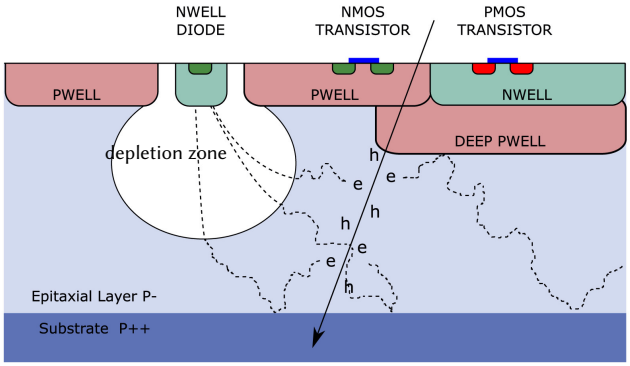


Figure 2.5: Geometrical cross-section of a MAPS pixel [19].

layer, it creates electron-hole pairs along its path, according to its mean energy loss (Equation 2.2). These pairs are initially assumed to be stationary, since their initial velocity is small compared to their drift velocity. Due to the higher concentration of carriers around the particle trajectory, they will then start diffusing isotropically[5], until hitting one the p-type walls, recombining with a hole or entering the depletion region. Similarly to the p-n junction, the hole concentration difference between the p- epitaxial layer and the p++ substrate (or PWELLS) creates a potential difference, acting like a reflective wall to the electrons. Charge carrier recombination under the emission of a photon occurs only when an electron exactly matches the energy of a hole, and is therefore a rather rare process.

When electrons cross the boundary of the depletion region, the electric field will accelerate them towards the NWELL collection diode, where they will finally be collected. The charge carrier movement induces a current on the collection electrode according to the Shockley-Ramo theorem:

$$I_{\text{coll}} = E_v q v, \tag{2.4}$$

where q is the charge of the particle, v is its instantaneous velocity (or the drift velocity in silicon $v_d \approx 5 \times 10^6\,\text{cm/s}$ [20]), and E_v the electric field component in the same direction. It is usually in the order of a few nA per electron.

[4]Light doping is denoted with a "-"-sign and refers to a donor concentration between $1 \times 10^{14}\,\text{cm}^{-3}$ and $1 \times 10^{16}\,\text{cm}^{-3}$. Heavy doping is shown with a "+"-sign and usually refers to a concentration between $1 \times 10^{18}\,\text{cm}^{-3}$ and $1 \times 10^{20}\,\text{cm}^{-3}$. Even higher concentrations are usually denoted by two "+"-signs.

[5]Again, the small initial velocity of the electron-hole pairs is ignored.

The input capacitance is typically charged by a non-zero voltage V_{reset}. On charge collection, the capacitance is discharged by I_{coll}, causing a voltage drop of

$$\Delta V_{\text{signal}} = \frac{Q_e}{C_{\text{pixel}}}. \tag{2.5}$$

This voltage drop is then discriminated and compared to a user-defined threshold V_{th} in the periphery. If $V_{\text{signal}} < V_{\text{th}}$, the sensor will register a particle hit. A reset current I_{reset} drives the voltage on the collection diode and restores it back to V_{reset}. The threshold value has to be tweaked in order to differentiate between noise on the collection diode, and an actual particle event, to ensure a low fake-hit rate (FHR) of the pixel.

Beyond this point, every MAPS will show slight differences in design paramters, such as pixel size, readout circuitry, collection diode geometry, epitaxial layer thickness, doping concentration etc. This is why a deeper look will now be taken into each of the prototypes that were investigated in this thesis.

2.2.3 Applications in electronics

The broadest application for semiconductor devices is their usage within integrated circuits. A basic p-n-junction, as it is described in Section 2.2.1, forms a *diode*. A diode is the simplest form of an electronic semiconductor device, with the attribute of letting electrons flow mainly in one direction – from the n-type side to the p-type side.

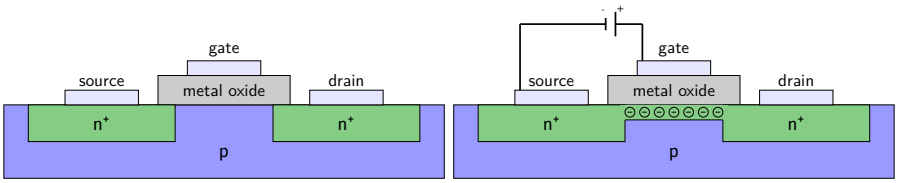


Figure 2.6: **(a)** Schematic cross section through an n-channel MOSFET in its off-state. No current can flow between the source and drain terminal. **(b)** When applying a voltage between the source and gate terminals, an n-channel with variable width will form, allowing electrons to flow from source to drain. The width of the n-channel determines the conductivity of the transistor, where higher gate voltages lead to wider channels and therefore higher conductivity.

A slightly more complex type of electronic device is the *transistor*. Transistors are the most frequently produced electronic devices, being used in any modern computer chip. The most widely used type of transistor is the MOSFET, which is fabricated by the controlled oxidation of silicon. They can be realized by combining two p-n junctions together into either a p-n-p (referred to as p-type metal-oxide-semiconductor (PMOS)) or an n-p-n (referred to as n-type metal-oxide-semiconductor (NMOS)) transistor. An example for a simple NMOS transistor is shown in Figure 2.6. In a logic circuit, its three terminals *source*, *gate* and *drain* are each

connected individually. The gate terminal is used to control current flowing between the source- and drain terminals. In its intrinsic state, the interface between n-type and p-type silicon will not allow any current to flow there (Figure 2.6 (a)). Applying any voltage between the source and the drain, will only enlarge the depletion region at either one of the n-type regions. If a positive voltage is applied between the source and the gate, electrons will be pulled towards the metal oxide insulator (Figure 2.6 (b)). Since these electrons cannot cross the insulator, this part of the transistor acts like a capacitor, trapping electrons between the two n-type materials. If the voltage is sufficiently high, the electrons form a channel between the source and the drain, through which current can flow. This type of transistor is also referred to as *enhancing*, since applying a voltage will increase its conductivity, as opposed to *depleting* transistors, where applying a voltage will increase their resistance instead. PMOS transistors function very similarly, with the polarity of the voltage between the source and the gate being reversed.

PMOS devices were the dominant semiconductor technology for integrated circuits between the late 1960s and early 1970s, but have been overtaken by NMOS devices shortly after. The reason for this is the difference in electron- and hole mobility. The electron mobility in an n-type channel of NMOS MOSFETs is about three times higher than the hole mobility in the p-type channel of PMOS MOSFETs. This allows for NMOS logic to achieve higher switching speeds, which is favourable in most applications, where their higher power consumption does not pose a problem. Logic consisting of complementary pairs of metal-oxide-semiconductor (MOS) transistors is called complementary metal-oxide-semiconductor (CMOS) logic. Since one transistor in the MOSFET pair of this combination is always off, it draws significantly less power than either PMOS or NMOS logic in its idle state, which is why CMOS technology has been the dominant MOSFET fabrication process for most integrated circuits since the 1980s.

An imporant application for CMOS logic is the memory cell. Typically, it is made up of six MOSFETs and can be in one of two stable states, which are used to denote 0 and 1. An example memory cell is shown in Figure 2.7. As long as the two cross-coupled inverters formed by $M_1 - M_4$ are connectetd to the supply voltage V_{DD}, they will continue to reinforce each other and remain in their complementary state. When the word line (WL) is low, the access transistors M_5 and M_6 are turned off. If the PMOS transistor M_2 is open, the potential on $\overline{Q}$ is high, and Q is connected to ground. In principle[6], the state can be read by asserting WL and measuring the voltage difference between BL and $\overline{BL}$. During a writing process, the bit lines have to be set to the desired state, and WL is pulsed, connecting Q and $\overline{Q}$ to the bit lines, forcing their current logic state into the memory cell.

[6]Because of parasitic capacitance between the bit lines the readout process is more complex, and requires precharging both bit lines before measuring the voltage drop that occurs when asserting the word line.

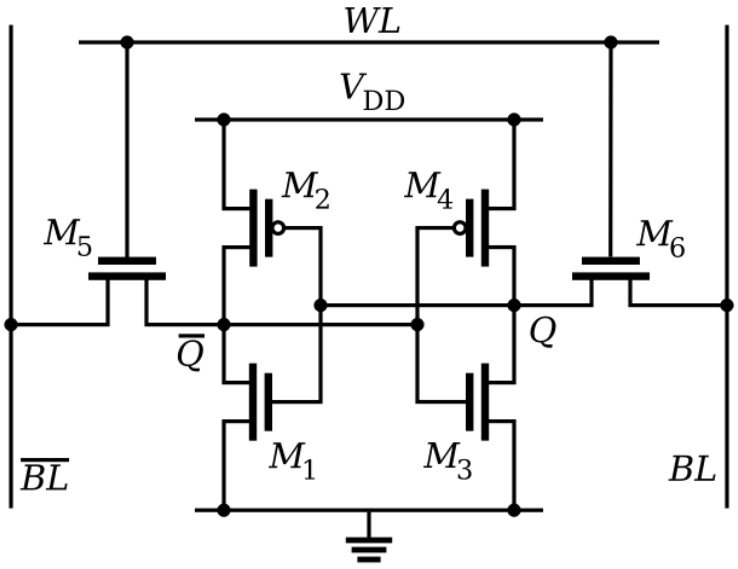


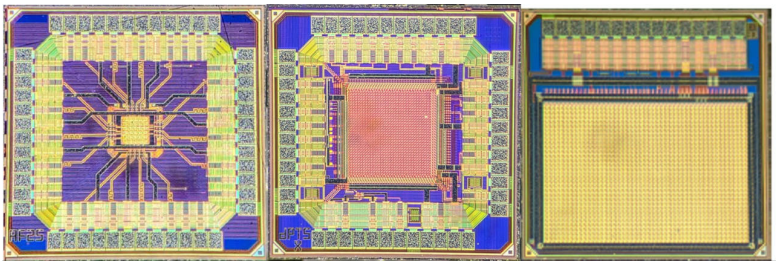
Figure 2.7: Typical 6T static random-access memory (SRAM) cell. Four transistors are used to form two cross-coupled inverters (M1 to M4) and two additional transistors are used for access during read and write operations (M5 and M6).

2.3 The Analog Pixel Test Structure (APTS)

The APTS sensor is part of the Multi Layer Reticle 1 (MLR1), which was the first submission in the 65 nm TPSCo CMOS technology, dedicated to investigate its capabilities for the ITS3 upgrade. The MLR1 was produced in summer 2021, though the work around this thesis has only been carried out in summer 2023. Three major pixel sensors were designed for testing: The APTS, the CE65 and the DPTS. Each sensor was fabricated multiple times with varying pixel pitch, readout circuitry, implant geometry, and methods of amplification. A brief overview of the MLR1 sonsors is given in Figure 2.8. Since the APTS will be the main focus of this thesis, it will be presented in-depth in the following section. The DPTS features a matrix of 32×32 pixels with a pitch of 15 µm and a deep implant structure, with gaps in the low dose n-type implant. It is equipped with an amplifier and a discriminator, and provides time encoded digital readout. The CE65 is a larger sensor with a matrix of 64×32 or 48×32 pixels, with analog readout and a rolling shutter configuration. All three sensors have undergone an extensive characterization campaign, which was carried out both in laboratory and test beam environments [21].

2.3.1 APTS chip architecture

The APTS sensor features a matrix of 6×6 pixels, with direct analogue readout of the inner 4×4 submatrix. Its design purpose is the testing of the pixel cell and comparing process modifications. For this, the sensor was produced in three different flavours, as shown in Figure 2.9. For this thesis, only one kind of the APTS was used for testing. It has a pixel pitch



Chip	# of dies / wafer	# of pixels	Pixel pitches:	10 µm	15 µm	20 µm	25 µm
APTS	34	6×6		✓	✓	✓	✓
CE65	4	64×32, 48×32		–	✓	–	✓
DPTS	3	32×32		–	✓	–	–

Figure 2.8: Photograph of the three main test sensors of the MLR1 run: (from left to right) the APTS, the Digital Pixel Test Structure (DPTS) and The Circuit Exploratoire 65 (CE65). All three chips measure $1.5 \times 1.5\,\mathrm{mm}^2$. The table lists all different manufactured versions of each chip [11].

of 15 µm, a basic source follower structure for signal amplification, and an additional deep implant with gaps in between pixels, which results in reduced charge sharing when compared to other iterations of the chip [22]. This flavour of the APTS shows the most promising results in terms of signal charge collection, compared to the version without gaps [23]. The pixel pitch in the modified with gap version has no significant effect as charge sharing between individual pixels is strongly suppressed. In general, smaller pixel pitches have the advantage of a higher spatial resolution, with the drawback of higher power density, and therefore heat generation. Another important effect of the pixel pitch is the charge collection efficiency. Its dependence on the pixel pitch is only relevant for the standard flavour of the APTS, as there, charge sharing is not suppressed. Larger pixel pitches will increase the charge transport path and together with the expected smaller relative lateral extension of the depletion region, will result in lower charge collection efficiency towards larger pixel pitches. In the modified with gap version, the charge collection efficiency is close to 100 % for all four pixel pitches. This is because the field induced by the gap counteracts charge sharing. In fact, the smaller relative size of the gap increases the charge collection efficiency slightly for larger pixel pitches [22]. This trend is not infinitely scalable, as fully depleting large pixels becomes increasingly more difficult.

The on-pixel circuit layout of the relevant APTS sensor is shown in Figure 2.10. The sensor is controlled via a voltage Digital-to-Analog Converter (DAC) V_{reset} and five current DACs: I_{reset}, I_{biasp}, I_{biasn}, I_{bias3} and I_{bias4}. Additionally, an external back bias voltage V_{BB} can be applied to the substrate, as well as the bulk of the NMOS transistors (PWELL) in each pixel, to increase the size of the depleted region. The source follower version of the APTS gets its name from its M2 transistor. It acts as a voltage buffer for the incoming signal from the

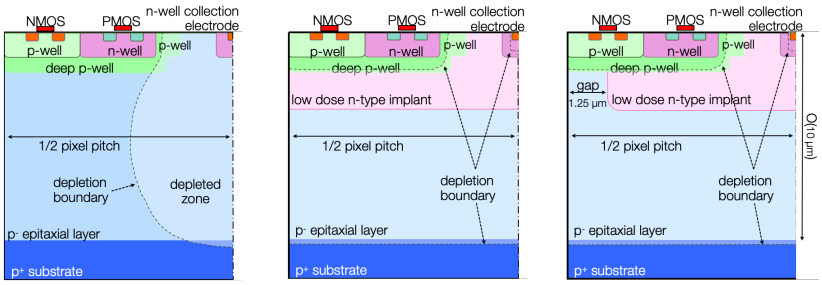


Figure 2.9: Three different sensor flavours: **(a)** standard, **(b)** additional low dose implant and **(c)** additional low dose implant with a gap at the pixel borders (referred to as *deep implant with gaps*) [22].

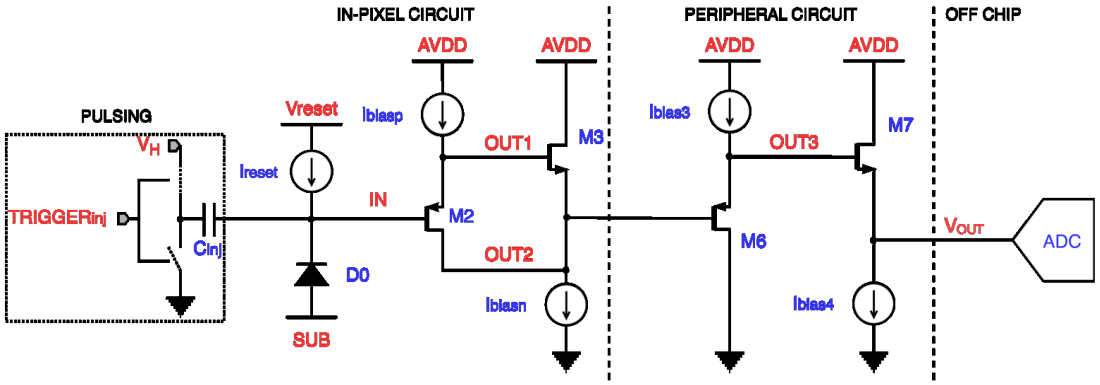


Figure 2.10: Schematics of the APTS pixel circuitry [22]

collection diode. A second source follower stage (M3) is used to further reduce the capacitive load on the collection diode. The signal is then transmitted to an off-chip ADC.

The collection diode is biased and reset using a constant current mechanism. In its initial state, the I_{reset} current only compensates for leakage currents, and the voltage on the collection diode is sitting close to its reset potential V_{reset}. After a particle hit, the current source delivers the constant current I_{reset}, discharging the collection electrode and driving the gate potential of the M2 transistor back to V_{reset}. For various test purposes, an injection capacitance $C_{\text{inj}} = 242\,\text{aF}$ is used to inject a variable charge pulse onto the signal line. The pulse height is controlled via the voltage DAC V_{H}. Figure 2.11 provides a visualization of the signal obtained from injecting charge via the pulsing capacitance C_{inj} for each of the 16 pixels. The reference voltage has been standardized to 0 V. Small fluctuations between pixels can arise due to noise and slight pixel variation during manufacturing, leading to different reset currents across the pixels. After about 10 µs, all pixels have restored their initial state.

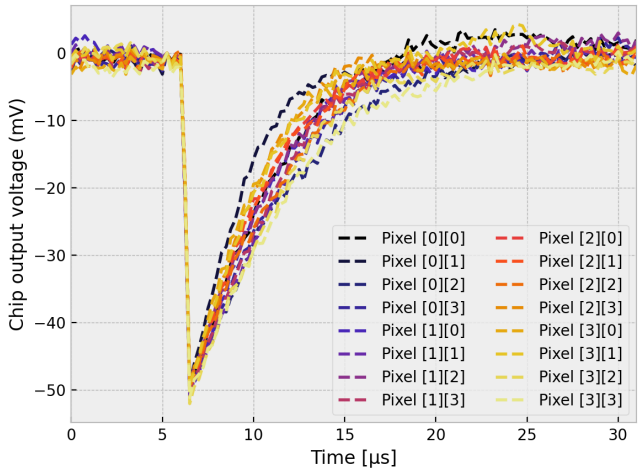


Figure 2.11: Signal shape distribution after charge injections across the 16 pixels of the APTS. The pixel coordinates are indicated as row and column.

2.3.2 Readout

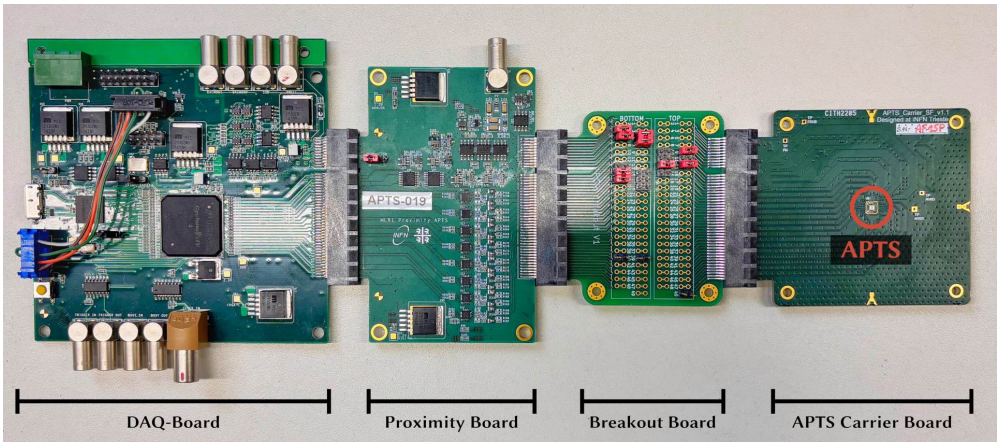


Figure 2.12: Experimental setup of the APTS featuring (from left to right): A Data Acquisition (DAQ) board, a proximity board, a breakout board (optional), and a carrier board, interfacing the sensor.

Figure 2.12 shows the main components of the APTS laboratory setup. The DAQ board is the primary interface between sensor and PC. It is responsible for reading and buffering data, as well as steering sensor (DAC) parameters via an integrated Field Programmable Gate Array (FPGA). Furthermore, it features voltage regulators including current monitoring circuitry, to supply the on-board chip circuitry and proximity card, as well as a temperature measurement circuit. A reverse bias voltage can be applied via an on-board LEMO connector. To trigger the sensor the DAQ board can either generate a trigger based on the chip output, or receive

an external trigger input via another dedicated LEMO connector. While data acquisition is in progress, a busy signal is generated to avoid multiple trigger inputs during the same data event. The board is designed to provide universal functionality to all MLR1 and Engineering Run 1 (ER1) sensors, as well as the well-established ALPIDE sensor.
To adapt to the specific chip type, a proximity card converts supply and steering voltage levels and bias currents from the DAQ board to the corresponding sensor standards. This is also, where the analog information, coming from the APTS is converted into digital information. For this, the proximity card contains Analog-to-Digital Converters (ADCs) to digitize the 16 analog outputs with a resolution of 16 bit and a sample rate of 4 mega-samples per second (MS/s) (corresponding to a sampling period of 250 ns). The breakout board is an optional interface which can be used in between any slot, to gain easy access to all of the 98 lines of the PCI express connector. The carrier board acts as an electronic interface to the sensor, which is wiredbonded and glued in its center. It is also equipped with additional electronic components, that act as a low pass filter which helps to reduce electronic noise. The filter behaviour of the carrier board specifically will be investigated in subsection 3.3.

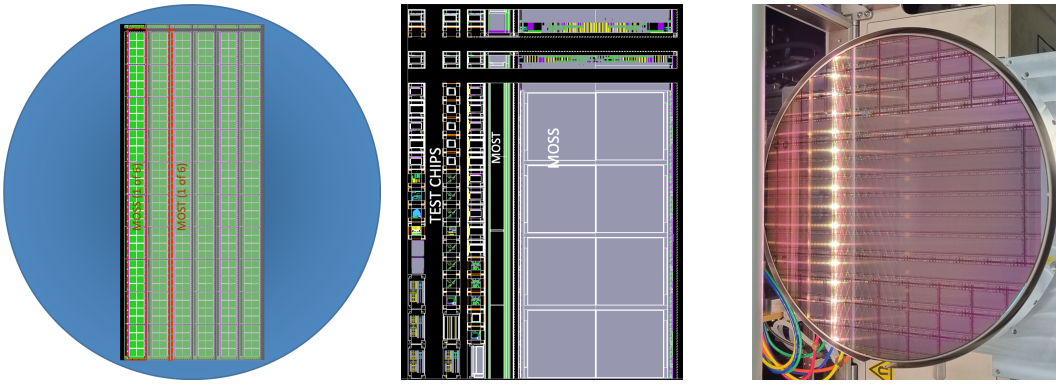
The APTS sensor is one of the few test sensors of the ITS3 project, where full access to the analog domain is possible. To measure the pixel output voltage V_{out}, a buffer has been implemented into the FPGA on the , that continuously stores the analog information of the sensor. When a read request signal is sent to the APTS, snapshot of 200 time frames of V_{out} (corresponding to a measurement of 50 µs) is sent to the digital endpoint of the sensor, and then read out via the on-board USB controller. This is long enough to contain the full rise (1 µs) and decay ($\approx$ 10 µs) of a signal originating from a particle event, such that a full analysis on the analog information of the pixel output can be performed.

2.4 The Monolithic Stitched Sensor (MOSS)

The following section is concerned with sensors of the ER1. The final goal is to replace flat single reticle sensors with wafer-scale stitched sensors. For this, two large stiched sensors, the MOSS and the Monolithic Stitched Sensor Timing (MOST) have been designed and submitted in 2022, together with many smaller test chiplets. The ER1 submission is shown in Figure 2.13. This work performed in the scope of this thesis solely focuses on the MOSS. 24 wafers have been produced in two splits, and all sensors are currently undergoing laboratory tests (further explained in Section 4.1). The sensors are named according to the wafer they originate from. For example, one of the sensors used from the first split, namely `MOSS-2_W02F4`, is named after its chip number 2 (from 1 to 6, directly corresponding to its position on the wafer), wafer `W02` and wafer suffix `F4`.

2.4.1 Sensor design

The MOSS is the first iteration of a wafer-scale pixel sensor, consisting of 10 repeated sensor units (RSUs), which is the largest individual sensor that can fit in the design reticle. Stitched



(a) (b) (c)

Figure 2.13: The ER1 submission: **(a)** conceptual drawing of the Engineering Run (ER) wafer, containing the two sensors MOSS and MOST, **(b)** the reticle, making up one repeated sensor unit and **(c)** A photo of the ER1 pad wafer.

together they form a sensor with an active area of nearly[7] $1.4 \times 25.9\,\mathrm{cm}^2$. Each RSU is composed of two half-units (HUs) labeled *top* and *bottom*, which themselves contain four matrices, reffered to as *regions*, with a pixel pitch of $22.5\,\mu\mathrm{m}$ for the top region (256×256 pixels), and a pixel pitch of $18\,\mu\mathrm{m}$ for the bottom region (320×320 pixels). Some of the regions are made from slightly different front-end variants (see Table 2). Since both top and bottom regions feature almost the same pixel circuit, they differ only in component density – and therefore power density. The analog power density is $7\,\mathrm{mW/cm}^2$ for the top matrix, and

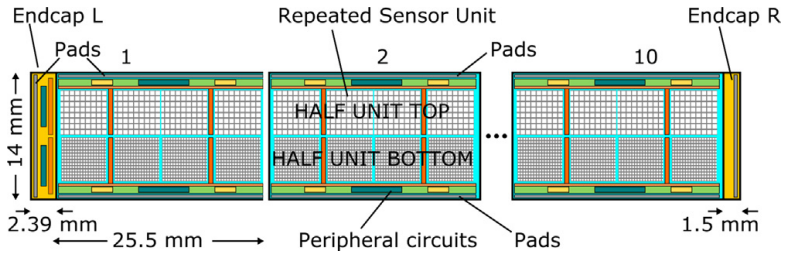


Figure 2.14: Concept diagram of the MOSS chip.

$11\,\mathrm{mW/cm}^2$ for the bottom matrix [24]. Each HU is a fully standalone functional unit with independent periphery, readout and powering. This makes it possible to supply RSUs via pads from the long edge, or via pads from the end-caps, making use of the interconnecting metal lines, which traverse the entire sensor from left to right. Since each HU can be tested independently, this allowes studying their yield and its possible dependence on the density of circuits.

[7] The actual active area is slightly smaller due to the reticle design, which also includes some dead area for readout periphery.

	Region 0	Region 1	Region 2	Region 3
TOP	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
BOTTOM	Standard	Standard	Standard	Slightly different layout

Table 2: Different front-end variants for the eight regions on a MOSS RSU.

2.4.2 Readout

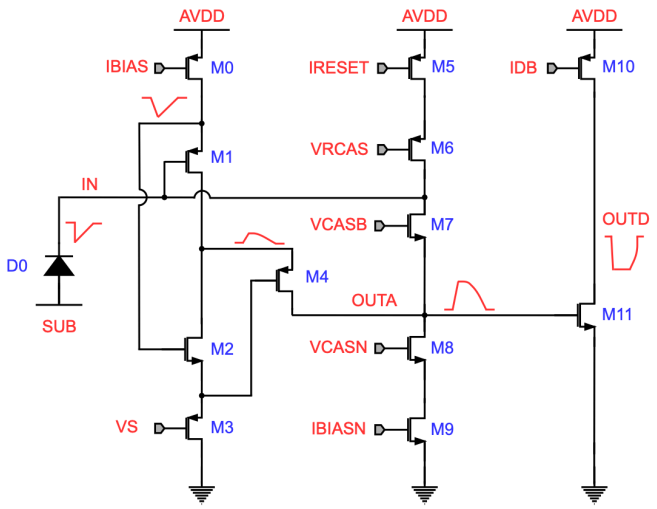


Figure 2.15: Simplified schematic of the MOSS analog pixel front-end

The analog in-pixel front-end of MOSS is adapted from the DPTS and is illustrated in Figure 2.15. It is mainly controlled via its four current DACs (I_{BIAS}, I_{RESET}, I_{BIASN} and I_{DB}) and its three voltage DACs (V_{S}, V_{VCASB} and V_{CASN}). Additionally, a pulsing voltage V_{PULSEH} can be set (similarly to V_{H} for the APTS) for injecting charge into the analogue in-pixel front end with an injection capacitance $C_{\mathrm{inj}} = 258\,\mathrm{aF}$ to investigate the sensor response. Also like with the APTS, an external bias voltage can be applied to the substrate in order to increase the size of the depletion region. If no back-bias voltage is applied, a shunt resistor ($0\,\Omega$) is instead used to avoid potential buildup. The initial signal is first processed by the transistor network M1-M9, where its inverted and amplified. The I_{RESET} current drives the signal line back to its operational potential of $1.2\,\mathrm{V}$. At transistors M10 and M11 it is then discriminated against a threshold and sent to the periphery.

The MOSS features a synchronous serial protocol for communication. Both powering and communication via the long edge and the left end cap is possible. Its address space consists of 12 bits, giving access to all relevant functions and registers. This leaves 512 registers for each

region and 2048 registers for the periphery. Data is transferred for each half unit separately via a slow control interface. Readout happens as a stream of bytes and is sequential for each region. It is possible, however, to exclude single regions from readout, which is important for the case where one of them is not functional, which would prohibit readout of the entire HU. Due to bandwidth limitations of the test system each region is assigned a maximum packet size of 2 MiB for readout over the long edge. For the firsts tests, readout and powering will solely be done via the long edge, allowing for the simplest power distribution scheme and higher bandwidth.

2.4.3 MOSS Experimental Setup

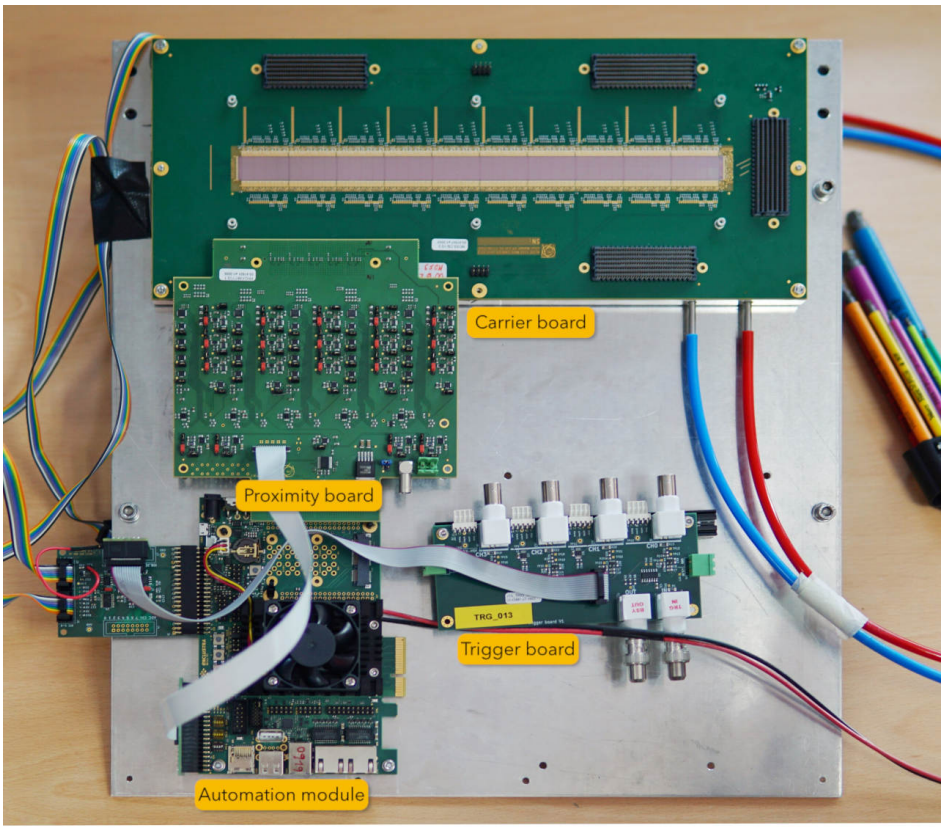


Figure 2.16: MOSS sensor on top of a carrier board, connected to a proximity card and an automation module. A trigger board is also connected supplying external trigger inputs which is used in conjunction with a scintillator trigger system during testbeam campaigns.

The MOSS test system consists of the sensor hosted on a carrier board, which features five individual 560-pin connectors along its perimeter for readout. Each slot connects to a proximity card, which itself is steered by an automation module (see Figure 2.16). Four of the five interfaces serve for the readout of the long edge, and therefore can only read out five of the HUs at once, while the side interface can read out the entire MOSS sensor at once over

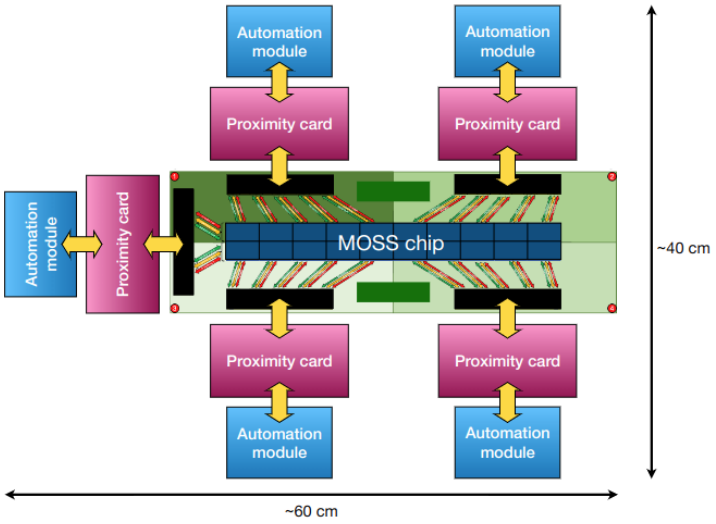


Figure 2.17: Concept for the test system.

the short edge. So far, only the readout over the long edge has been tested, such that in a full-readout setting, there are a total of eight boards (four proximity-, and four automation boards) connected at the same time. While reading out all units at once is technically possible and has been tested in the laboratory, due to the sheer size of the sensor, only one of the interfaces is used during a standard beam test, to keep the size of the setup manageable and accessible. A conceptual illustration of the full test system is shown in Figure 2.17.

2.5 The BabyMOSS test system

Since fitting a maximum of six individual MOSS onto a circular wafer leaves a lot the wafer surface area unused, both its top the bottom sections are utilised for the production of a smaller scale test system – the *BabyMOSS*. In this way, for each six MOSS in production, 23 BabyMOSS are also fabricated, which can be used to study basic functionality and performance of the individual regions of the chip. Several institutes outside of CERN are involved in this effort, and participate in a wide research programme consisting of (but not limited to) power and readout tests, efficiency and noise studies, irradiation studies, etc. Since both MOSS and BabyMOSS carry the same design architecture and analog front-end.

2.5.1 BabyMOSS Experimental Setup

While the MOSS is operated within its own DAQ infrastructure, an important advantage of the BabyMOSS is its ability to be operated with the same DAQ board as the APTS. Aside from its portability, this makes BabyMOSS the perfect prototype to be distributed amongst all the various institutes outside of CERN, which regularly participate in and contribute to the ITS3 research and development efforts. Figure 2.18 shows the BabyMOSS test system. The leftmost component is the BabyMOSS carrier card. It interfaces the sensor, and contains four

negative temperature coefficient thermistor (NTC) temperature sensors[8], situated close to the BabyMOSS. The middle component is the raiser board. Its purpose is to convert supply and steering voltage levels and bias currents from the DAQ board to the BabyMOSS standard. It also contains test points for the analog and digital domain on the chip, that can be used to supply voltage to the NTC. Finally, on the right side, the same DAQ-board as used for the APTS is connected.

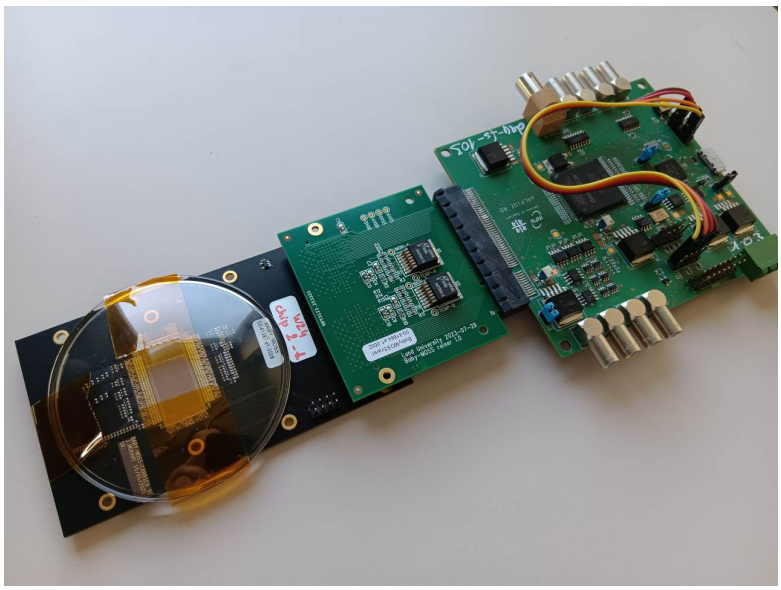


Figure 2.18: BabyMOSS test system featuring (from left to right) the BabyMOSS carrier card interfacing the sensor, a raiser board, and a DAQ-board.

Sensor tests performed with this test system include, but are not limited to: Fake-hit rate tests, threshold tests, single-event effect studies and irradiation studies. More on these tests can be found in section 4.

3 APTS characterization and noise studies

In the following chapter, an explanation of the basic operation and analysis procedure of the APTS is provided. The sensor performance is investigated under different conditions concerning the influence of electronic noise in the environment. There are several important steps to be performed before the data can be correctly evaluated. This includes a full gain- and energy calibration of the test system, translating arbitrary readout values into physical quantities. Both the gain- and the energy calibration are explained in more detail below.

[8] An NTC acts as a temperature dependent resistor. To measure a temperature, a reference voltage is applied to the NTC, and the current is measured. Higher temperatures reduce its resistance, resulting in higher current flow.

3.1 Gain calibration

Parameter	Min.	Typ.	Max.	Unit
Operating Temp.	-40	27	85	°C
Power Voltage AVDD		1.2		V
IBIASP		80	100	uA
IBIASN		-800	-1000	uA
IRESET	0.1	1	1	uA
IBIAS3		800	1000	uA
IBIAS4		-6	-8	mA
VRESET	200	500	800	mV

Table 3: Recommended operating conditions for the APTS

In its running state, the APTS continuously measures and stores the value of its pixel output voltage once every 250 ns. When an ionizing particle deposits enough energy in the epitaxial layer of the sensor, the collected charge overcomes the user-defined threshold and a snapshot of 200 time frames of the signal, (corresponding to 50 µs) will be stored inside of a multi-event buffer, where it can then finally be read out via USB. At this time, the signal amplitude is

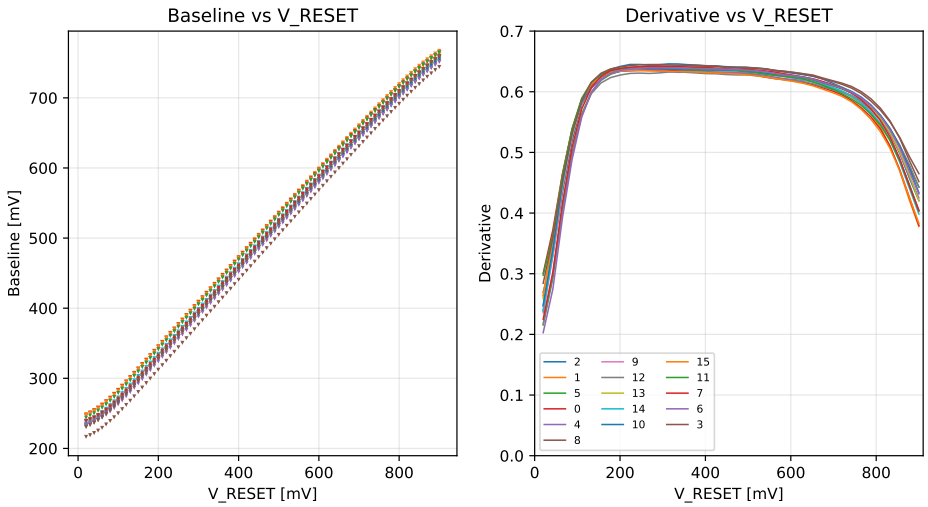


Figure 3.1: Gain calibration plots for all 16 pixels: Mapping the VRESET parameter in DAC unit to the V_{reset} voltage in mV (left), and the function derivative (right), which helps to determine the linear regime.

sampled in so called *DAC units*, providing a partly discretised approximation of the real pixel voltage. This unit can take values from 0 to $2^{16} - 1$ (16-Bit), which covers the entire dynamic range of the sensor. To translate it into a physical quantity (i.e. voltage), a *gain calibration* of

the sensor needs to be performed. During a gain calibration scan, the source voltage on the readout transistor M0 (see Figure 2.10) is repeatedly measured while the VRESET parameter is steadily increased. VRESET determines the baseline voltage to which the pixel will return to after charge injection. The result is then used to convert from DAC to mV. Around the nominal working point (see Table 3) the relation between the baseline voltage and VRESET is approximately linear, making it possible to convert between them with a single calibration factor. Only in this linear regime, it is ensured that the calibration factor can accurately describe the gain, and the sensor should only be operated here, otherwise the error of the energy calibration could increase significantly.

An example gain calibration curve is shown in Figure 3.1. Not only is the gain calibration necessary to quantify the signal, but it also gives an insight on sensor-to-sensor and pixel-to-pixel variation, which can arise from slight production differences or pixel damage.

3.2 Energy calibration

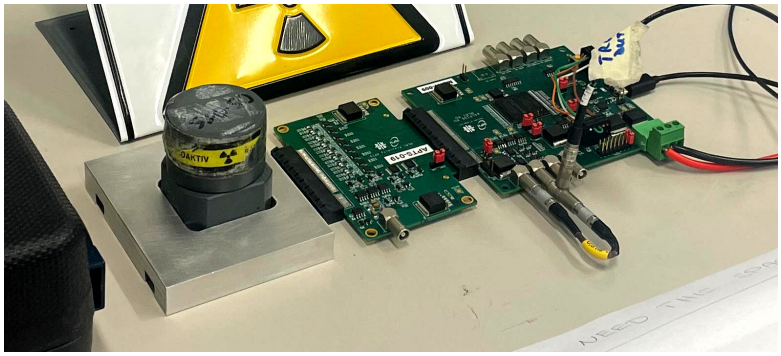


Figure 3.2: Experimental setup of an Fe-55 measurement for the energy calibration of the APTS.

For the final calibration of the APTS, the pixel signal amplitude is related to the energy deposit in the epitaxial layer in an energy calibration. For this, a reproducible particle event with a well-known energy has to be utilised. One example for this are X-Rays from the K-line of an ^{55}Fe β-decay. When ^{55}Fe decays into ^{55}Mn via the capture of one of its inner shell electrons, the vacancy is filled with an electron of its outer shells, resulting in the emission of X-Rays with characteristic energies (see Table 4). Due to the high photoelectric absorbtion coefficient of silicon for 6 keV X-rays of $\mu = 1.46 \times 10^2\,\mathrm{cm}^2/\mathrm{g}$ [25], most of these photons are fully absorbed within the sensor. The resulting energy deposit will lead to the production of around 1630 (in the case of K_α[9]) and 1800 (in the case of K_β) electron-hole pairs [18], which lies comfortably within the dynamic range of the sensor. This knowledge can be used to identify a relationship between the signal peak position and energy deposit inside the pixel. To verify

[9]The K_α line actually shows a substructure of two lines: K_{α_1} and K_{α_2}. This is due to the spin characteristics of the L-shell electrons. These lines are very similar, and are therefore often treated as mono-energetic, which is sufficient for an experiment with an energy resolution similar to the APTS

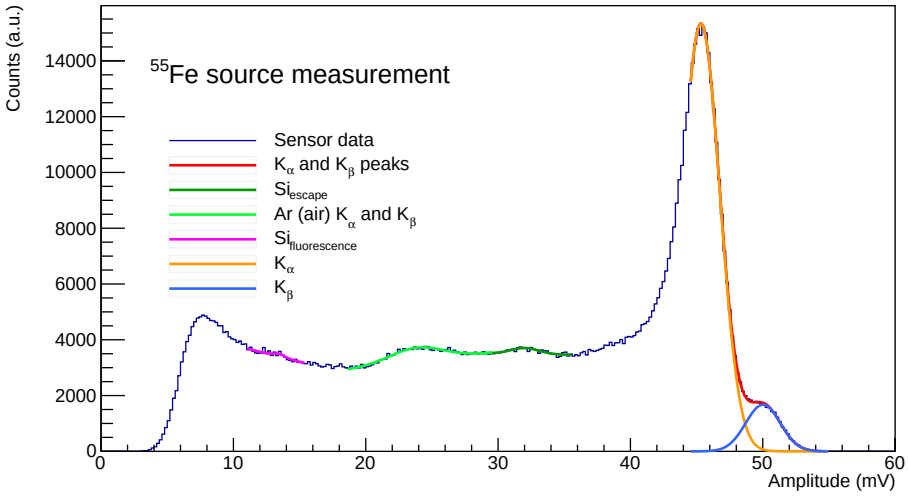


Figure 3.3: ^{55}Fe-Spectrum measured with the APTS without back-bias voltage applied. The spectrum is filled with the seed signals of the 4 central pixels. The background consists mostly from Auger electrons and bremsstrahlung.

the linearity of this relationship, the position of the silicon escape-, silicon fluorescence, and argon K_α peaks are also added to the curve. A fluorescence X-ray is emitted, when a K-shell electron of a silicon atom is liberated by the incoming photon, followed by the transition of an L-shell electron into the vacancy. If this X-ray escapes the sensor, the detected energy will decrease by 1.74 keV, resulting in the silicon escape peak at an energy of around 4.16 keV. The argon X-Rays result from photon-electron interactions with atmospheric argon.

Name	**Energy**	**Unit**
^{55}Fe K_{α_1}	5.89875 [26]	keV
^{55}Fe K_{α_2}	5.88765 [26]	keV
^{55}Fe K_{β}	6.49045 [26]	keV
^{40}Ar K_{α_1}	2.95778 [27]	keV
^{40}Ar K_{α_2}	2.95571 [27]	keV
^{28}Si Fluorescence	1.74 [28]	keV
^{28}Si Escape	4.16	keV

Table 4: Characteristic X-Rays of various elements used in the APTS energy calibration.

An example of an ^{55}Fe energy spectrum taken for the seed signal with a cluster size of up to four can be found in Figure 3.3. A cluster is defined as a three by three matrix of pixels centered around the pixel with the highest signal amplitude (the *seed* pixel), which have collected enough charge to overcome the threshold. For the analysis, only those clusters are

considered, which have a seed pixel in the center 4 pixels of the APTS matrix (in order to have access to all pixels in the cluster). The amplitudes of individual pixel signals of a cluster are then summed and included in the spectrum. All five peaks can generally be approximated with a Gaussian:

$$A \cdot \exp\left(\frac{-(x-\mu)^2}{2\sigma^2}\right) \tag{3.1}$$

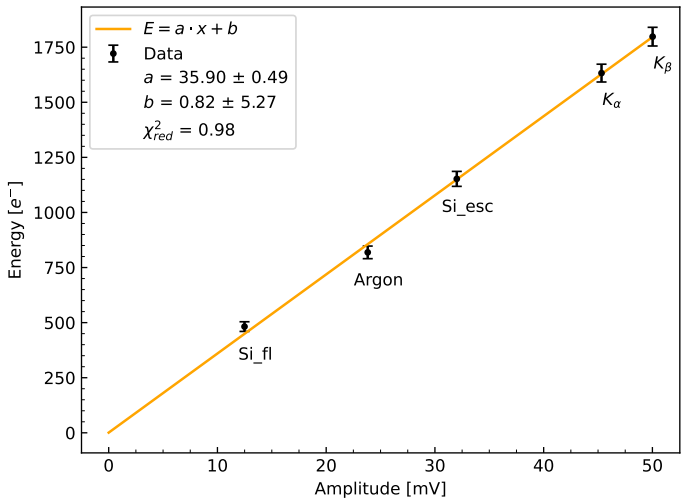


Figure 3.4: **(b)** The energy calibration of the APTS shows the amplitude of the seed pixel signal as a function of the photon energy.

However, since the peaks of K $_\alpha$ and K $_\beta$ are so close together, actually the sum of two Gaussians is used as a fit function. For the fluorescence and escape peaks, a linear polynomial is added to consider the relatively large background, which results from Bremsstrahlung and Auger electrons originating from the K or L shell:

$$A \cdot \exp\left(\frac{-(x-\mu)^2}{2\sigma^2}\right) + ax + b \tag{3.2}$$

The mean energies then contribute to the energy calibration (Figure 3.4). For each data point, a poisson error is assumed, since the number of charge carriers produced in each particle event follows a poisson distribution. The numerical fit uncertainty is negligibly small. Using this fit, an energy conversion factor can be calculated, which for the sensor operation without back-bias computes to

$$a = 35.9 \pm 0.5\,\mathrm{e}^-/\mathrm{mV}. \tag{3.3}$$

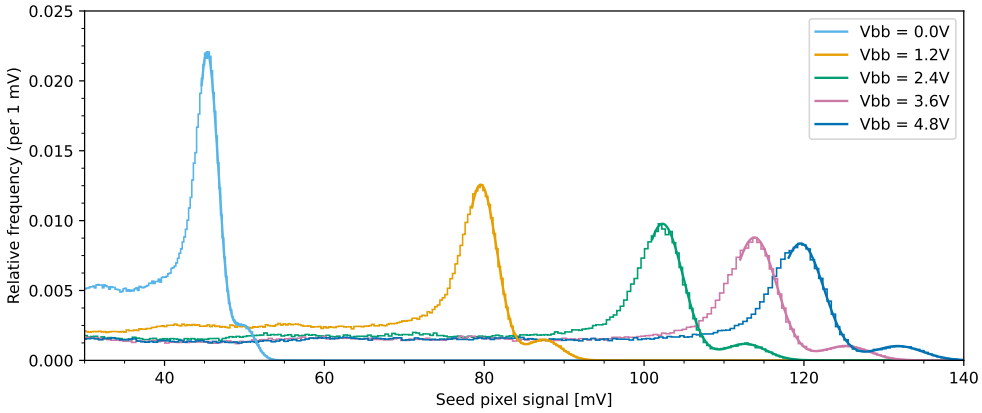


Figure 3.5: Seed signal amplitude distribution for different reverse bias voltages

Figure 3.5 shows an example for an energy calibration for different reverse bias voltages applied across the collection diode. The amplitude increases with increasing bias voltage. This is due to the increased size of the depletion region and the resulting reduced pixel input capacitance. The junction capacitance is similar to a parallel plate capacitor:

$$C = \frac{Q}{V} = \frac{n_{e^-} \cdot q_{e^-}}{V_{\text{Mn-K}_\alpha}} \tag{3.4}$$

where n_{e^-} is 1632 electrons[10], q_e^- the elementary charge and $V_{\text{Mn-K}_\alpha}$ comes from the respective fit parameters (i.e. the peak position $\mu_{\text{Mn-K}_\alpha}$) for different back-bias voltages. From this, we get a sensor capacitance for each back-bias voltage:

Back-bias voltage [V]	Capacitance [fF]	Electron conversion factor [electron/mV]
0.0	5.76	36.0
1.2	3.28	20.5
2.4	2.55	15.9
3.6	2.29	14.3
4.8	2.18	13.6

Table 5: Measured sensor capacitance for different back-bias voltage settings

Operating with a higher back-bias and therefore reduced capacitance reduces the noise level significantly, allowing lower thresholds, and an improved signal-to-noise ratio (SNR).
From the width of the K_α peak, the operational energy resolution can be obtained:

$$R_E = \frac{\text{FWHM}\,(\text{Mn-K}_\alpha)}{V_{\text{Mn-K}_\alpha}} \approx \frac{2.355\sigma}{\mu} \tag{3.5}$$

[10]Based on an electron- hole pair separation energy of 3.61 eV for silicon at 300 K [18]

For the APTS, this value computes to 7.4 % for a bias voltage of 0 V and ≈ 6 % for all voltages of 1.2 V or higher. To increase the energy resolution, a cut can be performed on the cluster size, such that only events with a cluster size of one are considered. Apart from this cut, each pixel can be evaluated individually for its energy resolution, such that pixel-to-pixel variation does not lead to an increased width, when their counts are summed up. This improves the energy resolution to 7.2 % for 0V and 5.2 % for all voltages of 1.2 V or higher. This is because the seed signal for events of cluster size of one generally have a higher SNR than the signal for events with cluster size > 1. This leads to a reduced fake-hit rate, and finally a slightly better pronounced peak in comparison.

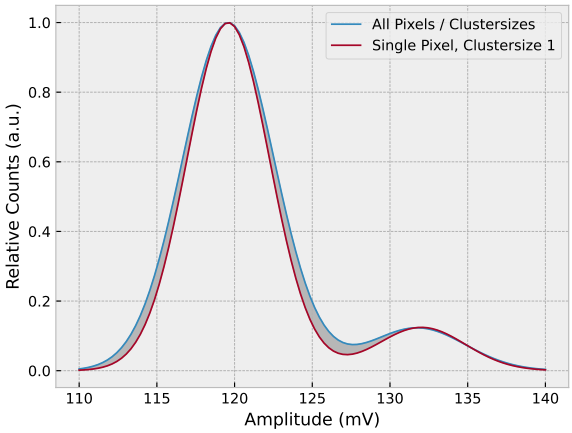


Figure 3.6: Qualitative comparison of the Mn-K_α and -K_β peaks using different analysis methods: The blue curve corresponds to the summing of all signals within a cluster, while the red curve shows the response of a single pixel, filtering all events with a cluster size higher than 1. For visual clarity, only the final fit function is shown in this graph.

The best achievable energy resolution for this sensor has been found to be 4% in [22], using a much lower reset current, a temperature-controlled environment and a high-sampling-rate oscilloscope.

3.3 Electronic noise on the APTS

One goal of this thesis is to investigate the effect of external electronic noise on the APTS performance. In order to understand the following section, a brief introduction to the analysis of electronic noise is given.

3.3.1 Electronic noise

The most important factor to quantify a detectors performance in regard to electronic noise is its signal-to-noise ratio (SNR). It describes the ability of a data acquisition system to distinguish a useful information signal suffering from undesired random disturbances. These disturbances are a result of unwanted energy from various sources, some of which is unavoidable, like thermal noise, and some of which can be attenuated, like noise stemming from electronic devices.

To calculate the SNR, both, signal and noise power must be measured at the same or equivalent points in an electronic circuit with the same bandwidth:

$$\text{SNR} = \frac{P_{\text{signal}}}{P_{\text{noise}}} \tag{3.6}$$

This notation of signal power is not the same as the conventional notion of power in physics, but one can convert between the two by taking into account the characteristic impedance of the signal transmission line. However since this quantity is unknown to us, and will cancel out for each individual measurement, it suffices to simply look at the signal power in terms of its root mean square (RMS) amplitude:

$$P_{\text{signal}} = V_{\text{RMS}}^2 \tag{3.7}$$

The SNR then equates to

$$\text{SNR} = \frac{V_{\text{RMS, Signal}}^2}{V_{\text{RMS, Noise}}^2}. \tag{3.8}$$

Since this definition is rather general, it can only describe the ratio of the RMS voltage of the desired signal to the RMS voltage of the noise, that is also present (i.e. for a known bandwidth and center frequency). If the signal can be represented by constant value (for example a maximum amplitude s), and the noise fluctuates around a mean voltage of 0, this equation then simplifies to

$$\text{SNR} = \frac{s^2}{\sigma_N^2}. \tag{3.9}$$

Signals measured with the APTS, are simply an array of values, each describing a single voltage measurement within a 250 ns time frame. The noise standard deviation is calculated from a subset of 50 time frames before the signal reaches its maximum amplitude. This subset contains values only associated with the baseline noise, and its duration is chosen as such, that it is comparable to the duration the voltage needs to return to baseline from the maximum signal amplitude under normal oprating conditions (as seen in Figure 2.11).

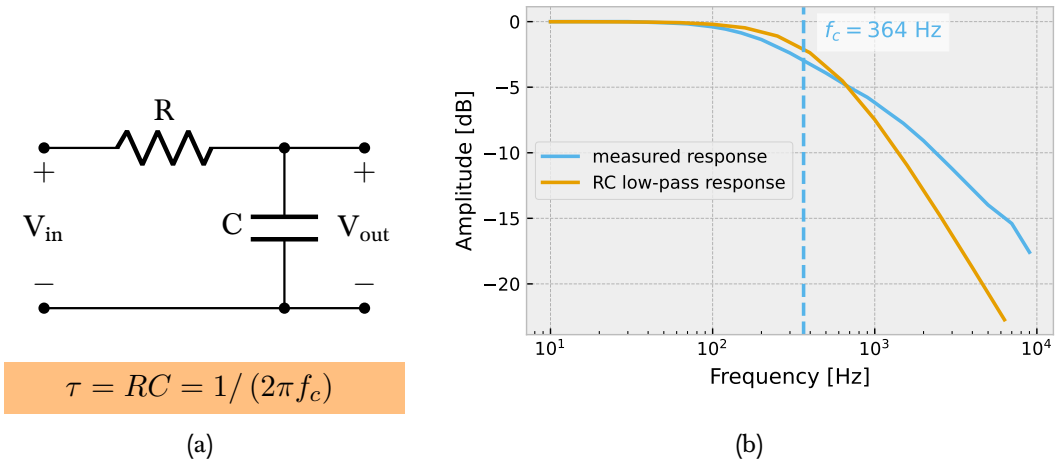


Figure 3.7: **(a)** Schematics and characterization of a simple RC low-pass filter. **(b)** Frequency Response of the capacitor network on the APTS carrier card next to the frequency response of a simple low-pass filter with the same time constant.

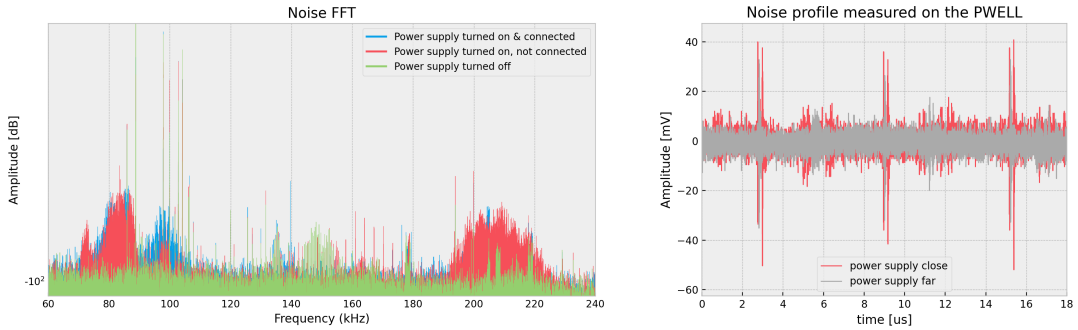
3.3.2 APTS noise attenuation

The APTS carrier board contains a network of capacitors, which decouple the analog domain of the chip from ground, while additionally acting as a low-pass filter. This has been chosen to reduce electronic noise on the signal line. A low-pass filter can be characterized by its time constant τ and cutoff frequency f_c. For a first order RC low-pass filter, the time constant and cutoff frequency are related in the following way:

$$\tau = RC = \frac{1}{2\pi f_c} \iff f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi\tau} \tag{3.10}$$

To measure the frequency response of a filter network, a constant amplitude sinusoid is applied at the input node, which is then stepped through a range of frequencies, and compared to the amplitude of the signal at the output node. For this measurement a sine signal was injected to the LEMO input connector responsible for applying V_{BB} (i.e. into the PWELL), and the amplitude has been measured at PWELL test point on the APTS carrier card. To measure the time constant of the APTS filter network, a square wave of 1 kHz was injected into the PWELL. The time constant can then simply be obtained by measuring the time the signal needs to reach $1/e = 63.2\%$ of its peak value at the test point. Both the positive and negative voltage domain has been measured, and yielded near identical results. Only signals with an amplitude of up to 100 $\mathrm{mV_{pp}}$ have been injected, in order not to create high positive currents on the PWELL, which could potentially cause irreversible damage to the pixels.

The time constant of the APTS filter is measured to be around $340.3 \pm 13.0\,\mu\mathrm{s}$. Its frequency response is slightly less steep than the frequency response of a first order RC low-pass filter with the same time constant (see Figure 3.7). The actual cutoff frequency, i.e. the frequency at which the injected signal is reduced to $-3\,\mathrm{dB} = 1/\sqrt{2}$ was measured to be around 364 Hz.



(a) (b)

Figure 3.8: **(a)** Fast Fourier-Transform of the measured PWELL-noise profile. When turning on the power supply, two new bands at ≈ 80 and 200 kHz become apparent. When connected, another band at 100 kHz appears. **(b)** Comparison of the noise profile measured on the PWELL between a best-case and a worst-case scenario.

All measurements were obtained by using the automatic measurement functionality of a Tektronix MDO3024 oscilloscope. For the frequency response, each point was measured for a few seconds, until the reading on the oscilloscope stabilised. The time constant error results from the oscilloscope's calculated standard deviation of the mean.

A direct product of the APTS filter is the chip's indifference to various noise sources in the environment. During this study, one of the biggest unavoidable noise sources has been identified to be the HAMEG power supply, providing DC power to the DAQ-board, as well as a DC voltage between 0 and 4.8 V for the reverse bias. When turned on, the power supplies' electronic components will produce a $100 - 200$ kHz switching noise, which is visible on the PWELL (see Figure 3.8). For this, the power supply does not need to be connected to the DAQ-board, but instead a big portion of the noise is actually transmitted through the air due to electromagnetic radiation being picked up by the APTS electronic lines. Since the power supply is needed to operate the APTS, its influence can not be completely avoided. However, to test the effect of the power supply noise, a best-case and a worst-case scenario have been simulated, by varying the distance between the power supply and the carrier board. Compared to the best-case (where the power supply is well isolated from the system), in the worst case (where the setup sits right next to the power supply) the noise power measured on the PWELL is increased by around 40% (See Figure 3.8 (b)).

To test whether this noise has any influence on the APTS performance, 1000 signals have been injected to the pixel front end via the injection capacitance. The resulting signals have been recorded and overlayed in an amplitude-over-time diagram. From all these samples, the baseline noise σ_N as well as the SNR is calculated and averaged over all pixels and events. Visually, there was no difference between any of the three measurements. In general, the variation between signals is an order 100 higher than the differences between the average

signal of each measurement, which is only around 0.1 mV. The consequent wave forms of this test are shown in Figure 3.9. From the 1000 signal injections we calculate the average SNR to be 1239 ± 71. Simulating a worst-case scenario, where the noisy power supply is sitting right next to the circuit board, yields a similar signal-to noise ratio of 1246 ± 72. To test the filter capabilities, a $100\,\mathrm{mV_{pp}}$ signal consisting of white noise was injected directly into the PWELL via an external function generator. This also had no significant effect on the signal, yielding a SNR of 1243 ± 71. The error on the SNR is calculated from the standard deviation of the mean of the 1000 samples.

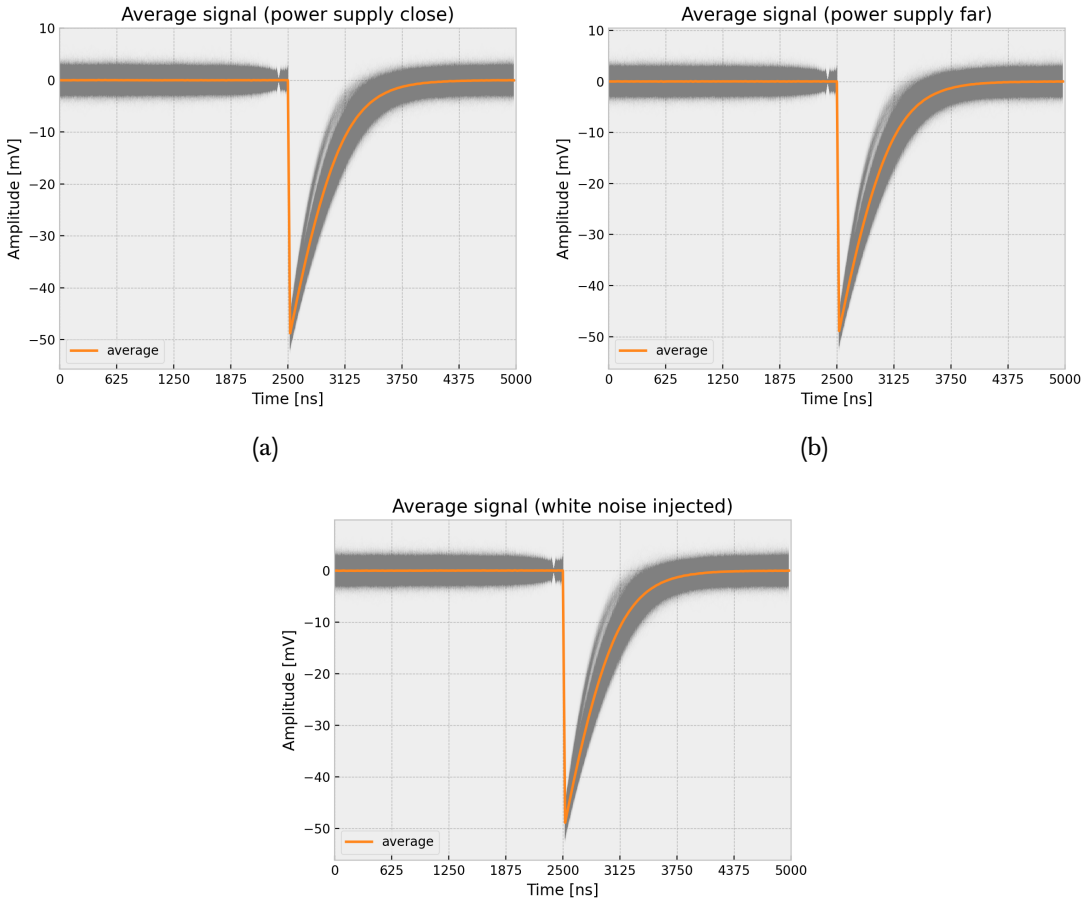


Figure 3.9: Comparison between the APTS signal injection. **(a)** APTS signal where the power supply is isolated as well as possible (minimum operation noise). **(b)** APTS position right next to the power supply, where the RF pickup is strongest. **(c)** $100\,\mathrm{mV_{pp}}$ of white noise is injected onto the PWELL.

4 MOSS and BabyMOSS studies

The following sections will describe the work performed within the scope of this thesis, with focus on the specific contributions to the MOSS and BabyMOSS characterization campaign. Any work described in the following was performed in collaboration and with guidance from CERN, and under the supervision of the ALICE ITS3 upgrade project. The results of this work have been presented at various internal meetings and parts of them will be published in the near future within technical reports, conference proceedings, or journal articles.

4.1 Laboratory tests and sensor scans

The MOSS and BabyMOSS sensors all undergo the same initial characterization process, where the chips are tested for power draw[11], functional defects, readout defects etc. Since in the scope of this thesis these scans have mainly been performed with the BabyMOSS test system, they will also be described in the following section with the BabyMOSS in mind. For the MOSS, they are equivalent with the only difference being the jkreadout system, and the scan order and complexity, since for each MOSS ten RSUs have to be characterized. The basic testing pipeline for each sensor consists of eight scans:

- A **power-on scan**, where both half units of the sensor are powered on and the reset current is established. The scan monitors three supply currents AVDD, DVDD and IOVDD for the analogue domain, the digital domain, and the readout, respectively. In case of a physical defect of the sensor, these can hint to a low-impedance path. If they overcome a threshold of 100 mA (which is enough to ensure functionality of the chip, without heating up any of the components), the sensor is turned off and the scan returns as `failed`. The sensor can then be put aside for some further investigation of the issue.

- Should the power-on scan succeed, a **register scan**, followed by a **shift register scan** are performed. These two scans write various patterns into all registers and attempt to read them back. In this way, memory defects can be identified.

- Next, a **DAC scan** follows, where the various on-chip bias DACs are tested. These voltage and current DACs, places in the periphery, steer the chip's in-pixel front-end response. The DAC scan will verify that each DAC is working by sweeping through all avaliable values. This scan is mainly done to verify the linear behaviour of the transistors, and check for any supply current anomalies.

- The first readout scans are the **digital scan** and the **analogue scan**. In both of these scans, the pixels are pulsed, and their response is read out. A digital pulse will always result in the pixel being asserted (i.e. registering a hit). For the analog pulse, a charge is injected via C_{inj}, while a strobe command is also sent, which is required to store the pixel state. The goal of the digital and analogue scans is to identify regions with readout problems, which are the most common problems across all MOSS and BabyMOSS and

[11] I.e. that the supply currents are within design specifications, and there doesn't exist a low impedance path.

during testing, this affected about 5% of all tested regions[12]. Should a region with a stuck or non-functioning readout be identified, it can simply be excluded from the following scans.

- Next, a **fake-hit rate scan** follows, where the sensor is repeatedly read out in the absensce of any external input for a set of given DACs. Any pixels that record a hit count towards the noise floor of the sensor. This scan serves as an important reference for any other measurement, so it will be properly explained in the following section (Section 4.1.1).

- Finally, a **threshold scan** is performed. This is the key test for any sensor, as the charge threshold is the parameter that allows to steer the chip's performance. The pixel threshold can be either measured for each pixel individually, or for a group of pixels forming an entire region. This scan will be explained in Section 4.1.2.

The characterization of all MOSS and BabyMOSS is, as of November 2024, still ongoing. To obtain final yield figures for the technology node and subsequent processing into final sensors, the characterization needs to be performed for both the operation without back-bias of the sensitive region, as well as with a 1.2 V back-bias voltage applied. An explanation about back-biasing is provided in Section 2.2.1.

4.1.1 Fake-hit rate scan

In a fake-hit rate scan, the sensor is set to its standard operation settings[13]. and every region is read out a predefined number of times N_{trg} (usually $N_{\text{trg}} = 100\,000$) without any external stimulus or internal pulsing. Nevertheless, a number of pixels per region will be registering a signal above threshold. Since there is no radioactive source, particle beam or similiar stimulus present in the lab during this scan and the sensor is shielded from light, these hits are attributed to noise. There are two main contributors for noise, namely *thermal noise* and so-called random telegraph noise (RTN), which is most likely an attribute of the MOS-transistors of the chip [29]. The noise can further be separated into two categories. First, there is temporal noise, which is almost completely random and varies over time. This stands in contrast to fixed-pattern noise (FPN), which is a pixel-to-pixel variation of the responsitivity of the sensor, and is usually much weaker than temporal noise [30].

The sum of all hits N_{hit} describes the fake-hit rate per pixel

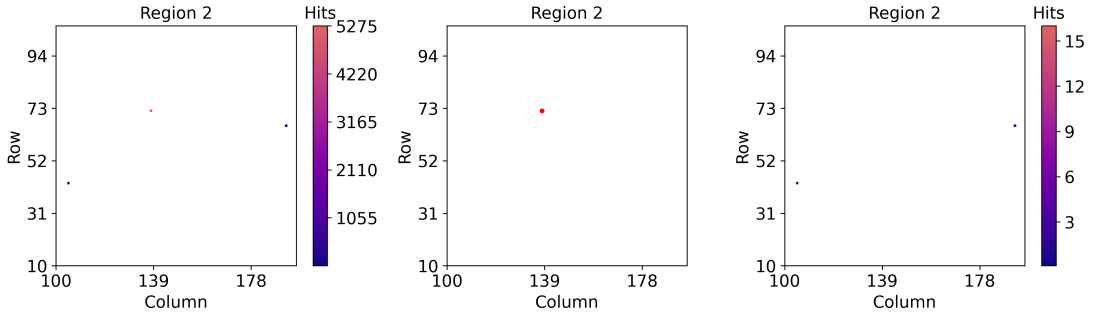
$$\text{FHR} = \frac{N_{\text{hit}}}{N_{\text{pix}} \cdot N_{\text{trg}}}, \tag{4.1}$$

where N_{pix} describes the total number of pixels of a region. A cut is then applied by masking every pixel that fires more than $N_{\text{hit}}/N_{\text{trg}} = 10^{-2}$ times. The goal of this test is to find pixels

[12] A thorough characterization of the entire sensor inventory will be published in a later report.

[13] These settings are determined by the ALICE ITS3 upgrade project, and are the same for all sensors. They are chosen such that an optimal trade-off between hit efficiency and fake-hit rate is achieved for most sensors. The standard settings used for MOSS can be found in Figure 4.23.

that frequently assert without external stimulus, and usually only in the order of 1 pixel per region turns out to be faulty. Figure 4.1 shows the results of an exemplary fake-hit rate scan, and the procedure of masking so called *hot* pixels.



(a) (b) (c)

Figure 4.1: **(a)** Fake-hit rate scan results of a BabyMOSS region, zoomed in to an area containing three fake hits. Two pixels (blue) registered hits, but not enough to reach the frequency threshold. One pixel (yellow) appears to register a lot of fake hits. **(b)** Identification of a *hot* pixel, i.e. its hit rate is higher than the fake-hit rate threshold (depicted in red). **(c)** The same hitmap, but now with pixel masking applied. Notice the scaling of the color bar, which is adjusted to the most frequent hitting pixels. The remaining pixel hits cannot be identified as being caused by a hot pixel, instead, they likely stem from random telegraph noise.

After masking, the fake-hit rate plays an important role in sensor characterization. The general ITS3 requirements specify, that the sensor application-specific integrated circuit (ASIC) must maintain a fake-hit rate of less than 10^{-6} (see Table 1). To decrease the fake-hit rate, the sensor settings can be tuned towards higher pixel thresholds, which has a negative effect on the hit efficiency of the chip (explained in Section 4.3). As a result, each sensor can only be operated for a limited threshold region, in which it still fulfills the requirement. This region of DAC parameters is referred to as the *operational margin*. The width of this margin is expected to decrease over the detector lifetime, due to the high particle flux in the ALICE experiment, and the resulting accumulated radiation damage on the sensors, which leads to a rise of the noise floor. A more in-depth study of the MOSS fake-hit rate can be found in Section 4.3.

4.1.2 Threshold scan

Similarly to the fake-hit rate scan, in the threshold scan, the sensor is first put to standard operational parameters. Then, a test charge is injected into all pixels by means of an injection capacitance C_{inj}. The amount of charge injected can be controlled via the DAC parameter `VPULSEH`, which controls the pulsing amplitude V_{PULSEH}

$$Q_{\text{inj}} = C_{\text{inj}} \cdot V_{\text{PULSEH}}. \tag{4.2}$$

Considering an injection capacitance of 258 aF (according to the MOSS User Manual [31]), the maximum possible injected charge is related to the supply voltage $V_{DD} = 1.2\,\text{V}$ and

corresponds to a charge of about $\approx 1932e^-$ at the highest DAC setting of 256 (8-Bit). The scan starts at VPULSEH $= 0$, corresponding to an amplitude of $V_{\text{PULSEH}} = 0\,\text{V}$. After injecting $N_{\text{inj}} = 25$ times, the next higher VPULSEH is chosen, and the injection procedure is repeated. The upper value for the injected charge is chosen as such, that the hit probability of all pixels is close to 100%. From this scan, a certain number of hits N_{hit} is obtained for every VPULSEH step and every pixel in which the injected charge overcomes the pixel threshold. If N_{hit} is plotted as a function of VPULSEH, the result is an s-curve for every pixel (see Figure 4.2), which – under the assumption of Gaussian noise – can be fitted with an error function

$$f(x) = \frac{1}{2}\left[1 + \text{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right], \tag{4.3}$$

where μ is the threshold and σ is the temporal noise of a pixel. The mean of the Gauss is slightly different for every pixel, and defines the pixel threshold in DAC. If there was no underlying noise present, the pixel threshold would be constant over time, and the s-curve would be a step function. However, the temporal noise smears this transition, and therefore the threshold is expressed as the mean of a Gauss instead.

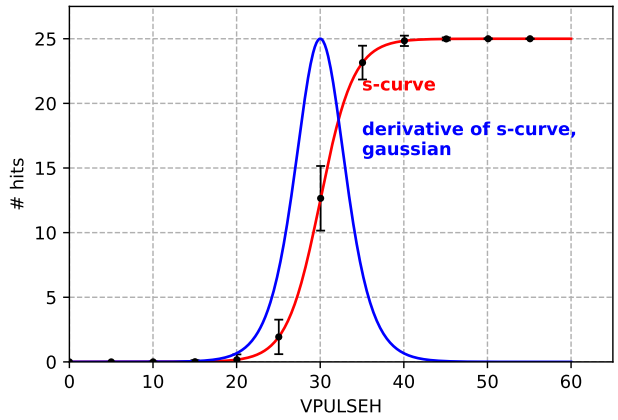


Figure 4.2: Conceptual illustration of a threshold scan. For every value of the chosen VPULSEH range DAC, 25 injections are performed. When crossing the pixel threshold, this results in a certain number of hits following an s-curve behaviour. The derivative of this curve is a Gaussian, where its mean represents the pixel threshold and its width represents the temporal noise on the pixel.

Figure 4.3 shows the distribution of pixel thresholds and noise for all regions. It can be observed, that the RMS of the threshold distribution is slightly higher than the noise, indicating for another noise source to be present. This noise is most likely FPN, leading to slight pixel-to-pixel variations. These can stem from variation of pixel size, material or interference of electric signals with the local circuitry. This difference in individual responsitivity also means, that the pixel threshold can very by as much as 20 DAC settings over the whole matrix for optimal parameter settings. The main parameter to control the pixel threshold is VCASB.

Plotting the mean μ of threshold and noise distributions from Figure 4.3 as a function of this parameter, yields the threshold response of the chip (see Figure 4.4). It can be observed, that while the threshold decreases with increasing VCASB, the noise slightly increases.

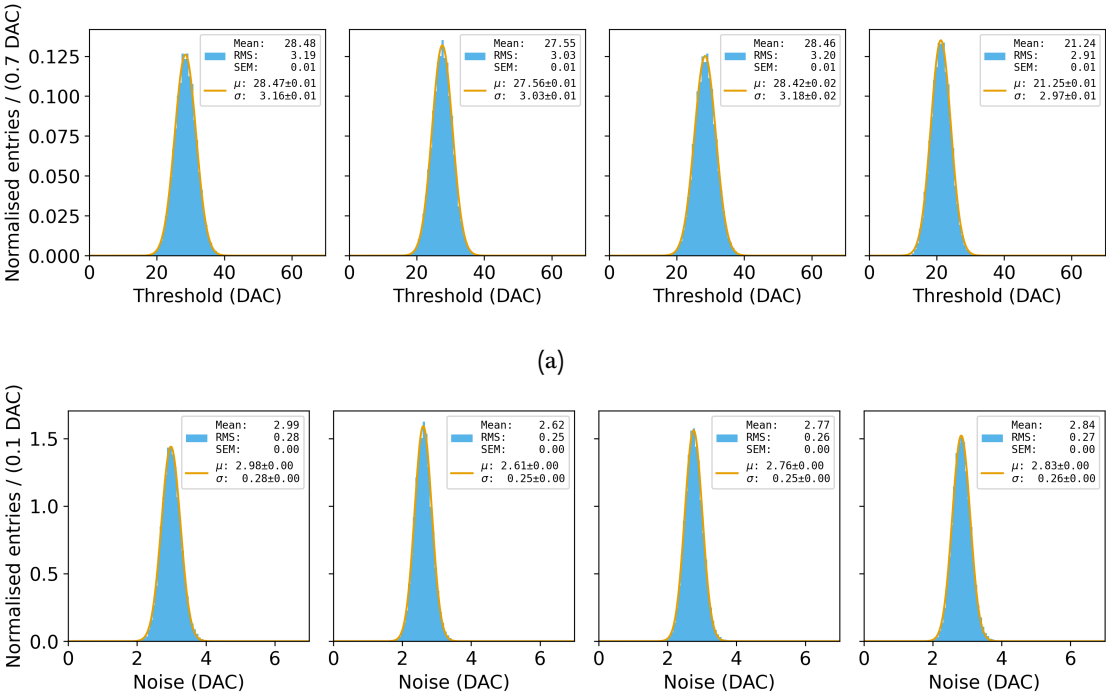


Figure 4.3: **(a)** Threshold distributions for the four bottom regions of a BabyMOSS. **(b)** Noise distributions for the four bottom regions of a BabyMOSS.

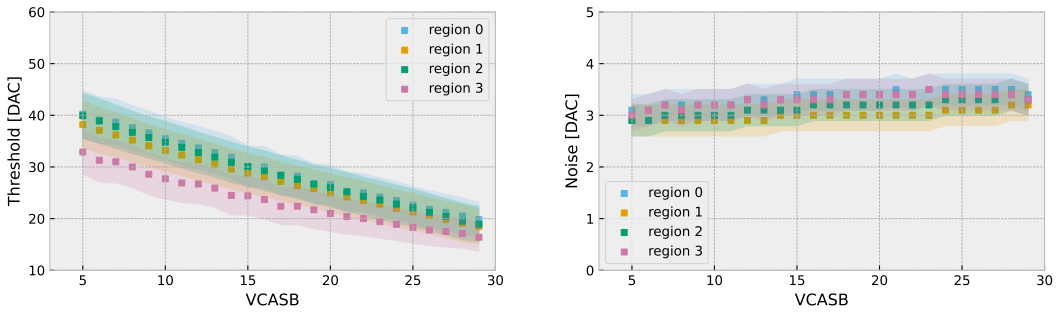


Figure 4.4: Threshold mean **(a)** and noise mean **(b)** per region for the bottom four regions of a BabyMOSS as a function of the VCASB DAC parameter (no back-bias). The shaded region represents the standard deviation of the mean, taken from Figure 4.3.

4.2 Single event effects

To qualify the sensors for usage in the ITS3, it is imperative to estimate a single event error probability, which is caused by the interaction of a single ionising particle with the silicon material or the chip circuitry in a single event effect (SEE). A SEE herein is defined as any measureable effect in a circuit caused by a single incident particle.

When the incident particle strikes a sensitive node (such as the drain of a transistor belonging to a logic element of the digital or analogue domain) in a semi-conductor device, a current pulse can be produced which can cause either soft (temporary) or hard (permanent) errors within the device. While the current pulses themselves are transient and mostly not harmful in low power devices, such as the MOSS, a hard error can be induced as a consequence. Such effects will be classified as destructive SEEs. There are several types of SEE with different levels of severity for the underlying device:

- Non-destructive effects
  - **single event upsets (SEUs)** – Bit flips altering the information stored in memory structures (discussed in detail in Section 4.2.1).
  - **single event functional interrupts (SEFIs)** – SEUs in device control logic, such as FPGAs. These potentially lead to a malfunction of the device, but can be fixed by reprogramming the sensor.
  - **single event transients (SETs)** – A disruptive voltage or current pulse, that can propagate through the circuit and cause a disturbance in the output signal. This can not be properly mitigated, as SETs are very hard to identify, possibly resulting in a fake-hit or the suppression of a real hit in a digital pixel sensor. Furthermore, modern submicron CMOS technologies generally seem to be more resistant to this type of error, due to the very thin gate oxide layer of the integrated transistors [32].
- Destructive effects
  - **single event burnouts (SEBs)** – A high instantaneous current which causes a junction breakdown. This affects mainly high-power MOS transistors, since the breakdown process is based on the heating (or melting) of material, which requires high currents.
  - **single event gate ruptures (SEGRs)** – A conduction path through the gate oxide of a MOSFET transistor. Like in the case of SEBs, this phenomenon occurs mainly in high-power transistors [33].
  - **single event latchups (SELs)** – The creation of a low-impedance path between the power supply rails of a MOSFET circuit (discussed in detail in Section 4.2.4). This is only a ***potentially*** destructive effect, because it can lead to the destruction of the component due to overcurrent, and therefore overheating, if the effect is not treated quickly. This outcome, however, is very unlikely for low power devices such

as the MOSS chip, because the supply currents are rather low. A power-cycle[14] resets the device and re-establishes proper functioning in a defined state.

Since the MOSS circuitry contains only low-power transistors, and SET are nearly impossible to mitigate, only SELs and SEUs have been studied during the characterisation of MOSS.

4.2.1 Single event upsets (SEUs)

In an upset process, an incident particle (usually a highly charged ion or low energy proton) strikes the sensitive location in an SRAM memory cell. In this kind of memory (as illustrated in Figure 2.7), transistors $M_1 - M_4$ form a dual inverter structure. If $\overline{Q}$ is a logic 1, its M_1 transistor is in an off-state. If the ionising particle hits the drain junction (Figure 4.5) a current transient is created from the collection of the generated charge carriers. This transient generally has a quick initial rise, followed by a slower, sustained current [34]. In an attempt to balance this current, the restoring transistor (in this case M_2) provides current to $M1$, causing a voltage drop, that can flip the inverter state. If the time it takes the struck node to

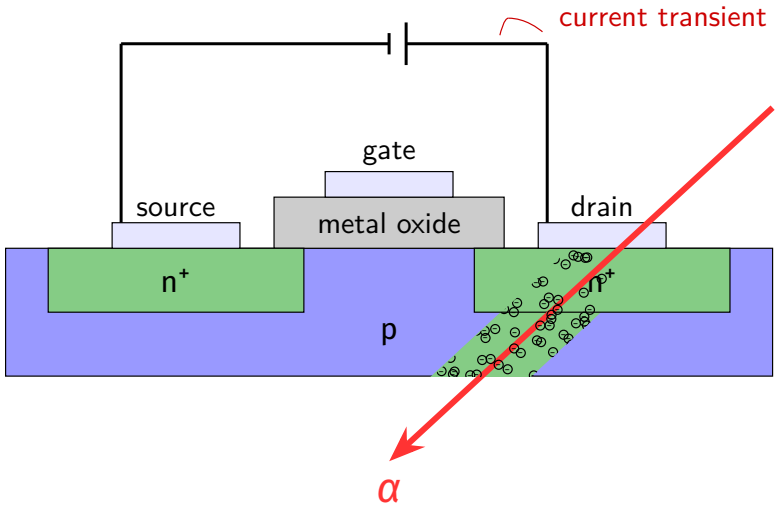


Figure 4.5: **(a)** Conceptual illustration of a single NMOS transistor being struck by an ionizing particle. Along its path, the particle liberates electron-hole pairs from the silicon, which causes a current transient.

recover is shorter than the time the restoring transistor needs to fall below its critical voltage, the system will preserve its logic state. However, if the transient persists long enough, the voltage drop on the restoring transistor will cause the memory cell to flip. The next time it is read out, the information contained within has been altered. The SEU sensitivity of a device is quantified as a cross section per bit (σ/bit) and can be calculated as follows:

[14] A power-cycle describes the process of shutting of the power to the device, before turning it back on again

$$\sigma = \frac{N_{\text{SEU}}}{\Phi \cdot \#_{\text{bits}}}, \quad [\sigma] = \text{cm}^2/\text{bit} \tag{4.4}$$

where N_{SEU} is the number of detected SEUs in a given time interval, Φ the particle fluence over that interval in $1/\text{cm}^2$, and $\#_{\text{bits}}$ the number of bits in the memory block. SEUs are caused by charged particles directly, or by charged collision products resulting from the interaction of an incoming particle with a nearby atom. They typically happen in SRAM cells and the cross section per bit is strongly dependent on the technology node and layout of the memory cell. Smaller architecture nodes are generally less susceptible to SEUs due to the reduced node volume. To avoid negative effects resulting from SEUs, a common method is to implement multiply redundant memory, where information is stored several times to detect and correct bit flips. However, the BabyMOSS chip does not feature any redundancy, as it is a prototyping chip, and the effects of SEU are purposefully studied.

4.2.2 The Cyclotron U-120M at the NPI of CAS

To provide proton beams for causing SEUs, the studies have been conducted at the U-120M cyclotron. Since the expected SEU cross section is very small, a high flux of protons is required to see sufficient occurences in a reasonable time frame. The U-120M cyclotron at the

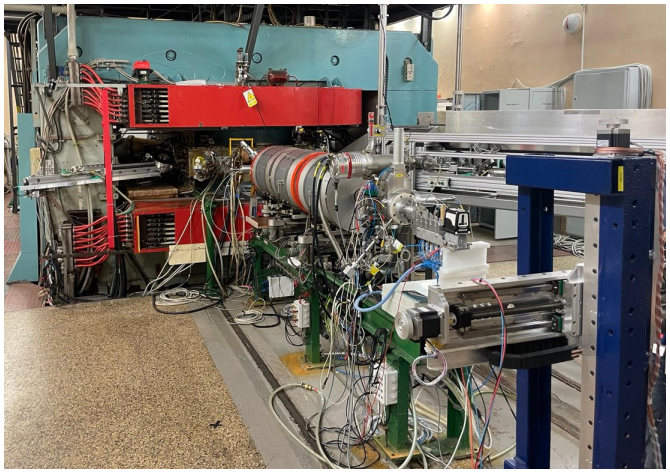


Figure 4.6: The U-120M cyclotron target station

Nuclear Physics Institute of the Czech Academy of Sciences is a warm magnet, multi-particle, isochronous cyclotron[15], which provides beams of accelerated ions with a mass-to-charge-ratio A/Z of 2 or less. It was commissioned in 1977 and received its most recent upgrade in 2022. It can reach proton energies of up to 40 MeV with very high currents of over 200 µA ($\approx 1.25 \times 10^{15}$/s) [35].

[15] A type of cyclotron, which alters its magnetic field during acceleration to account for the increase in the effective mass of relativistic particles

The cyclotron accelerates either negatively or positively charged ions and has been used many times during various ALICE ITS R&D campaigns for SEE- and irradiation studies [36]. Due to the high radiation level in the experimental area, stray particles, or particles that come from activation of the irradiated material could potentially affect high-fidelity electronic circuits, like power supplies or readout electronics. To remove any danger for laboratory equipment, the facility features a small bunker below the cyclotron hall. A little hole in the ground is used to route cables from the test setup down to the shielded electronic devices. In the center of the U-120M lies a Penning Ionization Gauge (PIG) ion source. It consists of two cathodes sitting on a very high potential (several tens of kV), and one anode in between. A magnetic field is applied in parallel to the beam direction. Via discharge, a plasma is formed between the anode and the cathodes, and the sputtered off components of the cathodes are ionised by the fast moving electrons within the plasma. The ions are accelerated towards an extractor cone, where they typically exit the source at around 30 keV, before they are injected into the cyclotron via an axial injection system [37]. Afterwards they are accelerated within the cyclotron plane up to the desired energy of around 30 MeV. The extraction of the beam depends on the charge of the accelerated ions. For positively charged ions, it is based on a system of electrostatic deflectors, which have to be preinstalled and cannot be changed afterwards, so that the operating mode is fixed. For negatively charged ions, the extraction is done via a carbon stripping foil. It strips most of the ions of their two valence electrons, after which the positively charged products are directed through a 3 m long beam pipe through the cyclotron hall. Finally, the beam exits the pipe through an aluminium exit window and is directed onto the sample (see Figure 4.7). Usually, studies performed within the scope of the ALICE ITS upgrade project are carried out using the negative mode [36]. For the BabyMOSS studies, proton energies of 28 MeV and 30 MeV were chosen with a particle flux of 4×10^8 to 4×10^9 protons/s, which is high enough to observe an SEU every few seconds[16].

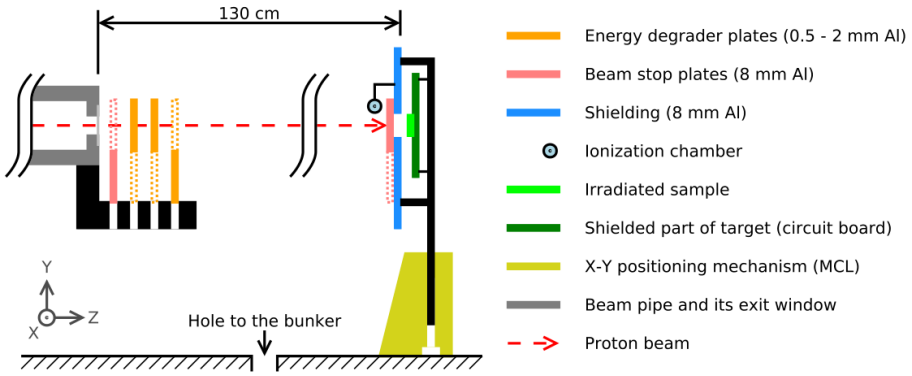


Figure 4.7: Sketch of the beam route through the extraction path. The sample, as well as the ionization chamber and the beam plates are height-adjustable

[16]The reason to tune the beam this way, is that duplicate SEUs (i.e. the same bit flipping multiple times) need to be avoided, since it would bias the measurement.

4.2.3 Single event upset (SEU) studies

The BabyMOSS setup was placed behind the aluminium shielding shown in Figure 4.7. A collimator ensures that the entire sensor is irradiated by the homogeneous profile of the beam, which has a width of $\sigma_{\text{profile}} = 22\,\text{mm}$, while the raiser- and DAQ board are shielded. In order to induce SEUs on the chip with a sufficiently high frequency to get high statistics, a high proton flux is required. During irradiation, the memory of the chip has to be monitored continuously. For this, a pattern was programmed into all of the registers of the vertical row steering block, which is the memory responsible for encoding the pixel address. This memory is positioned in between the four pixel regions and contains one bit for each row of the MOSS – this means for every top region there are 256 bits, while for each bottom region there are 320 bits. Since the collimator covers the borders of the chip slightly, the last of the four memory blocks was not exposed to the beam, and is excluded from analysis. Additionally, the vertical dimensions of the row steering block are $11.63\,\text{mm}$, while the collimator window height is only $10\,\text{mm}$, which is accounted for by multiplying the number of available bits by a shield ratio constant $R_{\text{shield}} = \frac{10\,\text{mm}}{11.63\,\text{mm}} \approx 0.86$. This reduces the final number of monitored bits to

$$3 \cdot (N_{\text{top}} + N_{\text{bot}}) \cdot R_{\text{shield}} = 1486\,\text{bits}. \tag{4.5}$$

Into these bits, a static pattern of only zeros or ones was programmed, and then monitored for the duration of the measurement. Using two different patterns makes it possible to test the SEU sensitivity for asymmetry, i.e. if there is a difference whether the bit flips from zero to one, or from one to zero. The method for testing was as follows:

- The sensor is turned on, programmed, and a monitoring script is run, which reads the sensor memory in a given interval, and reports on any differences in between each read cycle.
- First, the linear behaviour of the measurement is confirmed, by measuring the SEU frequency as a function of the beam flux. It is expected, that the frequency of SEUs increases linearly with the beam flux. Any deviation from this behaviour would indicate that there are underlying systematic errors in the measurement, such as saturation effects, charge collection or thermal effects, or radiation induced damage, etc.
- Afterwards, the beam current is then tuned until a SEU is measured every few seconds. This is because double bit-flips in between measurements should be avoided, which could occur at high rates and bias the measurement.
- The measurement is then repeated for different beam fluxes. The duration of each measurement is chosen, such that the statistics within each measurement are approximately the same (corresponding to a particle fluence of approximately $1 \times 10^{12}\,/\text{cm}^2$).
- Since they follow a Poisson distribution, all measurement points have been assigned a $\sqrt{N}$ uncertainty on their value. The uncertainty of the flux and time measurements are negligibly small compared to the $\sqrt{N}$ uncertainty.

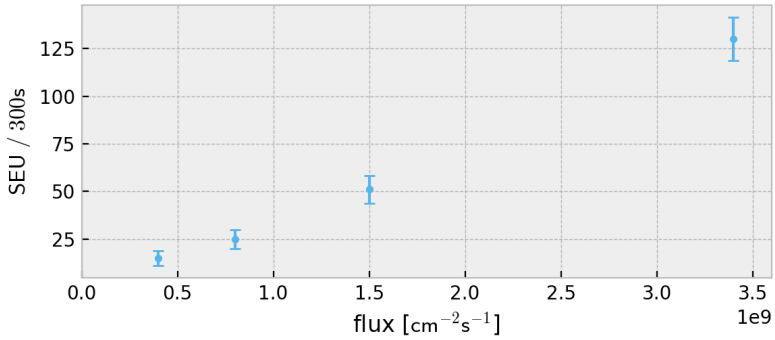


Figure 4.8: **(a)** SEU frequency as a function of the beam flux used to qualitatively verify the linearity of this relationship.

The SEU frequency as a function of the beam flux is confirmed to be linear, as shown in Figure 4.8. Figure 4.9 shows the SEU cross section as a function of the beam flux. For the lowest beam flux value of 4×10^8 cm^{-2}s^{-1}, it is required to measure for a longer time (with respect to higher beam fluxes) to get sufficient statistics. Due to time constraints, this measurement was not repeated with the second memory pattern and is excluded from the asymmetry study. The other values at higher proton flux clearly indicate, that there is no underlying asymmetry in the mechanism of the bitflip. This is to be expected, as SRAM memory cells are constructed symmetrically regarding their logic state (see Figure 2.7). Furthermore, the cross section does not show an obvious dependence on the beam flux.

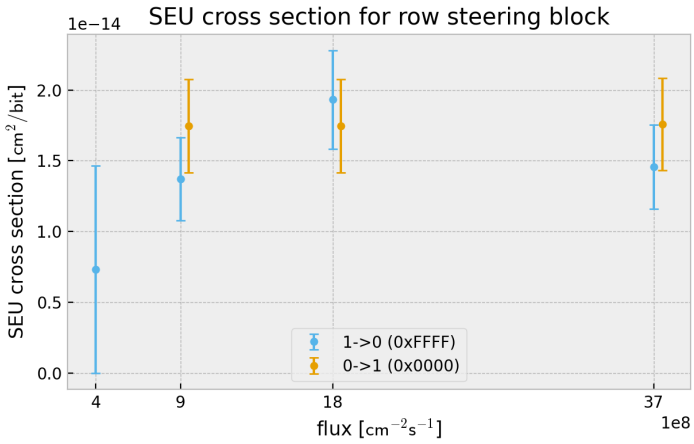


Figure 4.9: SEU cross section as a function of the beam flux, investigating asymmetry in bitflip direction. The blue points show the cross section for bitflips from one to zero, while the orange points show the cross section for bitflips from zero to one. The brackets in the legend contain the memory pattern, which was programmed into the row steering memory, which is either all ones or all zeros. The large error on the measurement during the lowest flux setting stems from the rather low statistics of that measurement.

The general value for the SEU cross section seems to be in the order of $1 \times 10^{-14}\,\mathrm{cm}^2/\mathrm{bit}$, which is in agreement with measurements made with dedicated memory structure chips for SEU tests. These measurements have been taken in November 2023 and have not been published, but instead served only as a qualitative reference for this campaign.

Another measurement was performed, in which the sensor is repeatedly irradiated to investigate the SEU sensitivity as a function of the total total ionising dose (TID)[17]. Figure 4.10 shows the SEU cross section as a function of the total radiation dose. It is apparent, that the general

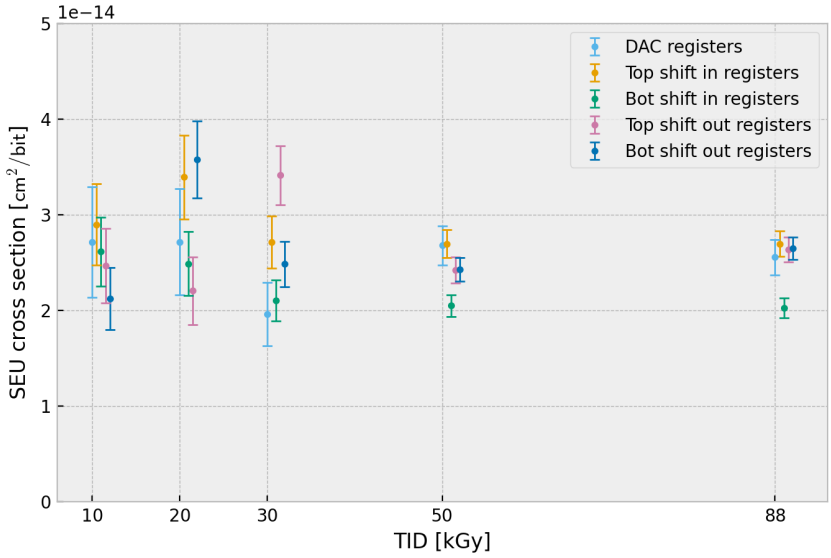


Figure 4.10: SEU cross section as a function of the TID. The relative errors gradually get smaller due to higher statistics available (stemming from higher beam flux). This measurement also shows the successful operation of the sensor at TID values which are nearly ten times higher than design specifications.

SEU sensitivity does not increase towards higher sensor irradiation. Table 1 lists the design specification regarding radiation hardness for the ITS3 to be 10 kGy. Even after irradiating the chip with 88 kGy, the sensor could still be operated. While this does not give any information about the effect of radiation damage on the sensor performance, it qualitatively proves the radiation-hardness of the chip, as the supply currents did not significantly change from the increase of radiation-induced defects in the silicon. In fact, after 100 kGy (no additional measurement was performed at this dose), the BabyMOSS was still functional. Additionally, five different registers were tested for SEU sensitivity, the DAC registers, and four different steering registers used for shifting in and out values to and from the row steering control. All registers showed similar sensitivities, which is to be expected as they are of the same digital circuit component.

[17] the total radiation dose applied to the device from ionising radiation

4.2.4 Single event latchups (SELs)

A SEL is a potentially destructive event that can affect CMOS devices. It can occur for semiconductor structures with four distinct regions, that are physically interconnected – a so called parasitic *thyristor* structure (pnpn or npnp), where there are multiple p-n-junctions (see Section 2.2.1).

Thyristors are essentially switchable diodes, allowing current to flow in one direction, but not in the other. They are usually found in high-power applications in conjunction with the use of highly robust material such as silicon carbide. However, they can also appear as parasitic transistor structures, which can be triggered electrically or as a result of the interaction of ionising radiation with semiconductor materials. Figure 4.11 illustrates a model for such a

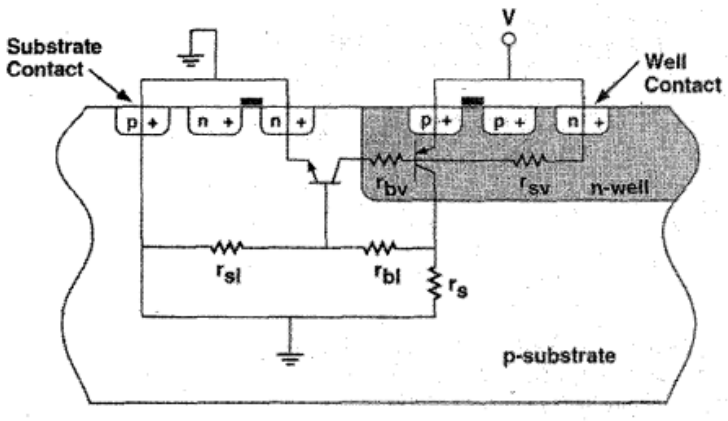


Figure 4.11: Parasitic thyristor structure responsible for SEL [38] featuring a vertical pnp-structure, where r_{bv} and r_{sv} are the distributed resistances of the n-well, as well as a lateral npn-structure, where r_{bl} and r_{sl} are the distributed resistances of the p-substrate. r_s describes their shared resistance to ground.

parasitic thyristor structure. In terms of the geometry illustrated in this Figure, a vertical pnp-transistor is formed by the drain used for the PMOS device within the n-well and p-substrate. Another npn-transistor is formed from the nwell, p-substrate and the source (or drain) of the NMOS device within the substrate. In its idle state, the thyristor is disabled – no current can flow because of the reversed biased junctions. In a SEL, a particle strikes the junction between p-substrate and n-well, and triggers a transient current, which depends on the distributed[18] resistances across the well and substrate. If it is sufficiently high, the current flow causes a voltage drop within the substrate, leading to the forward-biasing of the junction. A positive feedback loop is initiated by the current between well and substrate, which creates a stable low-impedance path. This is called a *latchup* and can lead to the overheating and destruction of connected components, but is usually easy to mitigate by monitoring

[18] A distributed resistance is the continuously distributed resistance of circuit material. This stands in contrast to the more common lumped-element model, which assumes that these values are lumped into electrical components that are joined by perfectly conducting wires.

M/Q	Ion	Energy [MeV]	Range on device [μm]	LET [MeV/(mg cm^{-2})]
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

Table 6: Available particles at the heavy-ion facility (HIF) of UCLouvain [39]. The particles not used for BabyMOSS studies are depicted in gray. M/Q is the mass-to-charge ratio of the ion.

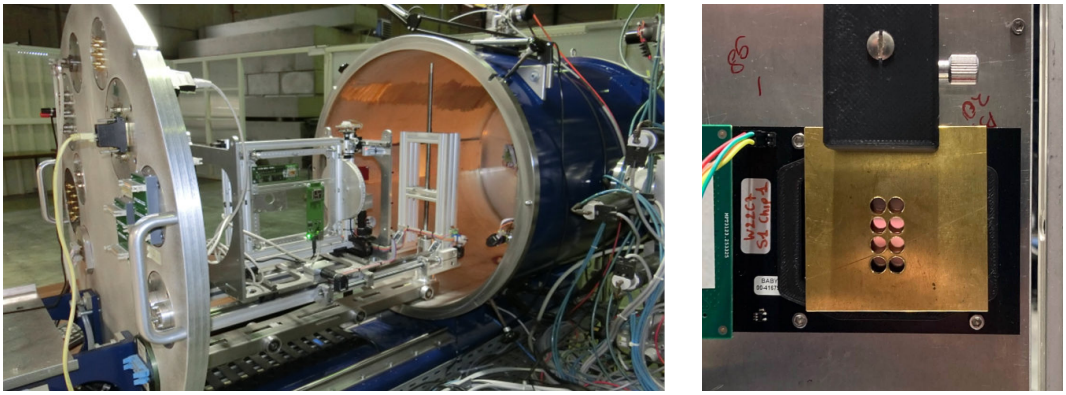
the supply current, and reducing the power supply voltage below the holding voltage (i.e. the voltage required to keep the feedback loop alive), should a latchup occur. In practice, to recover from a latchup, the system is power-cycled, which restores it to an operational state.

The SEL cross section is measured as a function of linear energy transfer (LET), which is usually expressed as a normalized unit of MeV/mg cm^{-2}. The cross section increases with higher LET values, before it reaches saturation. This is because the triggering of a latchup event depends on a critical threshold of energy deposition in the parasitic thyristor structure. At lower LET values, the energy deposition might not be sufficient to generate enough charge carriers to reach the critical threshold required to trigger a latchup, whereas higher LET particles will effectively trigger a latchup most of the time upon impacting a sensitive region. This results a sharp rise for lower LET values, before the curve flattens – in this case above $\approx 10\,\text{MeV/mg cm}^{-2}$.

4.2.5 The Heavy-Ion Facility at UCLouvain

The goal is to measure the SEL cross section as a function of the LET. For this, a variable beam of charged heavy ions is used, as the LET can be tuned by changing the ion species and, with that, its mass over charge ratio. The tests were carried out at the HIF at Université catholique de Louvain (UCLouvain), which houses the Cyclotron de Louvain-la-Neuve (CYCLONE). Built in 1972, it was the largest cyclotron in Europe at the time of construction and accelerates a variety of ions with an energy of 9.3 MeV per nucleon [39], covering a large domain of LET. The facility features a vacuum chamber, where the BabyMOSS is placed (see Figure 4.12 (a)), that provides interfaces to the outside, such as BNC, power, or USB. Inside, the sensor is irradiated by a beam with a beam diameter of 25 mm and 10% homogeneity[19]. Additionally, a matrix collimator has been designed that shields the entire sensor, leaving only eight small

[19] I.e. the intensity of the beam is locally accurate to ±10%.



(a) (b)

Figure 4.12: **(a)** The vacuum chamber at the HIF of UCLouvain [39]. **(b)** A collimator with circular openings for all eight regions to shield the periphery from the heavy-ion beam.

circular openings – one for each of the regions (see Figure 4.12 (b)). Two measurements have been conducted: A test with the collimator present at the highest LET and beam flux setting, and a second test on a variety of beam settings without the collimator. With the collimator

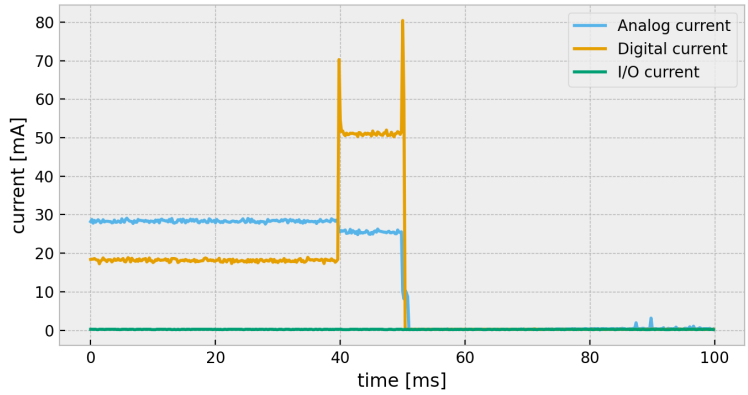


Figure 4.13: Example latchup observed in the digital domain of the BabyMOSS. At $t = 40\,\text{ms}$, the digital supply current jumps above the threshold. At $t = 50\,\text{ms}$, 10 ms after the latchup was detected, the chip automatically turns off. Because the power source is shared across all domains, the analog supply voltage slightly drops, when a latchup occurs in the digital domain.

installed, the latchup susceptibility of the pixel matrix can be tested, as the periphery registers are assumed to be completely shielded.

In case of a latchup, the supply currents will overcome a user-defined threshold, which in this case was dynamically set to be 10 mA above the initial supply current, and will remain

there until the system is power-cycled. An example latchup is illustrated in Figure 4.13. If the supply current stays above the threshold for 10 ms, the system automatically power-cycles and logs the latchup.

4.2.6 Single event latchup (SEL) studies

In the first test, the sensor is irradiated with $^{124}Xe^{35+}$ at the maximum rate[20] with the collimator installed. While SEUs continuously occurred, changing sensor settings and supply currents temporarily by flipping bits in the configuration registers, not a single latchup was observed during the 31 minute measurement period. This test is only conducted with the highest LET beam, since latchups are not expected to occur for the other ions, if they don't occur for $^{124}Xe^{35+}$. In this setting, only the pixel matrix is irradiated, while the periphery is fully shielded. This puts the limit for the SEL cross section for the sensor matrix at $\sigma_{\text{collim.}} \leq 3.58 \times 10^{-8}\,\text{cm}^2/\text{device}$. Unlike the SEU cross section, the SEL cross section is measured for the entire device instead of single bits, since a latchup will always result in a power-cycle of the whole system, no matter where it occurs.
For the second test, the collimator was removed. Similarly to the SEU studies, the test procedure is as follows:

- The sensor is turned on, programmed and put into idle state. A buffer was programmed into the firmware, to snapshot the three sensor supply currents AVDD, DVDD, and IOVDD every 200 µs.
- The measurement is started with the highest LET beam available, which is $^{124}Xe^{35+}$.
- The beam current is tuned until a latchup is measured every few seconds, since the system has to be power-cycled, which takes around 1 second, and during this time, no new latchups can be detected.
- Afterwards, the next lower LET beam setting is chosen and the measurement is repeated.
- Since the measurement points follow a Poisson distribution, they have been assigned a $\sqrt{N}$ uncertainty on their value. Like with the SEU studies, the uncertainty of the flux and time measurements are negligibly small compared to the $\sqrt{N}$ uncertainty.

Figure 4.14 shows the SEL cross section as a function of LET. As expected, there is a steep rise for LET values below $10\,\text{MeV/mg cm}^{-2}$, before the cross section saturates towards higher values, where the probability of a particle triggering a latchup upon impact on a sensitive region is close to 1.
In the final experiment, there are two contributors to sensor latchups. First, there are the collision products of the two ion beams, which consist mostly of hadrons like protons and pions, as well as light nuclei which might cause a latchup. Second, there is a small chance, that when a beam ion hits a collimator in the LHC, it will fragment into parts and exit the beam, carrying up to the total energy of the incident ion. These fragments can vary significantly

[20] $1.5 \times 10^4\,\text{ions/cm}^2\text{s}$

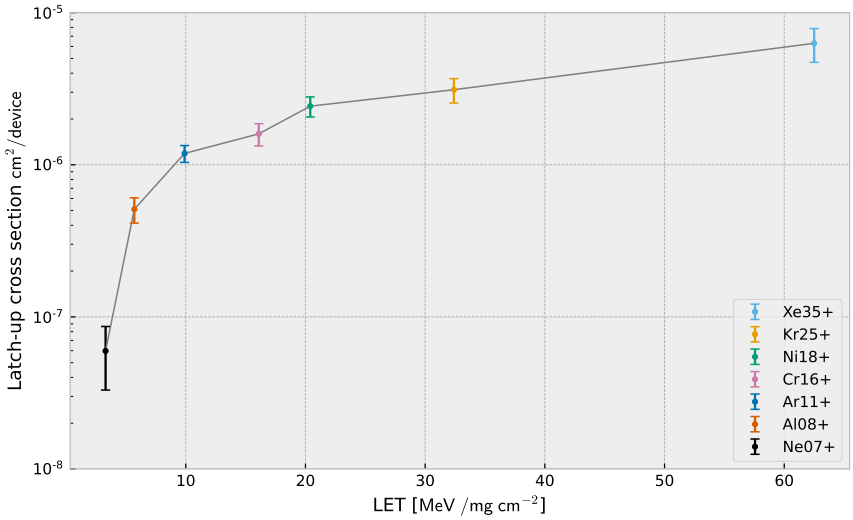


Figure 4.14: Latchup cross section as a function of linear energy transfer.

in mass and charge, but usually deposit only limited energy in thin silicon detectors. Simulations [40] have found that the maximum LET of these ions is around $9.75\,\mathrm{MeV/mg\,cm^{-2}}$. Looking back at Figure 4.14, the data point of $^{36}Ar^{11+}$ seems like a good reference point for this, as its LET is situated at $9.9\,\mathrm{MeV/mg\,cm^{-2}}$. The latchup cross section in this regime can be directly read from Figure 4.14, and has a value of $1.2 \pm 0.2 \times 10^{-6}\,\mathrm{cm^2/device}$. Since the flux of high LET ion fragments through the ITS3 is very low, this cross section is considered to be small enough in order to not cause any significant downtime for the detector.

These measured latchups have exclusively occured in the periphery (as opposed to the pixel matrix), and almost exclusively the digital domain showed signs of SEL sensitivity.

4.3 Detection efficiency of the MOSS detector

Part of the research and development campaign of the MOSS and BabyMOSS is the full characterization of all sensors from all wafers in terms of efficiency and fake-hit rate. Part of this thesis is the analysis of the efficiency and fake-hit rate of the first two splits of the MOSS sensor. Fake-hit rate scans for the BabyMOSS have been explained in Section 4.1.1. For the MOSS, the procedure is mostly the same – only the experimental setup is slightly different (see Figure 2.16). Fake-hit rate scans are usually performed right before an efficiency measurement in a temperature- and light-controlled environment. In this way, it is made sure that the same experimental conditions apply to both the scans and the measurement. The temperature is held constant by means of a cooling plate, which the sensor is mounted on. The cooling plate is actively watercooled by a minichiller. The goal is not to ensure that the measurement is performed at a specific temperature, but that the temperature during the entire measurement campaign stays constant. This is because during testing it has been found,

that the threshold can vary by as much as 0.6 DAC per degree C (M. Menzel, unpublished data from personal communication, 2024).

There are two iterations of the MOSS sensor, which are referred to as *splits*. Efficiency studies have been performed for the second MOSS split, and during the writing of this thesis, also for the first split. The first split of MOSS featured a slightly smaller gap in the pixel implant geometry in the top regions, which is similar to the design of the low dose n-type implant of the APTS (see Figure 2.9). The results of the first split efficiency and a comparison with the second split of MOSS will therefore be presented in this thesis. A full characterization of the splits combined is going to be released in a future technical design report.

To evaluate the efficiency of a detector, the sensor is exposed to a particle beam with well-known properties, replicating the conditions it would encounter in an actual experiment. During this beam test, the studied sensor, referred to as the device under test (DUT), is positioned at the center of a *beam telescope* (see Section 4.3.2). The beam telescope is an arrangement of reference sensors that have precisely known characteristics and are designed to track the beam particles with high efficiency and spatial resolution. The particle tracks are represented using mathematical models in three-dimensional space. For a given model, the track is interpolated at the position of the DUT, and a corresponding signal is searched in the pixels forming a narrow window around the track's intercept point. If the DUT detects the particle's passage at this location, the sensor is efficient. The detection efficiency can then be determined by comparing the number of efficient tracks to the total number of tracks

$$\varepsilon = \frac{k}{n}, \tag{4.6}$$

where k is the number of efficient tracks and n is the total number of tracks. The details of this procedure are discussed in the following sections.

4.3.1 The Proton Synchrotron at CERN

The Proton Synchrotron (PS) at CERN (see Figure 4.15) is mainly used as a pre-accelerator for the Super Proton Synchrotron (SPS), which itself is used for preparing particles to be injected into the even larger LHC. The PS has a circumference of 621 m and accelerates various nuclei as well as electrons and antiprotons up to 26 GeV [42]. Apart from serving as a pre-accelerator, it also provides test areas that can be used for various experiments, such as the characterisation of detector prototypes.

The PS experimental facility, located on the east side of the accelerator contains four beamlines: T8, T9, T10, and T11. It has received major upgrades during the CERN Long Shutdown 2 (LS2) (2019-2021), including complete renovations of the magnet system, beam stoppers, collimators, and beam profile monitors, allowing most parameters of the beam to be accessed and controlled remotely [43]. The beam is extracted from the PS at 24 GeV towards the exper-

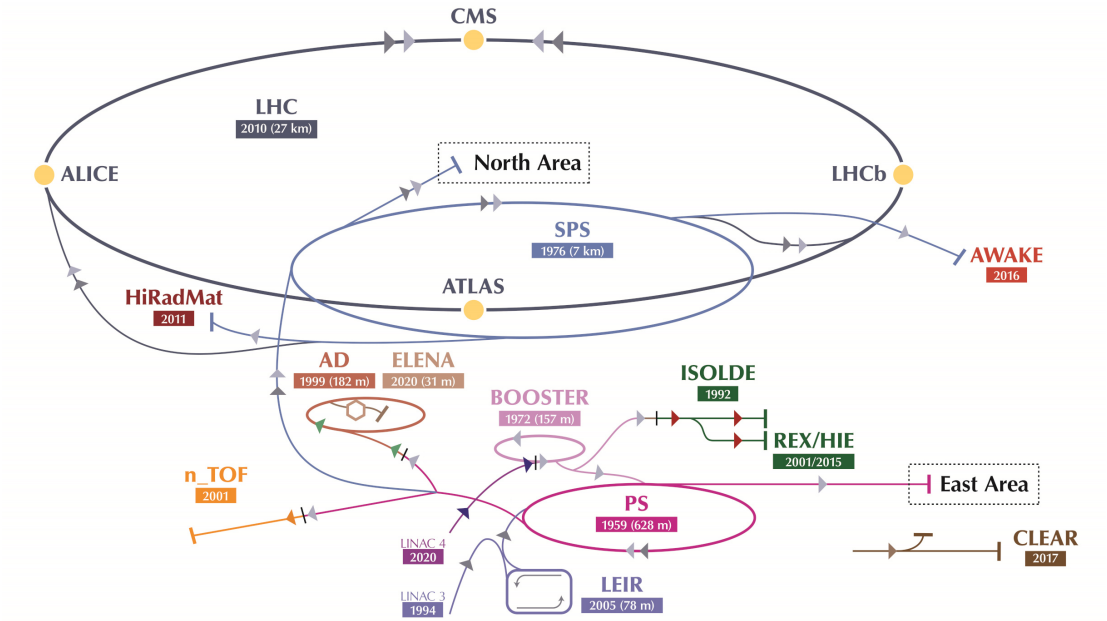


Figure 4.15: The CERN accelerator complex [41].

imental hall via the third-order resonance technique[21]. Figure 4.16 shows a schematic view of the four main beamlines. After extraction, the beam is focused and redirected via a C-shaped dipole either towards the north side (T9-T11) or towards T8, where it is again focused onto secondary targets. The beam in T10 (which is the beamline mostly used by the ALICE collaboration) is derived from target B under a slight vertical production angle in order to prevent primary protons to enter the experimental area. The non-interacting protons are dumped below the hall in a primary beam dump. Secondary particles are allowed to pass through a set of beam collimators, which define the central momentum and vertical and horizontal acceptance of the beamline. In between, lead foils are inserted to strip the beam of electrons,

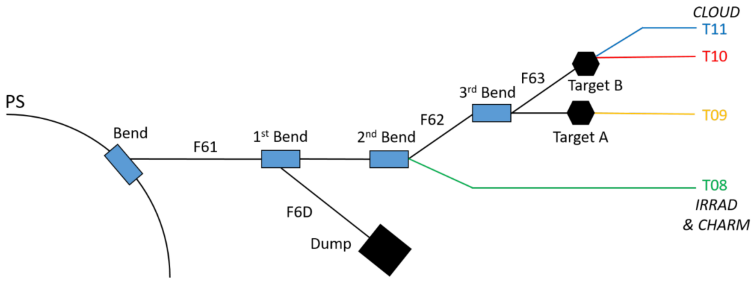


Figure 4.16: Schematic view of the layout in the PS experimental facility after renovation [43].

[21]The third order resonance technique is a beam extraction technique relying on the oscillation of a particle bunch around the beam trajectory. If the beam is tuned such that this oscillation becomes resonant, the bunch exits the beam in a spill

leaving an up to 99% pure hadron beam. A final dipole together with a focussing structure is then used to direct the beam towards the sample. Since the PS serves multiple users, it cycles them in a programmable sequence, which is called *supercycle*. Only a fixed number of spills can be performed per supercycle.

Maximum momentum	12 GeV/c
Momentum resolution	0.7 %
Maximum # of particles per spill	10^6
Maximum # of spills per supercycle	6
Typical duration of supercycle	45.6 s

Table 7: Secondary beam parameters for the T10 experimental hall [43].

Table 7 shows the secondary beam parameters of T10. According to the supercycle duration, number of spills per supercycle, and number of particles per spill, the average particle rate per second obtained is rather low, compared to continuous beams.

In July 2024, a measurement campaign was started to thoroughly characterise the first MOSS split in terms of efficiency and fake-hit rate, using a secondary beam of 10 GeV hadrons, consisting of mostly pions, with a beam profile of $\sigma = 15$ mm.

4.3.2 Beam telescope

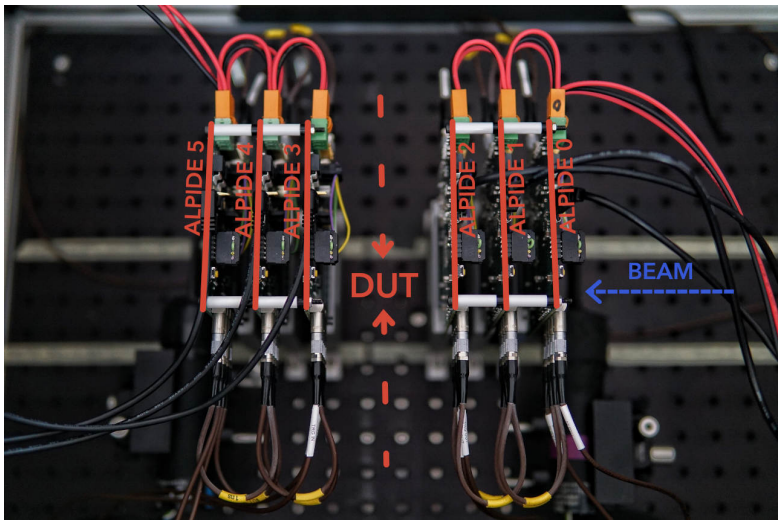


Figure 4.17: The MOSS beam telescope. Three ALPIDE sensors are placed upstream, and another three are placed downstream of the DUT. Two scintillators (not included in this image) can be situated to the left of ALPIDE 5 and right of ALPIDE 0, to serve as a coincidence trigger. The MOSS DUT is not present in the picture.

The beam telescope, seen in Figure 4.17 features six reference planes of the well-studied ALPIDE sensor [19], of which three are placed upstream, and another three downstream of the DUT. The spacing in between the first and last three layers is 2.5 cm. In the center, the MOSS sensor mounted on a cooling plate is inserted (Figure 2.16). The thick mounting board increases the spacing between the front side of the MOSS sensor and the next ALPIDE to 3.5 cm and on the backside to 4 cm (as shown schematically in Figure 4.18).

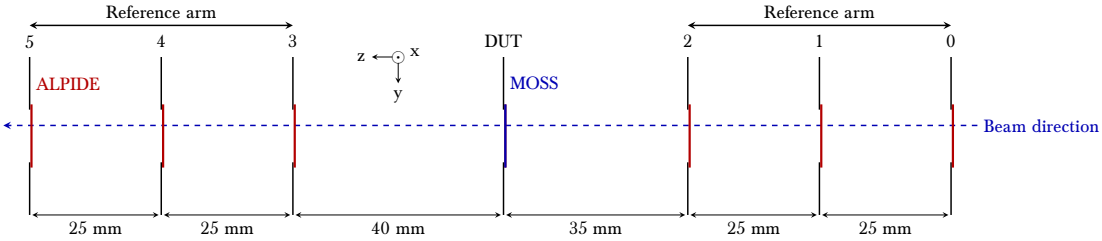
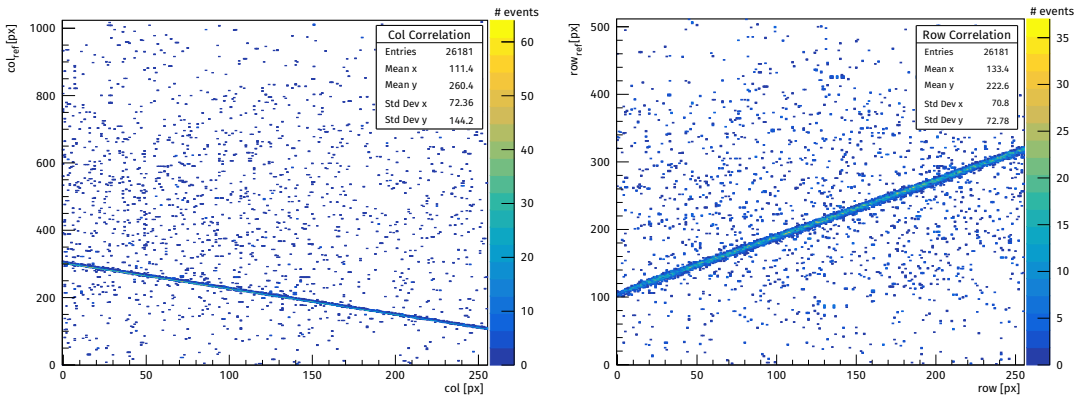


Figure 4.18: Testbeam telescope illustrated as seen in Figure 4.17.

Additionally, two scintillators have been placed upstream and downstream of the telescope. These act as a coincidence trigger. When a particle hits both scintillators, a signal is sent to a trigger board, which will then distribute a trigger signal to all DAQ-boards to read the current hit pixels. During configuration or readout the sensors will be in a BUSY state, which prevents new trigger signals from being accepted until all sensors have finished reading out the data. For every trigger, an event is created and the data is recorded in the data acquisition framework EUDAQ [44]. Each trigger will be assigned an ID and a timestamp, followed by the unprocessed detector data. All this information is written to a *raw* data file. This format is very useful, as it can sequentially be read out, making it possible to perform simple quality assurance and monitoring steps, such as visually checking if all sensors are operating as expected.

To verify data integrity and assess the crude alignment of the sensors, correlation histograms are created during monitoring. A correlation plot relates a measured coordinate of a particle hit on one detector to the coordinate on another detector. Monitoring these plots during a data taking run can help to quickly identify malfunctions of detectors, or mistakes in the configuration of the setup, such as strongly misaligned detectors. An example correlation plot is shown in Figure 4.19. In this plot, hits on the reference plane (for example ALPIDE 1) are correlated to hits on region 3 of the DUT. Two things are immediately apparent – the different size of the sensors and the flipped coordinate system. Since a MOSS region is only 5.76 mm wide, the entire range of pixels of MOSS region 3 only correlates to a small part of the pixel space of the much larger ALPIDE sensor, which measures $15 \times 30\,\mathrm{mm}^2$ (row $\times$ column). Furthermore, the plot shows the orientation of the DUT, which is rotated by 180 degrees around the y-axis. This results in a negative slope in the histogram showing the column correlation. The hits that lie far off the correlation line can be attributed to fake-hits. The row- and column correlation plots also serve as a first reference to the x- and y position of the sensor in the telescope. This, in turn, can be used to correct gross misalignment in a first step, providing better initial conditions for the alignment algorithms applied next. By



(a) (b)

Figure 4.19: **(a)** Correlation plot in the column directions between the reference plane (ALPIDE 1) with region 3 of the MOSS. Note that the MOSS sensor is rotated by 180 degrees, which is why the column correlation is inversed. **(b)** Correlation plot along the row direction between the reference plane with MOSS region 3.

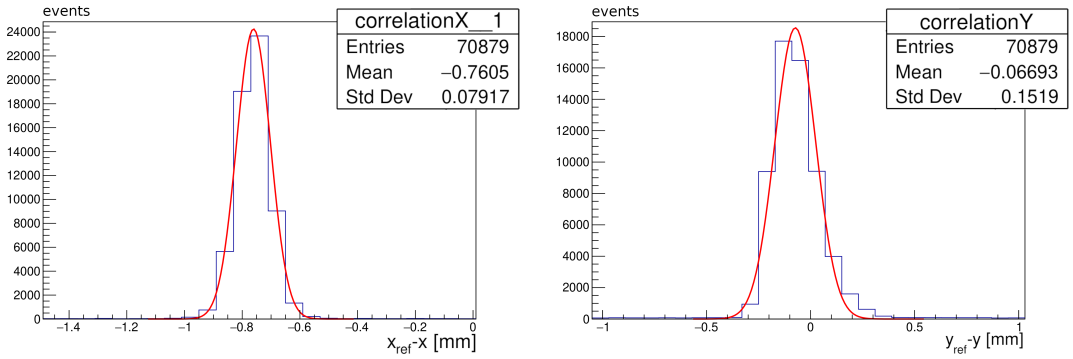
doing so, these algorithms are better seeded, and can converge more efficiently, eliminating the need to iterate over a wide range of potential alignments.

4.3.3 Testbeam data analysis

The data analysis software Corryvreckan [45] is used to decode the raw data files and perform track-based alignment using dedicated algorithms and extract parameteres of interest. The alignment step is purely virtual, as no actual moving of the detector layers is taking place, but instead, the (x,y,z)-coordinates of the data will be corrected with respect to the actual misalignment of the sensors.

The alignment consists of three steps in total: A prealignment, an alignment of the reference planes, and finally, the alignment of the four regions of the DUT. Within the first step, a **pre-alignment** is performed, in which hits from one reference plane are correlated to hits from another plane (Figure 4.19). One ALPIDE is picked as a reference detector, to which all other positions will be virtually aligned to. The correlation plots in x and y are used to identify the values of the respective x- and y-shifts. This distance is determined by a Gaussian fit on the correlation histogram. Figure 4.20 shows an example of the correlation step. All detector planes are shifted with respect to a reference plane, which in this case has been chosen to be ALPIDE 1. This serves as a first rough alignment of the x- and y-position of the detectors with respect to one another, and will be used as a foundation for further alignment steps.

In the second step, the reference planes are aligned using tracks reconstructed from clusters of hits on subsequent reference layers. This time, additionally to the x- and y-shift, a rotation



(a) (b)

Figure 4.20: **(a)** The correlation in x-direction of the reference detector plane (ALPIDE 1) and the first detector plane (ALPIDE 0). **(b)** The correlation in y-direction of the same planes. The x-axis represents a histogram of the distance between the hits on one plane to another plane. A Gaussian fit is applied to the data, and its mean is used to quantify the shifts in between planes in x- and y-direction.

around the z-axis is also introduced[22]. From corresponding hits on the the reference planes, a straight line in three dimensions is fitted for each event. The DUT will be skipped in this step, in order not to bias the analysis results. Instead, it will be aligned in the following step. To align the detector, the Millepede package is used [46]. In summary, it uses an alignment algorithm, based on the residuals (i.e. the deviations between the fitted and the measured data points) obtained from the measurement of a large number of particle tracks, meaning each track and its local parameters contribute to a global parameter set that describes the detector alignment.

To verify the alignment, the goodness of fit for each track can be calculated via

$$\chi^2 = \sum_k = \frac{\left|\mathbf{r}_k^2\right|}{\sigma_k^2}, \tag{4.7}$$

where k is equal to the number of measured points for the track. A large value of χ^2 indicates a bad fit. If the measurements are uncorrelated and normal distributed variables, the distribution of all tracks follows the probability density function f:

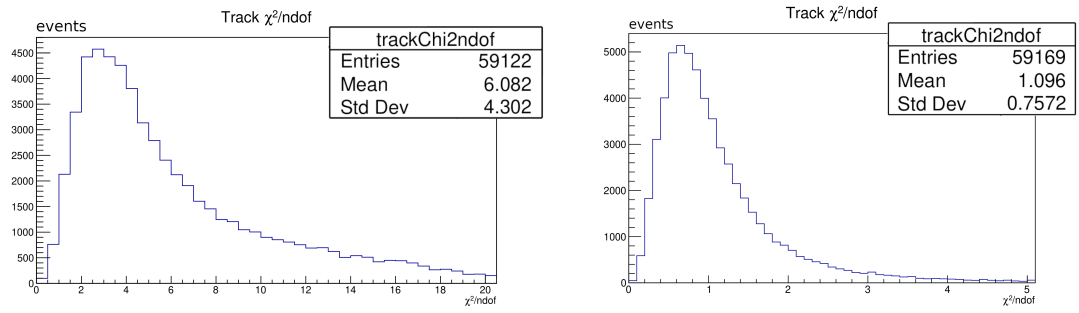
$$f\left(k, x\right) = \frac{x^{k/2-1} e^{-x/2}}{2^{k/2}\Gamma\left(\frac{k}{2}\right)}, \tag{4.8}$$

where k is the number of degrees of freedom[23] and $\Gamma(k) = \int_0^\infty x^{k-1} e^{-x} dx$ the gamma function [47]. The χ^2 distribution is often normalized to the number of degrees of freedom, which

[22] A rotation around the x- and y-axes is omitted, as the sensors are housed in a rigid frame. Therefore these rotations are small and do not contribute significantly to a shift in the pixel coordinate space.

[23] In the case of a straight line fit through a number n of planar detectors, measuring x and y coordinates, the number of degrees of freedom is $2n - 4$.

is referred to as χ^2_{red}. A good alignment is represented by a χ^2_{red} distribution peaking at 1, where the majority of tracks are optimally described by the model and the setup geometry. Figure 4.21 shows the χ^2_{red} distribution for the tracks of a single run of about 60000 events before and after the alignment process. Note that not every event has a track assigned to it.



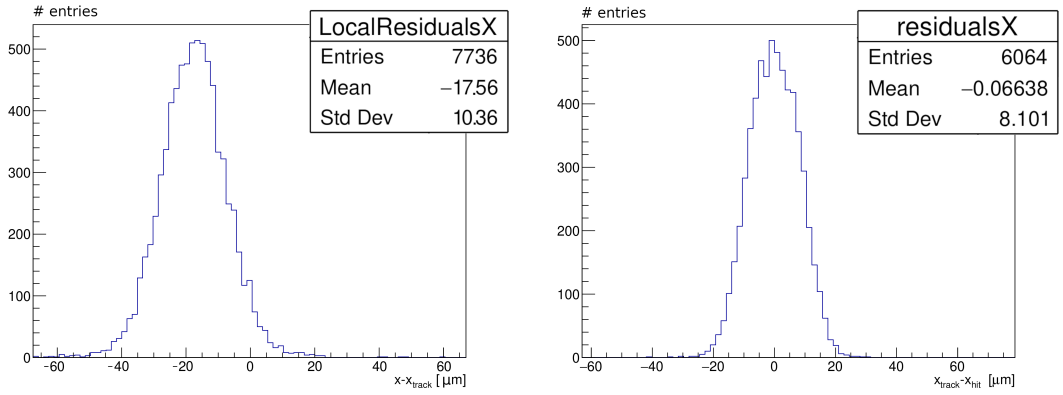
(a) (b)

Figure 4.21: The χ^2_{red} distribution of a single run **(a)** before and **(b)** after the alignment process. After aligning the detector, the distribution peaks around 1, and the tail of higher values is strongly reduced, indicating that a majority of the tracks are well described by the model. The slight discrepancy between the number of entries in both plots is due to various selection criteria given to the tracking module. In **(b)**, because of the improved alignment, more tracks actually fit those criteria.

This is due to some selection criteria, such as having only a single hit on each reference plane per track, as well as filtering out tracks with large residuals, which sometimes arise from fake hits or large angle scattering. Additionally, the cross-sectional area of the scintillator is larger than the area of the detector planes, which leads to a lot of events which have no detected hits assigned to them.

In the final step, the DUT is aligned with respect to the reference planes in a similar track-based approach. For this, the residuals on the DUT are considered. Ideally, they should be centered around 0 and gaussian shaped. The width is limited by the pixel pitch and the tracking resolution. Figure 4.22 shows the residual distribution in x-direction of one region of the DUT before and after the alignment. Before aligning the DUT, there was a clear shift in the residual, indicating a misalignment in x-direction. Furthermore, the distribution is slightly asymmetric. After aligning, this effect is much less pronounced.

After the setup has been aligned, all runs performed with the same configuration can now be analysed. Due to the large size of the MOSS, and the dimensional constraints of the testbeam telescope, only three of the 20 HUs have finally been measured: The 6th and 7th unit on the top side, referred to as `T6` and `T7`, respectively, and the 4th unit on the bottom side, referred to as `B4`. These three units serve as a reference for the entirety of the MOSS.



(a) (b)

Figure 4.22: Exemplary residual distribution for one MOSS region in x-direction **(a)** before the DUT aligment and **(b)** after the DUT alignment. Before the alignment, the residuals are shifted, which is corrected for in the alignment process.

4.3.4 MOSS detection efficiency

The detection efficiency is defined as the ratio of tracks featuring an associated signal on the DUT over the total number of reconstructed tracks. It is determined as a function of the detection threshold. The threshold is a parameter that defines the minimum amount of charge required to assert a hit on the sensor, therefore it is usually given in the unit of electrons (e^-). However, the MOSS is still in the process of being fully characterized and calibrated, so the conversion from DAC to electrons is not yet precisely known.
The reason for this is, that there is no way to access time-over-threshold (ToT) information, which is usually used to determine the conversion factor, as it was used earlier for the APTS in Section 3.2. Another way to obtain this conversion factor is to use a proof-of-principle method based on statistical strobing of the sensor. However, this method still shows a large discrepancy between the conversion factor which is obtained by the method, and the conversion factor which is expected from design parameters.
An approximation based on the injection capacitance has also been attempted, but yielded unsatisfactory results, yielding an error factor of over 2. The error on the injection capacitance has yet to be determined, and can vary significantly due to fabrication uncertainties. For all the reasons listed above, for the scope of this thesis, it was chosen to give the thresholds in units of DAC counts. In the future it is planned to determine the conversion factor more accurately, and to provide a calibration procedure for the MOSS sensors, which will be crucial to properly calibrate the final detector.

The lowest threshold value (configured via `VCASB`) is determined before the beam test in the laboratory and is chosen to be such that the fake-hit (see eq. 4.1) rate of each region is approximately 10^{-3} hits/pixel/event. Since the readout bandwidth is limited, this threshold sometimes leads to a timeout during the scan, in which case the next higher threshold

value was chosen. This setting will be reffered to as $\texttt{VCASB}_{\text{start}}$ and defines the upper limit of the parameter range[24]. From this setting the VCASB parameter range is scanned down to $\texttt{VCASB}_{\text{start}} - 36$, with a stepsize of 3, yielding 13 data points for each region. The determination of this range and its automatisation and implementation in software was a key part for the preparation of this campaign, and has now become part of the official MOSS and BabyMOSS testing software package [48].

An exemplary efficiency and fake-hit rate measurement for top region 6 and bottom region 4 of MOSS-2_W02F4 is shown in Figure 4.23 as a function of the pixel threshold. The efficiency and fake-hit rate errors are calculated by applying a Clopper-Pearson confidence interval of one sigma, which corresponds to the central 68.3 % of a binomial distribution, but taking into account a lower limit of 0 and an upper limit of 1 [45, 49, 50]. The fake-hit rate is shown on the right side of the plot on a symmetric logarithmic scale, allowing to visualise the data points, where the fake-hit rate is 0 (i.e. there were no hits measured from the total number of triggers N_{Trig}). A fake-hit rate of 0 is not a representative value, so the fake-hit rate sensitivity limit is also shown. This limit is also represented in the upper error, which results from the Clopper-Pearson interval bounds.

What is immediately visible from these plots, is that for low threshold values, the efficiency of the sensor nears 100 %, with a fake-hit rate of around 10^{-3} for the top HU and 10^{-4} for the bottom HU. With increasing threshold, the fake-hit rate decreases rapidly, while the efficiency slowly decreases until it reaches the 99 % design requirement. From there, going towards higher thresholds, the efficiency significantly decreases, as more and more charge is required to assert a pixel. This is especially true for the edges of the pixels, as the probability for the pixel to record a hit is even lower, if the charge is generated further away from the collection diode. However, the slow initial decline of the efficiency leads to a plateau region, where it is easy to identify an operational margin for each region of one HU. This margin describes the region where the detection efficiency is larger than 99 %, while the fake-hit rate is below 10^{-6} hits/pixel/event.
Another apparent detail of the plots, is the difference in performance of the regions. For example, below a threshold of 15 DAC counts, the noise on top region 1 is about two orders of magnitude higher than on top region two at comparable detection efficiency. This trend seems to continue for higher thresholds, where the noise on top region 2 stays below the noise of other regions, until differences become indistinguishable as the fake-hit rate sensitivity limit is reached. values for the pixel threshold, while top region 2 seems to have a quicker decline. This is true while the efficiency curves of these regions are almost identical. Generally, after a thorough characterisation of the entire sensor lineup, top region 2 shows promise of being identified as the best performing region, while bottom region 3 (shown in the pink curve on the bottom plot) seems to be the worst performing region. However, since the measurements are still ongoing at the time this thesis is submitted, no final statement can be made. The reason for the discrepancy between regions are the aforementioned differences in the region design, which lead to different charge collection and signal generation properties (Table 2).

[24] Higher values for VCASB correspond to a lower detection threshold.

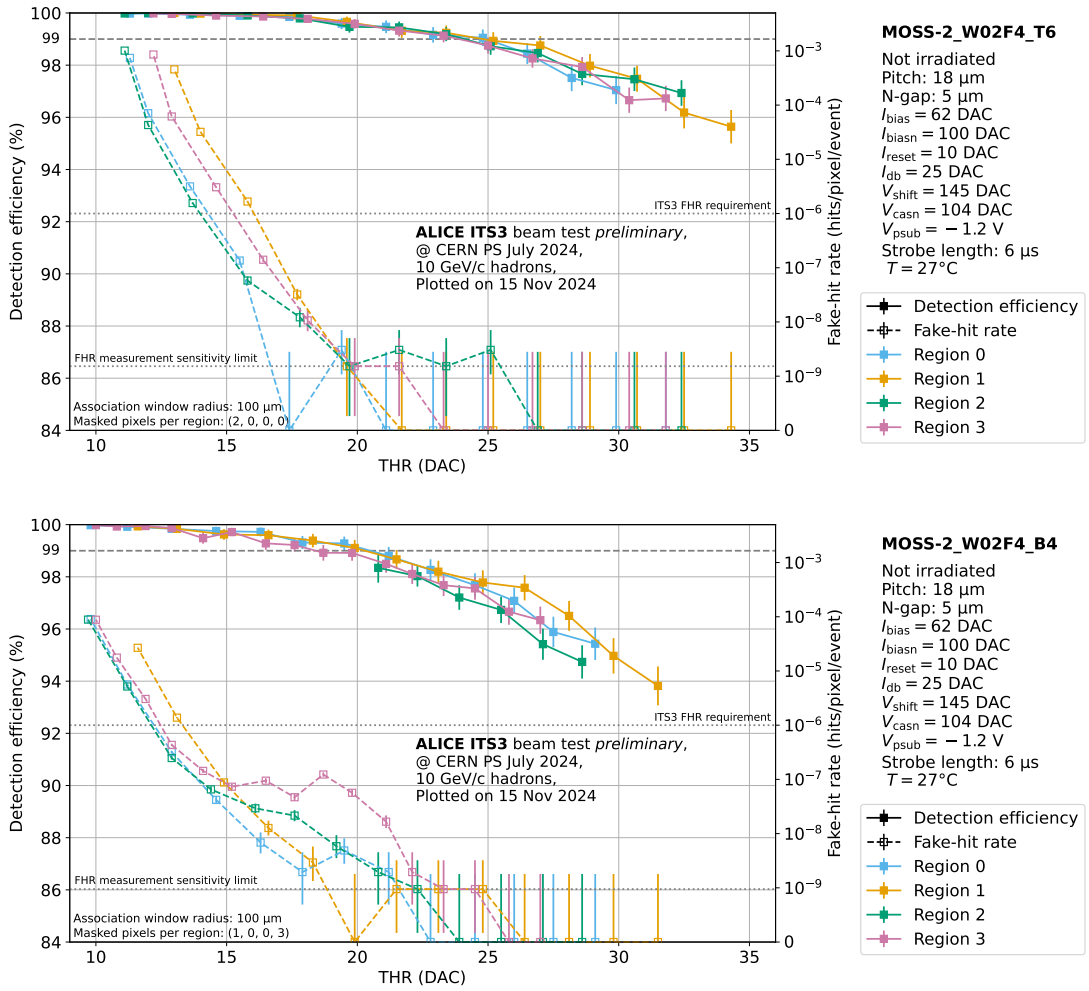


Figure 4.23: MOSS efficiency and fake-hit rate of one top and one bottom HU of a split 1 MOSS measured during a testbeam campaign in July 2024 as a function of pixel threshold, performed differentially for all four regions. The left y-axis shows the detection efficiency, i.e. the ratio of associated hits on the DUT to the total number of tracks, while the right y-axis shows the sensors fake-hit rate $\frac{N_{\text{hit}}}{N_{\text{trig}} \cdot N_{\text{pix}}}$. Marked by dashed lines are the ITS3 efficiency and fake-hit rate requirements. The settings for which the efficiency is above 99% and for which the fake-hit rate is $< 10^{-6}$ define the operational margin of the chip. Bottom region 2 has a reduced number of data points, which is due to time constraints that arose during the measurement.

Therefore, it is strictly necessary, that if the performance of different sensors is compared, this is done on a **region-by-region basis**. Figure 4.24 shows this comparison for all tested sensors during the July testbeam campaign. It displays the detection efficiency and fake-hit rate, as well as the operational margin, and the ITS3 requirements. The sensors from the first

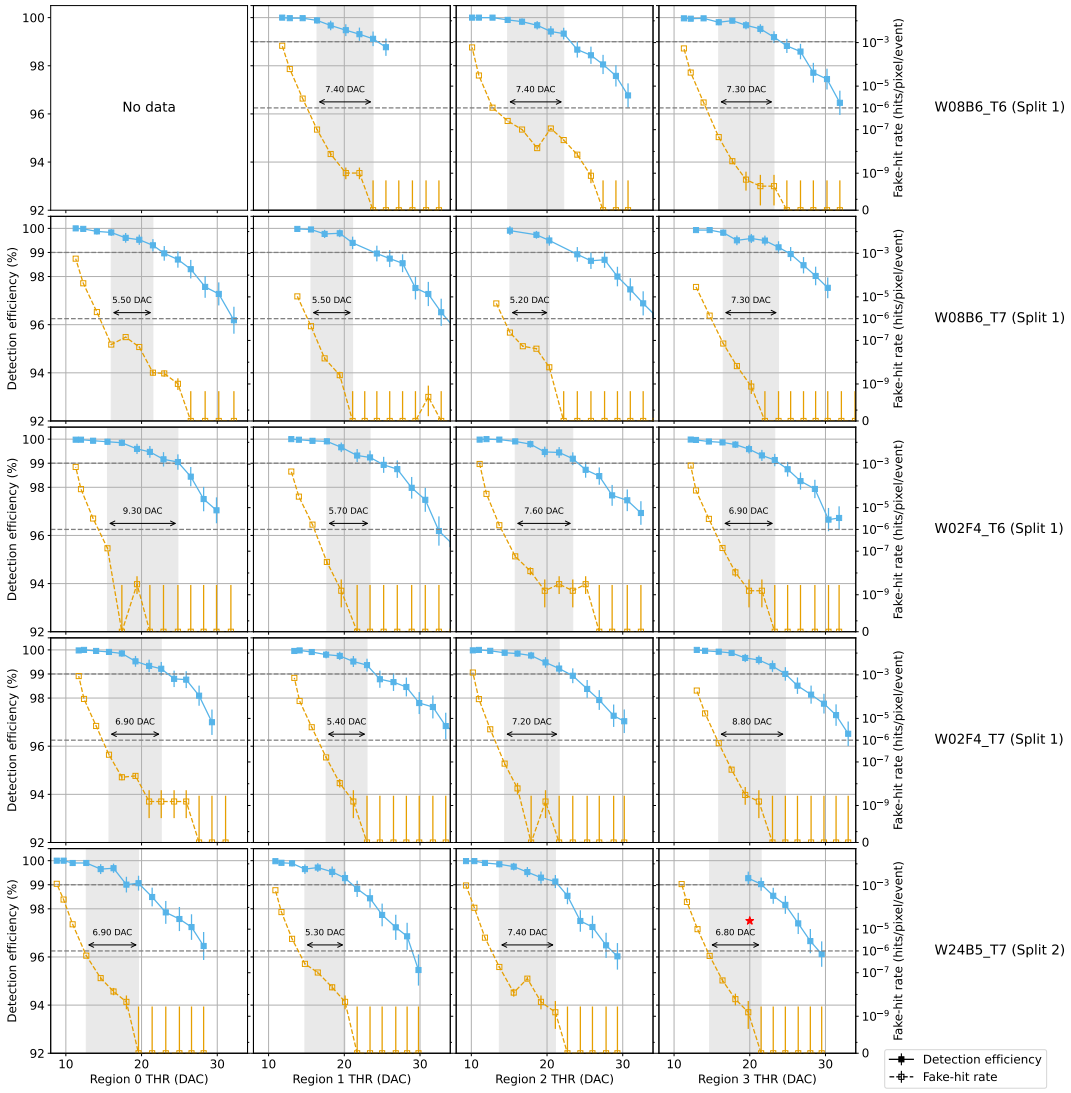


Figure 4.24: Detection efficiency and fake hit rate of the four top regions of all tested sensors during the July testbeam campaign. The first four rows represent sensors from the first split, while the last row shows the results of a sensor from the second split for comparison. The gray dashed lines represent the ITS3 requirements for efficiency ($> 99\,\%$) and the fake-hit rate ($< 10^{-6}$ hits/pixel/event). x-axes and y-axes are shared between all plots. A grey shaded area marks the operational margin of each region where a wider area generally stands for a better performing region. A red star in the bottom right corner indicates, that the measurement of the efficiency of this region is incomplete, however the operational margin can still be extrapolated, since the efficiency only increases towards lower threshold settings.

split are shown in the first four rows, while the last row shows the results of a reference sensor from the second split, which has also been tested with the same experimental setup. Even

if split 2 has been thoroughly tested before, and a comparison between the splits is possible with data from previous campagins, a measurement of a split 2 sensor under the exact same conditions as the split 1 sensors is still important to identify possible measurement-dependent systematic effects, arising from different environmental conditions or the beam profile. The columns of Figure 4.24 represent the four regions of each sensor, such that plots in one column always show corresponding measurements, that can be directly compared to one another.

It is evident that there is a significant variation in the width of the operational margin, even between sensors from the same split. Top region 0 of `W02F4_T6` for example, shows the widest operational margin of all tested regions, while the same region of `W08B6_T7` shows one of the narrowest margins. There are several reasons for this, the strongest contributor being the limited number of data points before and after the validity region, which can lead to a very strong cut of the actual operational margin. The best visualisation of this is probably region 1 of `W08B6_T7` in the second row. During this measurement, the data acquisition software crashed several times overnight. Even with the hard work of several colleagues to recover from this crash, following a strict time constraint for the campaign, data points for this unit were finally lost. Unfortunately, some of these point lie exactly on the edge of the operational margin, and the curve indicates, that they could have increased the apparent width of the margin by several points. Due to the time limited nature of beam tests, increasing the resolution of the operational margin determination by increasing the number of data points is not always feasible, as even a slight increase could very well double the time needed for the measurement.

However, in an attempt to find any performance differences between the splits, those measurements with missing data points can be excluded from the comparison. This shows, that indeed the operational margin of the first split seems to be generally wider than that of the second split, with the largest average increase seen in top regions 1 and 3 with 16 % and 11 % respectively. It needs to be stressed again, that this is only a preliminary result, based on a very small subset of the entire sensor lineup, but a trend is visible nevertheless. To further study this effect, a more detailed comparison between the splits considering the entire dataset of all tests is necessary. This comparison can only be performed, once the entire lineup of MOSS has been characterised. To improve on the determination of the operational margin, the granularity in which the parameter space is probed has to be increased, due to the large single-measurement variations in the efficiency and fake-hit rate, and also between different sensors. In terms of time-intensity, such a measurement would be much more demanding, and should be performed using a continuous particle beam, such as the electron beam available at the DESY testbeam facility in Hamburg, Germany.

Overall the MOSS shows promising results in terms of detection efficiency, and largely retains the efficiency of the MLR1 sensors, where it is worth mentioning that the matrix size increased by orders of magnitude compared to the MLR1 designs. Overall, the MOSS July testbeam campaign contributes to the demonstration of the implementation of wafer-scale stitched sensors, and yields some insights on the differences between split 1 sensors and split 2 sensors, that will be considered for the following sensor designs.

5 Conclusion and Summary

The topics and results of this work can be summarised into four main points.

ALICE and ITS3 During the next long shutdown period of the LHC (LS3, 2026 - 2028), the Inner Tracking System of the ALICE detector will undergo a major upgrade, in which the innermost three layers will be replaced by a new detector, the ITS3, featuring thin, wafer-scale bent monolithic active pixel sensors fabricated in the 65 nm CMOS process, in a low material budget setup that is air-cooled. The final design will feature a material budget of around $0.09\% X_0$ per layer [11], and be placed as close as 19 mm to the interaction point (Section 2). This is done in an effort to bring the ALICE Inner Tracking System to unprecedented levels of performance, especially in terms of spatial resolution and a higher efficiency for the track reconstruction of low-momentum particles, which is limited by the current material budget (Section 2.1).

APTS The APTS, together with the DPTS and CE65 is one of the first prototypes of sensors fabricated with the new 65 nm technology node, chosen for the new sensors of the ITS3, as a direct generational upgrade over the ALPIDE sensor, which is based on a 180 nm technology node. The APTS features direct individual analogue output of a 4×4 pixel matrix, and was fabricated in order to qualify the process and optimize the sensor for future iterations. Therefore, it has been produced featuring various doping levels, pixel geometries and pixel pitches. In the scope of this work, one of these sensors featuring a pixel pitch of 15 µm, produced using a process modification which has an additional gap in the low-dose implant (see Figure 2.9), as well as a source-follower based amplification scheme (see Figure 2.10) has been used to demonstrate the APTS calibration procedure and study the sensor response and energy resolution. The general testing procedure of the APTS has been described in Section 3, going all the way from basic signal readout to a full gain- and energy calibration of the sensor. The sensor has been calibrated using an ^{55}Fe source (Section 3.2), and its performance in terms of energy resolution has been determined both for the operation without any back-bias voltage applied, and with a back-bias voltage of -1.2 V applied to the substrate. By using the energy spectrum obtained with the ^{55}Fe source, the energy resolution of the sensor has been determined to be 7.4 % without back-bias, and 6 % with back-bias, using only the output of the sensor itself.
Another test has been performed, in which the APTS has been subjected to different noise conditions and directly injected noise profiles with an amplitude of 100 $\mathrm{mV_{pp}}$, all while observing the signal shaping process and measuring the signal-to-noise ratio of the chip. The results of this test show that the sensor is able to operate even in very noisy environments, and will not experience any significant loss in performance even with substantial electronic noise present (Section 3.3.1). Overall, these results demonstrate the feasibility of the 65 nm technology for particle detection and its readiness for the application in future sensor designs.

Single event effect studies with the BabyMOSS test system The next generation of 65 nm-based sensors is represented by the MOSS and the BabyMOSS. Both sensors feature a stitched design reticle, and consist of one (in the case of BabyMOSS) and ten (in the case of MOSS)

repeated sensor units (RSUs). Based on the new stitching technology, these sensors serve as the first test of wafer-scale pixel detectors, which is one of the key design aspects of the ITS3. A basic description of the MOSS and BabyMOSS chips including sensor design, readout, and laboratory test setups is given in Section 2.4 and Section 2.5, respectively. Part of the research and development campaign of the 65 nm stitched sensor technology is its characterisation in terms of single-event effects. For this, the BabyMOSS test system has been subjected to various charged particle beams at the U-120M Cyclontron at the NPI of CAS and the CYCLONE Cyclotron at the HIF at UCLouvain. Single event effects including single event upsets (SEUs) and single event latchups (SELs) have been described in Section 4.2 and thoroughly studied with the BabyMOSS at the aforementioned facilities.
The sensitivity of the BabyMOSS to SEUs has been studied in a proton beam and results have shown that ionising particles can cause the inversion of memory registers on the chip. This phenomenon has been characterised in terms of the inversion direction (i.e. whether a bit flips from 0 to 1 or the other way around), the different types of registers affected, and also, finally, studied as a function of sensor irradiation. The general value for the SEU cross section of the BabyMOSS registers has been determined to be in the order of $1 \times 10^{-14}\,\mathrm{cm}^2/\mathrm{bit}$ (Section 4.2.1), and does not depend on the inversion direction or the type of register affected.
The sensitivity of the BabyMOSS to SEL has been studied in a variable heavy-ion beam, effectively scanning the SEL cross section as a function of the linear energy transfer (LET) of charged particles onto the chip. It has been shown, that the sensitive nodes, which are located in the periphery of the chip, can be completely shielded using a matrix collimator, allowing only the active area of the sensor to be illuminated at the highest available LET available without causing latchups to occur. The sensitivity limit of the latchup cross section for the pixel matrix has been determined to be $\leq 3.58 \times 10^{-8}\,\mathrm{cm}^2$. Removing this collimator causes recoverable SEL mostly in the digital domain of the chip. Apart from the expected damage stemming from sensor irradiation, these latchups do not cause permanent damage, and can be reset by performing a power-cycle of the system. The cross section for SEL effects with unshielded periphery has been measured to be in the order of $1 \times 10^{-6}\,\mathrm{cm}^2$ in the relevant LET regime (Section 4.2.4). Both SEU and SEL results confirm earlier tests done with memory test structures in November 2023. The latchup cross section is low enough to not be a concern for the operation of the sensors in the ALICE environment, due to the low frequency of high LET particles, and the low power density of the ITS3, which makes a recovery from latchups possible, if the power is locally disconnected within 10 ms.
Another result obtained from the irraditation of the BabyMOSS is its continuous operation beyond a TID of 100 kGy, which is ten times higher than the design specification for the ITS3 (Table 1).
This result in conjunction with the measured single-event effect cross sections shows promising results for the applicability of the 65 nm technology, especially in terms of long-term operation in the ALICE detector environment.

Detection efficiency of the MOSS chip Finally, the detection efficiency of two MOSS sensors has been measured in a hadron beam at the PS at CERN. These two sensors belong to two different batches (so-called *splits*) of the MOSS production, and their results have been compared with special focus on the operational margin. The results show a wide opera-

tional margin, in which the sensors fulfill both the ITS3 requirements in terms of detection efficiency and fake-hit rate (Table 1). The detector setup inside of a telescope of ALPIDE reference sensors has been presented and the data acquisition process described in Section 4.3.2. The detector alignment process, consisting of a two-step track-based alignment procedure for the reference planes and the device under test (DUT) has been demonstrated, and yields very good tracking performance (Figure 4.21). For reference, a third MOSS sensor was used to directly compare the performance of the chips between the two different splits. The MOSS detection efficiency was determined as a function of the applied sensor threshold, and is visualised together with its fake-hit rate (Figure 4.24). From these plots, the operational margin for each submatrix of all sensors has been identified, and compared between the different splits. Split 1 generally shows a slightly wider operational margin than Split 2, though the performance of both splits is within the design requirements of the ITS3, and does not show significant differences. Especially considering the large sensor-to-sensor variations, the subset of MOSS sensors and low density of data points obtained during this study has been identified to be too small to warrant any further conclusions about the performance of different MOSS splits. To investigate these variations, a more thorough study with a larger set of sensors and a higher step granularity in the parameter space is proposed. The low spill rate of the PS would make such a measurement a very time demanding effort. Therefore using a continuous beam of minimum-ionising particles would be beneficial for such a study.
Nevertheless, this study serves to narrow down an operational regime for `VCASB` – the main DAC parameter, that steers the pixel threshold – and helps limiting the search window for future beam tests.

Summary The 65 nm technology has shown excellent performance regarding detection efficiency, radiation hardness, and single-event susceptibility, which makes it a valid candidate for the application within ITS3.
Within this work, the APTS has been characterised in terms of energy resolution and performance in noisy environments, and shows no significant loss in performance even with substantial electronic noise present.
Two stitched sensor prototypes, the MOSS and BabyMOSS, have been studied in terms of single-event effects and detection efficiency, contributing to the qualification of the technology for the use within the future ALICE detector after the Long Shudown 3 of the LHC. The sensors parameters have been optimised to meet the requirements of the ITS3 and show wide operational margins for prototypes of two different splits, providing a clear path for the next iteration of truly cylindrical wafer-scale pixel detectors to come.

Appendices

Acronyms

ADC Analog-to-Digital Converter. 12

ALICE A Large Ion Collider Experiment. 2, 3, 12, 26

ALPIDE ALICE Pixel Detector. 2, 3, 12

APTS Analog Pixel Test Structure. 0, 9–12, 15, 17, 18, 20–25, 29, 30

ATLAS A Toroidal LHC Apparatus. 2

CCD Charge-Coupled Device. 2

CE65 Circuit Exploratoire 65. 9, 10, 29

CERN European Organization for Nuclear Research. 3, 17

CMOS complementary metal-oxide-semiconductor. 9

CMS Compact Muon Solenoid. 2

DAC Digital-to-Analog Converter. 10–12, 15, 18

DAQ Data Acquisition. 12, 17, 30

DPTS Digital Pixel Test Structure. 9, 10, 15, 29

ER Engineering Run. 14, 30

ER1 Engineering Run 1. 12, 14, 30

FHR fake-hit rate. 9

FPGA Field Programmable Gate Array. 12, 26

HU half-unit. 14–16

ITS Inner Tracking System. 2, 3, 17

LHC Large Hadron Collider. 2

LHCb LHC-beauty. 2

MAPS Monolithic Active Pixel Sensor. 2, 8, 9, 29

MLR1 Multi Layer Reticle 1. 9, 10, 12, 29

MOS metal-oxide-semiconductor. 9, 26, 27

MOSFET metal-oxide-semiconductor field-effect transistor. 3, 9, 27

MOSS Monolithic Stitched Sensor. 0, 3, 14–17, 26, 27, 30

MOST Monolithic Stitched Sensor Timing. 14

NMOS n-type metal-oxide-semiconductor. 9

PMOS p-type metal-oxide-semiconductor. 9

QGP Quark-gluon plasma. 2

RMS root mean square. 23

RSU repeated sensor unit. 14, 15, 30

SEB single event burnout. 27

SEE single event effect. 26

SEFI single event functional interrupt. 26

SEGR single event gate rupture. 27

SEL single event latchup. 27

SET single event transient. 26, 27

SEU single event upset. 26, 27

SNR signal-to-noise ratio. 21–23, 25

TPSCo Tower Partners Semiconductor Co., Ltd.. 0, 3, 9

TTL transistor-transistor-logic. 3

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List of Figures

List of Tables

Additional figures

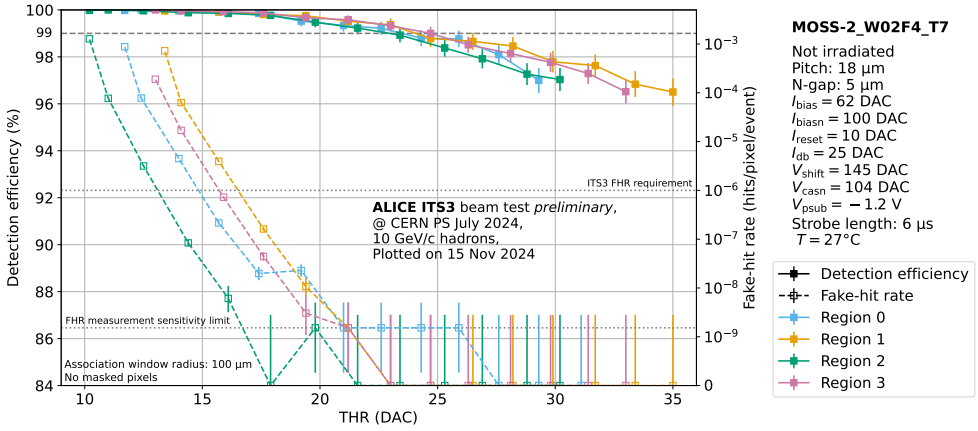

Figure 5.1: MOSS efficiency and fake-hit rate of top region 7 of the tested split 1 module as a function of pixel threshold, including all four regions.

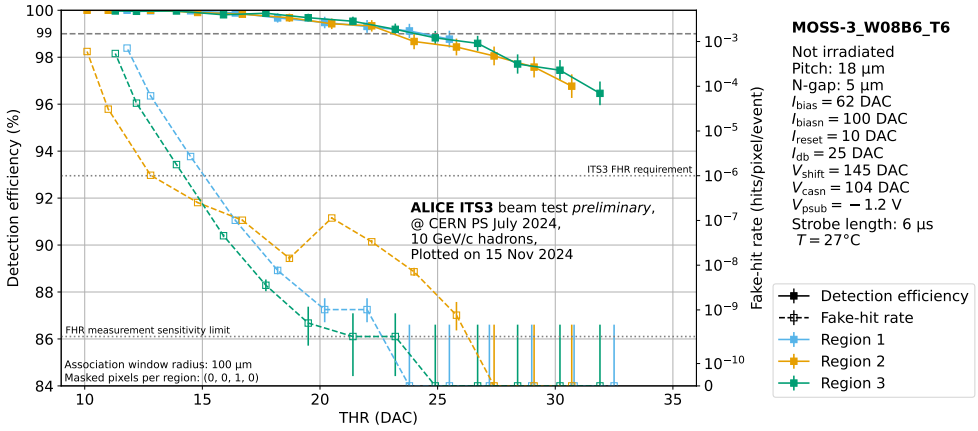

Figure 5.2: MOSS efficiency and fake-hit rate of top region 6 of a tested split 2 module as a function of pixel threshold, including region 1, 2 and 3. Region 0 was not measured because of time constraints.

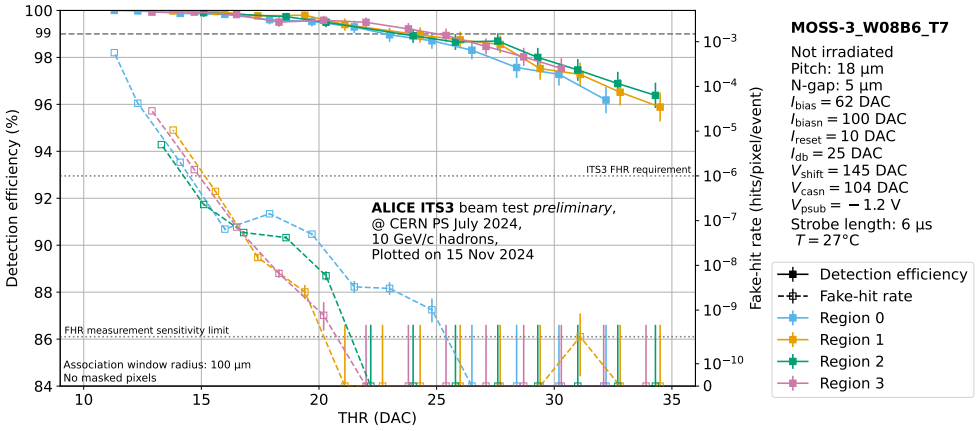

Figure 5.3: MOSS efficiency and fake-hit rate of top region 6 of a tested split 2 module as a function of pixel threshold, including all four regions.

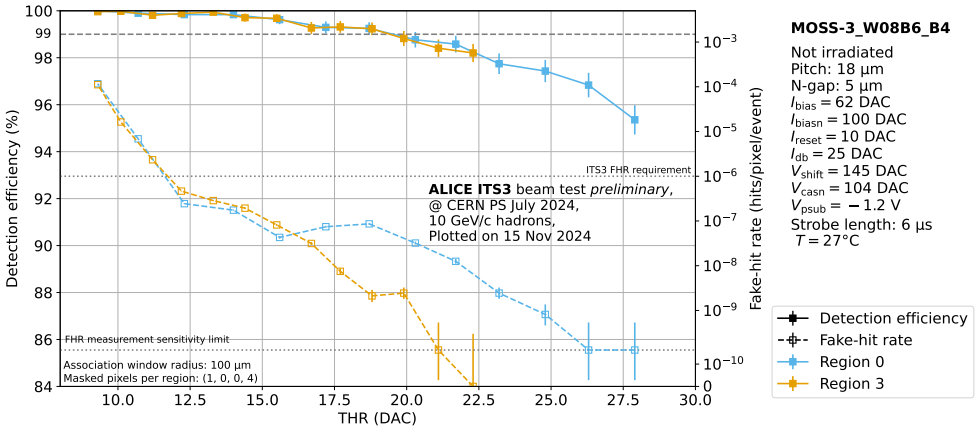

Figure 5.4: MOSS efficiency and fake-hit rate of bottom region 4 of a tested split 2 module as a function of pixel threshold, including region 0 and 3. Region 1 and 2 were not measured because they feature the same architecture as region 0 and are expected to yield similar results.

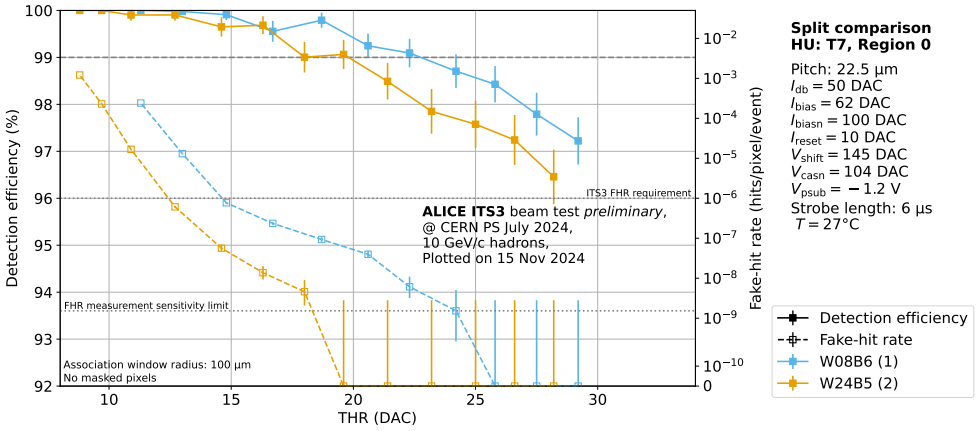

Figure 5.5: MOSS efficiency and fake-hit rate comparison between region 0 of the two different splits. While there is a clear x-shift in the curve, the overall performance is comparable. This is just one example measurement of the summary shown in Figure 4.24.

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Declaration

I declare that this thesis has been composed solely by myself and that it has not been submitted, in whole or in part, in any previous application for a degree. Except where states otherwise by reference or acknowledgment, the work presented is entirely my own.

Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

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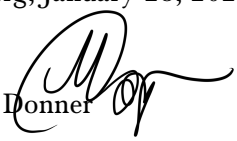

Maurice Donner