Department of Physics and Astronomy

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Master thesis

in Physics

submitted by

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born in Preetz

2019

Characterization of ATLASPix1, an HV-CMOS Demonstrator for the Phase-II Upgrade of the ATLAS Inner Tracker

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Abstract:

For the operation at the High Luminosity Large Hadron Collider the ATLAS Inner Detector will be fully replaced. For the outermost pixel layer cost effective monolithic CMOS sensors are considered as alternatives to the foreseen baseline hybrid technology. ATLASPix1, a High Voltage Monolithic Active Pixel Sensor prototype produced in the aH18 process by AMS, is studied for that purpose. The technology combines fast charge collection via drift with a full readout state machine in a monolithic architecture.
In this thesis, two different versions of ATLASPix1 are studied, which differ in the implementation of the in-pixel comparator. ATLASPix_Simple has a pure NMOS comparator, whereas ATLASPix_Simple hosts a CMOS comparator. The pulse shaping of the amplification stage is investigated as well as the signal transmission to the digital cell. The observations are put into context with the time resolution of both sensors. For ATLASPix_Simple a time resolution before offline corrections of about 11.8 ns for the entire sensor is measured, whereas for ATLASPix_IsoSimple it is of about 8.7 ns. The better time resolution of the ATLASPix_IsoSimple is an effect of the faster CMOS comparator. After offline corrections, the mean time resolution of the single pixel analysis is below 6 ns for both sensor types.

Zusammenfassung:

Für den Einsatz am High Luminosity Large Hadron Collider wird der Inner Detector des ATLAS-Experiments vollständig ersetzt. Für die äußerste Pixellage wird die Verwendung von kostengünstigen monolithischen CMOS-Sensoren als Alternative zur vorgesehenen hybriden Technologie in Betracht gezogen. Zu diesem Zweck wird ATLASPix1 untersucht, ein hochspannungsbetriebener monolitisch aktiver Pixelsensorprototyp hergestellt im aH18-Prozess von AMS. Die Technologie kombiniert schnelle Ladungssammlung durch Drift mit einer vollständigen Auslesesarchitektur in einem Chip.
In dieser Arbeit werden zwei unterschiedliche Versionen des ATLASPix1 untersucht, die sich in der Implementierungen des Komparators in der Pixelzelle unterscheiden. Der Komparator des ATLASPix_Simple hat ein reines NMOS-Design, wohingegen ATLASPix_IsoSimple einen CMOS-Komparator besitzt. Im Rahmen dieser Arbeit wird die Pulsformung des Verstärkers ebenso untersucht wie die Signalübertragung zur Auslesezelle. Die Beobachtungen werden benutzt, um die Zeitauflösung beider Sensoren zu untersuchen. ATLASPix_Simple erreicht vor Offline-Korrekturen eine Zeitauflösung von etwa 11.8 ns für den gesamten Sensor, wohingegen für ATLASPix_IsoSimple etwa 8.7 ns gemessen wurde. Die bessere Zeitauflösung liegt dem schnelleren CMOS-Komparator des ATLASPix_IsoSimple zu Grunde. Nach Offline-Korrekturen liegt die mittlere Zeitauflösung der einzelnen Pixel für beide Sensortypen unter 6 ns.

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Part I

Introduction

1 Introduction

The Standard Model of Particle Physics (SM) is a theoretical framework, which comprises all fundamental particles and their interactions. Up to date, the SM predictions are confirmed to a stunning precision. Despite that, observed phenomena which are not covered by the SM, like the matter-antimatter asymmetry or dark matter, cannot be explained. This indicates that the theory is not complete and models beyond the SM are therefore tested in modern particle physics experiments.
At the intensity frontier, experiments like the planned Mu3e [1] experiment search for contributions of unknown particles to quantum loops, which induce deviations from the SM prediction. At large colliders like the Large Hadron Collider (LHC), the search continues at the energy frontier. Due to the high center-of-mass energy of colliding particles, unknown heavy particles could be produced directly.
The ATLAS experiment is one of four major experiments at the LHC. With the increase of the luminosity at 2026, the tracking system will be fully replaced by an all silicon detector, which consists of strip and pixel detector modules. The foreseen baseline technology of the pixel detector are so-called hybrid sensors, which consist of a pixel sensor bump bonded to a readout chip. With the fast advancement of commercially available CMOS technologies, alternative technologies for the outermost pixel layer are considered.
One of these alternatives is the High Voltage Monolithic Active Pixel Sensor (HV-MAPS) technology. Here, pixel sensor and readout chip are combined to one entity. Compared to hybrid technologies, the fabrication with commercial HV-CMOS processes yields the benefit of low cost and a high production capability of the foundries. Depending on the substrate resistivity and supplied high voltage, a typical depletion zone in the order of 20 µm to 30 µm is created. The charge is collected via drift and the signal is processed by the embedded readout circuitry.
In the course of this thesis the first HV-MAPS prototype as demonstrator for the Inner Tracker Phase-II upgrade of the ATLAS Experiment, ATLASPix1, is investigated. ATLASPix1 includes two different sensor versions, ATLASPix_Simple and ATLASPix_IsoSimple. Both host an in-pixel comparator, which has a pure NMOS design in case of ATLASPix_Simple, whereas ATLASPix_IsoSimple uses a CMOS design for the comparator. The implemented comparator is the only design difference for both sensors. ATLAPix_IsoSimple has not been investigated before. The commissioning of this sensor is performed within this thesis.
The performance of the pixel cell and periphery cell circuitries are characterized. Therefore, the pulse shapes of two test outputs are measured for different operation settings. One test output is used to observe the signal after the amplification stage, the other is the signal after the discrimination by the comparator. This allows an optimization in terms of power consumption and fine-tuning of the sensor's components. Furthermore, the time resolution capabilities of both sensors are studied in the laboratory using a

radioactive source and a scintillating tile as time reference.

2 The Standard Model of Particle Physics

The theoretical framework known as the Standard Model of Particle Physics (SM) describes the fundamental particles and their interactions on the quantum scale. Figure 2.1 illustrates these particles, which comprise twelve fermions with spin 1/2, four gauge bosons with spin 1 and the Higgs boson with spin 0. The SM particles are distinguished by their respective quantum numbers.

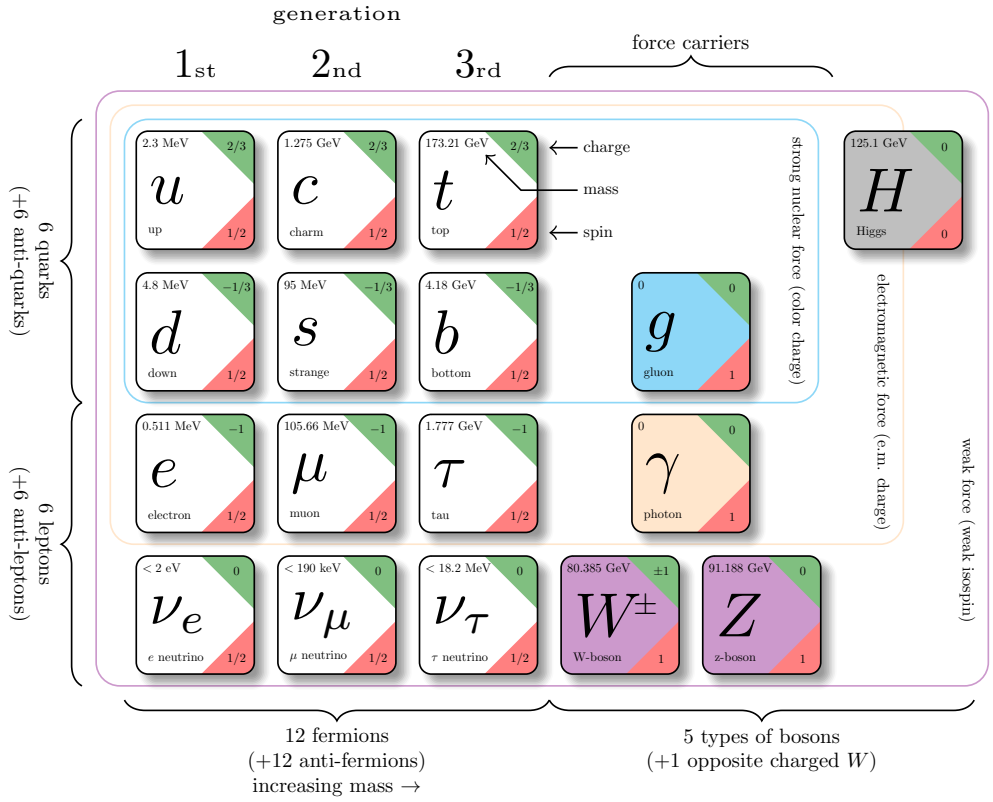


Figure 2.1: The Standard Model of Particle Physics. Data taken from [2].

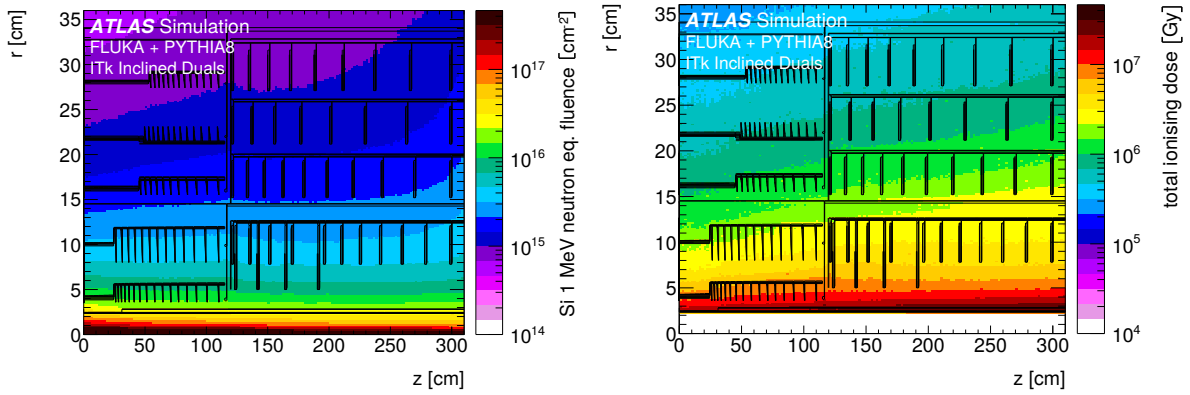
The fermions as well as their respective anti-particles are arranged in two groups: quarks and leptons, and three generations according to their increase in mass. Since a particle strives to be in the lowest energy state, higher mass particles are instable and decay to particles of lower generation.
In addition to the electrical charge, quarks carry a color charge associated to the strong interaction, which is mediated by the massless gluon. Since gluons carry a color charge themselves, they are interacting with each other, limiting the range of the strong interaction to the scale of a nucleus. Concurrently, quarks and gluons are confined to color

neutral objects, called hadrons. Two types of quarks exist: 3 up-type and 3 down-type quarks, which carry an electrical charge of $+2/3$ and $-1/3$, respectively.
Leptons are split into charged leptons, electron, muon and tau with negative electrical charge, and their corresponding neutrinos, which carry no electrical charge.
The massless photon is the mediator of the electromagnetic force, which interacts with all electrically charged particles, consequently excluding the neutrinos. These only participate in the weak interaction, responsible for all transitions of particles between different generations. The mediators of the weak interaction are the two oppositely charged W-bosons with a rest mass of $\approx 80.4\,\mathrm{GeV/c^2}$ and the neutral Z-boson with a rest mass of $\approx 91.2\,\mathrm{GeV/c^2}$. Up to this day, the weak and the electromagnetic force are the only interactions which can be unified to one, called electroweak interaction [3].
The discovery of the Higgs boson [4, 5] by the ATLAS and CMS experiment added the last predicted fundamental particle to the SM. The Higgs boson is a result of the spontaneous symmetry breaking in the electroweak interaction, also called Higgs-mechanism, which bestow the W- and Z-boson their mass. Also, the mass generation of fermions can be correlated to the Higgs boson for which the Yukawa coupling could be measured [6, 7].
Despite the high precision of theory predictions and congruent measurement results in the SM, effects incompatible with the SM are observed. Up to date, the origin of dark matter, baryon-anti-baryon asymmetry in the universe and gravitation on the quantum level are unexplained. This requires models beyond the SM, which are tested for example at large collider experiments like ATLAS.

3 HL-LHC Operation of ATLAS

In 2026, the High-Luminosity Large Hadron Collider (HL-LHC) is planned to start its operation. It is expected to reach a peak instantaneous luminosity of 7.5×10^{34} cm^{-1} s^{-1} [8]. This corresponds to an average pile-up of about 200 inelastic proton-proton collisions per beam-crossing. With a beam-crossing rate of 40 MHz and 10 years of operation, the ATLAS experiment aims to collect a data set of 4000 fb^{-1}. The main goals are the precision measurement of boson scattering and precise study of the Higgs sector. Deviations from the SM predictions could give indications about theories beyond the SM.
For the HL-LHC run of ATLAS the entire Inner Tracker Detector will be replaced. In the following the Inner Tracker (ITk) Phase-II upgrade of the ATLAS experiment will be introduced. The following information refers to the Technical Design Report of the ATLAS Inner Tracker Pixel Detector [8].

3.1 The Inner Tracker Phase-II Upgrade of ATLAS



(a) 1 MeV neutron equivalent fluence (b) Total ionizing dose

Figure 3.1: The fluence and dose distribution for the pixel detector normalized to 4000 fb^{-1} [8].

The ITk consists of two subsystems, the Strip Detector and the Pixel Detector. The Strip Detector comprises four barrel layers and six end-cap disks, which have a petal design. Both are composed of double modules. Each double module has a small stereo angle between the modules to add z(R) resolution. The Strip Detector is isolated from the Pixel Detector by the Pixel Support Tube. The Pixel Detector consists of five barrel layers (layer 0-4), made up by hybrid sensor modules. The two innermost layers are additionally separated from the outer layers by the Inner Support Tube. Since a harsh

radiation environment is expected (see Figure 3.1), it enables the replacement of this modules.
The pixel modules consist of pixel sensors bump-bonded to front-end chips. The foreseen technologies for the pixel sensors are 3D pixel sensors in layer 0 and planer pixel sensors in the other layers. The readout chip is under development by the RD53 collaboration of ATLAS and CMS. The front-end chip integrates the collected charge and amplifies and digitizes the signal. Since the dimensions of the pixel front-end chip are not yet defined, a size of $19.2 \times 20\,\mathrm{mm}^2$ for the active pixel matrix (384×400 pixel) and $2 \times 20\,\mathrm{mm}^2$ for the periphery is assumed.

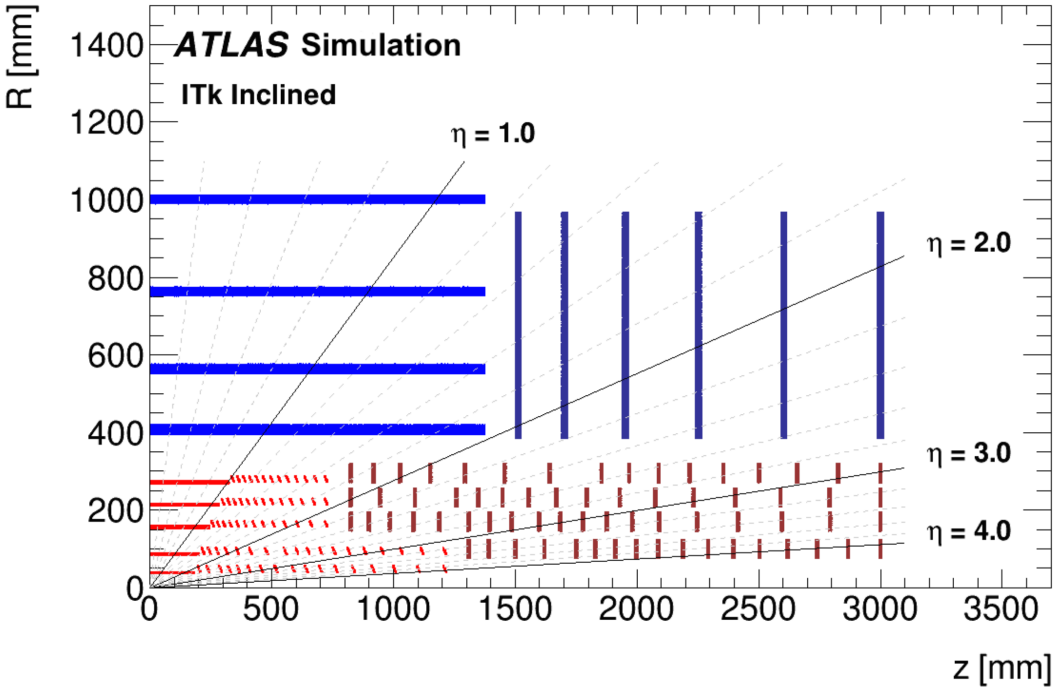


Figure 3.2: Schematic layout of the ITk. One quadrant of the active detector elements is shown. Presented are the barrel layers (blue) and end-cap disks (dark blue) of the Strip Detector as well as the barrel layers (red) and end-cap rings (dark red) of the Pixel detector [8].

3.1.1 Alternative Pixel Technologies and Requirements for the Outermost Pixel Layer

For the outermost pixel layer, called pixel layer 4, alternative pixel technologies are considered. Monolithic sensors exploit the potential of recent HV (high-voltage)- or HR (high-resistivity)-CMOS technologies. Here, pixel sensor and readout chip are combined in one entity, benefiting from fast charge collection and CMOS logic circuitry embedded within the pixels. The use of commercial foundries yields the benefit of comparatively low price and production cost.
The increased luminosity gives a significant rise of the occupancy and radiation damage

of a sensor and the feasibility of the sensors has to be shown. The requirements for the pixel layer 4 are listed in Table 3.1.

	Flat Barrel	Inclined Barrel	End-cap
Occupancy[1] $[\frac{<hits>}{\text{chip}}/\text{event}]$	9.9	9.1	9.3
Fluence[2] $[10^{14}\text{n}_{\text{eq}}/\text{cm}^2]$	28	30	38
Dose[2] [MGy]	1.6	2.0	3.5

Table 3.1: Requirements for the pixel layer 4. ([1]for $50 \times 50\,\mu\text{m}^2$ pixels using $t\bar{t}$ events with 200 pile-up; [2]values for $4000\,\text{fb}^{-1}$ have been multiplied by a safety factor of 1.5) [8].

At a bunch crossing rate of 40 MHz, the time frame to read out detected hits amounts to 25 ns. Since no distinct information of the time resolution requirement is quoted, it is assumed that all hits have to be within the time frame according to the in-time efficiency. An in-time efficiency of 99 % is demanded, whereas at the end-of-life of the ITk an inefficiency of 3 % is considered.
To calculate the corresponding time resolution a normal distribution is assumed:

$$\text{Efficiency} = erf\left(\frac{x}{\sqrt{2}}\right) \tag{3.1}$$

In this equation x represents the range around the mean in units of sigma. Using equation 3.1 the time resolution for the in-time efficiency of 99 % is calculated to be $\sim$4.85 ns.

4 Particle Interaction with Matter

Particles interacting with a medium can be detected by energy transfer, which can be processed as a signal. The amount of transferred energy and the probability of the interaction depend on the medium and the characteristics of the incident particle, like charge, mass and initial energy.
This chapter addresses the interaction of particles with matter concerning pixel detectors in modern experiments.

4.1 Photons

Interactions of photons with matter can be described by the photoelectric effect, Compton scattering and pair production. Depending on the photon's energy and charge number Z of the absorber material, each of these effects occurs with a different probability, see Figure 4.1.

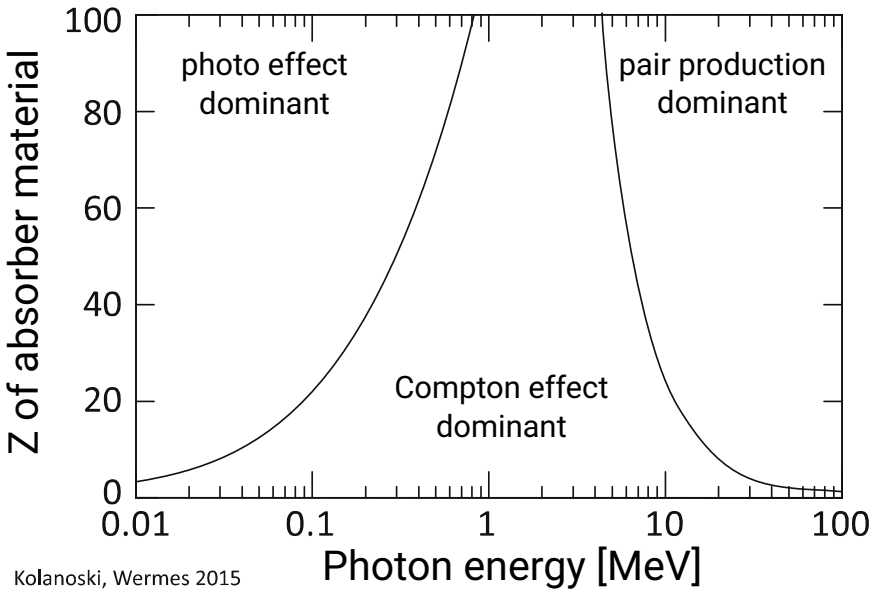


Figure 4.1: Dominant domains of different photon processes depending on the photon energy and the charge number of the absorber material [9] (edited).

Photoelectric Effect

With the photoelectric effect the total energy of the photon is transferred to an atom. The absorbed energy is emitted in form of an electron, leaving a vacancy on a shell of the atom, which is occupied by an electron of a higher shell subsequently. The released energy of this transition is then emitted in form of another photon. The condition for the photoelectric effect, is that the initial photon energy E_γ has to exceed the binding energy E_B of the emitted shell electron.
Exempli gratia for the K-shell: The total absorption cross section is defined by the Born-cross section with a significant dependency on the E_γ and the charge number Z of the medium [9]:

$$\sigma \sim \frac{Z^5}{E_\gamma^{3.5}}. \tag{4.1}$$

Compton Scattering

Compton scattering is an elastic scattering process of an incident photon on a quasi-free electron. The momentum of the photon is partially transferred to the quasi-free electron, which increases the wavelength of the photon. The energy E'_γ of the scattered photon depends on the scattering angle θ_γ,

$$E'_\gamma = \frac{E_\gamma}{1 + \frac{E_\gamma}{m_e c^2}(1 - cos\theta_\gamma)}. \tag{4.2}$$

The cross section of Compton scattering per atom, which increases linearly with the charge number Z of the absorber material, is given by the Klein-Nishina-Formula [10].

Pair Production

Pair production is the conversion of a photon inside the Coulomb field of nuclei into an electron-positron pair. In this process the initial photon energy is fully transferred to the mass and kinetic energy of the final state particles. The threshold energy of pair production for the photon is given by:

$$E_\gamma = 2m_e c^2. \tag{4.3}$$

The pair production cross section is [9]:

$$\sigma_{\text{pair}} \approx \frac{A}{\lambda_\gamma N_A \rho} = \frac{7}{9}\frac{A}{X_0 N_A \rho} = \frac{7}{9}\frac{1}{X_0 N_{\text{atoms}}}, \tag{4.4}$$

directly depending on the photon absorption length λ_γ, whereby X_0 is referred to as the radiation length (see equation 4.9) of the medium, and the density of the scattering center N_{atoms}, defined by the material density ρ, the Avogadro's number N_A and the nucleon number A.

4.2 Charged Particles

Charged particles interact with the atoms of the traversed medium via the electromagnetic force, which is directly depending on the charge z of the incident particle. In the subsequent sections, the different interactions of charged particles with matter are introduced.

4.2.1 Heavy charged Particles

"Heavy" charged particles include all charged particles with a rest mass above 100 MeV, consequently excluding the electron and positron. The main contribution to the energy loss by charged particles traversing matter is ionization. The energy loss itself is described by a Landau distribution, while the mean energy loss per path length in matter is described by the Bethe-Bloch-Formula [11]:

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi n z^2}{m_e c^2 \beta^2} \cdot \left(\frac{e^2}{4\pi\epsilon_0} \right)^2 \cdot \left[\log\left(\frac{2 m_e c^2 \beta^2}{I \cdot (1-\beta^2)} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right]. \tag{4.5}$$

The formula is parametrized by the incident particle velocity given as its fraction of speed of light β and its charge number z, the density-effect correction $\delta(\beta\gamma)$, as well as the electron density n and mean excitation energy I of the medium. Other parameters are natural constants like the electron mass m_e, the speed of light in vacuum c and the vacuum permittivity ϵ_0.

Figure 4.2 displays the energy loss behavior, depending on the initial kinetic energy for different materials.
For small kinetic energies the β^2-dependency of the Bethe-Bloch-Formula is dominant. The particles require more time traversing the material, resulting in an increased number of interactions and a consequently higher energy loss.
The global minimum of the mean energy loss is at $\beta\gamma \approx 3$. Particles of this energy are labeled as minimum ionizing particles (MIP). Inducing a minimum of collectible charge inside a detector, MIPs are the baseline to measure the efficiency of a detector, consequentially making them a favored object to study.
For $\beta\gamma > 3$ a logarithmic rise of the mean energy loss emerges and the influence of δ-electrons (see section 4.2.3) increases.

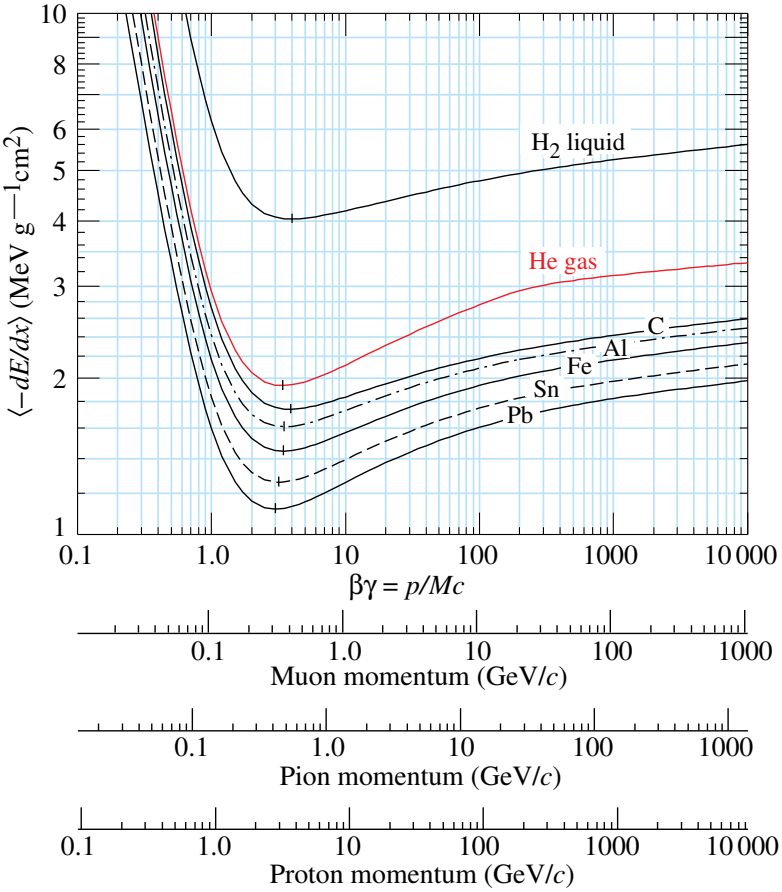


Figure 4.2: Mean energy loss of heavy particles for different materials described by the Bethe-Bloch formula [2].

4.2.2 Electrons and Positrons

Electrons and positrons are a special case in terms of energy loss. The mean energy loss via ionization is described by the Berger-Seltzer-Formula [12]:

$$-\left\langle \frac{dE}{dx} \right\rangle = \rho \frac{0.153536}{\beta^2} \frac{Z}{A} \cdot \left(B_0(T) - 2\log(\frac{I}{m_e c^2}) - \delta \right). \tag{4.6}$$

The formula is parametrized by the fraction of the speed of light of the incident particle β and their density correction δ, as well as a momentum depending stopping power $B_0(T)$, the density ρ and the ratio of protons to nucleons Z/A of the medium. The mean energy loss as function of the kinetic energy is illustrated in Figure 4.3. The difference in energy loss between electrons and positrons is caused by two effects. The positron can be annihilated by a shell electron, whereas the incoming electron is indistinguishable from a shell electron. The repulsion of electrons due to the Pauli Principle increases the energy loss.

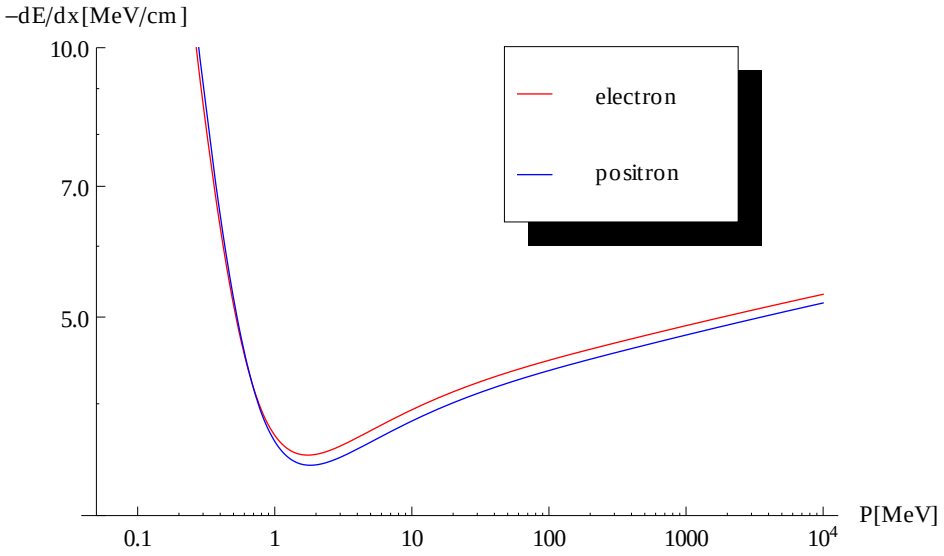


Figure 4.3: Mean energy loss of electrons and positron in silicon in an energy range from 50 keV to 10 GeV [12, 13].

4.2.3 Energetic knock-on electrons: δ-ray/electron

A δ-electron is a recoil particle, caused by a central collision of an incident particle with a shell electron in the traversed medium. The δ-electron features a high kinetic energy, creating secondary ionization inside the medium. Thus, it represents secondary radiation, also called δ-ray. δ-electrons contribute to the measured energy fluctuation of a detector [9].

4.2.4 Bremsstrahlung

The phenomenon of energy loss by emission of photons is called Bremsstrahlung [9]. A prerequisite for this effect is a highly relativistic charged particle and the probability is depending on the initial energy and Z of the interaction medium:

$$P_{\text{Bremsstrahlung}} \sim Z^2 \frac{E}{m^2}. \tag{4.7}$$

This effect predominantly occurs for electrons, due to their low rest mass with respect to other charged particles. The energy loss by Bremsstrahlung is described by:

$$-\frac{dE}{dx} = -\frac{E}{X_0}, \tag{4.8}$$

whereas the radiation length of a certain material is approximated to [9]:

$$X_0 = \frac{716.4\,\text{g/cm}^2 \cdot A}{Z(Z+1) \cdot \log(287/\sqrt{Z})}, \tag{4.9}$$

depending on the charge number Z and the nucleon number A of the material.

4.2.5 Multiple Coulomb Scattering

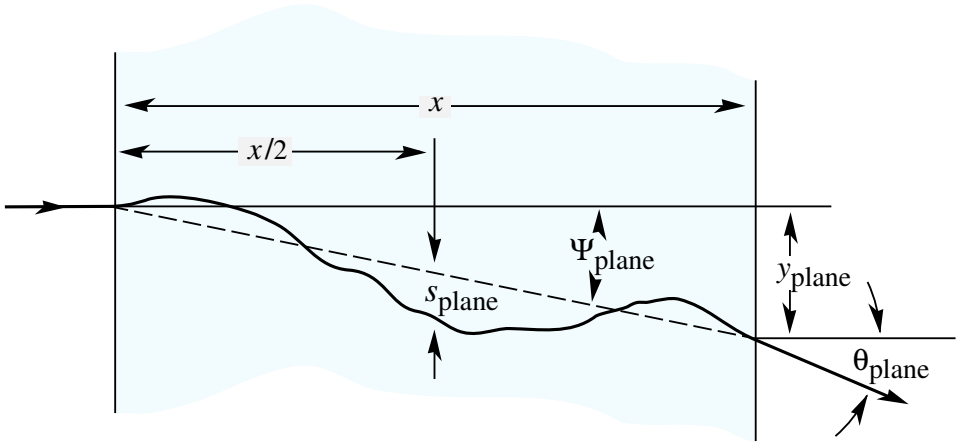


Figure 4.4: Sketch of multiple Coulomb scattering of an incident particle in matter [2].

An incident particle traversing matter is deflected multiple times by small-angle scatters, due to the interaction with the Coulomb field of the nuclei. This is called multiple Coulomb scattering. Each scattering contribution is described by the Rutherford cross section [9]. The central limit theorem implies that the net scattering and displacement distribution is given by a Gaussian. The angular distribution can be approximated by a Gaussian with a RMS width described by the Highland formula [2]:

$$\Theta_{\text{plane}}^{rms} = \frac{13.6\,\text{MeV}}{\beta cp}\, z\sqrt{\frac{x}{X_0}}\left[1 + 0.038\ln\left(\frac{xz^2}{X_0\beta^2}\right)\right]. \tag{4.10}$$

The incident particle's impact is represented by the momentum p, its velocity given in the fraction of speed of light β, as well as its charge number z. The traversed medium affects the distribution only by its thickness, given in units of the relative radiation length x/X_0.

5 Semiconductor Detector Physics

A semiconductor is a material, which has all states in the valence band occupied by electrons at a temperature of T = 0 K, whereas the conduction band is empty. At this temperature, the semiconductor is a perfect insulator. At higher temperatures, the conductivity of a semiconductor increases, caused by electrons thermally excited into the conduction band, which in turn leave behind vacancies in the valence band. These vacancies act as positive space charges, called "holes". A hole can be occupied by another electron via recombination. The entire process of thermal excitation and recombination describes the movement of a charge in the valance band of the solid state medium and is constrained by the Fermi-Dirac-statistic.

5.1 Semiconductor Materials

Semiconductors can be used to build pixel detectors for the detection of particles and photons. Typically used materials are: silicon (Si), germanium (Ge), gallium arsenide (GaAs) and cadmium telluride (CdTe). The latter two are primarily used for the detection of X-rays, based on the high atomic number Z, which provides good absorption properties for photons (see section 4.1). Since germanium has a low band gap [9], it has to be cooled to be used as a detector material. The most common material used for pixel detectors is silicon, which can be operated at room temperature. The properties of silicon are summarized in Table 5.1.

5.2 Extrinsic Semiconductor

For pure silicon, the intrinsic charge carrier density compared to the atomic density is so low that conductivity is negligible. The quantity of free charge carriers is increased by adding impurities into the lattice of silicon, which is a group IV element. This process is called doping and appears in two forms, p- and n-type doping:

- **p-type doping:** An acceptor of a group-III element like boron, aluminum, gallium or indium is added to the lattice. It captures a valence electron, consequently decreasing the quantity of free electrons. The holes are the majority charge carriers in this case.
- **n-type doping:** A donor of a group-V element like phosphorus, arsenic, antimony, bismuth or lithium is added to the silicon lattice. It releases an electron to the conduction band, consequently increasing the quantity of free electrons. The electrons are the majority charge carrier in this case.

Since the semiconductor remains in an electrically neutral state, the excess of free charge carriers has to recombine. This can be exploited by bringing n- and p-doped

materials into contact to create pn-junctions, which are explained in detail in the subsequent section.

Property		Value	Unit
Atomic number	Z	14	
Atomic mass	m_a	28.09	u
Density	ρ_{Si}	2.328	$\mathrm{g/cm^3}$
Crystal structure		diamond	
Lattice constant	a	5.431	Å
Atomic density		$5{\times}10^{22}$	$\mathrm{cm^{-3}}$
Intrinsic charge carrier density	n_i	$1.01{\times}10^{10}$	$\mathrm{cm^{-3}}$
Dielectric constant	ϵ_{Si}	11.9	ϵ_0
Specific resistivity	ρ	$2.3{\times}10^{5}$	$\Omega\,\mathrm{cm}$
Average energy for e/h-pair creation	w	3.65	eV
Indirect band gap	E_{gap}	1.12	eV
Radiation length	X_0	9.36	cm
Mobility electrons	μ_n	1450	$\mathrm{cm^2\,V^{-1}\,s}$
Mobility holes	μ_p	500	$\mathrm{cm^2\,V^{-1}\,s}$
Life time e/h	$\tau_{e/h}$	> 100	µs
Fano Factor	F	0.115	

Table 5.1: Properties of silicon at 300 K [9].

5.3 The pn-Junction

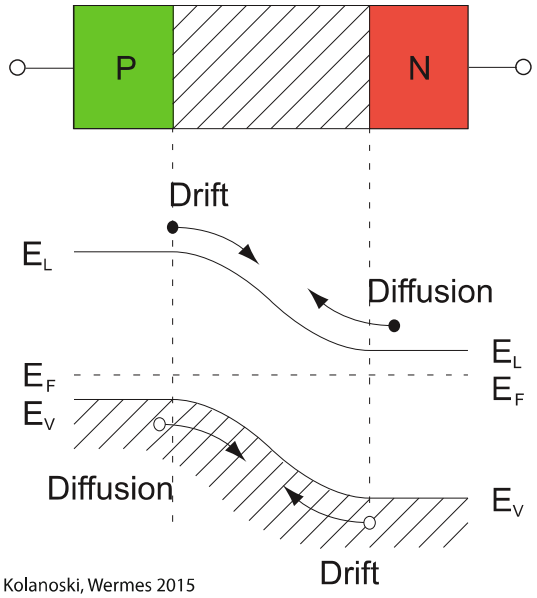


Figure 5.1: Drift and diffusion current of a pn-junction [9].

If a contact between n-doped and p-doped semiconductor material exist, a so-called pn-junction accrues, see Figure 5.1. A high concentration gradient of free charge carriers at the boundary causes a diffusion current. The electrons of the n-doped material diffuse into the p-doped material and recombine with the holes. A zone free of charge carriers develops, called depletion zone. An intrinsic electrical field emerges, creating a drift current, which flows in the opposite direction of the diffusion current. Without an externally supplied bias voltage, the diffusion and drift current reach a stable equilibrium, resulting in a diffusion voltage [9]:

$$V_{bi} = V_T \cdot ln\left(\frac{N_A \cdot N_D}{n_i^2}\right), \tag{5.1}$$

which depends on the thermal voltage $V_T = \frac{k_B T}{e}$ (k_B: Boltzmann constant, e: elementary charge),the doping concentrations N_A and N_D, as well as the intrinsic charge density of the semiconductor n_i.
By solving the one-dimensional Poisson equation (potential Φ, charge density ρ, dielectric constant ϵ_{Si} and the vacuum permittivity ϵ_0):

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_o \epsilon_{\mathrm{Si}}}, \tag{5.2}$$

the width of the depletion zone can determined:

$$w = \sqrt{\frac{2\epsilon_0 \epsilon \cdot V_{bi}}{e} \frac{N_A + N_D}{N_A \cdot N_D}}. \tag{5.3}$$

By applying of an external bias voltage V_{ext}, the width of the depletion zone changes depending on the polarity of V_{ext}:

- **forward bias:** $V_{\mathbf{ext}} > 0$
  The drift current decreases with respect to the diffusion current and the width of the depletion zone shrinks.

- **reverse bias:** $V_{\mathbf{ext}} < 0$
  The diffusion voltage increases, while the diffusion current decreases. The width of the depletion zone grows.

In particular, the reverse bias case is of interest, due to the increase of the detection volume, the depletion zone. The width of the depletion zone for the case of an external bias voltage is given by:

$$w = \sqrt{\frac{2\epsilon_0 \epsilon \cdot (V_{bi} - V_{\mathrm{ext}})}{e} \frac{N_A + N_D}{N_A \cdot N_D}}. \tag{5.4}$$

and can be simplified for $V_{bi} \ll V_{\mathrm{ext}}$ and $N_A \ll N_D$ to:

$$w(V) \approx \sqrt{\frac{2\epsilon_{\mathrm{Si}}\epsilon_0}{eN_A} V_{\mathrm{ext}}} = \sqrt{2\epsilon_{\mathrm{Si}}\epsilon_0 \mu_p \rho V_{\mathrm{ext}}}, \tag{5.5}$$

$$\uparrow$$

$$N_A = \frac{1}{e\rho\mu_p}$$

whereas ρ is the substrate's (lower doping concentration) resistivity.
For the capacitance, the depletion zone is approximated by a parallel plate capacitor, whose interface area is given by A:

$$C(V_{\text{ext}}) = \frac{\epsilon_{\text{Si}}\epsilon_0 A}{w(V_{\text{ext}})} \approx A\sqrt{\frac{\epsilon_{\text{Si}}\epsilon_0}{2V_{\text{ext}}\rho\mu_p}} \tag{5.6}$$

This equation takes effect, if the external bias voltage is smaller than the full depletion voltage of the sensor diode.

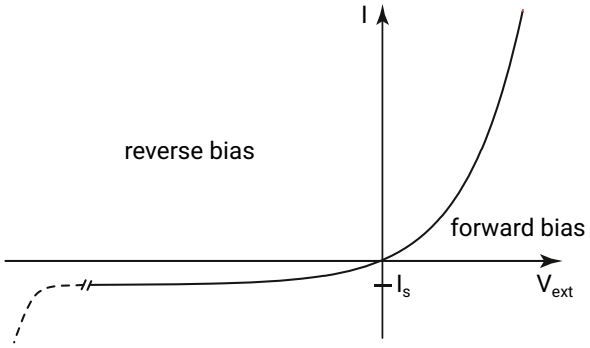


Figure 5.2: Ideal characteristic line of Schottky equation. The dashed line indicates the breakdown at high reverse bias voltages [9] (edited).

For the current-voltage (I-V) characteristic of the diode it is assumed that only the characteristic of the depletion zone determines the current, which is given by the Schottky equation (in ideal form):

$$I(V_{\text{ext}}) = I_S \cdot (e^{\frac{V_{\text{ext}}}{V_T}} - 1), \tag{5.7}$$

whereby I_S is the saturation current.
So-called leakage or dark current is the main source for noise inside a diode, caused by diffusion of free charge carriers from the undepleted volume into the sensitive space charge region and thermal generation of charge carriers inside the depletion zone. The current is highly temperature dependent, according to [14]:

$$I(T) \propto T^2 e^{-\frac{1.21\,\text{eV}}{2k_B T}} \tag{5.8}$$

5.4 Particle Detection: Charge Collection

As introduced in section 4, charged particles or photons (via secondary particles) can ionize the material of a silicon detector. The deposited energy creates electron-hole pairs, which can be collected via diffusion or drift by an electrode. For the reverse bias case, diffusion can be neglected, due to the slower velocity with respect to the drift velocity. This only occurs inside the electric field of a depletion zone, and can be calculated according to the Drude model [9]:

$$\vec{v}_{\text{drift}} = Q_{\text{e/h}} \times \mu_{\text{n/p}} \times \vec{E}. \tag{5.9}$$

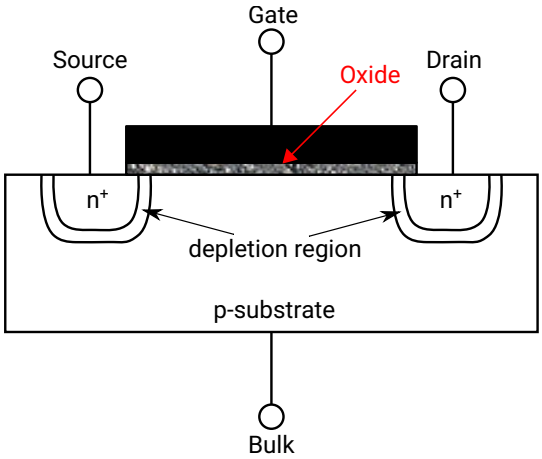
The charge carriers are separated inside the electric field $\vec{E}$ and drift to the charge collection electrodes. Due to the higher mobility μ_n of the electrons inside silicon, they function as the predominantly collected charge to create an influence signal.
The maximum time the charge carriers require to cross the depletion zone is given by:

$$t_{\text{drift}} = \frac{w}{|\vec{v}_{\text{drift}}|}, \tag{5.10}$$

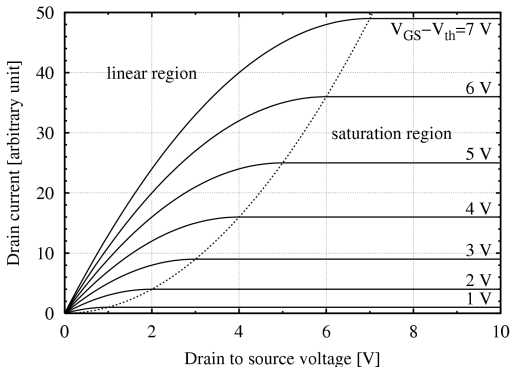
and is for the subsequent introduced detector diode on the ns level.

5.5 MOSFET

The metal-oxide-semiconductor-field-effect transistor, short MOSFET, belongs to the group of field-effect transistors. It has an isolated gate and is a voltage-controlled switching element. Two types of MOSFET exist: n-channel (NMOS) and p-channel (PMOS), which can be combined to a complementary MOS (CMOS) circuitry realized on the same substrate. To accomplish this, NMOS and PMOS transistors are embedded in specially doped regions, so-called wells. The benefit of CMOS technologies are the logic elements, as a current flows only in the moment of switching reducing the power dissipation. The structure of an NMOS transistor is illustrated in Figure 5.3a and is used to explain its functionality.



(a) Cross section of an NMOS transistor.



(b) MOSFET drain current vs. drain-to-source voltage [15].

Figure 5.3: NMOS transistor.

Two heavily-doped n^+ regions (source and drain) are diffused into a lighter doped p-well, called substrate or bulk. At the surface between source and drain is a gate electrode, separated from the silicon by a thin dielectric material, typically silicon dioxide (SiO_2). In the state of thermal equilibrium, the p-substrate and the n^+ doped regions of source and drain form a pn-junction. The gate and the p-substrate form a parallel plate capacitor. By applying a positive potential at the gate, positive charge is accumulated at the gate and negative charge in the substrate beneath it, whereas the latter is created by mobile holes pushed down into the substrate, leaving behind fixed-donor atoms.
A control voltage between gate- and source-electrode V_{GS}, allows the development of a channel between source and drain and the current (I_D) flow can be adjusted.
The transistor can be operated in three different modes, introduced in the following (channel-length modulation effects are neglected):

- **Sub-threshold mode:** $V_{\mathrm{GS}} < V_{\mathrm{threshold}}$
  The transistor is off and can be used as switch if V_{GS} exceeds $V_{\mathrm{Threshold}}$. As a turned-off switch only a weak inversion current flows, called sub-threshold leakage

current [16]:

$$I_D = \frac{W}{L} I_{D0} \cdot \left[e^{\frac{V_{\mathrm{GS}}}{nV_T}} \right] \tag{5.11}$$

- **Linear mode:** $0 < V_{\mathrm{DS}} < (V_{\mathrm{GS}} - V_{\mathrm{threshold}})$
  The transistor is turned on and a channel is created between drain and source, allowing a current flow. The transistor operates as resistor, which is controlled by the voltage between drain and source. The current flow increases with this voltage according to [16]:

$$I_D = \frac{\mu_0 C_{ox} W}{L} \cdot \left[(V_{\mathrm{GS}} - V_{\mathrm{threshold}}) - \frac{V_{\mathrm{DS}}}{2} \right] \cdot V_{\mathrm{DS}} \tag{5.12}$$

- **Saturation mode:** $0 < (V_{\mathrm{GS}} - V_{\mathrm{threshold}}) \leqq V_{\mathrm{DS}}$
  At this point the current I_D is independent of V_{DS} and is primarily controlled by the gate-source voltage [16]:

$$I_D = \frac{\mu_0 C_{ox} W}{2L} \cdot (V_{\mathrm{GS}} - V_{\mathrm{threshold}})^2 \tag{5.13}$$

Definition of new parameters and constants:

- $V_{\mathrm{DS}} = V_{\mathrm{drain}} - V_{\mathrm{source}}$: voltage between gate and source
- $V_{\mathrm{threshold}}$: transistor threshold voltage
- μ_0: surface mobility of the channel
- C_{ox}: capacitance per unit area of the gate oxide
- W: effective channel width
- L: effective channel length

Part II

HV-CMOS Sensors

6 Pixel Sensors

To date, silicon sensors represent the foundation of almost every tracking detector of modern particle physics experiments, like ATLAS or CMS. The innermost layers are made up by pixel sensors, which are mostly hybrid sensors. In the following, an introduction to these sensors as well as other technologies is given.

6.1 Hybrid Sensors

Hybrid sensors consist of a pixel sensor bump bonded to a readout ASIC (Application-Specific Integrated Circuit). The possibility to develop sensor and readout chip separately, allows a distinct characterization of both and fine tuning of each component. Decades of research on hybrid sensors set a reliable foundation of knowledge about the technology, making it the baseline for experiments like ATLAS. Advantages in terms of radiation hardness as well as high granularity are opposed by the natural limits of a high material budget, due to the required bump bonding, and the high cost of non-commercial processes.

6.2 Monolithic Active Pixel Sensors

The MAPS technology represents a different approach to pixel detectors. Here, the complete readout circuitry as well as the active sensor are integrated in one chip. The application of commercial CMOS processes reduces the production cost and material budget.
An example of a MAPS is the ALPIDE pixel sensor chip [17], which is used for the upgrade of the ALICE Inner Tracking System. The active sensor volume of the pixels is a high-resistivity epitaxial layer. The charge is collected via diffusion by an n-well implant, while additional n- and p-wells host the in-pixel circuitries. However, diffusion is a slow process compared to charge collection via drift, limiting time resolution to the microsecond range (event time resolution of 2 µs [18]), whereas high occupancy experiments like ATLAS require a time resolution on the nanosecond level.

6.3 High-Voltage Active Pixel Sensor Concept

HV-MAPS combine the advantages of hybrid sensors and MAPS. The sensors are produced in commercially available HV-CMOS processes, which reduces the cost significantly. The low material budget can additionally be reduced by thinning the sensors down to 50 µm. A reverse bias voltage in the order of −60 V is supplied to enhance the fast charge collection via drift in the detection volume, the depletion zone. A time resolution on the nanosecond level can be achieved. The general concept is represented

in Figure 6.1, displaying the deep n-well inside the p-substrate forming the sensor. The in-pixel electronics is implemented inside the deep n-well. The NMOS and PMOS transistors are decoupled from the deep n-well by additional shallow p- and n-wells, respectively.

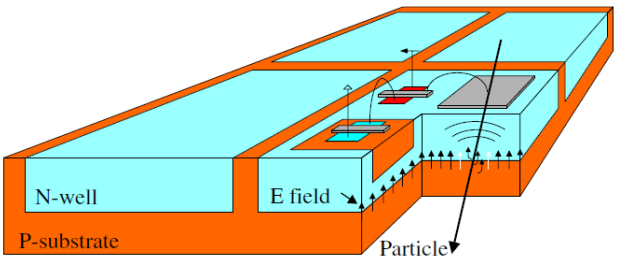


Figure 6.1: HV-MAPS concept [19].

6.3.1 Development of HV-MAPS

The first HV-MAPS prototypes were developed for the Mu3e experiment. This technology was chosen for the ambitious construction of an ultra-low material budget tracking detector [1].
Based on several generations of prototypes for Mu3e, ATLASPix1 was developed (see Figure 6.2). It is a prototype for a demonstrator for the ATLAS ITk upgrade, which has to meet the requirements of the high-luminosity operation of the ATLAS experiment (see section 3.1.1).
The benefit of high radiation hardness [20], low cost of commercially available HV-CMOS processes and low material budget demonstrate a promising future for upcoming tracking detectors, which can replace sensors of different types inside a tracking system.

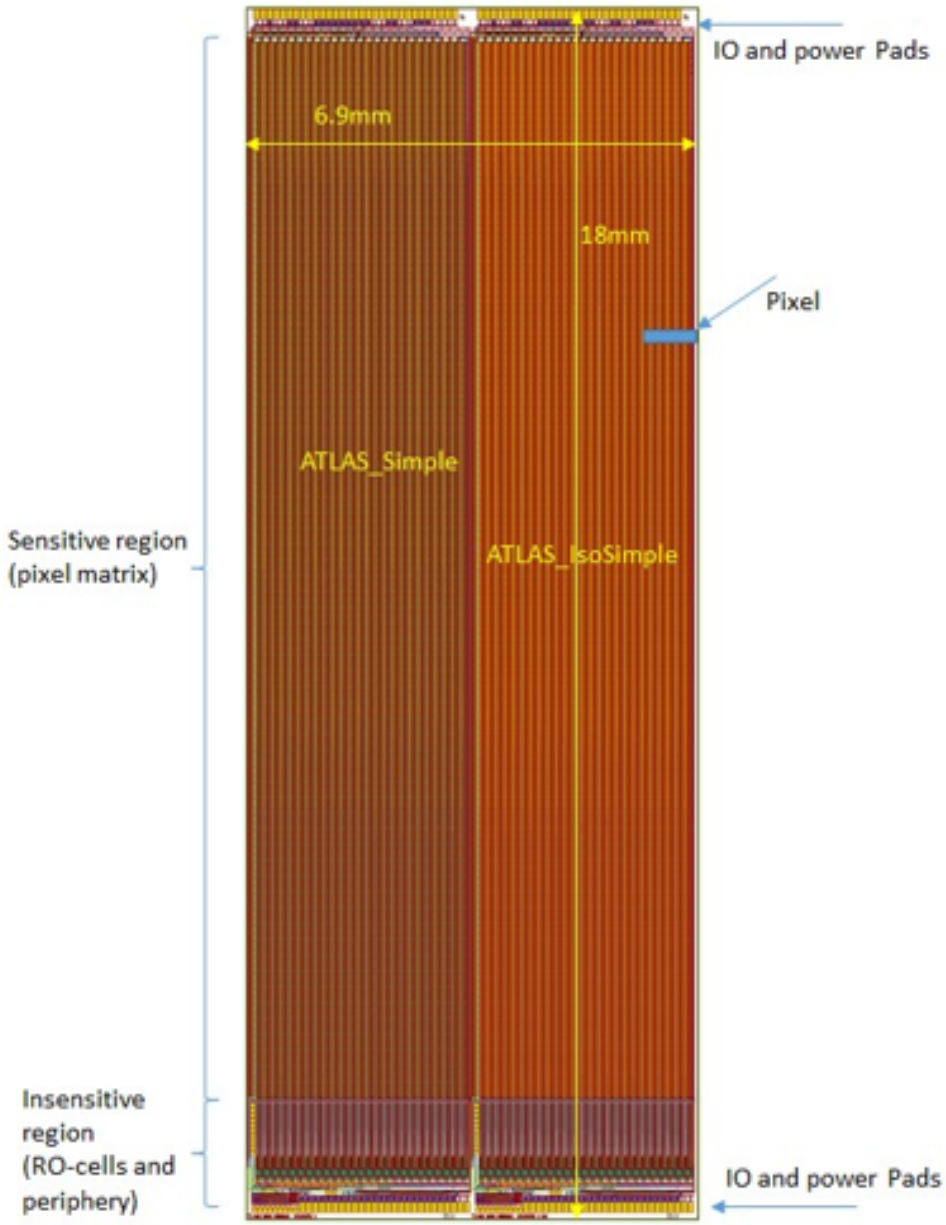


Figure 6.2: Schematic of ATLASPix_Simple and ATLASPix_IsoSimple [21].

7 ATLASPix1

ATLASPix1 has been designed for the ATLAS HV-CMOS project and was produced by AMS in the aH18 process with a minimum transistor gate length of 180 nm. For further increase of radiation hardness, NMOS transistors have a circular design. The radiation tolerance is expected to fulfill at least the ATLAS ITk requirements of the outermost pixel layer (see section 3.1.1).
The reticle with a size of about $21.3 \times 22\,\mathrm{mm}^2$ contains four large chips: MuPix8, ATLASPix_M2, ATLASPix_Simple and ATLASPix_IsoSimple.
This thesis focuses on the ATLASPix_Simple and ATLASPix_IsoSimple, which differ only by an additional deep p-well implant in the deep n-well in the case of the ATLASPix_IsoSimple. Here, the deep p-well isolates the PMOS transistors of the comparator, which are once more embedded in a shallow n-well. This allows for an in-pixel CMOS based comparator in contrast to the ATLASPix_Simple, which uses a purely NMOS based comparator. Otherwise, both chips have an identical structure.
The readout structure of ATLASPix1 is illustrated in Figure 7.1.

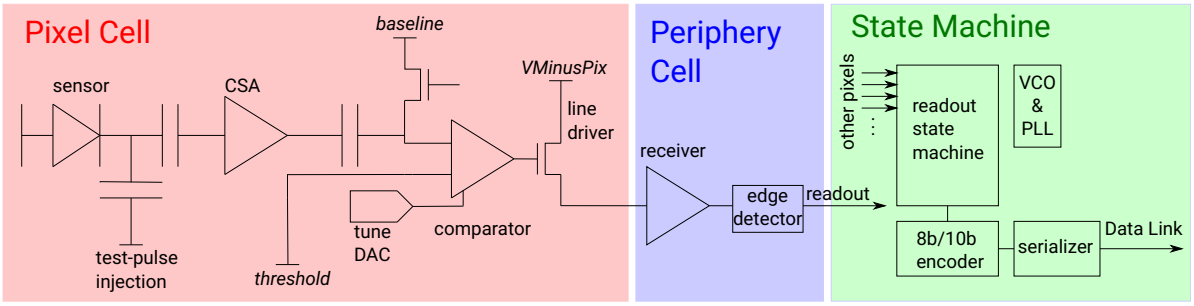


Figure 7.1: Schematic of the ATLASPix1 readout concept.

The sensor has an active pixel matrix of 25×400 pixels with a pixel size of $130 \times 40\,\mu\mathrm{m}^2$, resulting in an active area of:

$$\mathrm{A}_{\mathrm{active}} = (25 \times 400) \times (130 \times 40\,\mu\mathrm{m}^2) = 0.52\,\mathrm{cm}^2. \tag{7.1}$$

Each pixel has a point-to-point connection to an associated periphery cell. The dense line routing of 400 pixels per column is realized by placing two periphery cells with a size of $62.5 \times 4.2\,\mu\mathrm{m}^2$ side by side per column, resulting in a total area of:

$$\mathrm{A}_{\mathrm{periphery}} = (25 \times 400) \times (62.5 \times 4.2\,\mu\mathrm{m}^2) = 0.0263\,\mathrm{cm}^2. \tag{7.2}$$

In the digital part all required hit information, namely pixel addresses and time stamps, are generated and the on-chip state machine controls the column drain readout. The zero suppressed digital information is 8 b/10 b encoded, serialized and sent out via one 1.25 Gb/s Low-Voltage Differential Signaling (LVDS) link.

Voltages like threshold and baseline are generated via voltage digital-to-analog converters (DACs). To guarantee stable operational voltages, additional external reference voltages are supplied.

7.1 Pixel Cell

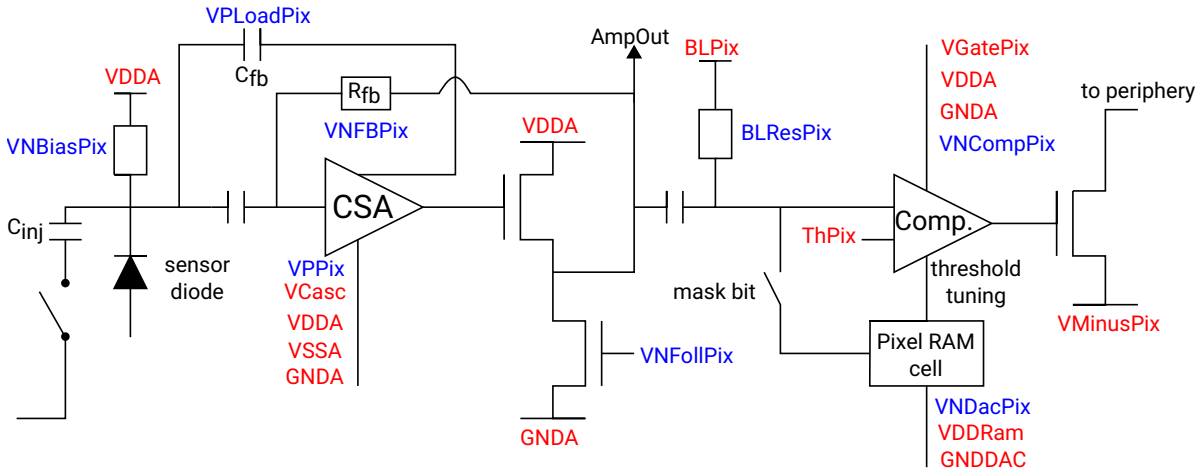


Figure 7.2: Schematic of the ATLASPix1 pixel cell. Blue names indicate DACs, red names indicate voltage levels.

The pixel cell electronics (see Figure 7.2) is embedded in the deep n-well, unaffected from the diode potential, as "floating logic". Required potentials for the p-substrate and the pixel logic (*VDDA*, *VSSA* and *GNDA*) are supplied externally.
Created by ionization, the charge carriers drift to the charge collection electrodes, creating an influence signal. The signal charges the feedback capacity C_{fb}, whereas the resistive feedback R_{fb} subserves its discharging process. The signal itself is amplified by a charge sensitive amplifier (CSA), whose feedback loop is stabilized by a subsequent source follower.
The amplified signal is capacitively coupled to the baseline, determined by the voltage level *BLPix*, removing all DC components of the signal. Furthermore, the baseline restoration acts as a high pass filter.
In a simplified representation, the unipolar pulse shaping of an amplifier circuitry can be described as a CR-RC shaper. The high-pass is referred to as "differentiator" with time constant τ_{diff} and the low-pass as "integrator" with time constant τ_{int}. The input signal of the detector electrode for a CSA can be approximated by a step function, resulting in a convoluted function with the prior mentioned CR-RC part [22]:

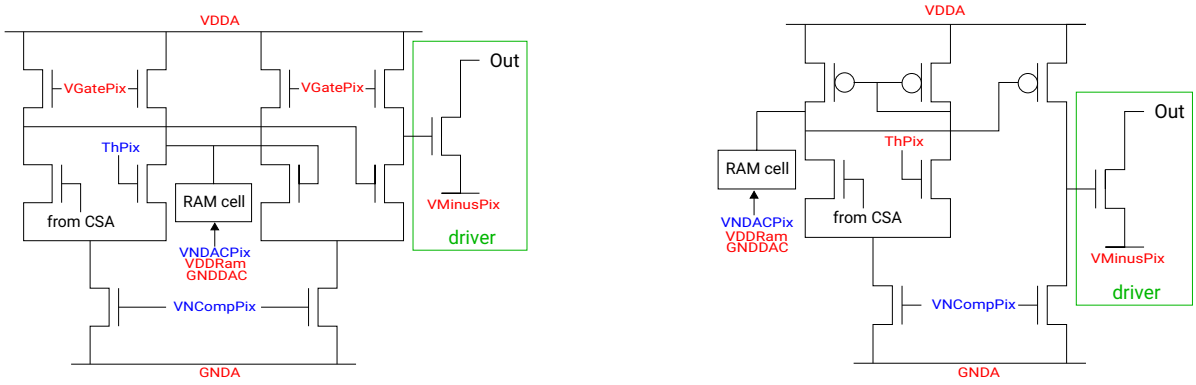
$$V(t) = V_0 \frac{\tau_{\text{int}}}{\tau_{\text{diff}} - \tau_{\text{int}}} \left(e^{-\frac{t}{\tau_{\text{diff}}}} - e^{-\frac{t}{\tau_{\text{int}}}} \right). \tag{7.3}$$

In reality, the amplification is more complex, including the feedback loop, which has a significant impact on the pulse shaping. The resistive feedback flattens the steepness of the falling edge, whereas the capacitive feedback increases steepness of the rise of the leading edge. Summarized, for the signal pulse itself a triangular shape can be

anticipated.
The in-pixel comparator compares the signal level with a chosen threshold, ThPix, discriminating it to a rectangular shaped normed pulse.
The last stage is the signal driver to the periphery cell. The voltage amplitude of the line signal is in the range from VDD (power domain of digital part) to about VMinuspix and can be approximated with:

$$V_{\text{line signal}} \approx \underbrace{\text{VDD}}_{\text{high level}} - \underbrace{\text{VMinusPix}}_{\text{ground level}}. \tag{7.4}$$

As previously mentioned, ATLASPix_Simple and ATLASPix_IsoSimple have different comparator designs.
For the ATLASPix_Simple comparator, shown in Figure 7.3a, a purely NMOS-based comparator is used, whose logic is implemented in a shallow p-well to decouple it from the deep n-well. In addition, an extra voltage level, called VGatePix, is necessary, which concedes the transistors to switch and limits the current flow.
On the one hand the ATLASPix_IsoSimple comparator, shown in Figure 7.3b, consists of NMOS- and PMOS-transistors, forming a CMOS-based circuitry. To decouple the PMOS-transistors from the deep n-well, they are embedded in a deep p-well. Advantages of this approach are the possibility of a higher radiation tolerance and a lower power consumption with respect to the purely NMOS-based comparator [21].
The required bias voltages for the pixel cell are listed in Table 7.1.



(a) NMOS-based comparator

(b) CMOS-based comparator

Figure 7.3: NMOS- and CMOS-based comparator versions of ATLASPix_Simple with line driver.

A test output for the CSA, called AmpOut, is implemented in each pixel cell of column zero. This requires an additional source follower driver, steered by the DAC VPFoll. The signal has to be terminated by a 1 kΩ resistor, which is placed on the custom designed printed circuit board (PCB), the Insert PCB of the ATLASPix1, see section 8.2.
To test the performance of pixel and periphery cell the possibility of a signal injection is implemented in each pixel cell. Realized by a capacitor before the CSA, an external voltage charges the capacitance, which discharges after release into the deep n-well. The injection method can be selected for individual pixels.

Bias Voltage	Source	Function
VPPix	DAC	Main current source for CSA
VPLoadPix	DAC	Feedback Capacitor and amplifier load
VNFBPix	DAC	Resistive feedback
VNFollPix	DAC	Feedback stabilization by source follower
VCasc	Internal (fixed)	Amplifier cascade voltage
BLPix	Internal/External	Reference voltage for baseline
BLResPix	DAC	Resistor of baseline restoration
VPFoll	DAC	AmpOut test output control
ThPix	Internal/External	Threshold of comparator
VGatePix	External	Gate level for NMOS comparator
VNCompPix	DAC	Current source of comparator
VMinusPix	External	Ground level of driver
VDDRAM	External	High level for pixel RAM cells
VNDACPix	Internal/External	Reference voltage for tuning

Table 7.1: Bias voltages for the pixel cell.

7.2 Periphery Cell

The incoming low voltage signal from the line driver of the pixel cell (see Figure 7.4) is converted into a CMOS amplitude (GND to VDD) by the receiver, controlled by the bias voltages VNBiasRec and VPBiasRec.
Subsequently, the signal is digitized by the edge detector. The short rectangular pulse is synchronously to the leading edge of the comparator signal, raising the hit flag. The column and row addresses as well as the two time stamps of the rising and falling edge of the comparator signal are stored.

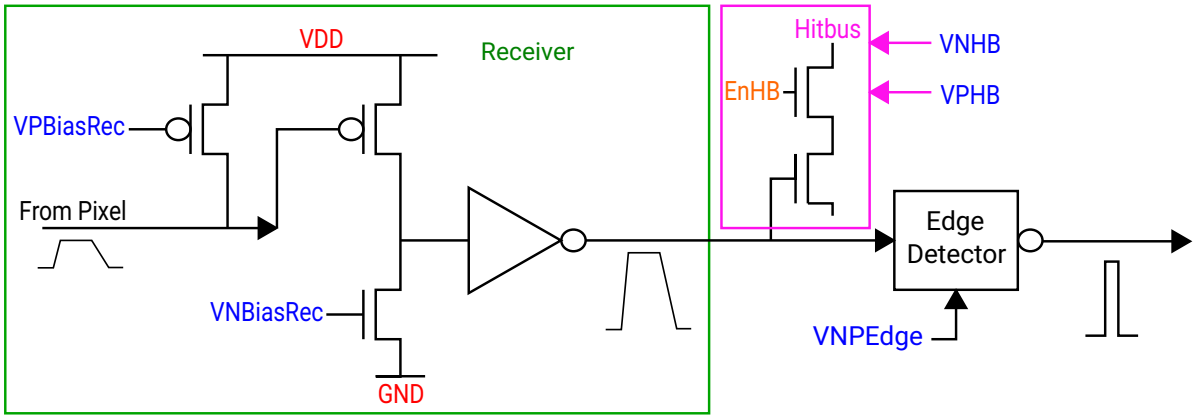


Figure 7.4: Schematic of the ATLASPix1 Periphery Cell. Blue names indicate DACs, red names indicate voltage levels.

The two time stamps TS1 (10 bit) and TS2 (6 bit) are derived from the same base clock, whereas only the TS1 is sampled after a minimum of two clock cycles (one clock cycle equals 8 ns) instead of one. The sampling speed of each time stamp can be steered by clock dividers (ckdivend and ckdivend2) into integral multiples of the base clock.

To achieve the best time resolution the clock divider of TS1 is set to zero. The time stamps are Gray encoded [23] on-chip. Consequently, only a single bit flip is required per clock cycle, which reduces the power consumption and errors by sampling the hit information during a bit transition.
The information of two time stamps enables the calculation of the time-over-threshold (ToT), which is linearly correlated to the signal amplitude in a certain operation range:

$$\text{ToT} = TS2 \times (1 + ckdivend2) - TS1 \times (1 + ckdivend) \tag{7.5}$$

This gives the possibility to correct for time walk to achieve better time resolution. Time walk depends on the time of arrival of a signal correlated to its amplitude, illustrated in Figure 7.5. The time difference for different threshold crossings of the signal amplitudes (Δt), according to equation 7.3, is associated to a concurrently different ToT.

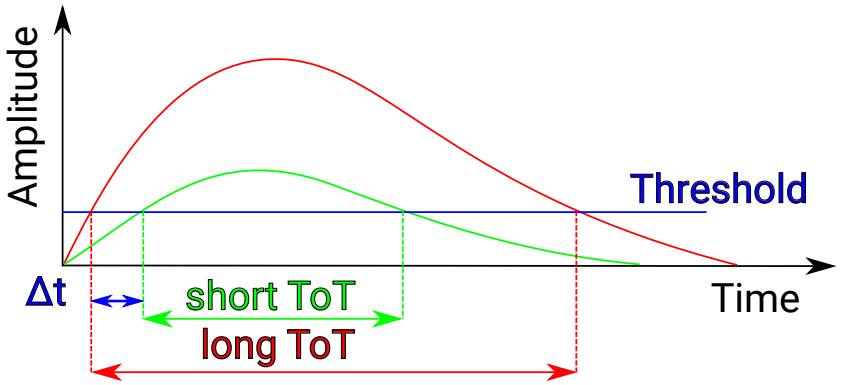


Figure 7.5: Concept of time walk [24].

The Hitbus is a test output of the signal after the receiver, whose driver can be controlled by the DACs VNHB and VPHB. Two signal lines per column are reserved for the Hitbus from pixel 0 to 199 and 200 to 399 (row address). The respective output is a logical OR of a signal from pixel blocks of 200 each. A disadvantage of this method, is caused by a design mistake in the masking implementation. If one pixel of such a block is masked, the Hitbus is disabled for its entire pixel block.
The allocated bias voltages for the periphery cell are summarized in Table 7.2.

Bias Voltage	Source	Function
VPBiasRec	DAC	Input level of receiver (PMOS)
VNBiasRec	DAC	Input level of receiver (NMOS)
VNPEdge	DAC	Current source for edge detector
VPHB	DAC	Hitbus test output control (PMOS)
VNHB	DAC	Hitbus test output control (NMOS)

Table 7.2: Bias voltages of the periphery cell.

7.3 Readout State Machine

The readout is controlled by the state machine. If a hit is registered in the periphery cell, a signal is sent to the end-of-column (EOC) cell. Per column two EOC cells are utilized, shared by blocks of 200 pixels each. Due to the priority encoder, the hit with the lowest row address in a block is read out first, subsequently followed by upper ones. If the EOC cell contains hit data, it is transmitted to the serializing logic. With this method only one hit per readout cycle per EOC cell can be read out, not retaining the chronology of the hits.
The full sequence of logical states of the readout state machine is explained in [25].
The readout speed of the state machine is adjustable via the external supplied reference clock. The internal clock is synchronized to the reference clock by a phase-locked loop (PLL). The sensor is designed for an operation with a reference frequency up to 160 MHz, whereas a reference frequency of 125 MHz is used primarily. The PLL consists of a voltage-controlled oscillator (VCO), configurable by the bias currents VPVCO and VNVCO, a phase detector (PD) and a charge pump. The VCO is implemented as a ring oscillator with 8 differential buffer stages and an inverted feedback loop. The internally produced clock is compared by the PD with the reference clock. A detailed explanation of the PLL is given in [26]. The bias voltages for the PLL are listed in Table 7.3.

Bias Voltage	Source	Function
VPVCO	DAC	VCO bias
VNVCO	DAC	ChargePump Bias
VPPump	DAC	ChargePump Bias
EnablePLL	DAC	Enables PD
Invert	DAC	Clock inverter

Table 7.3: Bias voltages of the PLL.

The clock frequency of the state machine ($f_{\text{state machine}}$) itself is set by half the externally supplied reference frequency, which can be slowed down by the register value of the clock divider *timerend*:

$$f_{\text{state machine}} = \frac{f_{ref}}{2 \times (1 + timerend)}. \tag{7.6}$$

To sample the ToT in the correct way, the state machine has to be slowed down [24] by the maximum *timerend* value of 15. Otherwise the hit is already read out, before the TS2 is sampled. In addition, the register value *slowdownend* is set to the same value to gain additional time by increasing the quantity of repeated states in the state machine. The configuration bits for the state machine are listed in Table 7.4.

Register DAC	Effect
timerend	Clock divider to slow down state machine
resetckdivend	Quantity of synchronization cycles
slowdownend	Maximum number of wait cycles after LoadPixel
ckdivend	Clock divider for TS1
ckdivend2	Clock divider for TS2
sencounter	Sets state machine output to 24 b counter
maxcycend	Limit of hits per readout cycle

Table 7.4: Register DACs of the state machine.

The readout scheme from the state machine to the output link is illustrated in Figure 7.6. The state machine sends the hit information to the differential current mode logic (Dcl) serializer as 8 b/10 b encoded data. The necessary clocks on the chip are derived from the internal clock of the PLL and distributed by the clock generation tree. The readout link hosts the possibility of a pre-emphasis to increase the slew rate of the data signal. At the end, the serial output sends out the data as LVDS signal at 1.25 Gb/s. The register DACs and bias voltages of the Dcl serializer are listed in Table 7.5.

Bias Voltage	Function
VPDcl	Global Dcl bias
VNDcl	Global Dcl bias
VPDelDcl	Delay for Dcl clock
VNDelDcl	Delay for Dcl clock
VPDelDclMux	Delay for Dcl mux clock
VNDelDclMux	Delay for Dcl mux clock
VNLVDS	Strength of LVDS buffer
VNLVDSDel	Strength of pre-emphasis
VPDelPreEmp	Delay of pre-emphasis
VNDelPreEmp	Delay of pre-emphasis
Serializer_reset_n	Serializer reset
Aurora_Reset_n	8 b/10 b encoder reset

Table 7.5: Bias voltages and register DACs of the Dcl serializer.

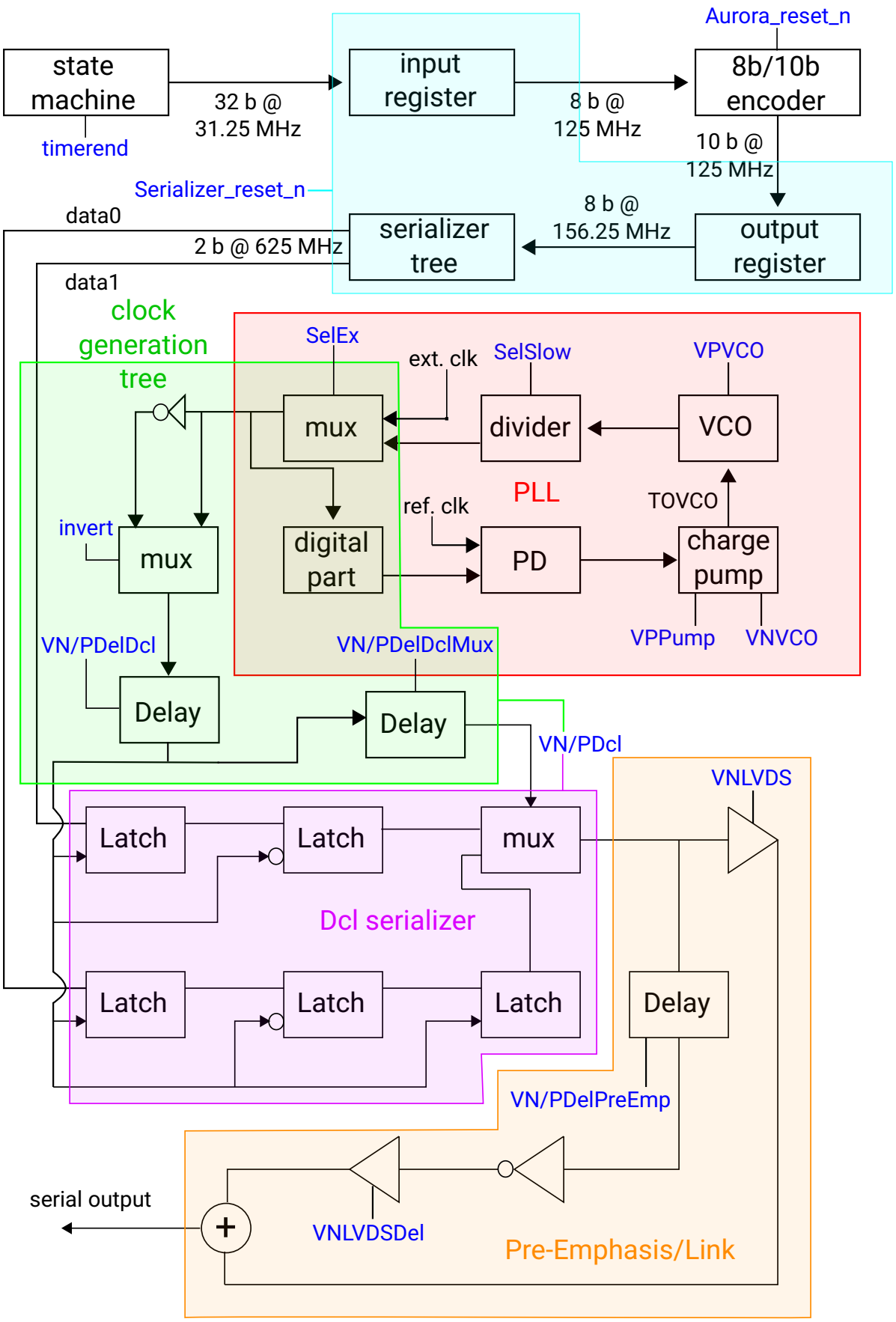


Figure 7.6: Readout scheme adapted from [25] and [26].

8 Measurement Setup

In the subsequent sections, the components of the sensor characterization setup as well as the utilized signal sources are introduced.

8.1 Motherboard PCB

The motherboard printed-circuit-board (PCB) is the base of all characterization setups in the Heidelberg HV-CMOS group (see Figure 8.1). Several types of sensors can be investigated with the same setup. An insertable PCB (highlighted in white), explained in the subsequent section, is connected with the motherboard via a mini edge card socket [27].
In the following a detailed explanation of the input/output (I/O) interface of the motherboard PCB is given, illustrated in Figure 8.1. For this thesis the external power version of the motherboard is used, which is able to bypass the on-board power regulators, in order to monitor the main supply voltages directly.

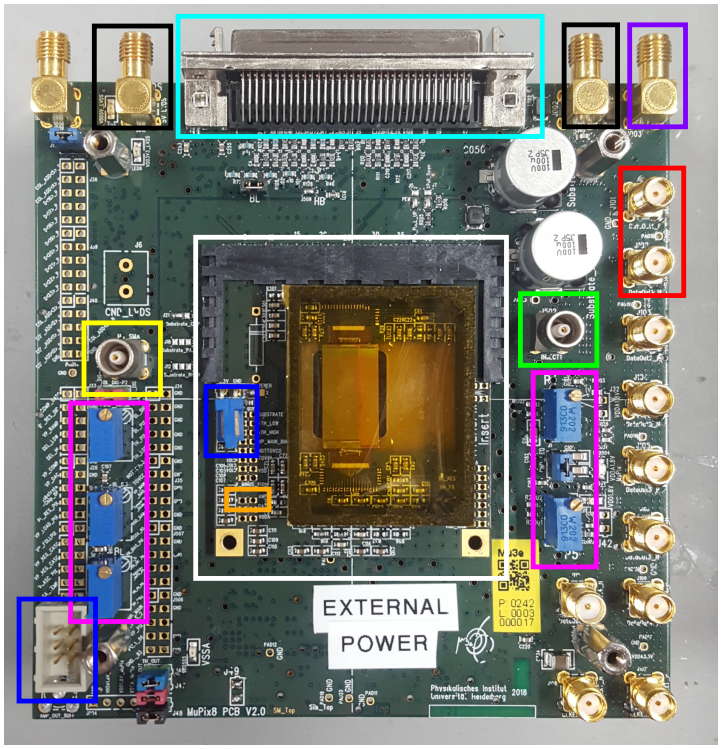


Figure 8.1: Motherboard PCB with the Insert PCB. Color coding explained in the text.

The purple highlighted (top right) SMA connector is the input for the high voltage. In black, the power input for the LVDS on-board receiver and repeater and the power

input for the so called Low-Voltage (LV) are displayed. Both voltages have an input level of 5 V, stepped down by on-board power regulators.
In magenta, potentiometers to tune required external reference voltages are marked. With them the voltages VDD and VDDA, used as reference voltages for on-board threshold DACs, as well as the external voltages VMinusPix, BLPix and VDDRAM can be fine-tuned.
The main bias voltages for the sensor are supplied via the dark blue surrounded connectors: VDD, VDDA, VSSA and VGatePix (only required by the ATLASPix1_Simple),
Several test outputs are supported by the motherboard: The LVDS link for the data output (red), the injection signal (green), the Hitbus (yellow) and the AmpOut (orange) can be accessed.
In bright blue highlighted is the SCSI-3 connector, which is the interface between the motherboard and the DAQ PC.

8.2 Insert PCB

The insertable PCB (called "Insert PCB") for the ATLASPix1 [28] is designed such that either the ATLASPix1_Simple or the ATLASPix1_IsoSimple can be bonded, illustrated in Figure 8.2.

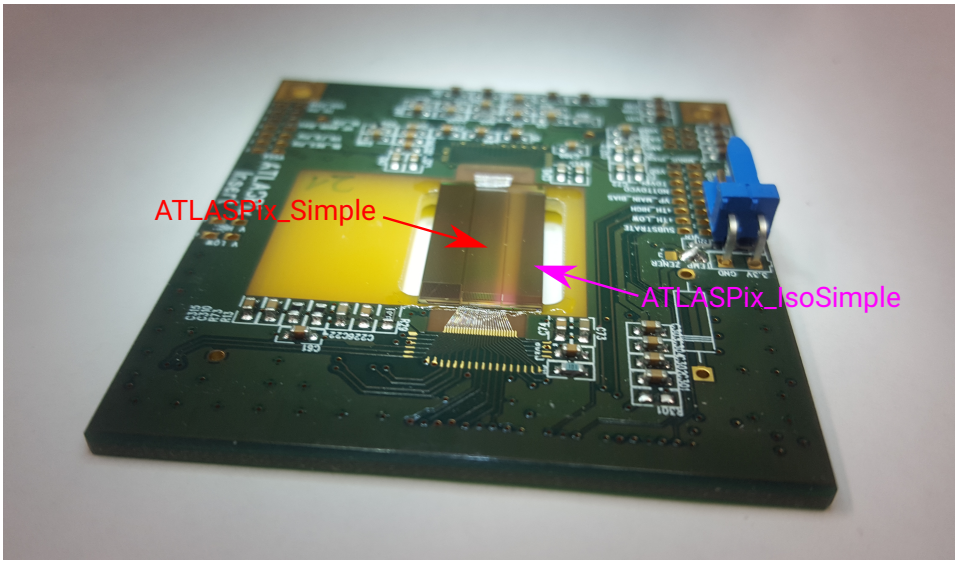


Figure 8.2: Insert PCB.

The general idea of an Insert PCB is that different versions of the same sensor or other sensor types can be characterized with the same setup. This minimizes the systematic errors and enables the re-usability of the motherboard PCB. This enables an easier change of sensors in case of failures. Except for the sensor, the Insert PCB only hosts passive components. To safeguard the sensor by exterior influence like dust and protecting the fragile wire bond connections, a 3D-printed frame is mounted on top of the insert, sealed by a polyimide tape.

8.3 Timing Reference: Tile PCB

A scintillating tile, read out by a silicon photomultiplier (SiPM), is used to provide reference time information. The scintillating material BC-408® [29] is provided by Saint-Gobain Crystals® and cut into a cuboid with dimensions of $20 \times 20 \times 4\,\mathrm{mm}^3$. Therefore, the tile features a larger active area than the ATLASPix1, covering its whole active region.
The tile is wrapped in a mantle of aluminum polyimide laminate, which reflects the light on all surfaces except at the interface of tile and SiPM. In addition, the tile is placed in a 3D printed frame and once again covered by black vinyl tape and black acrylic paint for further light tightness.
The SiPMs are commercially available MPPCS13360-3050CS® from Hamamatsu Photonics K.K.® with a sensitive area of $3 \times 3\,\mathrm{mm}^2$ and a pixel pitch of 50 µm.
The so-called Tile PCB [30] supports up to two tiles with a logic output with an adjustable threshold for the comparator, respectively. The discriminated signal is forwarded to a NIM output, which can be directly connected to a SCSI control card [31]. The latter one serves as interconnection between the motherboard and the FPGA, connected by a SCSI-3 cable.
With a setup of two tiles a coincidence time resolution of about 2 ns [24] was measured. The time information is sampled in 2 ns bin sizes by an FPGA (see section 8.4).

(a) Tile-PCB (b) Tiles

Figure 8.3: Tile PCB and tile with light guide [24].

8.4 Field-Programmable Gate Array Interface

The Field-Programmable Gate Array, short FPGA, is an integrated circuitry with a discrete quantity of configurable logic elements. The Stratix IV GX Development Board [32] is directly connected with the DAQ computer via a PCI-e socket. It provides an adjustable reference clock (default 125 MHz) and handles the configuration as well as the data processing of the HV-CMOS sensor.

8.5 Data Acquisition System

The data acquisition (DAQ) software for a sensor characterization setup is a common development for the MuPix telescope [33], which can handle up to 8 sensors at once, and the single sensor characterization setup. In case of the ATLASPix1, the software is adapted for the demands of operating a single ATLASPix_Simple or ATLASPix_IsoSimple.

8.6 Radioactive Isotopes as Signal Source

In addition to the signal injection other signal sources like radioactive isotopes are utilized. In the following, the characteristics of radioactive sources used in this thesis are presented.

Strontium-90

Strontium-90 [34, 35] is an unstable isotope decaying via the beta minus decay to yttrium-90 with a half-life time of 28.79 years. The end-point energy of the free electron amounts to 0.546 MeV. However, the decay product yttrium-90 [36] itself is instable, too. With a half-life time of 64 h and an end-point energy of 2.2787 MeV, it decays again via the beta minus decay into zirconium-90, which is stable.

Iron-55

Iron-55 [34, 37] decays via electron capture to manganese-55 with a half-life time of 2.737 years. Subsequently, the vacancy is compensated by an electron of a higher shell. This transition emits the energy in form of an Auger electron in 60 % of the cases. The released energy amounts to 5.19 keV with a low probability of the electron to leave the source. For that reason, the contribution of the Auger electron to the Iron-55 spectrum is neglected.
Other processes with high probability of occurrence are photon emissions due to electron capture of the K-shell. The transitions from the $K_{\alpha 1}$ and $K_{\alpha 2}$ occur with a probability of 16.2 % and 8.2 %, releasing an energy of 5.898 75 keV and 5.887 65 eV respectively. Due to the small energy difference of the transitions, they can be treated as a mono-energetic line of 5.9 keV.
The last transition of K_{β} line is a magnitude less in probability with 2.85 % and releases an energy of 6.490 45 keV.
For this work iron-55 is assumed to be a monochromatic X-ray source of 5.9 keV.

8.7 Climate Chamber

For investigation of the ambient temperature dependence on the sensor the Binder MK53 [38] climate chamber is used. The ambient temperature can be adjusted down to −40 °C. The climate chamber is acting like a Faraday cage, shielding from exterior influences. However, voltage peaks are observed on the test output signals, induced by the climate chamber, which results in the loss of DAC settings. To minimize the erroneous impact

on the measurements a porcelain plate is directly seated beneath the test setup. This reduced the observed effect, but not exterminating it. All required cabling is introduced to the climate chamber via a grommet on top, sealed by a synthetic material plug. Controlled by a LabView program on an external connected computer, the ambient temperature can be adjusted and read out. In addition, a water condensation protection is implemented to prevent electric shorts and corrosion. To ensure stable measurement conditions and verify the set temperature, a Pt-100 [39] is used for cross-check, resulting in a maximum deviation from the set and LabView® given temperature by less than 1 °C, which is taken as uncertainty for the following measurements.

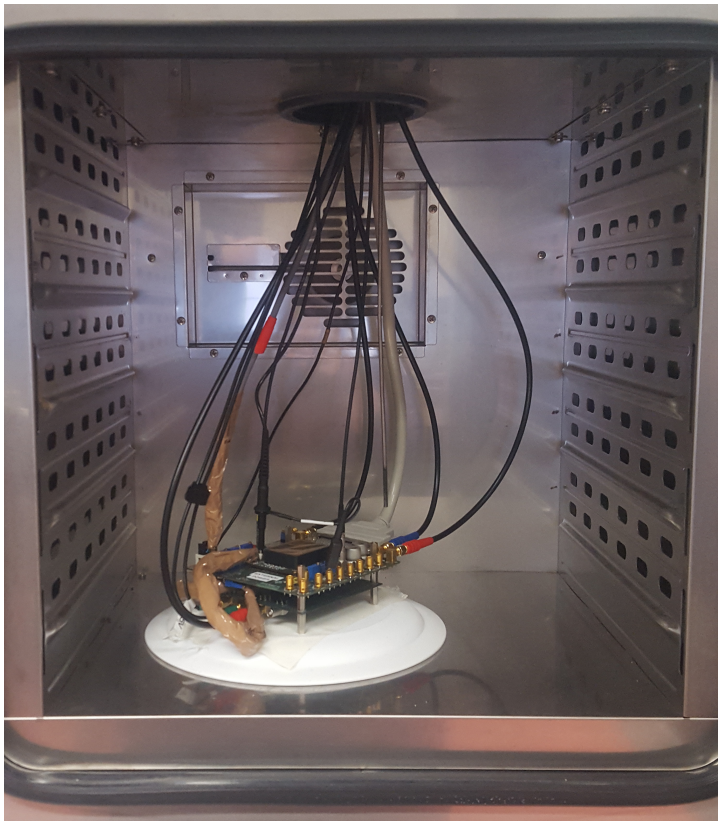


Figure 8.4: Climate chamber.

Part III

Performance Study on ATLASPix1

9 Characterization of ATLASPix_Simple

For the characterization of the sensor components, analog measurements are performed, meaning the investigation of the pulse shape parameters of test outputs as well as the injection with an oscilloscope. The AmpOut is used to study the performance of the amplification stage, whereas the Hitbus is the discriminated signal accessed after the receiver. The Hitbus is used to investigate the baseline restoration, the comparator performance and the signal transmission from the pixel cell to the periphery cell. In addition, the power consumption is monitored for each sensor configuration.

9.1 Principle of Sensor Characterization

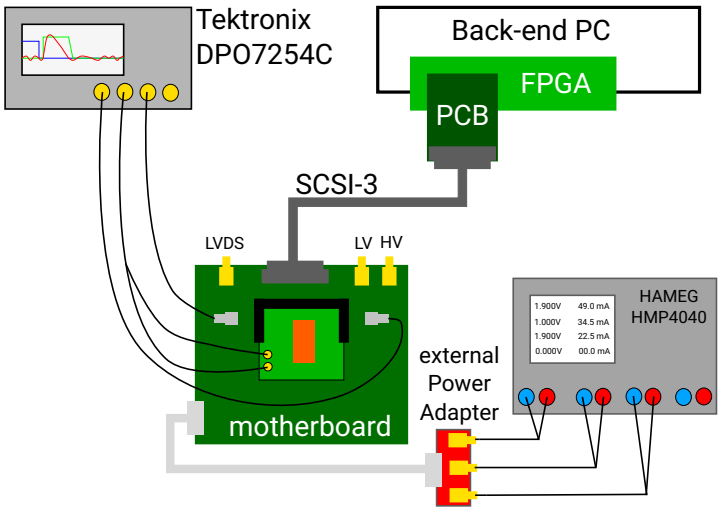


Figure 9.1: Sketch of setup for analog measurements.

The test setup for the following measurements is illustrated in Figure 9.1. The sensor has a dedicated power supply to monitor the DAC's influence on the power consumption for each measurement. A detailed explanation is given in section 9.2.
The performance of the analog circuitry in the pixel cell as well as the digital circuitry in the periphery cell is primarily inspected with a test pulse provided via the injection circuitry. The measurement of the injection pulse as well as the test outputs, Hitbus and AmpOut, is done with a Tektronix DPO7254C [40] oscilloscope. To prevent current flow into the oscilloscope instead of the pixel, a termination of 1 MΩ for the injection is used at the oscilloscope. In addition, the injection signal serves as a trigger, set on its falling edge.
As mentioned in section 7.1, the AmpOut can be utilized to study the performance of the CSA. The test output requires a 1 kΩ termination, directly placed on the Insert

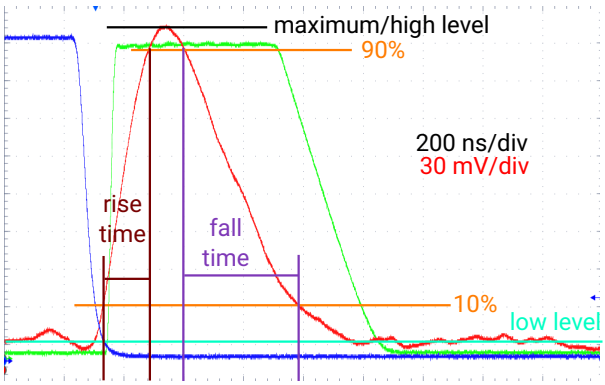
PCB, and is probed via a Tektronix P6139B [41] passive probe. The key performance indicators of the amplifier pulse are the amplitude and the slew rates of the rising and falling edge. The amplitude is important in terms of efficiency, whereas the rising edge affects the time resolution. Based on the fact that every unipolar pulse shaping has a bipolar component, an undershoot can be observed, which is undesired for the determination of the pulse amplitude. To account for this the low level is used, which is the most probable value of the baseline fluctuation and excludes the undershoot. The AmpOut pulse amplitude can be calculated as follows:

$$\text{amplitude}_{\text{AmpOut}}\ [\text{mV}] = \text{maximum} - \text{low level} \tag{9.1}$$

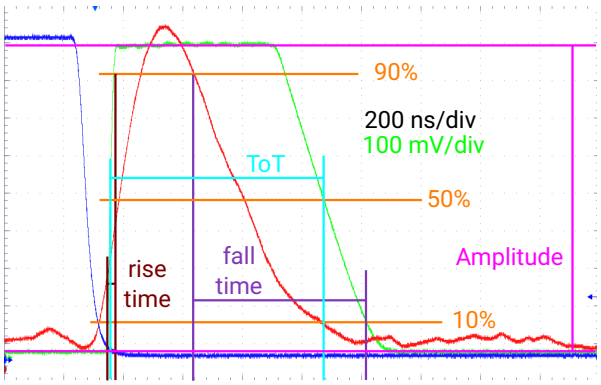
To calculate the slew rates the rise and fall time of the signal edges are measured. They are defined as the time difference between the voltage level crossing of 10 % and 90 % of the amplitude. The reference levels are the low level and the high level, where the latter can differ from the maximum and is monitored as well. The slew rates, rise and fall, are calculated according to:

$$\text{rise/fall}\ [\text{mV}\,\text{ns}^{-1}] = 0.8 \times \begin{cases} \frac{\text{high level}-\text{low level}}{\text{rise time/ fall time}} & \text{, for AmpOut} \\ \frac{\text{amplitude}}{\text{rise time/ fall time}} & \text{, for Hitbus} \end{cases} \tag{9.2}$$

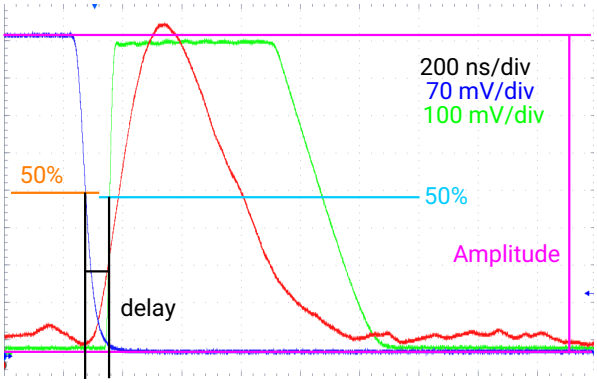
The Hitbus gives a handle on the performance of the baseline restoration, comparator and signal transmission to the periphery cell (see section 7.2). The oscilloscope termination of the Hitbus is set to 50 Ω. With this test output the ToT can be determined. In this thesis it is defined as the time difference at the 50 % voltage level crossing with respect to the amplitude. In addition to the amplitude, rise and fall time are monitored, as well as the delay to the injection pulse. The slew rates are calculated as defined in equation 9.1. The delay is measured between injection and Hitbus as time difference of the 50 % voltage level crossing of their respective amplitudes.
The oscilloscope's bandwidth for each of the three signals is limited to 20 MHz to reduce impairments on the measurement parameter due to high frequency noise. If not indicated otherwise all following measurements are done at room temperature, while running the setup for a reasonable amount of time beforehand to allow for a thermal equilibrium.
All measurement values are determined from the mean and the standard deviation are provided by the oscilloscope. To decrease the statistical error at least 2000 samples per measurement point were taken, reducing it to 2.2 % or less, assuming a normal distribution for the measured parameters. All previously mentioned measured pulse shape parameters for the three signals are illustrated in Figure 9.2. Attention should be paid to the circumstance that both, AmpOut and Hitbus require a driver, which influences the pulse shape parameters. Therefore, the investigated pulse shape parameters are not exactly representing the pulses processed by the on-chip circuitry.



(a) AmpOut (red curve) pulse shape measurement parameters



(b) Hitbus (green curve) pulse shape measurement parameters



(c) Injection (dark blue curve) pulse shape measurement parameters

Figure 9.2: Analog measurement parameters.

9.2 Power Consumption

For the operation in an experiment, the sensor's power consumption has to be known for the design of an appropriate cooling system. For ATLASPix1, the power consumption is divided in three parts that are addressed independently.
Apart from the high voltage, three main bias voltages are supplied to the sensor: VDDA = 1.9 V, VSSA = 1.0 V and VDD = 1.9 V. The pixel sensor part has its own power domain, enabled by a dedicated bias block, defined by VDDA and VSSA. The power consumption for the active area (equation 7.1) can be calculated with:

$$\mathrm{P}_{\mathrm{VDDA,\ Active}}\ [\mathrm{mW\,cm^{-2}}] = \frac{V_{\mathrm{VDDA}} \cdot I_{\mathrm{VDDA}}}{\mathrm{A}_{\mathrm{active}}} \tag{9.3}$$

$$\mathrm{P}_{\mathrm{VSSA,\ Active}}\ [\mathrm{mW\,cm^{-2}}] = \frac{V_{\mathrm{VSSA}} \cdot I_{\mathrm{VSSA}}}{\mathrm{A}_{\mathrm{active}}} \tag{9.4}$$

The power is normalized to the size of the active area (equation 7.1) to give the possibility to extrapolate for a full-scale sensor.
A second bias block is reserved for the periphery, made up by the periphery cells and the readout state machine. The supply voltages are VDDA and VDD, where the former

is responsible for analog circuitries like the PLL and the latter for digital circuitries.
The periphery cells are only powered by VDD and their power consumption can be calculated with:

$$\mathrm{P_{VDD,Periphery}}\ [\mathrm{mW\,cm^{-2}}] = \frac{V_{\mathrm{VDD}} \cdot I_{\mathrm{VDD}}}{\mathrm{A_{periphery}}} \tag{9.5}$$

The power is again normalized to the total area (equation 7.2) of the periphery cells, given by equation 7.2, since every pixel requires its own periphery cell.
The power consumption of the periphery cells depends on the occupancy of the sensor. The achievable hit rates in the laboratory do not exceed 300 kHz, whereby a change in the current of VDD could not be observed. The same applies for the DACs of the periphery cell.
The readout circuitry is composed of the state machine logic, a PLL, the Dcl serializer and the link. The ATLASPix1 contains only one readout link per sensor, whereas a full-scale sensor will contain several links. Each part exists only once per sensor and is for that reason not normalized to their size. The total power consumption is mirrored in the current flow of VDD and VDDA and can be calculated as followes:

$$\mathrm{P_{VDDA/VDD,\ Readout}}\ [\mathrm{mW}] = V_{\mathrm{VDDA/VDD}} \cdot \begin{cases} I_{\mathrm{VDD}}(\text{State Machine}) \\ I_{\mathrm{VDDA/VDD}}(\text{PLL+Dcl serializer}) \\ I_{\mathrm{VDD}}(\text{Link}) \end{cases} \tag{9.6}$$

PLL and Dcl serializer are combined in one entity for the power consumption calculation, since they are affected by each other.
The following power consumption measurements are done with a Hameg HMP4040 [42]. The error for each measurement point is taken as the maximum deviation from the most probable observed value. Almost all measurements are done with low occupancies, whereby the inaccuracy due to fluctuations of the measured current is about 0.1 mA.
In Table 9.1, the power consumption of each individual chip component is listed for the default DAC settings (see Table A.1). By selective enabling and disabling of the DACs of the individual chip components, the specific power consumptions can be derived. Attention should be paid to the fact that the power domains are not totally disentangled, resulting in interference of different chip components in terms of power consumption.

Chip component	$\mathrm{P_{VDDA}}$	$\mathrm{P_{VSSA}}$	$\mathrm{P_{VDD}}$	$\mathrm{P_{total}}$	unit
Active pixel area	126.14	66.15	-	192.29	$\mathrm{mW\,cm^{-2}}$
Periphery	-	-	0*	0*	$\mathrm{mW\,cm^{-2}}$
State machine	-	-	8.27	8.27	mW
Pll + Dcl	20.52	-	14.82	35.34	mW
Pre-Emphasis/Link	-	-	22.8	22.8	mW

Table 9.1: Power consumption split for each chip component (*value to small too be measured with power supply.)

With the these measured values the total power consumption of the ATLASPix_Simple amounts to:

$$P_{\text{total}} \approx 166\,\text{mW}. \tag{9.7}$$

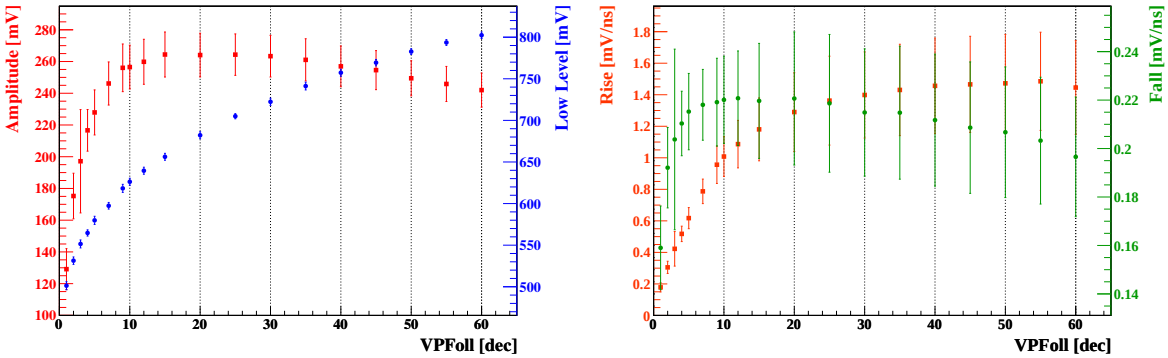
ATLASPix_Simple does not yet have the size of the final demonstrator chip, which will contain 150 columns and 400 rows. Assuming the exact same design for a full-scale sensor ($A_{active} = 2.6\,\text{cm}^2$) with 125 columns and 4 readout links, the total power consumption results in:

$$P_{\text{total, full scale}} \approx 635\,\text{mW}. \tag{9.8}$$

For the following DAC parameter scans the power consumption is given as difference from the default value, to observe the impact of the individual DAC.

9.3 Characterization of the Amplifier Signal Driver

As previously mentioned, the AmpOut requires a driver, whose performance can be steered by *VPFoll*. The influence on the pulse shape parameters is illustrated in Figure 9.3.
The amplitude peaks around $VPFoll = 20$ and decreases afterwards. This value is taken as default for all previous and subsequent measurements in this thesis. Up to this DAC value the rise increases and then saturates. The fall is stable within the uncertainties for DAC values larger 5. A slight decrease is observed for lower DAC values.
Another reason for the chosen working point is the low level, which increases steeply with larger VPFoll values. Every circuitry has a limited operation range. If the low level increases, the voltage range shrinks. Large VPFoll values are therefore not recommended.
Overall measurement, but rather a qualitative approximation to characterize the amplifier performance.

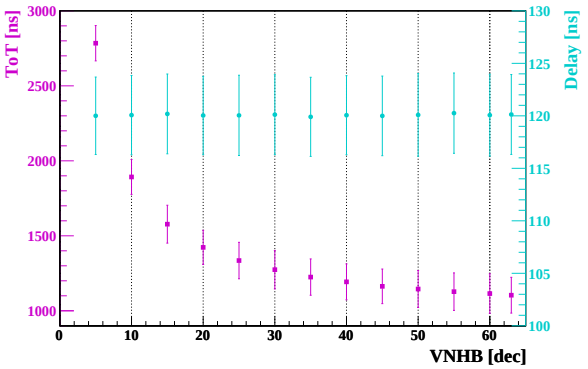


(a) Amplitude and Low Level versus VPFoll (b) Rise and Fall slew rates versus VPFoll

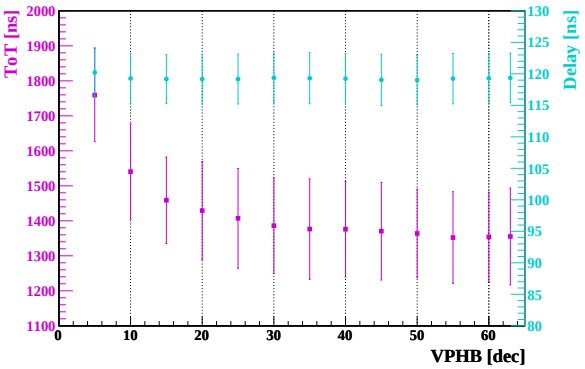
Figure 9.3: AmpOut pulse shape parameter dependence on VPFoll for pixel 0/0 (column/row).

9.4 Characterization of the Hitbus Signal Driver

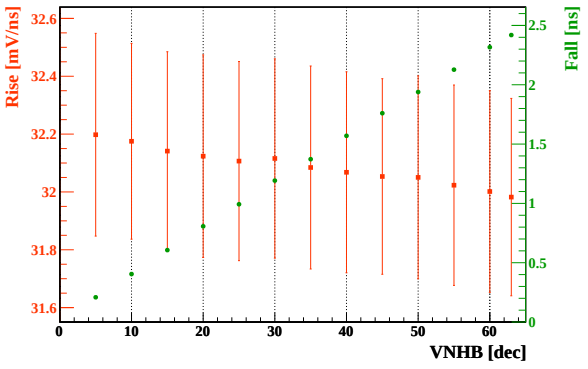
The Hitbus is the comparator signal output after the receiver in the periphery cell and requires a driver. The driver is adjustable by the two DACs, called *VNHB* and *VPHB*. In Figure 9.4, the Hitbus pulse shape parameters are presented (reference DAC value *VNHB*=*VPHB*= 20). A significant influence on the ToT is observed for both DACs. A steep decrease with higher DAC values is measured, which saturates to the highest value. In addition, *VNHB* shows a considerable impact on the fall, consequently influencing the ToT itself, whereas for *VPHB* the measurement values are stable within their uncertainties. The delay between injection and Hitbus is not affected by the two DACs and is stable within the uncertainties. To minimize the DAC's influence on the Hitbus signal, *VNHB* and *VPHB* are set to 63, whereby the ToT is in a saturated domain. All previous and subsequent measurements were done with these values.



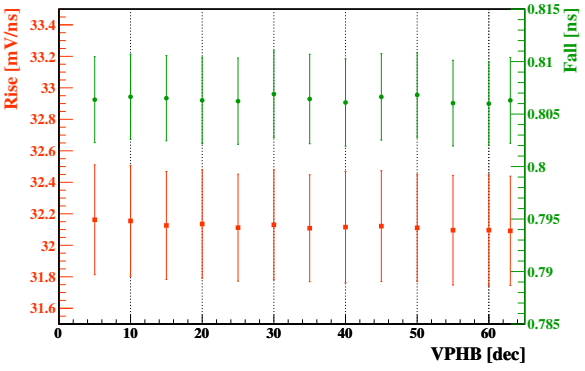
(a) ToT and Delay versus VNHB (VPHB = 20)



(b) ToT and Delay versus VPHB (VNHB = 20)



(c) Rise and Fall versus VNHB (VPHB = 20)



(d) Rise and Fall versus VPHB (VNHB = 20)

Figure 9.4: Hitbus measurement parameter dependence on VNHB & VPHB for pixel 0/0 at a threshold of 150 mV above the baseline.

9.5 Injection Characterization

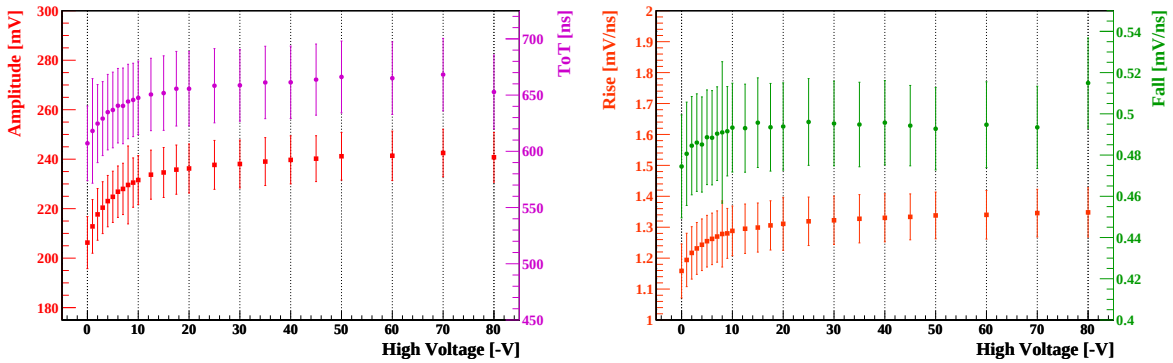
The injection method is a valuable tool to study the performance of the pixel and periphery cell. The injection can be adjusted in terms of amplitude, duration and frequency of its repetition. If not otherwise indicated, the listed values of Table 9.2 are used for all measurements. A long duration time is chosen, since reflections at the beginning of the rising edge of the injection for the AmpOut and Hitbus were observed on the oscilloscope, deteriorating their measurement parameters. With the large chosen value, the rise of the negative injection pulse is outside of the measurement window of the oscilloscope.

Parameter	Value	Unit
Amplitude	*500/600	mV
Duration	5000	8 ns
Frequency	100	Hz

Table 9.2: Injection input parameter for analog measurements (*previous/subsequent measurements).

HV Dependence

Due to the implementation of the injection, the charge is released directly into the n-well and with that a dependency on the high voltage is expected as observed with the several MuPix sensor generations [43]. Figure 9.5 shows the measurement results of the pulse shape parameters of the AmpOut and Hitbus for different high voltages, which increase proportionally to the square root of the reverse bias voltage. The behavior is similar to the growth of the detection volume, the depletion zone, with the supplied reverse bias voltage, see equation 5.4.
The pulse parameters increase steeply up to $-10\,\mathrm{V}$ and saturates at about $-80\,\mathrm{V}$, which is a point where the high voltage current start to increase and the diode is going into the breakdown domain. The operation below $-10\,\mathrm{V}$ is undesired, due to the efficiency loss and instabilities of sensor components, which can be affected by the bias voltage.
The test beam operation voltage is typically $-60\,\mathrm{V}$, which is chosen in this thesis as operating point for all previous and subsequent measurements, if not indicated otherwise.



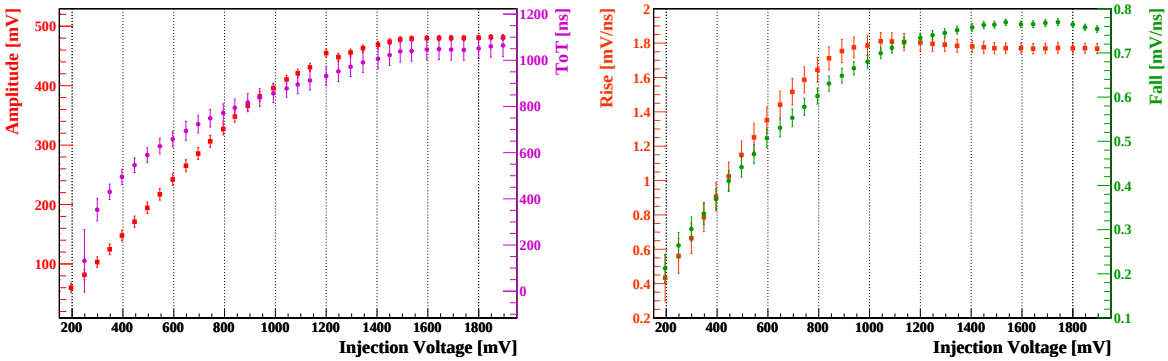
(a) Amplitude (AmpOutplifier) and ToT (Hitbus) versus high voltage

(b) Rise and Fall slew rates of AmpOut versus high voltage

Figure 9.5: Test output signals dependence on reverse bias voltage for pixel 0/1 (column/row).

Injection Voltage dependence on Test Output

The injection amplitude is adjustable between 0 V and 1.9 V and can be used to mimic different charge depositions in the depletion zone. Since the CSA has only a certain linear region of operation, the dependency of chosen injection voltages is studied. Between 200 mV and approximately 1000 mV the pulse shape parameters of the AmpOut display a linear behavior, subsequently saturating up to 1900 mV, see Figure 9.6. For smaller injection voltages, the observed AmpOut pulse amplitude is too small with respect to the low level fluctuations to be measured correctly by the oscilloscope. For this measurement, a high threshold of 150 mV above the baseline is chosen. The ToT increases linearly up to approximately 1400 mV. For injection voltage levels below 300 mV the ToT is unstable, because the signal just barely crosses the threshold. Here, the ToT cannot be sampled precisely anymore.
For subsequent analog measurements an injection voltage of 600 mV is chosen, which results in a pulse amplitude large enough to be unaffected by the noise floor and small enough to not be in the saturation domain.



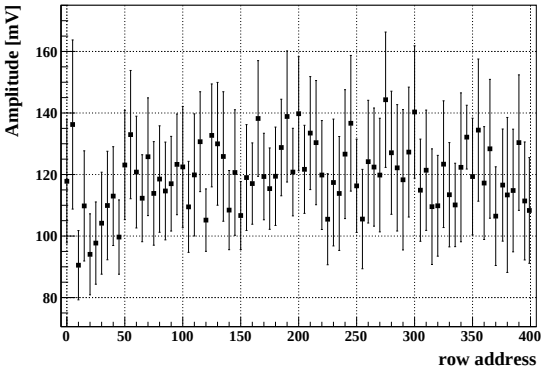
(a) Amplitude (AmpOut) and ToT (Hitbus) versus Injection Voltage

(b) Rise and Fall slew rates of AmpOut versus Injection Voltage

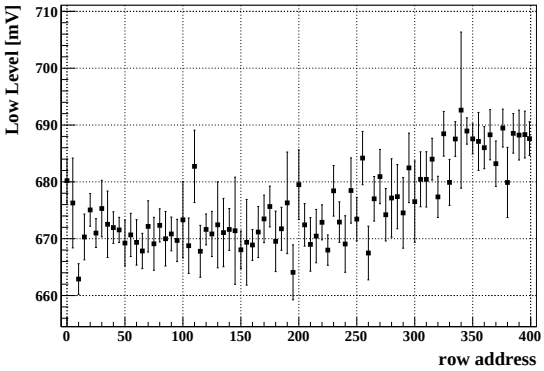
Figure 9.6: Test output signals dependence on Injection Voltage for pixel 0/1 (column/row)

9.6 Row Dependence

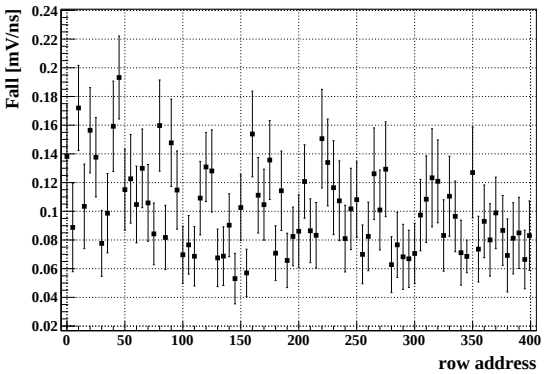
To investigate the position of the amplifier dependence on the row address of the sensor on the amplifier pulse an Iron-55 source is used, see section 8.6. The injection method cannot be used for this measurement as the injection signal might depend on fluctuations to production variations among the pixel injection capacities [44].
For this measurement at least 1000 points were taken for each fifth row address. The measurement results on amplitude, low level, rise and fall are displayed in Figure 9.7. Within the high fluctuations of the measurement values no significant impact for the pulse parameters are observed. However, for the amplitude somewhat smaller values are measured between row 10 and 50, but the large uncertainty of these measurements presents no convincing evidence. The low level is stable up to row 250, where it starts to increase up to row 350. This could be an effect of the power distribution, since VSSA is supplied from the top of the sensor. The fall scatters a lot among different rows. The effect decreases with higher row addresses to lower fall values, presumptively caused by the same power distribution issue. Since, no significant deviation in the amplitude is observed and the fall decreases to higher row addresses, an increase of the ToT with higher row addresses could be observed.



(a) Amplitude versus row address



(b) Low Level versus row address



(c) Fall versus row address

Figure 9.7: AmpOut pulse shape parameter dependence on the row address.

9.7 Performance Study with the AmpOut

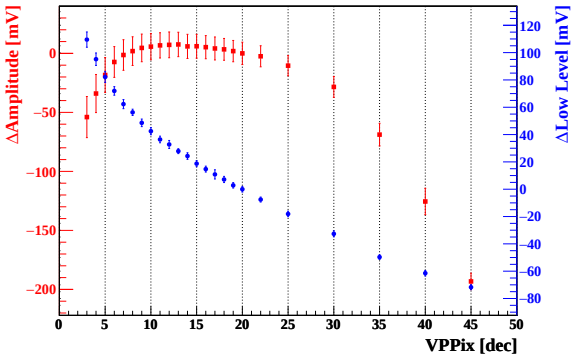
The influence of the DAC parameters can be measured with the AmpOut up to the baseline restoration. In the following, the analog performance of the amplifier circuitry is investigated in detail for the pixel 0/1 (column/row). Since the driver influences the pulse shape parameters, the measurement values do not exactly equal the actual amplifier signal. Therefore, all subsequent measurement values are plotted as difference to a default value. The averaged pulse shape parameter values at the default DAC settings are listed in Table 9.3.

Parameter	Average Value	Unit
Amplitude	242.708 ± 0.664	mV
Low Level	671.925 ± 0.438	mV
Rise	1.354 ± 0.003	$\mathrm{mV\,ns^{-1}}$
Fall	0.505 ± 0.003	$\mathrm{mV\,ns^{-1}}$

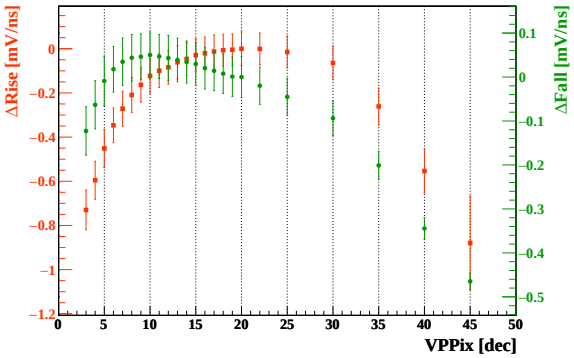
Table 9.3: Pulse shape parameter values averaged for all DAC scans at the default DAC settings.

VPPix

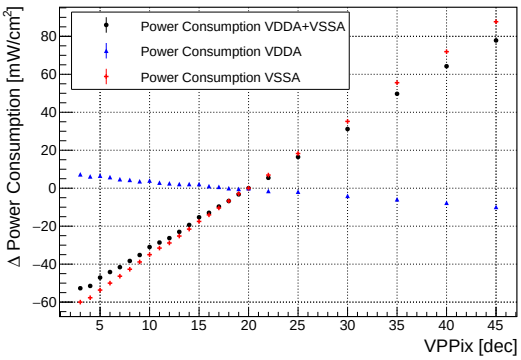
VPPix is responsible for the current supply of the CSA and with that is is directly affecting the amplification and its stability. In terms of single hit efficiency a large amplitude is desired, which is stable for *VPPix* values between 7 and 20. The power consumption is dominated by the power domain of VSSA, which increases linearly with higher DAC values, whereas the power consumption associated with VDDA slightly decreases. As a consequence, a smaller DAC value is favored in terms of lower power consumption. The rise, which directly affects the time resolution, reaches a plateau between 15 and 30, and decreases for DAC values outside of this range. A trade-off for the DAC value between time resolution, power consumption and efficiency has to be chosen.
The low level decreases steeply with higher *VPPix* values, which could affect the measured pulse shape parameters. The fall peaks around a value of 10 and decreases steeply to both sides. If a shorter pulse is desired, a *VPPix* value of 10 is recommended.
However, an increase in noise for values lower than the default is observed. A detailed discussion of this effect is given in section 10.5.



(a) ΔAmplitude and ΔLow Level versus VPPix



(b) ΔRise and ΔFall slew rates versus VPPix

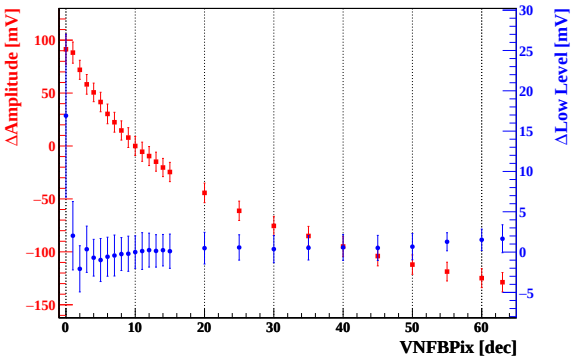


(c) ΔPower consumption versus VPPix

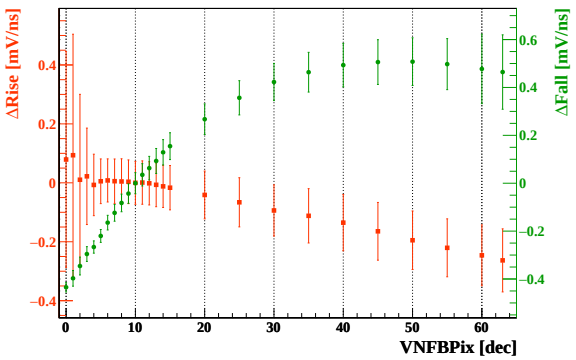
Figure 9.8: AmpOut pulse shape parameter and power consumption dependence on VPPix with respect to the default value at VPPix = 20.

VNFBPix

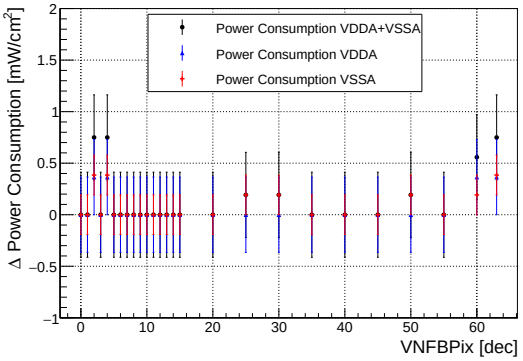
The main impact of the linear feedback is to shorten the pulse width by increasing the steepness of the falling edge's slew rate. This can be adjusted by the DAC *VNFBPix*. According to Figure 9.9, the expected impact is observed for the fall, which increases significantly with higher DAC values at cost of a decreasing signal amplitude and slightly lower rise. Independent from the chosen DAC value, a value larger than 5 is recommended in terms of noise, due to instabilities of the rising edge values below $VNFBPix = 5$.
A change of the default value of 10 does not change the power consumption, which is unaffected over the entire measurement region. If *VNFBPix* does not interfere significantly with the efficiency and the time resolution, higher values can be considered to shorten the pulse length. This is required, if the readout window is limited and the ToT information has to be sampled. However, this has to be verified. Only the time resolution is studied in this thesis.



(a) ΔAmplitude and ΔLow Level versus VNFBPix



(b) ΔRise and ΔFall slew rates versus VNFBPix

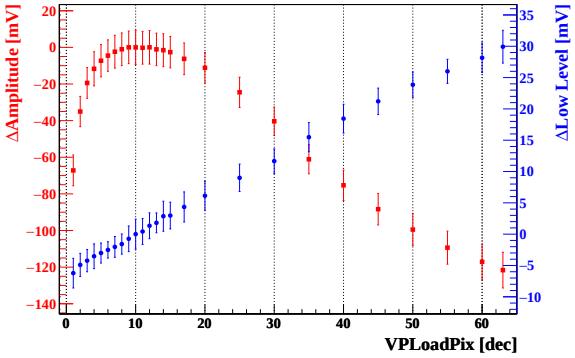


(c) ΔPower consumption versus VNFBPix

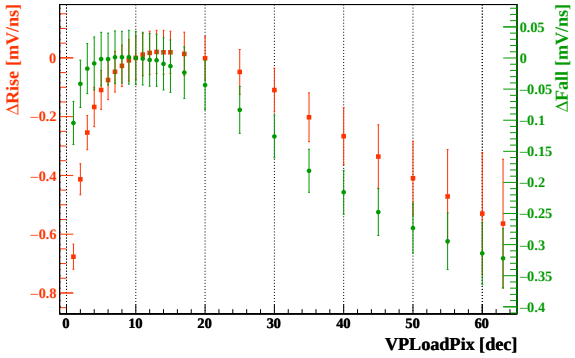
Figure 9.9: AmpOut pulse shape parameters and power consumption dependence on VNFBPix with respect to the default value at VNFBPix = 10

VPLoadPix

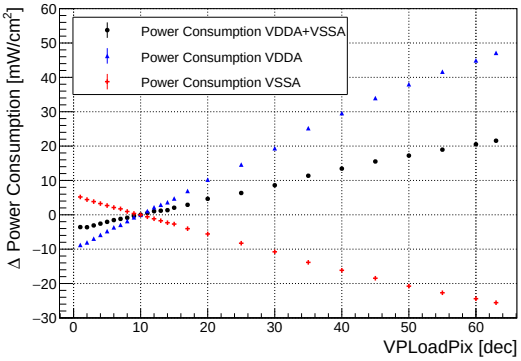
The influence of the DAC *VPLoadPix* can be approximated with a change of the feeback capacity, which has a significant impact on the pulse shape parameters, see Figure 9.10. The desired operation region is around the default value *VPLoadPix* = 10 and is stable between 5 and 15, for the amplitude and the fall. For DAC values outside of this range the amplitude as well as the fall decrease steeply. The rise is stable within a range of *VPLoadPix* from 10 to 20, decreasing steeply outside of this range, too. The low level increases linearly with higher *VPLoadPix*, but the steepness of the increase should be too low to influence the measurements significantly.
The total power consumption is dominated by the power domain of VDDA, which increases linearly with higher DAC values, whereas the power consumption associated with VSSA decreases. The decrease of the VSSA current reduces the current supply for the CSA, which can be the cause of the amplitude's reduction with higher *VPLoadPix* values. In terms of lower power consumption, a change from the default value is not recommended, whereas an effect on the time resolution is studied for larger values, see section 10.4.



(a) ΔAmplitude and ΔLow Level versus VPLoadPix



(b) ΔRise and ΔFall slew rates versus VPLoadPix

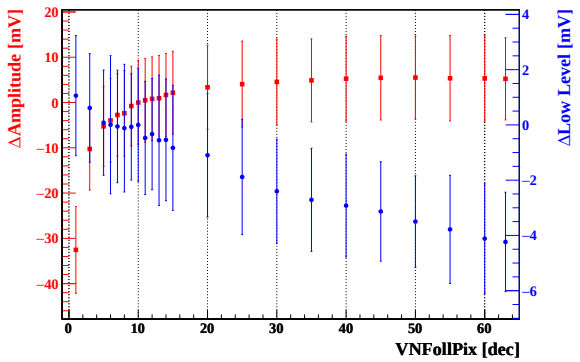


(c) ΔPower consumption versus VPLoadPix

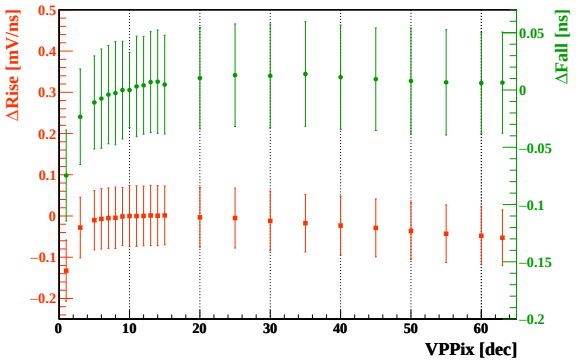
Figure 9.10: AmpOut pulse shape parameters and power consumption dependence on VPLoadPix with respect to the default value at VPLoadPix = 10

VNFollPix

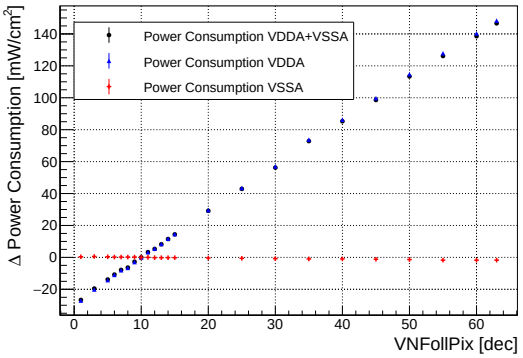
VNFollPix is the internal feedback driver and responsible for the stabilization of the CSA feedback loop. As a source follower, it requires a significant amount of power. The power consumption of VDDA is dominating and increases linearly with higher DAC values, whereas the power consumption for VSSA is stable over the entire DAC region. Consequently, a low DAC value is favored in terms of lower power consumption.
The amplitude increases steeply up to *VNFollPix* = 10 and saturates subsequently up to the maximum value. The slew rates also increase slightly up to 5 and stay within the uncertainties afterwards. The low level decreases marginally with higher *VNFollPix*, thus the other measured parameters are not affected. In terms of a low power consumption a DAC value between 10 and 15 is recommended.



(a) ΔAmplitude and ΔLow Level versus VNFollPix



(b) ΔRise and ΔFall slew rates versus VNFollPix



(c) ΔPower consumption versus VNFollPix

Figure 9.11: AmpOut pulse shape parameter and power consumption dependence on VNFollpix with respect to the default value at VNFollPix = 10

9.8 Performance Study with the Hitbus

All sensor components after the internal feedback driver up to the edge detector can only be accessed by the Hitbus for study. In the following, the impact of the DAC parameters are studied for pixel 0/1 (column/row) with a threshold of 100 mV above the baseline to not be influenced by noise. The slew rates of the Hitbus are measured to observe any influence on the measured ToT and delay. As for the AmpOut measurements, the values are plotted as difference to a default value. The averaged parameter values at the default DAC settings are listed in Table 9.4.

Parameter	Average Value	Unit
ToT	666.078 ± 3.154	ns
Delay	96.712 ± 0.149	ns
Rise	32.733 ± 0.032	$\mathrm{mV\,ns^{-1}}$
Fall	2.461 ± 0.001	$\mathrm{mV\,ns^{-1}}$

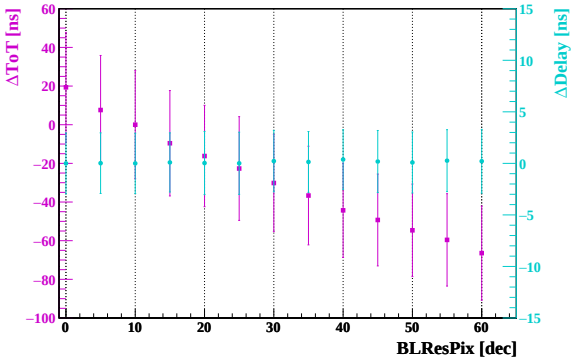
Table 9.4: Averaged parameter values of Hitbus measurements of VNCompPix, VPBiasRec, and VNBiasRec at the default DAC settings.

BLResPix

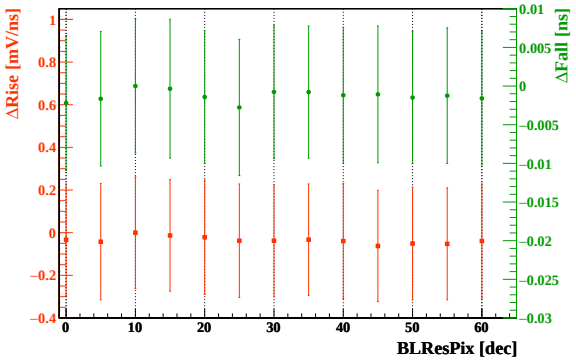
BLResPix controls the resistor of the high pass of the baseline coupling (see Figure 7.2). Higher DAC values should decrease the noise. For MuPix7 a similar baseline restoration was implemented and an increase of the fall was observed, see [26]. An equal impact can be expected for the ATLASPix1. However, the AmpOut couples out before the baseline restoration and the Hitbus is used for this measurement. The delay as well as the slew rates are stable over the entire operating range, according to Figure 9.12. Only the ToT decreases linearly with higher *BLResPix*. Since the power consumption is not affected by *BLResPix* higher values than the default of 10 are recommended, due to a lower observed noise.
The measurement values at the default DAC settings differ from the ones in Table 9.4. For this measurement the setup was reassembled and LEMO® cables with different length were used. A lower threshold value than 100 mV was used, which results in a deviation of ToT and delay.

Parameter	Mean Value	Unit
ToT	761.820	ns
Delay	80.890	ns
Rise	32.689	$\mathrm{mV\,ns^{-1}}$
Fall	2.438	$\mathrm{mV\,ns^{-1}}$

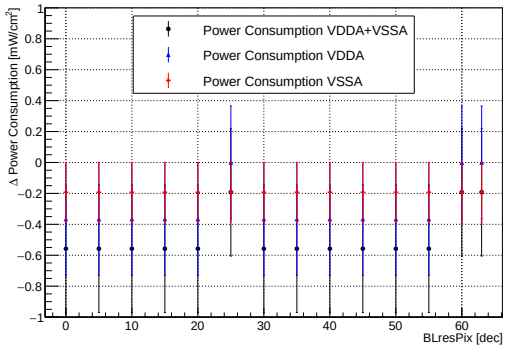
Table 9.5: Mean parameter values of Hitbus measurement at the default DAC settings.



(a) ΔToT and ΔDelay versus BLResPix



(b) ΔRise and ΔFall slew rates versus BLResPix



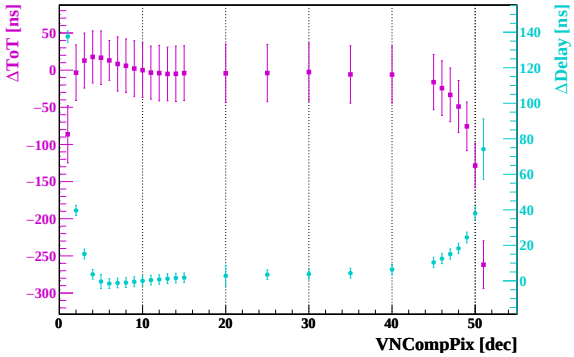
(c) ΔPower consumption versus BLResPix

Figure 9.12: Hitbus measurement parameter and power consumption dependence on BLResPix with respect to the default value at BLResPix = 10

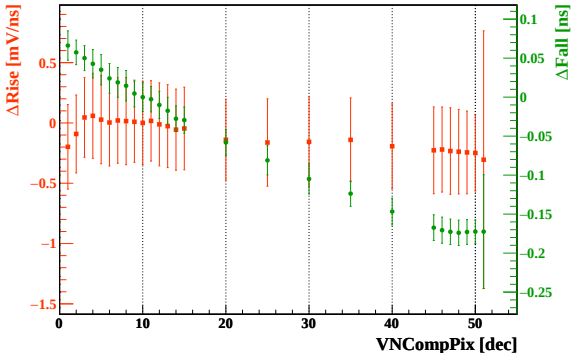
VNCompPix

The current flow and the speed of the comparator of ATLASPix_Simple can be adjusted by the DAC *VNCompPix*. In Figure 9.13 the effect of the DAC value on the ToT, the delay, the slew rates and the power consumption are presented. In terms of ToT and delay a stable range of operation between DAC values of 5 and 45 is observed. For lower and higher values the comparator is too far from the optimal operation point and cannot function properly anymore. While the rise is stable over the entire DAC range, the fall decreases linearly up to *VNCompPix* = 45 and saturates subsequently. For *VNCompPix* values larger than 51 the comparator is not responding anymore.
The power consumption associated with VDDA dominates the total power consumption and increases linearly up to a *VNCompPix* value of 45. Subsequently, the power consumption saturates. The power domain of VSSA is unaffected by the comparator DAC, being stable over the entire DAC range. The behavior of the power consumption for VDDA can be explained by the characteristic line of the NMOS transistors. In the linear regime of the NMOS transistor the current increases linear with a higher voltage level between drain and source (V_{DS}), which is controlled by *VNCompPix*. If V_{DS} reaches a certain level, set by the difference of the potentials between gate voltage and

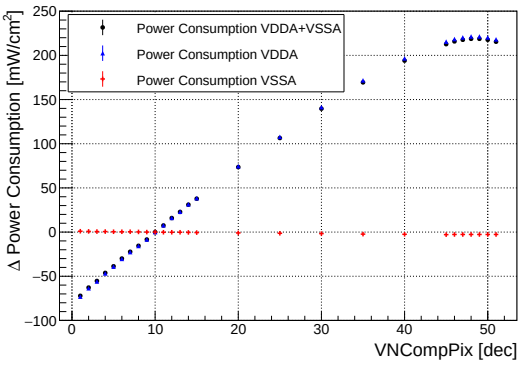
the internal threshold voltage of the transistors, the current characteristic saturates and the transistor is operated in the active mode. In terms of lower power consumption, a low value of *VNCompPix* is favored.
The impact on the time resolution and the efficiency has to be considered to choose an optimal working point of the comparator, whereas only the former is studied in this thesis.



(a) ΔToT and ΔDelay versus VNCompPix



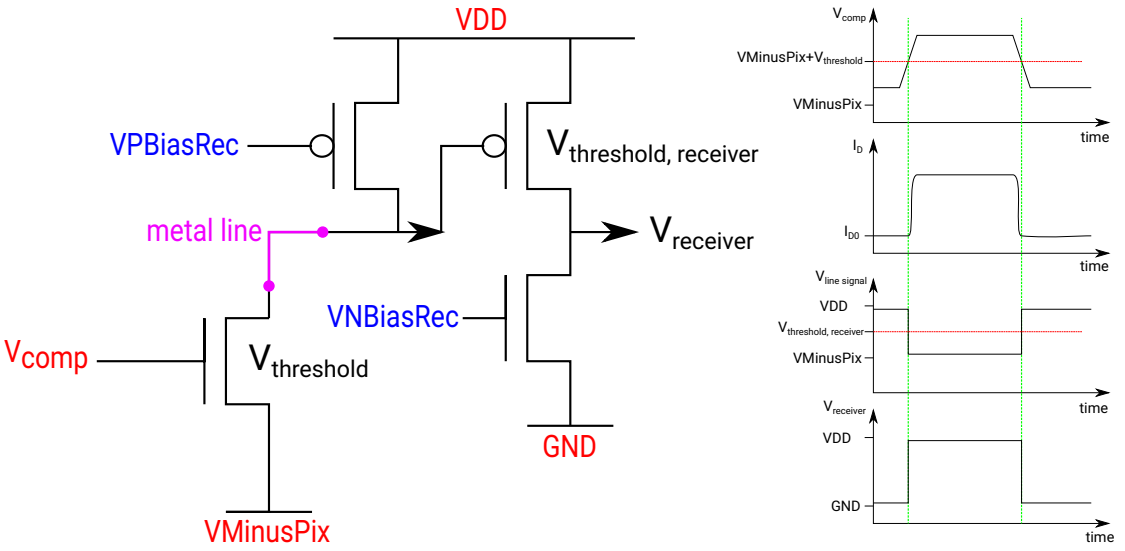
(b) ΔRise and ΔFall slew rates versus VNCompPix



(c) ΔPower consumption versus VNCompPix

Figure 9.13: Hitbus measurement parameter and power consumption dependence on VNCompPix with respect to the default value at VNCompPix = 10

Line Driver: VMinusPix



(a) Schematic of the signal driving logic.

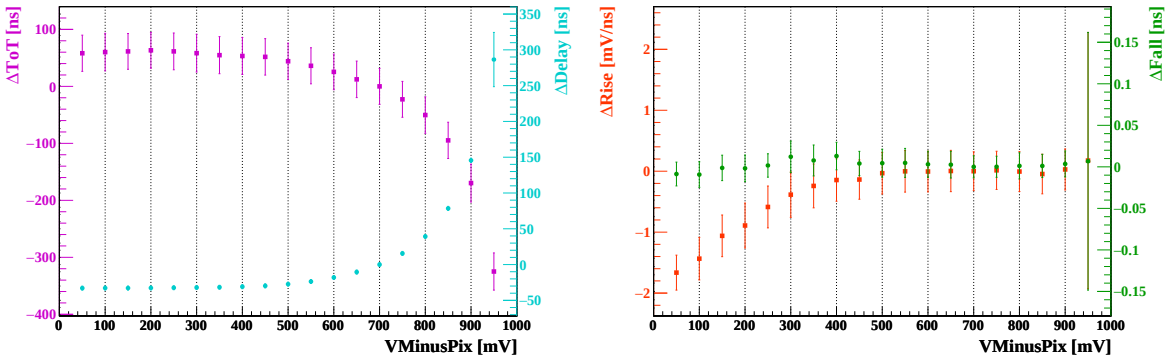
(b) Schematic of characteristic curves for the signal transmission from the pixel cell to the periphery cell

Figure 9.14: Schematic of the signal driving from the pixel cell to the periphery cell.

VMinusPix is not a DAC, but a voltage level externally applied to the line driver. The line driver consists of an NMOS-transistor seated in the pixel cell and a PMOS transistor of the receiver logic in the periphery cell, see Figure 9.14. The NMOS transistor is functioning as a switch, whose voltage levels are determined by the comparator output level (V_{gate}) and *VMinusPix* ($= V_{\text{source}}$). If a hit is detected by the comparator, $V_{\text{GS}} = V_{\text{gate}} - V_{\text{source}}$ increases above threshold voltage ($V_{\text{threshold}}$) and a current can flow. This current (I_D) is regulated by the PMOS transistor controlled via *VPBiasRec*. If the current is flowing the voltage on the line drops towards *VMinusPix*. This voltage drop is detected by the receiver branch controlled by *VNBiasRec* and converted to a pulse with a CMOS-like amplitude.
During test beam campaigns a significant impact on the time resolution for supplied *VMinusPix* voltage levels was observed, with a major improvement for lower levels at the cost of an increase in noise. From this, the default voltage level of 700 mV was derived [28].
As displayed in Figure 9.15, the ToT increases with lower *VMinusPix* values, while the delay decreases. The fall stays within the uncertainties over the entire measurement region. For the rise the same effect is observed down to a *VMinusPix* value of 400 mV. Below, the rise decreases, which is an effect of the increased current flow on the signal lines, influencing the line signal (see Figure 9.16b). The maximum voltage level of *VMinusPix* is at 950 mV, for higher voltages some pixels are unresponsive.
For this measurement a *BLResPix* value of 63 was used to decrease possible influences of noise. The mean values of the parameters are listed in Table 9.6.

Parameter	Mean Value	Unit
ToT	614.326	ns
Delay	96.952	ns
Rise	32.726	$\mathrm{mV\,ns^{-1}}$
Fall	2.455	$\mathrm{mV\,ns^{-1}}$

Table 9.6: Mean parameter values of Hitbus measurement at the default DAC settings with BLResPix set to 63.



(a) ΔAmplitude and ΔLow Level versus VMinusPix

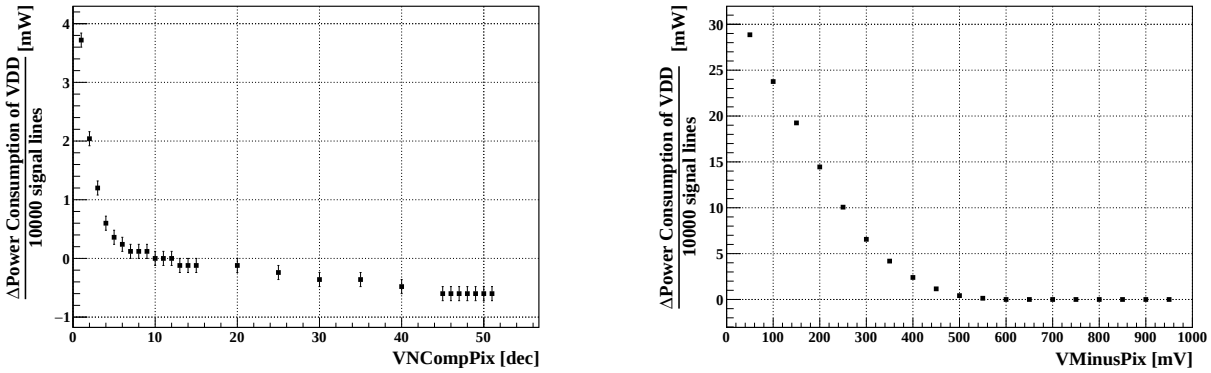
(b) ΔRise and ΔFall slew rates versus VMinusPix

Figure 9.15: Hitbus measurement parameter dependence on VMinusPix with respect to the default value at VMinusPix = 700 V

Power Consumption of VDD as Function of VNCompPix and VMinusPix

Over the course of the analog measurements of *VNCompPix* and *VMinusPix*, a change in the current of VDD is observed. For both parameters an increase of the current for lower values is measured, see Figure 9.16.
If V_{GS} is increased either by the comparator output level or with lower *VMinusPix* levels, the gate-source-voltage can be permanent above $V_{\mathrm{threshold}} = 350\,\mathrm{mV}$ [45]. As a consequence, the NMOS transistor passes from the sub-threshold mode to the linear mode and a permanent current flow emerges, which increases linearly with higher V_{GS} levels. The permanent current leads to detection of artificial noise signals with a rate increase at higher V_{GS} levels. This effect takes place if *VMinusPix* is set to 500 mV. The driver is then sensitive to an output swing of the comparator (at default value of *VNCompPix*) between this voltage level and the maximum voltage level of 950 mV. For the default value for *VMinusPix* a *VNCompPix* value smaller than 10 is not recommended due to the same increase in power on the signal lines and the consequentially increase in noise. The averaged power dissipation along the signal lines (10000 in total) is calculated as follows:

$$P = (VDD - VMinusPix) \times I_{\mathrm{VDD}}(\mathrm{VNCompPix,\ VMinusPix}) \tag{9.9}$$



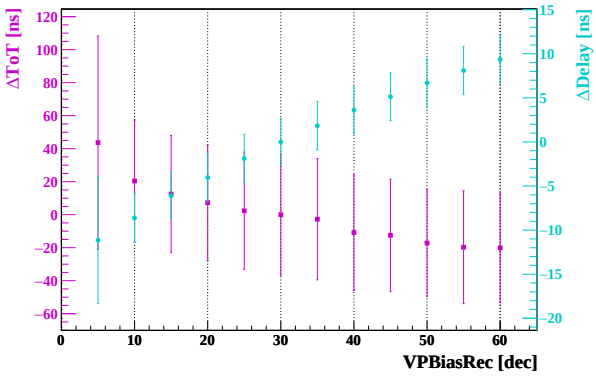
(a) ΔPower consumption for VDD at VMinusPix = 700 mV versus VNCompPix

(b) ΔPower consumption for VDD for VNCompPix = 10 versus VMinusPix

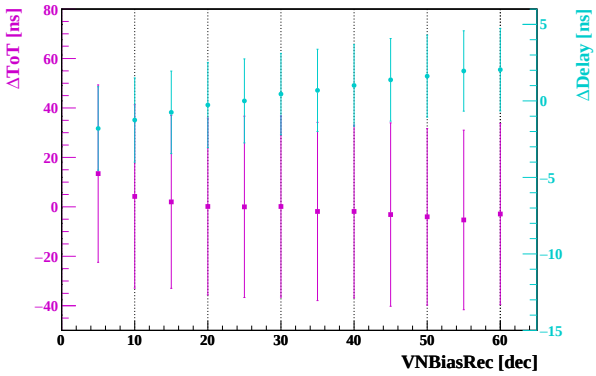
Figure 9.16: Power consumption of VDD dependent on VNCompPix and VMinusPix averaged for 10000 signal lines with respect to the default values at VNCompPix = 10 and VMinusPix = 700 mV.

VPBiasRec & VNBiasRec

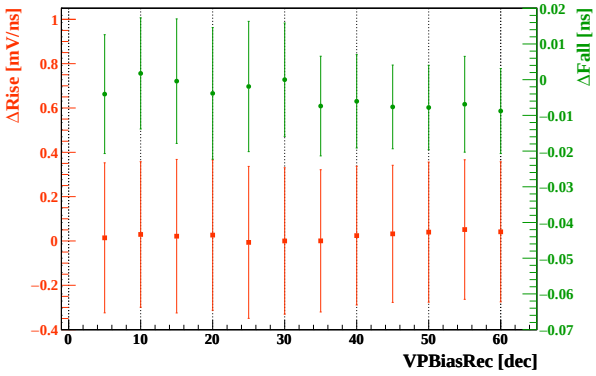
The back-end of the signal transmission from the pixel cell to the periphery cell is the receiver, whose performance is controlled by the DAC values of *VPBiasRec* and *VNBiasRec*. The receiver converts the incoming low-voltage amplitude from the pixel cell into a CMOS amplitude for the edge detector. As a consequence, both DACs have a shaping characteristic on the Hitbus signal.
Figure 9.17 shows the measurement results for these DACs. While *VNBiasRec* has no significant impact on the Hitbus pulse shape parameters, *VPBiasRec* decreases the ToT and increases the delay with larger values. For *VPBiasRec* the slew rates are unaffected. Since the DACs regulate the conversion to a CMOS amplitude, the chosen settings are influenced by the voltage amplitude on the line and should therefore be fine-tuned for a chosen voltage level of *VMinusPix*.



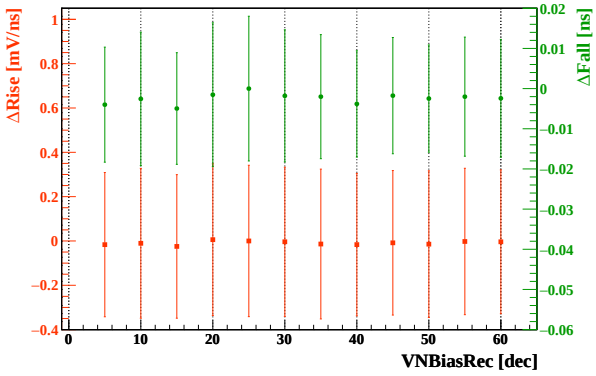
(a) ΔToT and ΔAmplitude versus VPBiasRec



(b) ΔToT and ΔAmplitude versus VNBiasRec



(c) ΔRise and ΔFall versus VPBiasRec



(d) ΔRise and ΔFall versus VNBiasRec

Figure 9.17: Hitbus output signal dependence on VPBiasRec & VNBiasRec with respect to the default values at VNBiasRec = 25 & VPBiasRec = 30

10 Time Resolution of ATLASPix_Simple

In the following sections, the impact of the DAC settings on the time resolution of the ATLASPix_Simple is investigated. The same sensor (ID: 1-21) as on previous sections with 200 Ω cm substrate resistivity is used and noisy pixels are masked (see Table A.2). First, the measurement setup is introduced, followed by time resolution studies for varying DAC settings and ambient temperature. Finally, sensor-to-sensor variations and the single pixel time resolution are investigated.

10.1 Setup and Analysis Framework

The test setup for the following time resolution studies is illustrated in Figure 10.1. Beneath the sensor a scintillating tile is placed, whose signal provides time reference measurement (see section 8.3). In the following, the reference time stamp is labeled as trigger. As signal source strontium-90 is chosen, which is placed above the sensor and centered on the pixel matrix such that the whole sensor is illuminated. Since the source is unfocused, the intensity directly beneath the source is higher, decreasing with distance. Depending on the distance between source and sensor, the impact angle of the traversing particle decreases with the distance to the center of the source. This is primarily an effect along the row address of the sensor, due to its dimensions.

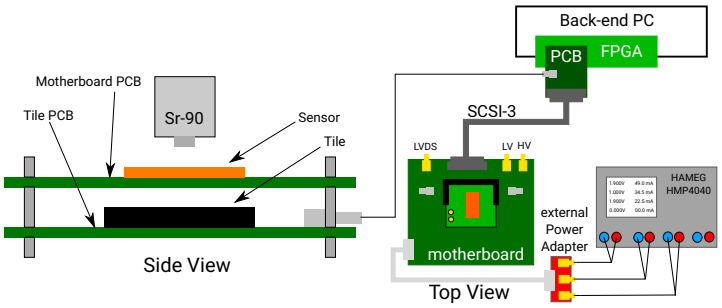


Figure 10.1: Time resolution study test setup.

The analysis framework for the laboratory characterization of the time resolution with a radioactive source was developed for MuPix8 [24] and has been adapted for ATLASPix1.
Since only one hit per column can be read out during a readout cycle, called frame, a simultaneous hit of same column and higher row address migrates in the subsequent frame. After a trigger is registered, the trigger time stamp is stored in the following readout cycle. Consequently, sequential frames are merged into one, labeled as merged frame, until an empty frame is send by the sensor.
The ambiguity of hit time stamps associated to a trigger time stamp within this measurements requires a correlation of all trigger time stamps to a hit time stamp within a

merged frame. The time difference between both time stamps is histogrammed in bins of the more precise time base of the trigger (2 ns).
The distribution can be described by a Gaussian and a background of all accidentally correlated events. The difference of two random variables, which do not originate from the same event, introduces a triangular shaped distribution. To obtain the time resolution, the following function is fitted to the data:

$$f(x) = \underbrace{A \times e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2}}_{\text{Guassian time distribution}} + \underbrace{B \times (C - |x|)}_{\text{background}} \tag{10.1}$$

For the Gaussian: A is the scaling parameter, μ displays the mean delay to the trigger and σ is taken as the time resolution in units of the bin size. For the background: B is again a scaling parameter and C is the maximum difference between hit time stamp and trigger in the time stamp base of the latter. For all shown measurement values, the mean and statistical error of the fit are presented. Influences of systematical errors are not included. An example distribution for all hit time stamps correlated to the triggers is shown in Figure 10.2.

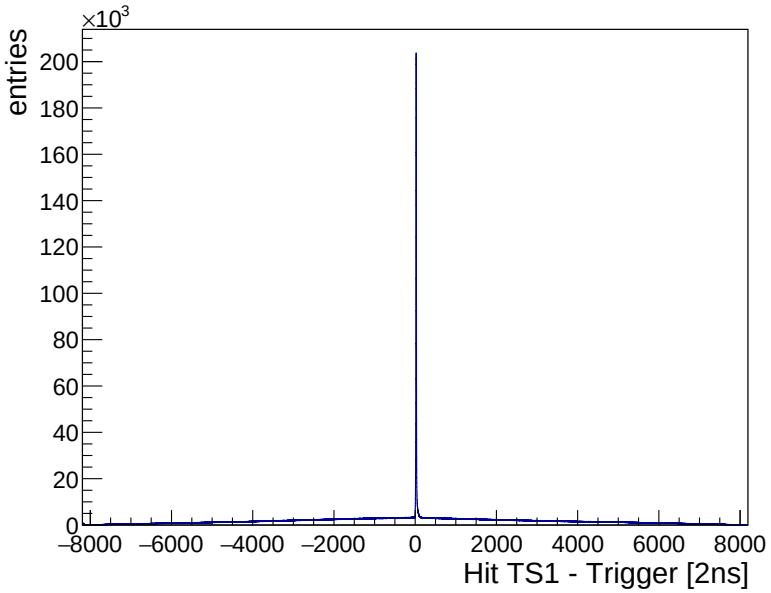
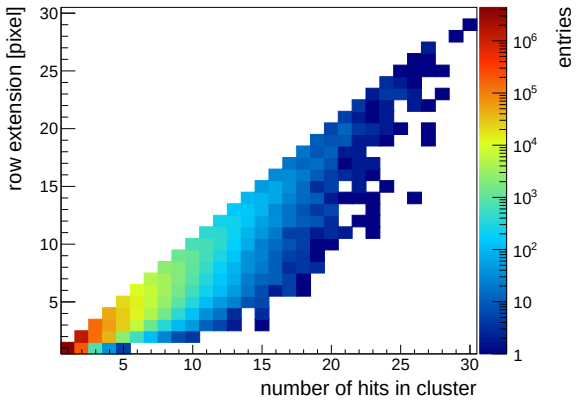


Figure 10.2: Example time stamp distribution correlated to the trigger for all hits.

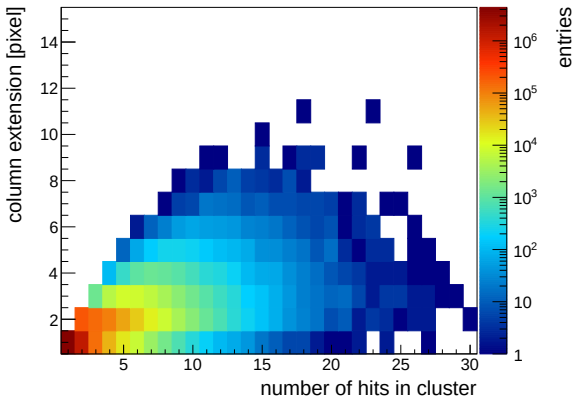
The initial latency distribution can be deteriorated by factors like internal chip delays or time walk, and is therefore corrected offline. It has to be noted that the time resolution is limited by the binning contribution of $16\,\text{ns}/\sqrt{12}$, which is the standard deviation of the uniform probability distribution, and pixel-to-pixel variations. The latter contribution includes variations in the comparator threshold. A individual tuning of the pixels is not performed. A single particle can create so-called clusters, whereby the ionization charge is distributed over multiple pixels. To account for this, a cluster analysis is applied. In the following sections a detailed explanation of these correction steps is given.

10.1.1 Cluster and Crosstalk

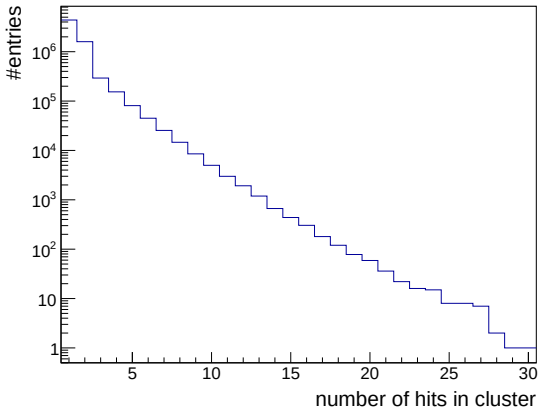
In this thesis a cluster is defined as directly neighboring pixels responding in a merged frame. The size of a cluster is the number of contributing hits. Cluster formation can be caused by different effects: Charge sharing between pixels, cross talk or particles traversing multiple pixels, e.g. a δ-electron. The former is created by a particle traversing the sensor at pixel borders, addressing up to four pixels at once. During the ionization process δ-electrons can emerge, see section 4.2.3 and Figure 10.3d, whose high kinetic energy allows secondary ionization in several pixel until the particle is stopped.
An example for the number of hits in a cluster as well as their extension in column and row direction is given in Figure 10.3. Due to the asymmetrical pixel dimensions, clusters can arise with a larger extension in row than column direction. Since the incident angle of an incoming particle decreases with the distance to the source center, larger cluster sizes can emerge along the row than the column, too.



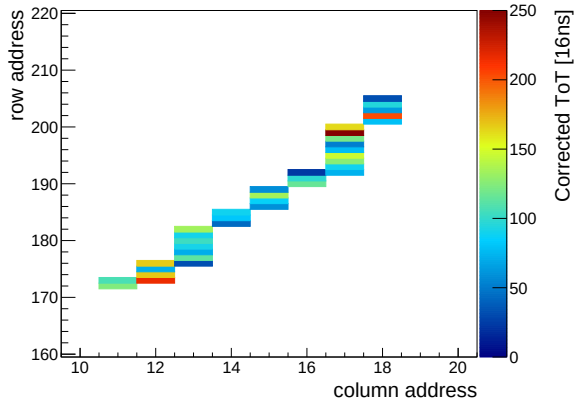
(a) Row extension of cluster



(b) Column extension of cluster



(c) Count of different cluster sizes



(d) Example event display of a δ-electron

Figure 10.3: Example plots for clustering.

Cross talk occurs in different forms, based on a capacitive coupling between two entities, e.g. pixel diodes or transmission lines between pixel and periphery cell. In the following, only the latter is investigated, labeled as line cross talk. However, influences

of other cross talk sources cannot be excluded. In the case of line cross talk, only the occurrence probability for clusters with two or three hits, labeled as double and triple clusters, is studied. Line cross talk can only emerge between consecutive pixels with the same column address. It is impossible to distinguish between a cross talk event and a physical event of a traversing particle. The only handle is to study the asymmetry between clusters along the row and column, since line cross talk can only emerge in a column. An illustration for geometrical occurrence of cross talk and charge sharing is displayed in Figure 10.4.

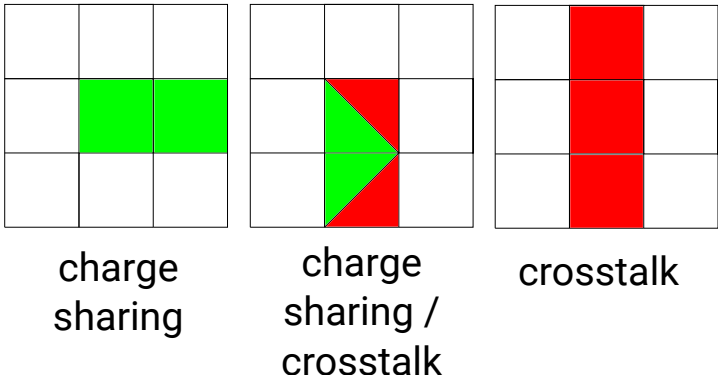


Figure 10.4: Charge sharing and cross talk [33].

The crosstalk probability is calculated by the difference between the quantity of vertical cluster (extension in row address) and horizontal cluster (extension in column address). In addition, only one-dimensional clusters are used, whose extension is only in row or column direction, respectively. The difference is calculated for each row and normalized to the total number of clusters in it:

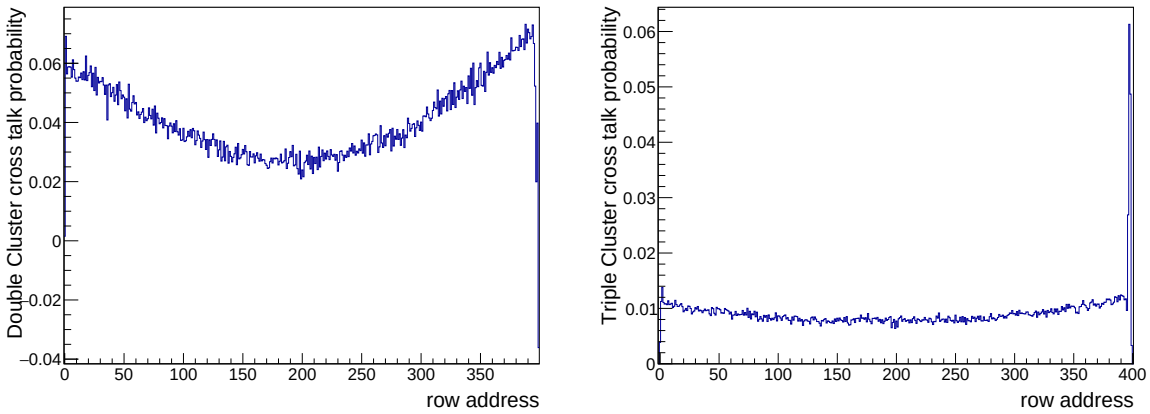
$$P_{xt}(row) = \frac{\frac{40\,\mu m}{130\,\mu m} \cdot n_{vertical}(row) - n_{horizontal}(row)}{n_{total}(row)} \tag{10.2}$$

Regarding the dimensions of the pixels, the probability of charge sharing is higher between neighboring pixel in a column than in a row and is therefore approximately corrected by a factor of $40\,\mu m/130\,\mu m$. An example for the cross talk probability of ATLASPix_Simple is shown in Figure 10.5. The increase of cross talk probability to higher and lower row addresses is caused by the geometry of the measurement setup. Here, more clusters with a size larger than one can emerge along the row address. Consequently, the absolute cross talk probability is overestimated. The triple cluster cross talk probability is smaller, compared to the cross talk probability for double clusters. Only a significant rise in cross talk probability is observed for the highest row addresses. This is a result of the longer signal lines with an increased inter-capacitance. Regarding, the in-pixel comparator a low cross talk probability is expected, due to small line signals, which cannot couple to a neighboring signal line. A lower voltage level of *VMinusPix* increases the line signal amplitude (see equation 7.4). Therefore, the dependence of the

observed cross talk is studied for the parameters, which influence the line signal. Due to the geometry of the setup, the subsequent measurements are only quantitative. In the following the average cross talk probability of the sensor is studied, calculated as follows:

$$P_{xt} = \frac{\frac{40\,\mu m}{130\,\mu m} \cdot n_{vertical} - n_{horizontal}}{n_{total}}, \tag{10.3}$$

as well as the maximum cross talk probability in a row (see equation 10.2), labeled in the following as maximum cross talk probability.



(a) Double cluster cross talk probability versus row address

(b) Triple cluster cross talk probability versus row address

Figure 10.5: Example of cross talk probability of ATLASPix1.

For line crosstalk, primarily the fast component of the line transmission signal couples to a neighboring line, resulting in an earlier detection.
For the analysis of the time resolution and cross talk study only the hit with the earliest time stamp is considered. Cross talk affects the time resolution, but due to its low probability, the influence is marginal.

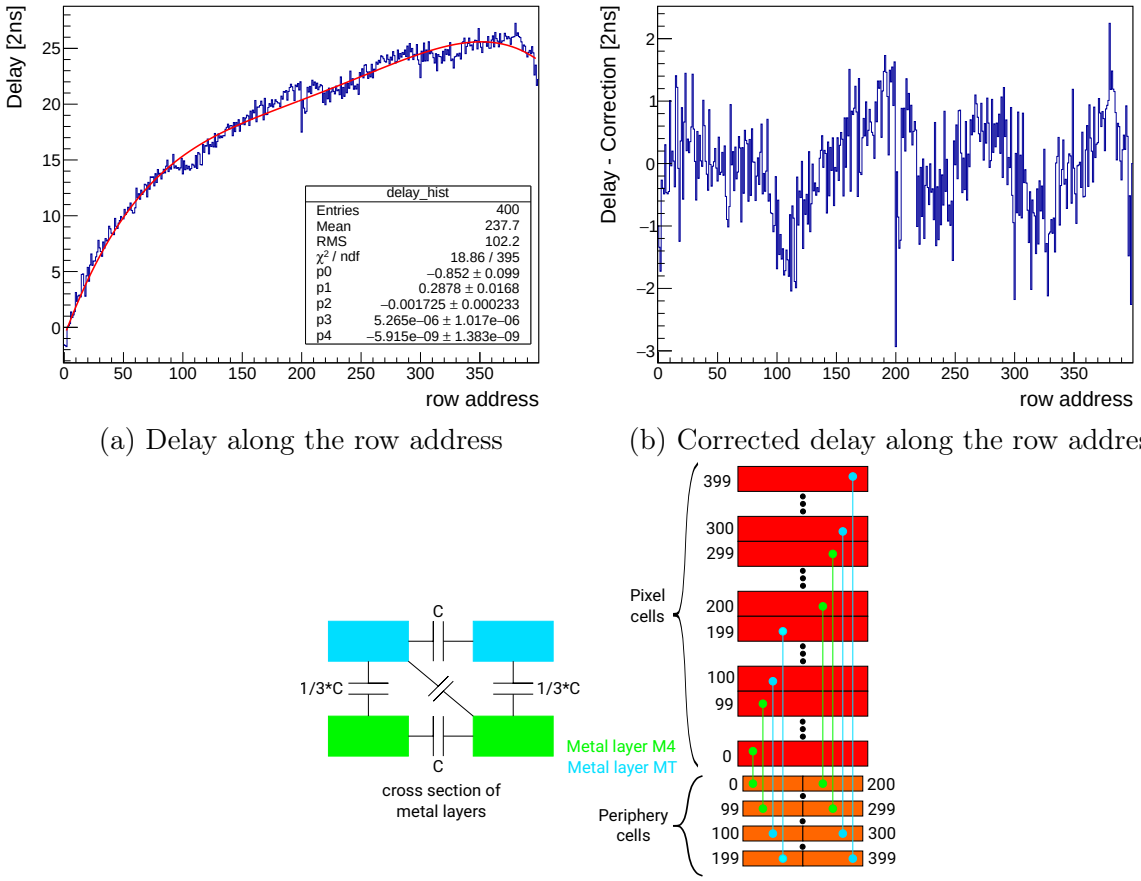
10.1.2 Delay Correction

As aforementioned, each pixel cell has a point-to-point connection to its digital partner, the periphery cell. The main influence on the delay is observed along the row address with an increase in the delay with higher row addresses. The different length in transmission lines as well as the capacitive coupling between the metal layers on the chip result in a different delay to the trigger time stamp for each pixel. Due to limited statistics, pixels are grouped in blocks of 1×25 (row×column). The delay is corrected according to the following fit function:

$$\text{Delay}(row) = \text{Offset} + A \times \text{row} + B \times \text{row}^2 + C \times \text{row}^3 + D \times \text{row}^4. \tag{10.4}$$

Figure 10.6 displays an exemplary measurement of the delay along the row address as well as the fit result and the consequential correction afterwards. Larger deviations

from the fit function are observed at around row address 100, 200 and 300. This can be explained by metal layer transitions, see Figure 10.6c. The metal layers comprise the signal lines of the point-to-point connections between pixel and periphery cell. Two metal layers are used for the signal transmission, alternating connected to pixel blocks of 100 in row direction. Consequently, the capacitance between signal lines changes at such a transition, causing a change in the delay.



(a) Delay along the row address

(b) Corrected delay along the row address

(c) Schematic of the ATLASPix1 point-to-point connection routing

Figure 10.6: Example of delay correction for ATLASPix1.

10.1.3 Time Walk Correction

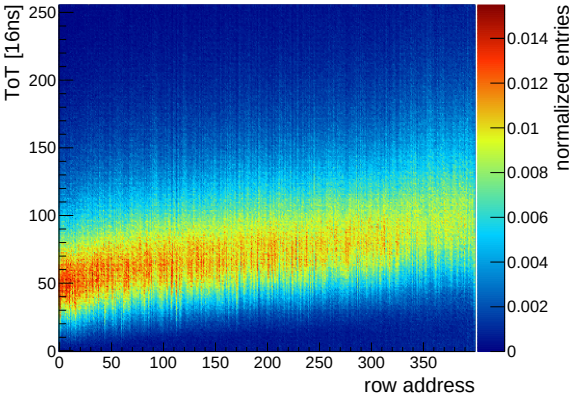
The crossing time of the comparator is correlated to the amplitude of a signal. A signal with larger amplitude crosses the threshold earlier in time than a signal with smaller amplitude, resulting in time-walk. In addition, the signal with larger amplitude stays longer over the threshold. The ToT is the difference between the two crossing times of the comparator threshold and can be calculated according to equation 7.5. The crossing time is correlated to the ToT to observe the time walk and can therefore be used to correct for it.

ToT Correction

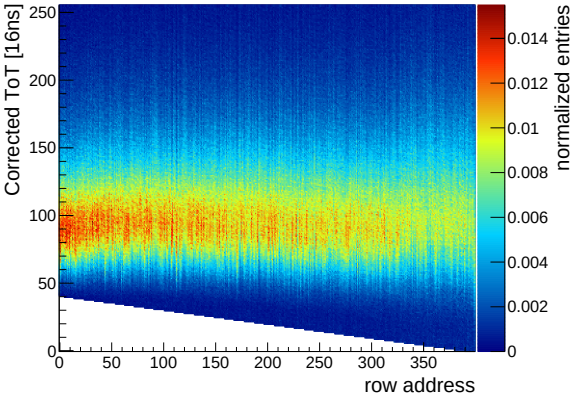
The ToT dependence for row and column address is displayed in Figure 10.7. The ToT spectrum is normalized to an integral of 1 for each roe address. An increase of the most probable ToT is observed for higher row addresses. Since, no significant deviation for the amplitude has been observed along the row, the ToT itself is corrected, before it is used for time walk correction. Lower ToT values with the same latency as higher ToTs would smear out the time walk distribution and deteriorate the precision of its correction. The correction is done by a linear fit to the most probable ToT of a row address:

$$ToT(row) = Offset + A \times row \tag{10.5}$$

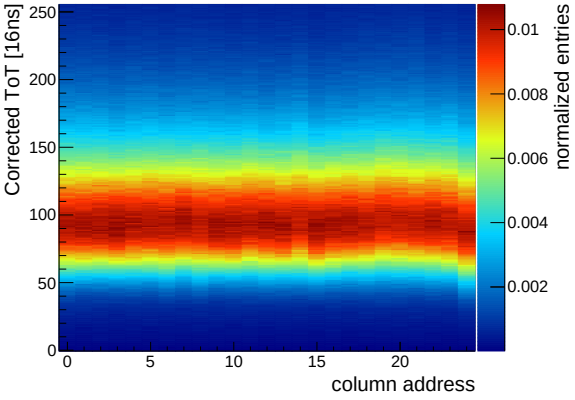
which is defined as the weighted average of the maximum bin and seven bins to each side, rounded to the nearest integer bin. No ToT dependency on the column address is observed.



(a) ToT row projection before correction



(b) ToT row projection after correction



(c) ToT column projection

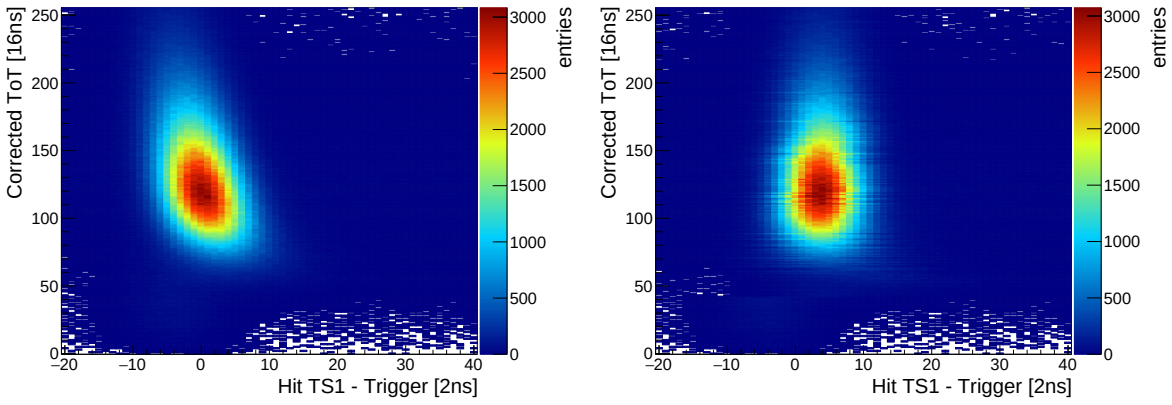
Figure 10.7: ToT projection for row and column of a Sr-90 source for earliest TS1.

Time Walk Correction

To correct for the time walk effect all ToTs are plotted versus the latency, defined as the difference of trigger and hit time stamp. The aforementioned delay correction as well as the ToT correction are applied beforehand. For each ToT value the maximum of the latency distribution is taken, defined again as weighted average of the maximum bin and seven bins to each side rounded to the nearest inter bin. Low significance ToT values with less than 10000 entries are neglected due to low precision and significance. The time walk corrected time difference is given by:

$$\Delta t_{\text{twc}} = \Delta t_{\text{latency}} - \mu(ToT) \tag{10.6}$$

Here, $\Delta t_{\text{latency}}$ is the latency and $\mu(ToT)$ the arithemtic mean of the corrected time difference for each ToT slice. Figure 10.8 shows an example of time walk before and after time walk correction (TWC), which is small for the given threshold.



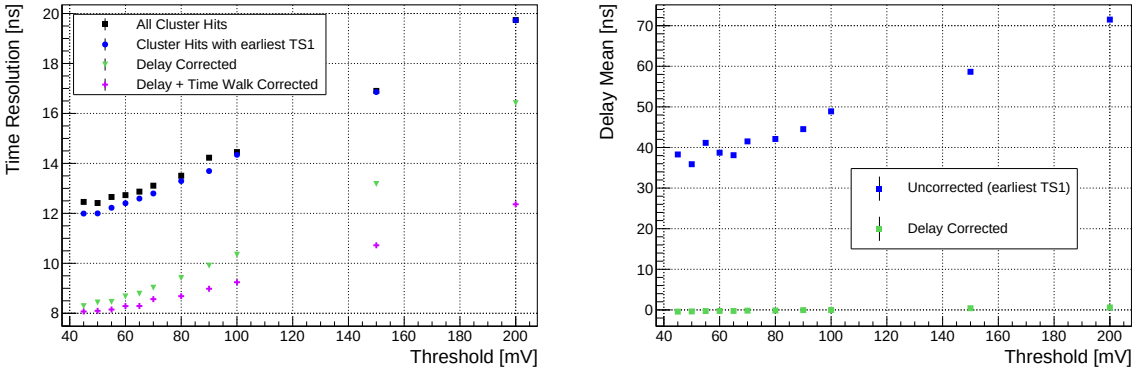
(a) Latency versus ToT before TWC

(b) Latency versus ToT after TWC

Figure 10.8: Latency versus ToT before and after TWC at a threshold 60 mV above the baseline.

10.2 Threshold Dependence

Figure 10.9 shows a steep improvement of the time resolution with lower *ThPix*, which saturates at around 60 mV, when the noise starts to contribute. Figure 10.10 shows a result of a testbeam measurement, for which the noise increases steeply to lower thresholds, whereas the noise rate is at a constant level at thresholds higher than 70 mV. Due to different operation conditions, the threshold level, where the noise rate starts to increase, is higher than in the laboratory.
Simultaneously, the delay mean decreases, caused by earlier crossing of the comparator threshold. As consequence of a lower threshold, the cluster size increases, caused by the detection of low amplitude signals arising from charge sharing. The contribution of these hits is accounted for by using only the earliest time stamp of each cluster. For subsequent measurements a threshold of 60 mV above the baseline is chosen as working point, since the improvement of the time resolution at lower threshold is marginal and the noise contribution is not yet significant.



(a) Time resolution versus threshold

(b) Delay mean versus threshold

Figure 10.9: Time resolution study on the threshold at HV = −60 V.

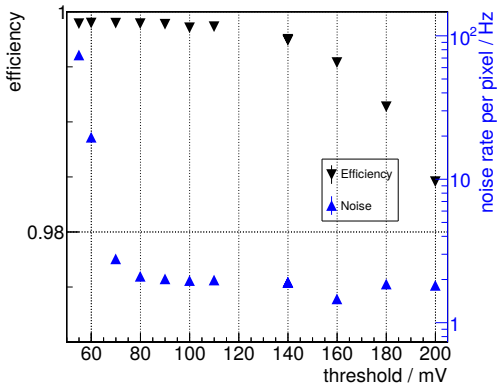


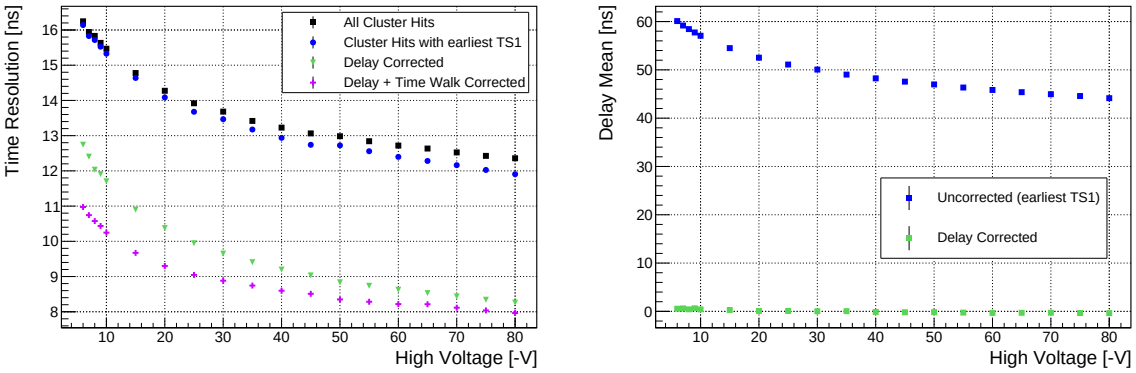
Figure 10.10: Testbeam measurement of efficiency and noise rate [46].

10.3 HV Dependence

The time resolution improves with higher high voltage, see Figure 10.11. Simultaneously, the contribution of large clusters induced by charge sharing increases, due to the growth of the depletion zone. This is shown in the increasing deviation of the time resolution between all cluster hits and only earliest TS1 of a cluster. In addition, the contribution of time walk decreases, caused by larger charge collection and consequential larger signal crossing the comparator earlier in time. Furthermore, the charge collection time decreases with the high voltage, due to a higher electric field [22]:

$$\langle E \rangle = \frac{V_{\text{ext}}}{d}, \tag{10.7}$$

resulting in a steeper rise of the amplified signal. For a parallel plate geometry with a uniform field, the latter increases linearly with the supplied bias voltage V_{ext} according to equation 10.7. In this formula, d is the charge collection electrode spacing.
For all prior and subsequent measurements $-60\,\text{V}$ is chosen as working point. This value enables comparisons with testbeam measurement results done at the same high voltage level. In fact, the time resolution increases with higher voltage levels of the supplied reverse bias voltage. At $-80\,\text{V}$ the sensor reaches the breakdown domain of the pixel diodes.



(a) Time resolution versus reverse bias voltage

(b) Delay versus reverse bias voltage

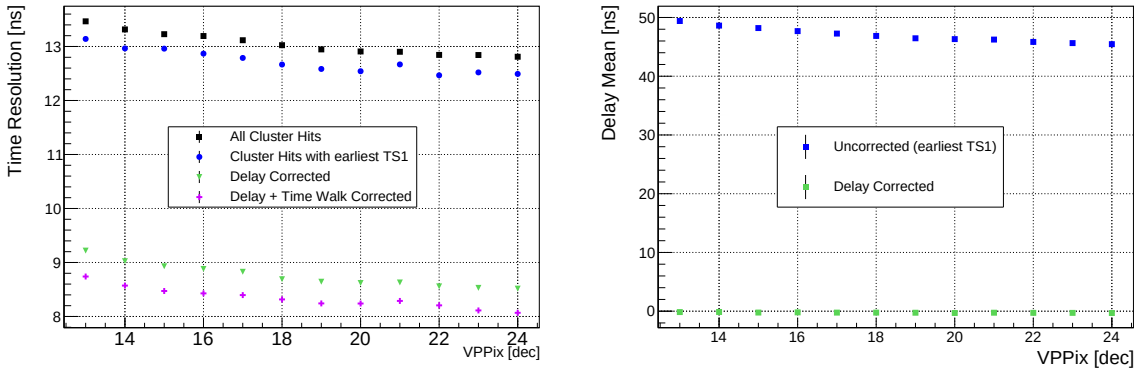
Figure 10.11: Time resolution study on the reverse bias voltage.

10.4 Time Resolution and DAC Settings

Several DAC parameters have shown a significant impact on the amplifier signal and the power consumption, see section 9.7. This measurement results have to be compared to the achievable time resolution and efficiency for each parameter. The influence on the time resolution is presented in the following. Only the DAC scans, which are used to improve the time resolution are discussed. More measurement results are presented in the appendix, see section B.

VPPix

All measured time resolutions improve for higher values of *VPPix* (see Figure 10.12), which is consistent with the observation of an increase of the rise, see section 9.7. The same applies for the delay mean. Albeit an increase of the power consumption is associated with higher DAC values. A trade-off between slightly better time resolution and increased power consumption has to be considered. Measurements with larger *VPPix* values than 24 are done in the course of the temperature dependence and are discussed in section 10.5.



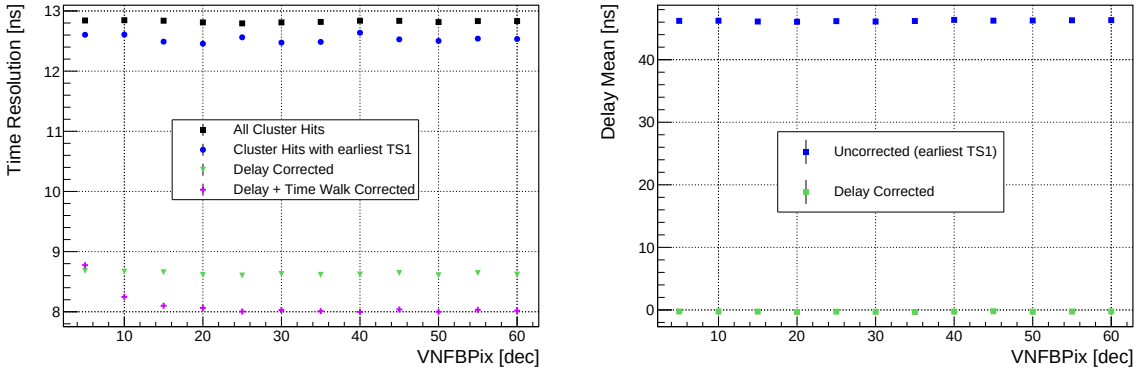
(a) Time resolution versus VPPix

(b) Delay versus VPPix

Figure 10.12: Time resolution study on VPPix.

VNFBPix

According to the analog measurements in section 9.7, no significant deviation for the rise is observed for *VNFBPix*. Since, the amplitude decreases with higher DAC values, an influence due to amplified noise signals decreases too. If the efficiency is not significantly influenced by the decrease of the amplitude, larger operational values could be considered. Figure 10.13 shows the measurement results on the time resolution for different *VNFBPix* values. The measured time resolution before time walk correction stable over the entire measurement region. The same applies for the delay mean. After time walk correction, the time resolution is deteriorated for *VNFBPix* smaller 15. As a consequence, *VNFBPix* larger than this value are recommended, if no change in the efficiency is observed.

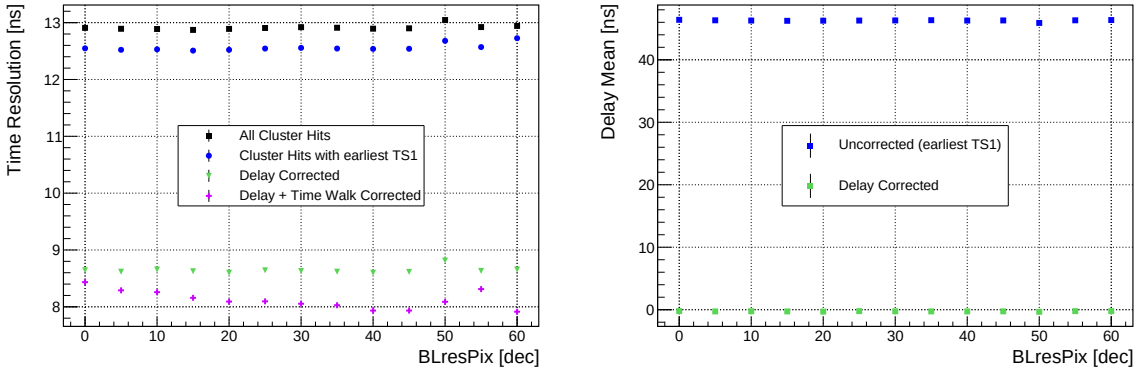


(a) Time resolution versus VNFBPix (b) Delay versus VNFBPix

Figure 10.13: Time resolution study on VNFBPix.

BLResPix

A change of the DAC value of *BLResPix* has shown no change in the efficiency of ATLASPix_Simple [28]. Higher DAC values are favored since the effect of white noise is expected to be reduced. Figure 10.14 shows slight variations of the time resolution before time walk correction and the delay mean. Since, the time resolution is not affected by a change of the DAC value, the rise of the amplifier signal is not significantly affected, too. The time walk corrected data improves slightly to higher *BLResPix*. This is a result of less fluctuations of the falling edge of the amplified signal and less noise, which enables a better time walk correction. As a result, the operational DAC value can be chosen freely between 20 and 60. Larger DAC values are recommended, since a smaller noise rate is observed.

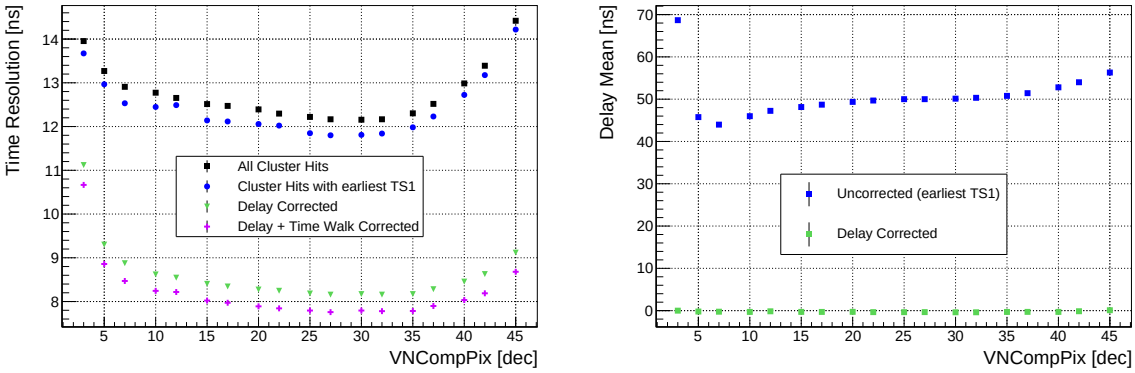


(a) Time resolution versus BLResPix (b) Delay versus BLResPix

Figure 10.14: Time resolution study on BLResPix.

VNCompPix

The time resolution improves strongly for *VNCompPix* values up to 10 and further minimizes up to a DAC value of 25. Between a *VNCompPix* of 25 and 35 the time resolution is constant and then deteriorates to higher DAC values. Consequently, a DAC value between 10 and 35 is recommended for operation. For *VNCompPix* values between 15 and 35, a time resolution below 8 ns can be achieved. While taking data, a decrease of the noise was observed with higher DAC values, which is caused by the stabilization of the comparator with higher current flows. The associated faster switching of the comparator improves the time resolution, but causes an increase of the power consumption. A larger value than the default of 10 is recommended in terms of time resolution. However, the single hit efficiency for these DAC values has to be studied.



(a) Time resolution versus VNCompPix

(b) Delay versus VNCompPix

Figure 10.15: Time resolution study on VNCompPix.

VMinusPix Study

As discussed in section 9.8, *VMinusPix* has a significant impact on the time resolution. Its operation range was chosen to be between 450 mV and 900 mV. Similar to the delay mean, the uncorrected time resolution increases steeply for smaller *VMinusPix* voltage levels. Since the line driver influences the line signal shaping in addition to the delay, the time walk corrected time resolution is deteriorated for higher voltage levels. Simultaneously, an increase of the cross talk probability for double and triple clusters is observed for lower voltage levels. For *VMinusPix* lower then 650 mV, the triple cluster cross talk dominates over double cluster cross talk, whereby the probability for double clusters decreases. The increase of cross talk probability is caused by a larger line signal amplitude (see equation 7.4), whose high frequency component can couple to neighboring signal lines. An example plot for the triple cluster cross talk probability is displayed in Figure 10.16, which shows that the cross talk probability starts to rise at row address 300 and increase significantly to higher row addresses.
Since no significant improvement on the time resolution for *VMinusPix* lower than 700 mV is observed and an increase of cross talk emerges, lower voltage levels than the this value are not recommended.

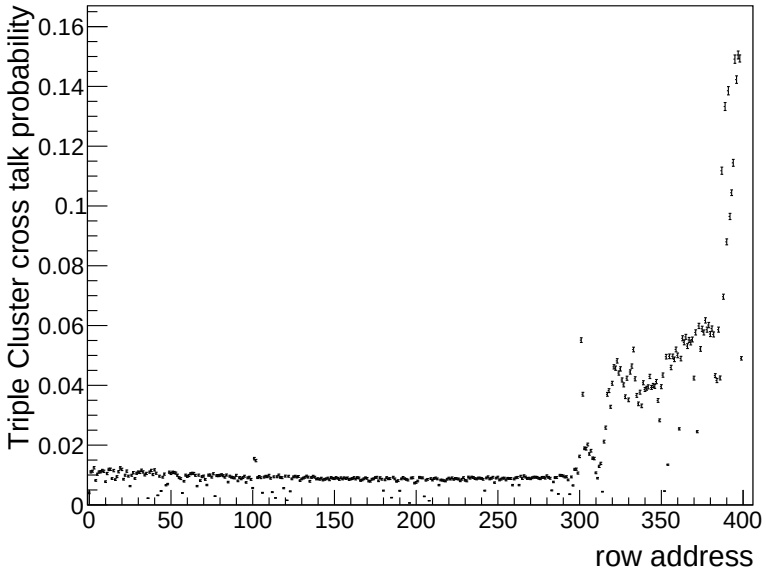
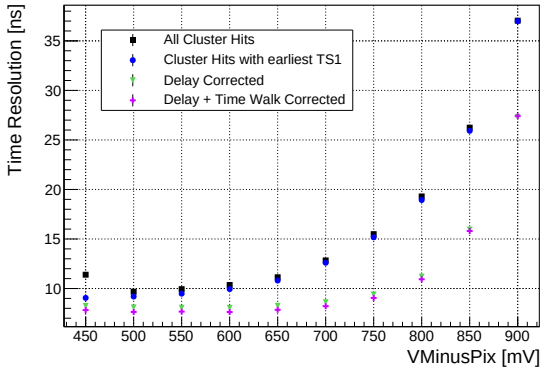
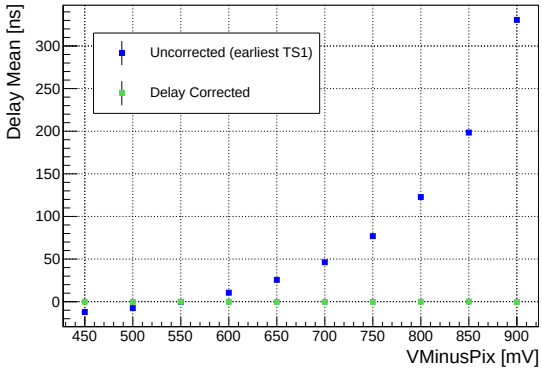


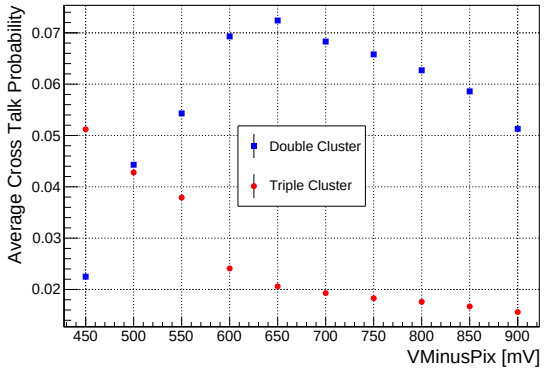
Figure 10.16: Triple cluster cross talk probability versus row address at VMinusPix = 550 mV



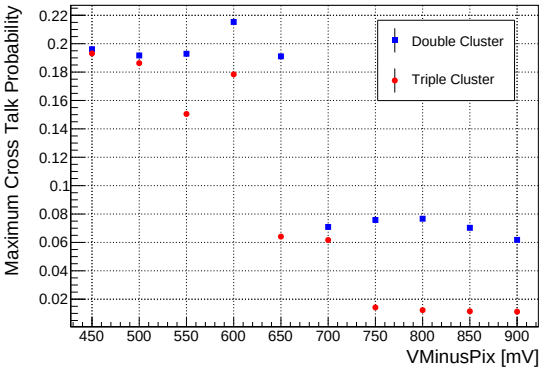
(a) Time resolution versus VMinusPix



(b) Delay versus VMinusPix



(c) Average cross talk probability versus VMinusPix

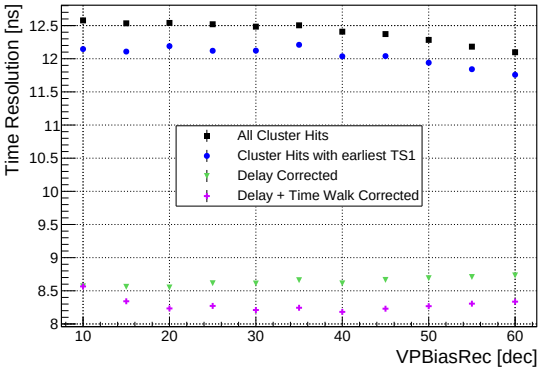


(d) Maximum cross talk probability in a row versus VMinusPix

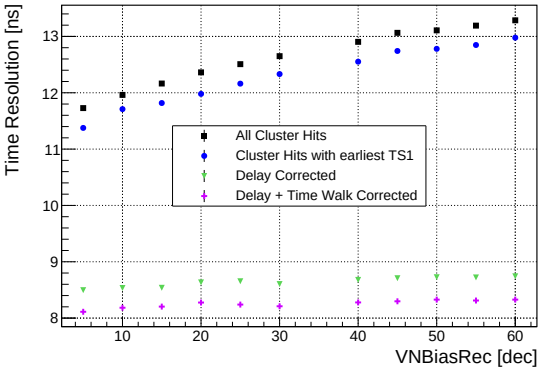
Figure 10.17: Time resolution study on VMinusPix.

VPBiasRec and VNBiasRec

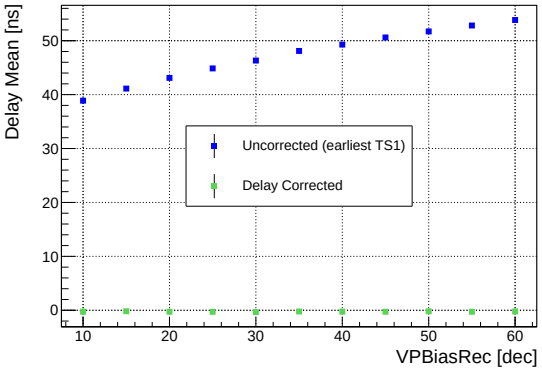
The DACs *VPBiasRec* and *VNBiasRec* control the conversion of the low-amplitude line signal into a CMOS amplitude for the edge detector. The associated pulse shaping influences the time resolution and is therefore studied. Figure 10.18 shows the individual DAC influence on the time resolution and the delay mean. For the given situation, only the value of one DAC was changed and the other is set to the default value. The delay mean decreases for both DACs linearly. For *VNBiasRec* the same linear improvement is reflected in the improvement of the time resolution before delay correction. After delay and time walk correction, the time resolution is stable for the entire DAC range. For *VPBiasRec* the time resolution before delay correction deteriorates to smaller DAC values. Simultaneously, only a fluctuation of the time resolution is observed for delay corrected data. The time walk correction seems to be affected at *VPBiasRec* values lower than 20. Thus, a *VPBiasRec* value smaller 20 should not be used for operation.



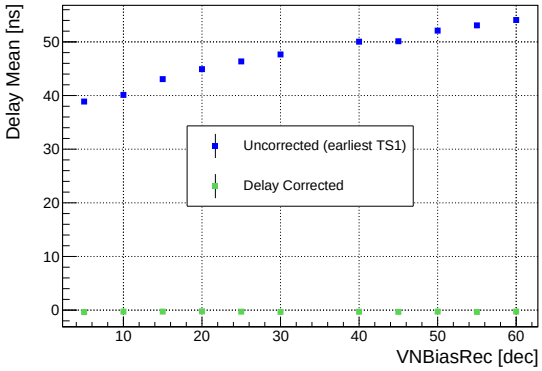
(a) Time resolution versus VPBiasRec



(b) Time resolution versus VNBiasRec



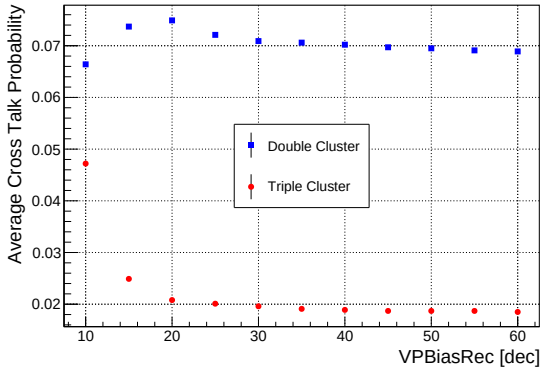
(c) Delay versus VPBiasRec



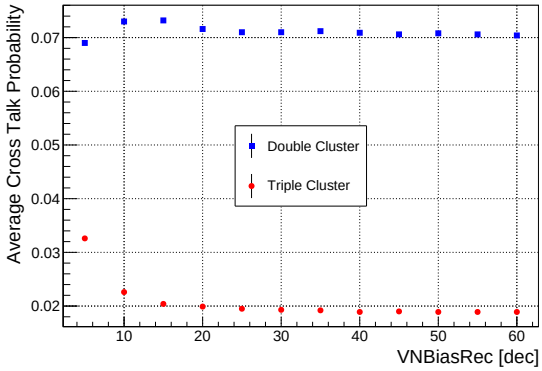
(d) Delay versus VNBiasRec

Figure 10.18: Time resolution study on VPBiasRec and VNBiasRec.

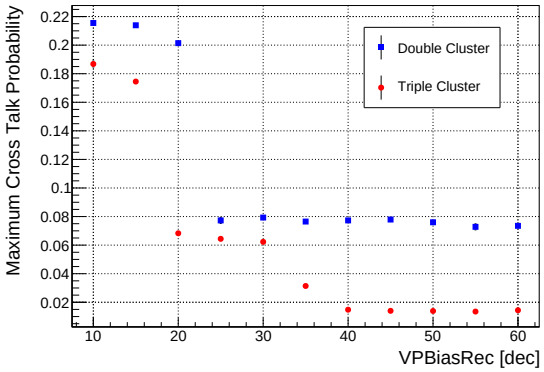
The measurement results for the cross talk probability is shown in Figure 10.19 for both DACs. Both display a similar behavior of the change of cross talk probability for a DAC alteration with respect to the default values. For the average cross talk probability no significant deviation is observed for *VPBiasRec* between 30 and 60 and for *VNBiasRec* between 25 and 60. For lower DAC values the cross talk probability for triple cluster increases and for double cluster at first a slight increase is observed, subsequently decreasing, when the triple cluster cross talk start to increase significantly. For the maximum cross talk probability a significant increase is observed for DAC values lower 20. For higher values, the double cluster cross talk probability is stable. The same applies for the triple cluster, if one of the DAC values is chosen to be larger than 40. A fine tuning, for the desired *VMinusPix* value can be done with the DACs in terms of cross talk. If the efficiency is not affected, a DAC value of 40 for *VPBiasRec* is recommended.



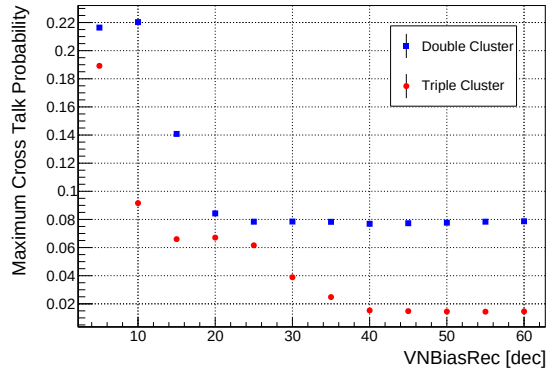
(a) Average cross talk probability versus VPBiasRec



(b) Average cross talk probability versus VNBiasRec



(c) Maximum cross talk probability in a row versus VPBiasRec



(d) Maximum cross talk probability in a row versus VNBiasRec

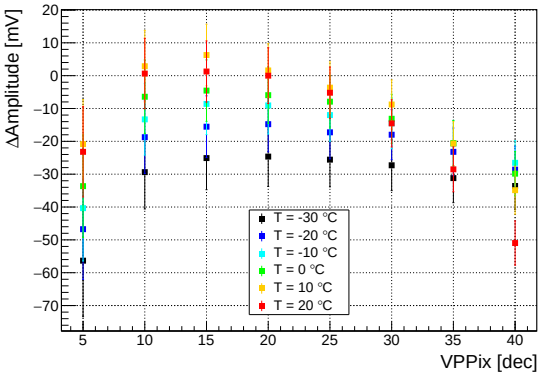
Figure 10.19: Cross talk study on VPBiasRec and VNBiasRec.

10.5 Temperature Dependence of ATLASPix_Simple

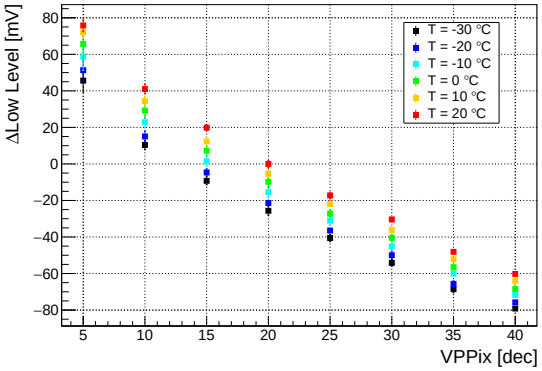
In the ATLAS experiment the pixel sensors are cooled down to −30 °C, which reduces the dark current of the pixel diodes and the pixel noise (see equation 5.8). However, ATLASPix1 consists of transistors, whose working point can shift with temperature. For this reason, the influence on the time resolution dependence on the ambient temperature is investigated in a climate chamber (see section 8.7).
For decreasing ambient temperature a significant increase in noise was observed in contrast to the expectation, which disfavors the operation at the default DAC settings. A major impact on the noise was found to be the current supply of the CSA, controlled by *VPPix*. Higher DAC values lead to a lower noise. To investigate the temperature dependence on the CSA, a *VPPix* scan with the AmpOut is performed for ambient temperatures between 20 °C and −30 °C in steps of 10 °C. All measurement values are given with respect to the default value of $VPPix = 20$ and an ambient temperature of 20 °C. The mean value of the pulse shape parameters of the AmpOut for this setting are listed in Table 10.1.

Parameter	Mean Value	Unit
Amplitude	247.269	mV
Low Level	667.360	mV
Rise	1.292	$\mathrm{mV\,ns^{-1}}$
Fall	0.501	$\mathrm{mV\,ns^{-1}}$

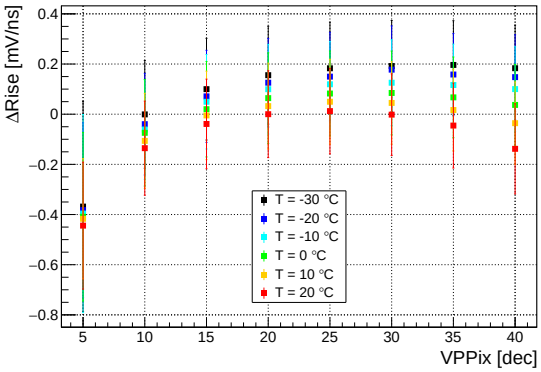
Table 10.1: Mean pulse shape parameter values at the default DAC settings at 20 °C.



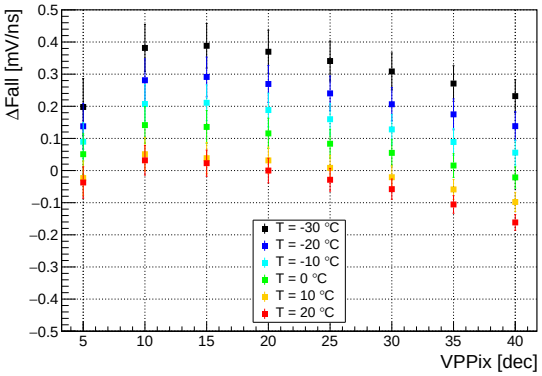
(a) ΔAmplitude versus VPPix for different temperatures



(b) ΔLow Level versus VPPix for different temperatures



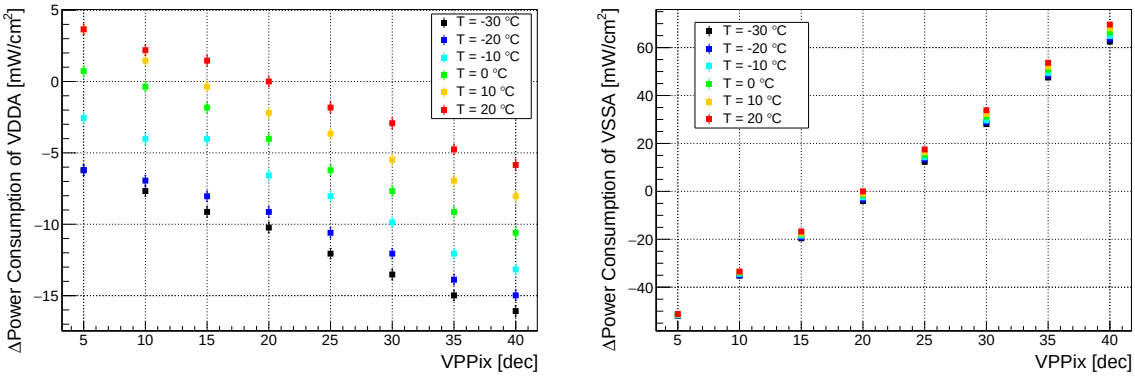
(c) ΔRise versus VPPix for different temperatures



(d) ΔFall versus VPPix for different temperatures

Figure 10.20: AmpOut pulse shape parameter dependence on VPPix for different ambient temperatures.

The measurement results of the pulse shape parameters are shown in Figure 10.20. The influence on the amplitude depending on *VPPix* is similar for all temperatures. For VPPix values between 5 and 25, the amplitude first increases with decreasing temperature. For temperature lower than 10 °C it decreases again. For VPPix larger 25, the amplitude decreases faster for higher temperatures. The low level shows the same dependence on *VPPix* for all temperatures, whereby the voltage level decreases with lower temperatures. For the slew rates the same influence of the DAC value is observed, which increase with lower ambient temperatures. In summary, with temperatures below 10 °C the amplifier pulse shrinks, while the steepness of the slew rates increases, which shortens the pulse length.
Furthermore, the power consumption for VDDA and VSSA is monitored for each DAC value and temperature, see Figure 10.21.

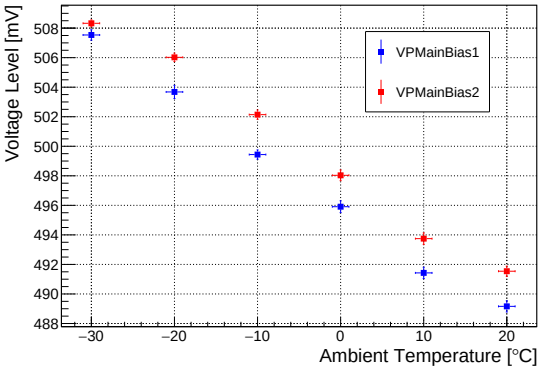


(a) Power consumption for VDDA versus VPPix for different temperatures

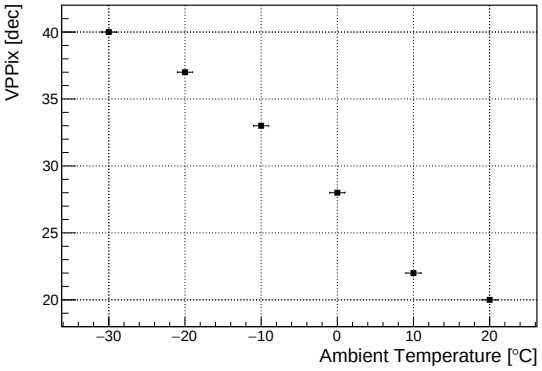
(b) Power consumption for VSSA versus VPPix for different temperatures

Figure 10.21: Power consumption dependence on VPPix for different ambient temperatures.

The power consumption of VDDA decreases with lower temperatures and the DAC dependency shows an equally linear decrease with higher *VPPix* values. Also, for VSSA the linear increase for each ambient temperature is observed, whereas the steepness slightly decreases for lower temperatures.
The decrease of current flow as well as the impact on the amplifier pulse with the temperature can be related to a change of the main bias voltages, *VPMainBias1* (digital block) and VPMainBias2 (analog block). They provide a current reference for the sensor and therefore control the working point of the circuitry. If the reference current changes with the temperature the working point and the drawn current shift as observed. According to Figure 10.22a, the both voltage levels increase linearly with lower temperatures.



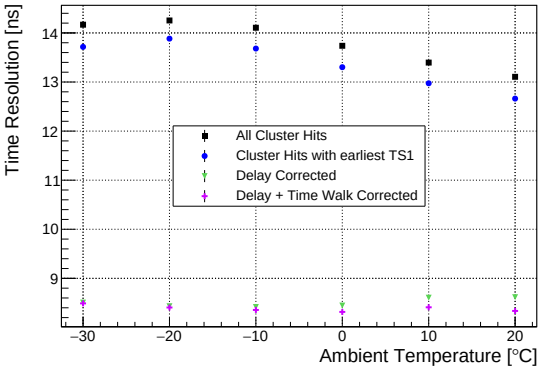
(a) Main bias voltage versus ambient temperature



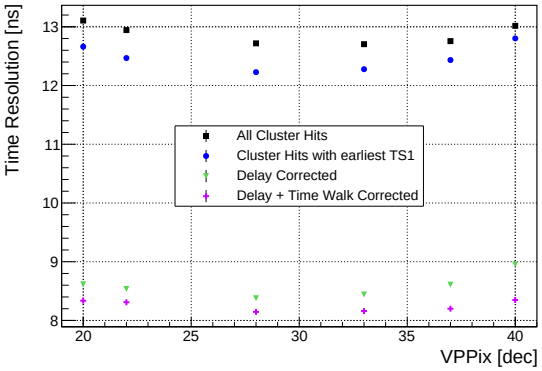
(b) VPPix value for equal noise response versus ambient temperature

Figure 10.22: Working point dependence on ambient temperature.

To achieve equal noise response for the time resolution measurement at different temperatures, the DAC value of *VPPix* is adjusted according to Figure 10.22b.
The temperature dependence on the time resolution is displayed in Figure 10.23a. The uncorrected time resolution improves with higher ambient temperatures, whereas the delay corrected time resolution improves slightly with lower temperature. The influence of time walk decreases with lower temperatures, caused by the steeper rise of the amplified signal .
The high *VPPix* values that are used to compensate the noise increase for lower temperatures were not investigated in section 10.4. The time resolution for these *VPPix* values at 20 °C is therefore given in this section (see Figure 10.23b). The time resolution before and after corrections shows the same DAC dependence. The time resolution slightly improves up to a *VPPix* value of 28 and deteriorates for even higher values.



(a) Time resolution versus ambient temperature.



(b) Time resolution versus VPPix at 20 °C.

Figure 10.23: Time resolution study on at different ambient temperatures and VPPix values.

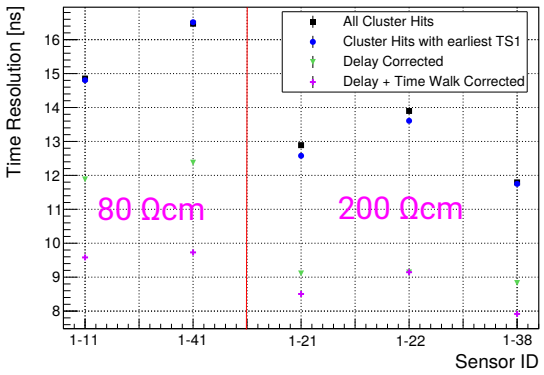
10.6 Sensor to Sensor Variations

All previous measurements are done with the same sensor (1-21) with a substrate resistivity of 200 Ω cm. ATLASPix1 was produced with four substrate resistivities, 20 Ω cm, 80 Ω cm, 200 Ω cm and 1000 Ω cm. Only sensors with 80 Ω cm and 200 Ω cm are studied. In addition, sensor-to-sensor variations are expected [33]. In the following the different substrate resistivity sensors are labeled as 80 Ω cm and 200 Ω cm sensors. To observe variations in the production, the time resolution is investigated for five sensors from four different wafers. Due to the low statistics of available sensors at the time of this measurement, a statement on sensor-to-sensor variations, but not on wafer-to-wafer variations, can be made. The production information for each investigated sensor is listed in Table 10.2.

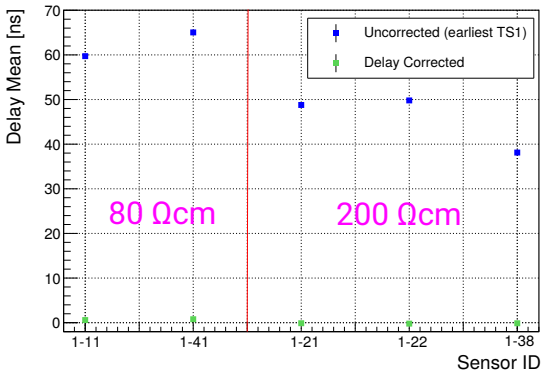
sensor ID	Substrate resistivity [Ω cm]	Thickness* [µm]	Wafer ID
1-11	80	70	9
1-41	80	70	10
1-21	200	100	22
1-23	200	100	22
1-38	200	100	23

Table 10.2: ATLASPix_Simple Sensor production information (*ordered thickness, can differ in reality).

All measurements are done at a threshold value of 80 mV above the baseline and a high voltage of −60 V. The higher threshold is chosen, to reduce influences by increased noise for the 80 Ω cm sensors, which arises from the higher capacitance of the pixel diode, see equation 5.6. For the 80 Ω cm sensors to be equal to the 200 Ω cm sensors in terms of the width of the depletion zone and pixel diode capacity at −60 V, a high voltage of −150 V would be required, see equation 5.4. However, these sensors reach the breakdown domain before that. Therefore, the prior mentioned high voltage level is chosen.
The 80 Ω cm sensors show a similar time resolution of about 9.6 ns after delay and time walk correction. Before delay correction the time resolution differs, due to the different sensor delays and larger time walk. A worse time resolution with respect to the 200 Ω cm sensors is expected, due to the smaller signal amplitude at the same high voltage.
The 200 Ω cm sensors can reach a time resolution of about 8 ns (for sensor ID 1-38). For the sensors from wafer 22, the delay mean is similar, but the initial time resolution differs by around 1 ns. The sensor from wafer 23 shows a better delay mean, represented in an improved initial time resolution. After delay correction, the time resolution for all 200 Ω cm sensors is similar. Large deviations are observed after the time walk correction. The sensor 1-22 shows no improvement, while the time resolution of the other two improves. The deviations could be evoked by a deterioration of the line signal, influenced by the comparator, the driver and the receiver, caused by variations in the production process.



(a) Time resolution versus sensor ID



(b) Delay versus sensor ID

Figure 10.24: Time resolution study on Sensors.

10.7 Optimization of Time Resolution

An optimization in terms of time resolution according to prior measurements is performed. Figure 10.25 shows the individual optimization steps for improved time resolution. By increasing the DAC value of *BLResPix*, the time walk can be corrected more precisely. In addition, larger values for *VPPix* and *VNFBPix* are used, to improve the rise and lower the noise. The main contributions for improved time resolution is set by a higher *VNCompPix* value of 25. The increased high voltage, results in larger signal amplitudes and decreases the effect of time walk. With these measures the time resolution improves from 8.2 ns to 7.2 ns.

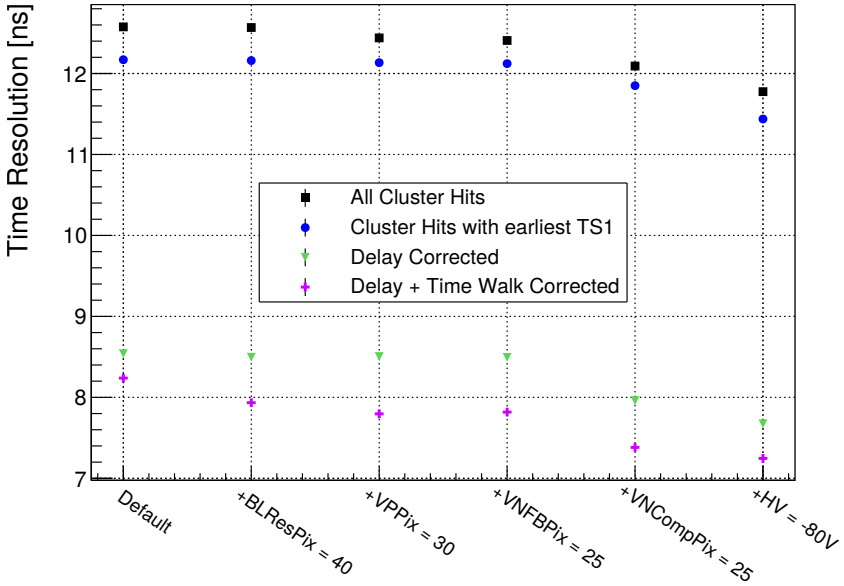


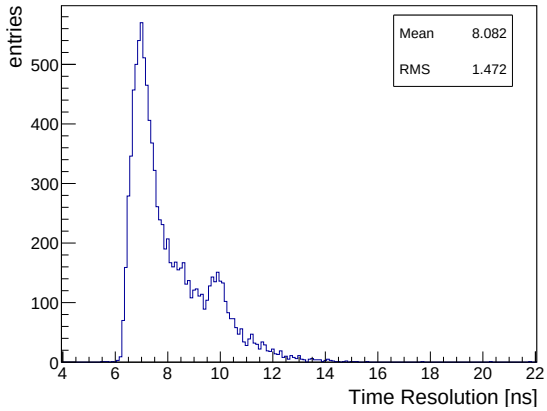
Figure 10.25: Steps for improving the time resolution.

10.8 Single Pixel Time Resolution

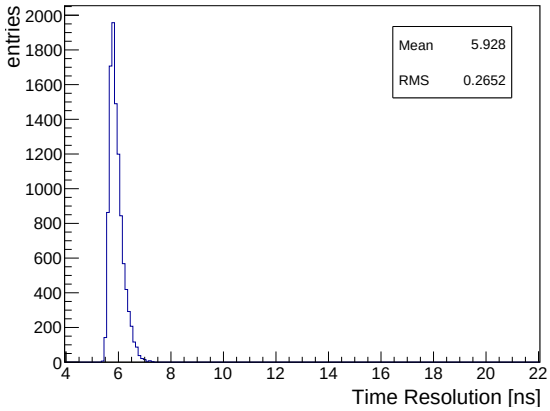
To observe the achievable time resolution of single pixels, a large number of measurements is taken to reach enough statistics for each pixel. For this measurement the optimized setting from section 10.7 are used.
One should note that the data from multiple files are combined in this analysis and the delay may change slightly from file to file. This study is done with sensor 1-21 and the correction steps are performed according to corrections mentioned above. The delay correction is not performed for each pixel time stamp, but used in the time walk correction. The individual time resolution is taken from the fit procedure. Since not all fits converge in this procedure, a $\mathcal{X}^2_{\text{red}}$ cut and a cut on the number of peak entries is performed.
Figure 10.26 shows the time resolution before and after TWC. Before TWC, the mean of single pixel time resolution is at $8.082 \pm 1.472\,\text{ns}$. The time resolution distribution shows two peaks, one around 7 ns and one around 10 ns. This is caused by increased time walk influences to higher and lower row addresses and can therefore be corrected for. In addition, worse time resolution is observed for some pixels between row 0 and 100. This could be an influence of a line signal deterioration. In addition, a higher gradient of the signal delay is observed in this range. After TWC the mean single pixel time resolution improves to $5.928 \pm 0.2652\,\text{ns}$ and the time resolution pixel map displays an uniform distribution for all pixels between row address 0 and 350. For higher row addresses slightly worse time resolution is observed, represented in a small tail to higher values in the time resolution distribution.
If the binning contribution of $16\,\text{ns}/\sqrt{12}$ is subtracted, the intrinsic time resolution capability of the ATALSPix_Simple is shown:

$$\text{intrinsic time resolution} = \sqrt{(\text{measured time resolution})^2 - \left(\frac{16\,\text{ns}}{\sqrt{12}}\right)^2} \tag{10.8}$$

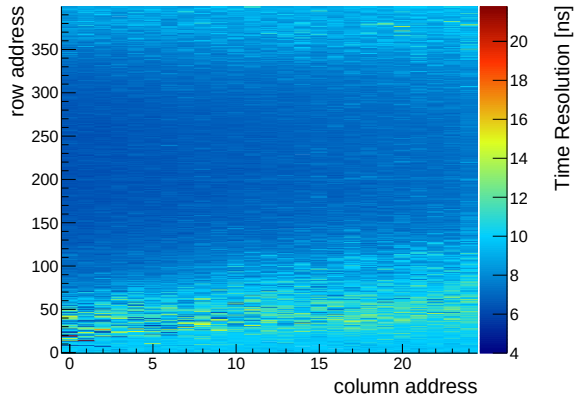
Using equation 10.8 to correct the mean time resolution of the single pixel distribution, gives rise of an intrinsic time resolution of about $3.708 \pm 0.423\,\text{ns}$. The corresponding error is calculated by error propagation and using the RMS value as error. This displays that the technology is in principle capable of fulfilling the requirements of ATLAS (see section 3.1.1).



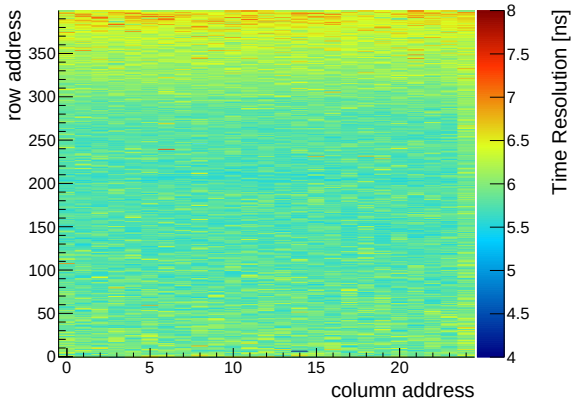
(a) Single pixel time resolution distribution before TWC



(b) Single pixel time resolution distribution after TWC



(c) Time resolution pixel map before TWC



(d) Time resolution pixel map after TWC

Figure 10.26: Single pixel time resolution study on sensor 1-21.

11 Commissioning of ATLASPix_IsoSimple

ATLASPix_IsoSimple is investigated for the first time within the scope of this thesis, which is why no efficiency information from testbeams is available at the time of writing. As explained in section 7.1, the only difference to the ATLASPix_Simple is the comparator, which is implemented in CMOS design instead of NMOS. In this thesis, only one sample is investigated with a resistivity of 200 Ω cm. The used DAC settings are adapted from the ATLASPix_Simple and adjusted in terms of noise response. Higher noise rates are observed at the default setting, which can be compensated by a higher value of *VPPix*. In addition, a higher DAC value for *BLResPix* is used to decrease noise signals. For the line driver an operation voltage for *VMinusPix* of 900 mV is supplied. Lower voltage levels result in higher activity regions in the pixel matrix, which could be caused by an increased cross talk influence (see example in Figure 11.1). However, this has to be studied, yet. All changes of parameter values for ATLASPix_IsoSimple with respect to the simple version are listed in Table 11.1.

Parameter	Simple	IsoSimple	unit
VPPix	20	30	dec
BLResPix	10	40	dec
VMinusPix	700	900	mV

Table 11.1: Change of operational parameters for the ATLASPix_IsoSimple.

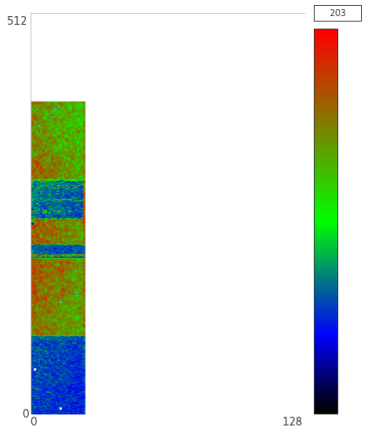


Figure 11.1: Example hit map provided by the DAQ for VMinusPix = 500 mV (pixel indicated in white are masked).

11.1 Analog Performance Study

In the following sections, the performance of ATLASPix_IsoSimple is studied similar to ATLASPix_Simple. As for the ATLASPix_Simple analog measurements, the values are plotted as difference to a default value, which are listed in Table 11.1. Due to the minimal change in design, only the dependence on the CSA, the comparator and the subsequent driver is investigated. The former is studied, by measuring the impact of the DAC parameter *VPPix*. All analog measurements are done with the pixel 0/1 (column/row) and a threshold value of 100 mV above the baseline.

Parameter	Mean Value	Unit
Amplitude	300.293	mV
Low Level	650.916	mV
Rise	1.386	$\mathrm{mV\,ns^{-1}}$
Fall	0.105	$\mathrm{mV\,ns^{-1}}$

(a) Mean AmpOut pulse shape parameter values

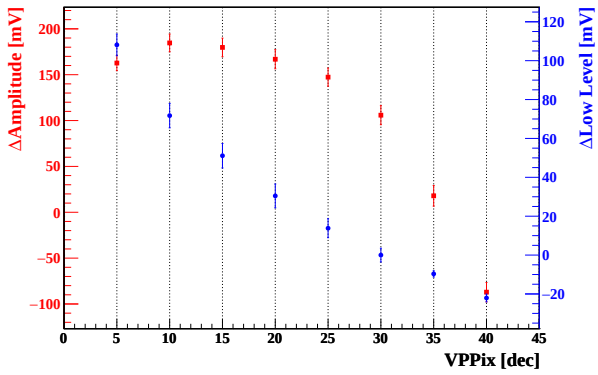
Parameter	Mean Value	Unit
ToT	1582.219 ± 13.279	ns
Delay	58.093 ± 0.384	ns
Rise	33.391 ± 0.021	$\mathrm{mV\,ns^{-1}}$
Fall	2.374 ± 0.001	$\mathrm{mV\,ns^{-1}}$

(b) Averaged Hitbus parameter values

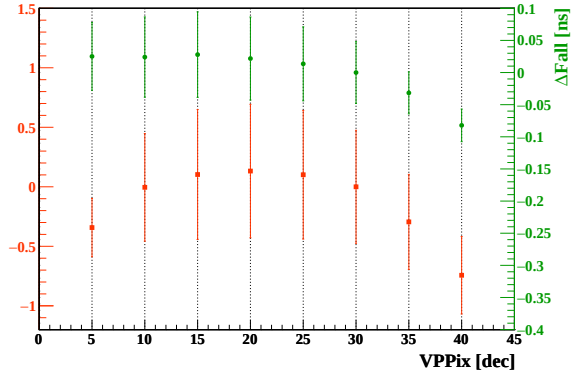
Table 11.2: Reference parameter values for AmpOut and Hitbus measurements at the default DAC settings adjusted according to Table 11.1

11.1.1 The Amplifier: VPPix

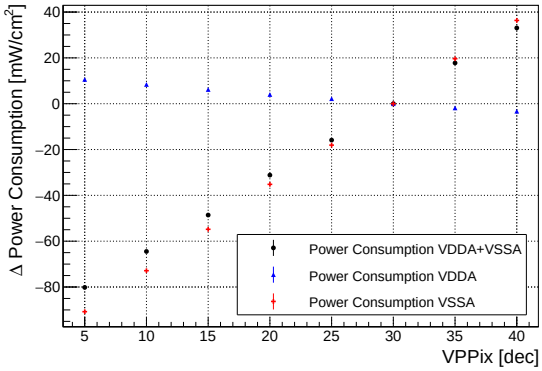
As mentioned before, a high current supply stabilizes the CSA and reduces the amount of noise. The operation range increases towards lower threshold levels, which is desired in terms of better time resolution. According to Figure 11.2 the amplitude peaks around a *VPPix* value of 10 and decreases for lower and higher values. A DAC value higher than 30 should not be used, due the steep decrease of the amplitude afterwards. The fall is constant, staying within the uncertainties up to a *VPPix* value of 30 and then decreases slightly. In general, the measured fall values seem to be too small. In the light of the other results, this measurement appears to be affected by a systematic error, which cannot be determined at the time of writing. The rise has a stable operation range between 10 and 30. For lower an higher values of *VPPix*, it decreases steeply. The power consumption is dominated by the power domain of VSSA, increasing linearly with higher DAC values. On the other hand, the power consumption for VDDA slightly decreases linearly with higher *VPPix* values. For subsequent measurements a *VPPix* value of 30 is chosen, due to the lower noise. If a higher amplitude is required in terms of efficiency, lower DAC values down to 10 are recommended.



(a) ΔAmplitude and ΔLow level versus VPPix



(b) ΔRise and ΔFall versus VPPix



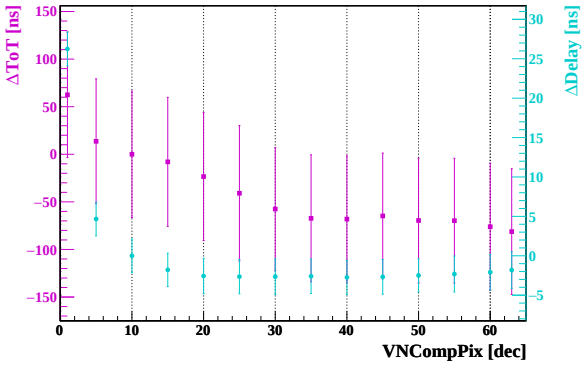
(c) ΔPower consumption versus VPPix

Figure 11.2: AmpOut pulse shape parameter and power consumption dependence on VPPix

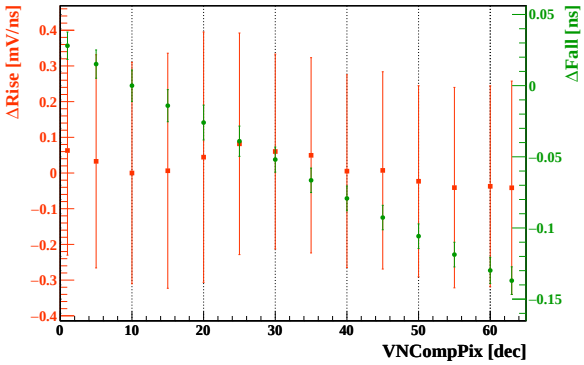
11.1.2 The Comparator: VNCompPix

The CMOS-based comparator, controlled by *VNCompPix*, is the only difference to ATLASPix_Simple. Figure 11.3 shows the measurement results of the *VNCompPix* scan. Operation is possible for the entire DAC range between 1 and 63. For smaller DAC values than 10, an increase in the delay is observed, for which no change in the rise is observed. The rise stays within the uncertainties over the entire DAC range, whereas the fall decreases linearly with higher *VNCompPix* values. Consequently, the measurement of the ToT is influenced by the change of the falling edge's steepness.
The total power consumption is dominated by the power domain of VDDA, increasing linearly with higher DAC values. Since no saturation of the current is observed, the transistors regulating the current flow in the comparator stay in the linear regime. At the same time the power consumption for the VSSA domain is stable over the entire DAC range. For the chosen *VMinusPix* voltage level the power dissipation along the signal lines is only marginally influenced by *VNCompPix*. The power consumption decreases slightly with higher DAC values. The steps in the measured power consumption are a result of the precision of the measuring device.
Based on the lower delay a *VNCompPix* value of 20 is recommended, since higher values

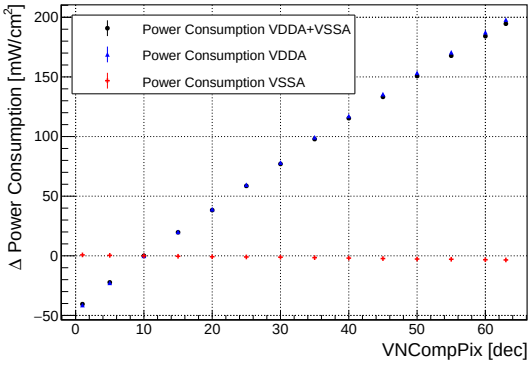
increase the power consumption significantly.



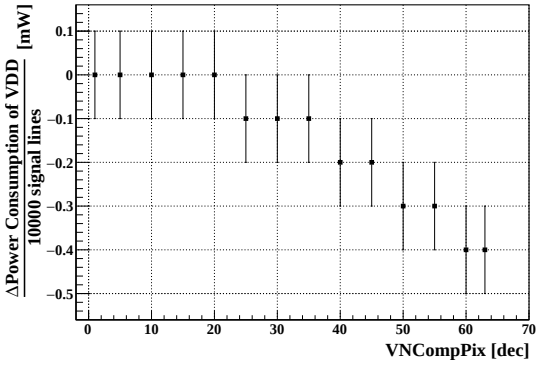
(a) ΔToT and ΔDelay versus VNCompPix



(b) ΔRise and ΔFall versus VNCompPix



(c) ΔPower consumption versus VNCompPix

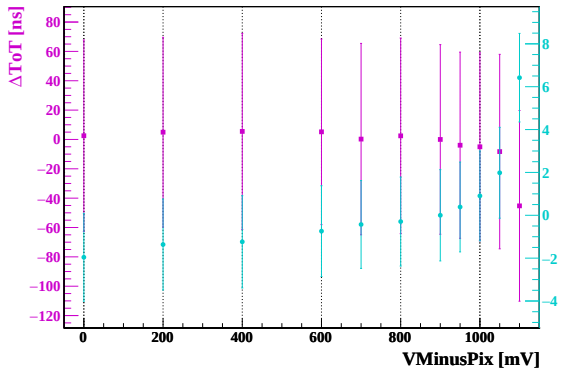


(d) ΔPower consumption of VDD versus VNCompPix

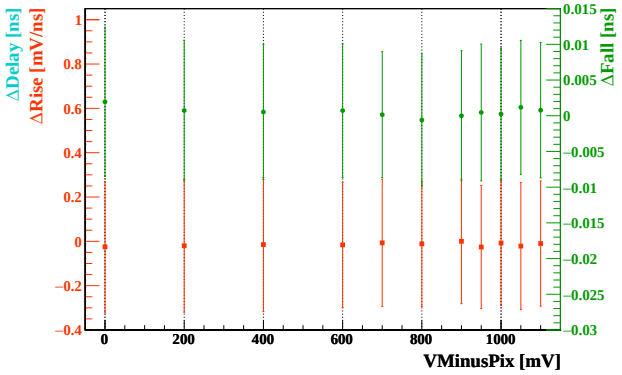
Figure 11.3: Hitbus measurement parameter dependence on VNCompPix.

11.1.3 The Driver: VMinusPix

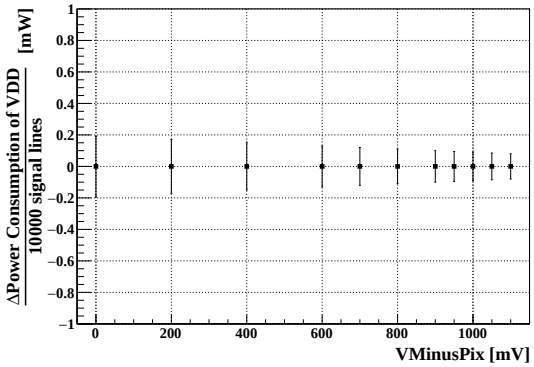
For ATLASPix_IsoSimple, the line driver is sensitive for a comparator output swing between *VMinusPix* voltage levels of 0 mV and 1100 mV, see Figure 11.4. The lower level is not limited as for the ATLASPix_Simple, represented in a stable power consumption for VDD down to 0 mV. Since the saturation domain of the transistor is not reached and no increase in noise is observed, in principle the entire voltage range can be used for operation. Albeit, an operation at low values is not recommended, because the receiver in the periphery cell is not designed for such high line signal amplitudes.
The measurement results on the Hitbus pulse shape parameters show no influence on the slew rates, which stay within the uncertainties over the entire voltage range. The ToT increases slightly with lower voltage levels of *VMinusPix*, while staying within the uncertainties, too. For the delay a small increase is observed with higher *VMinusPix* voltage levels. Therefore, an operation below 1000 mV is recommended.



(a) ΔToT and ΔDelay versus VMinusPix



(b) ΔRise and ΔFall versus VMinusPix

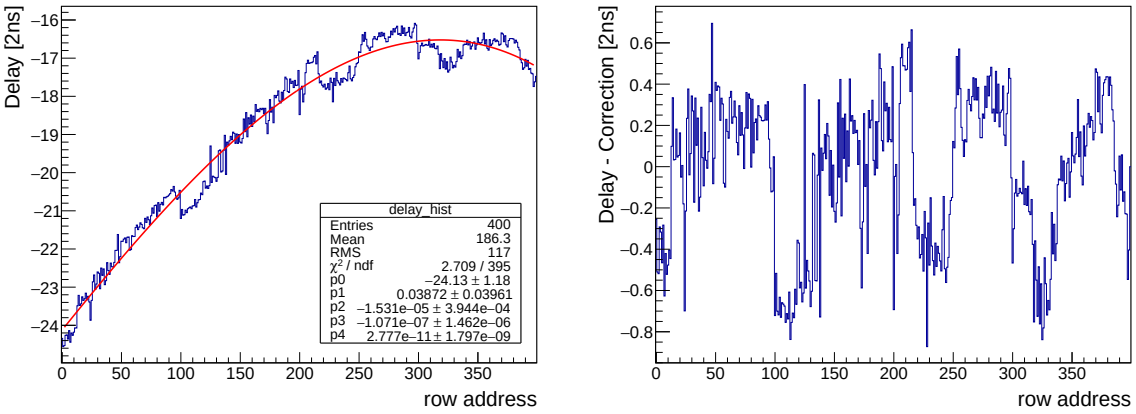


(c) ΔPower consumption of VDD versus VMinusPix

Figure 11.4: Hitbus measurement parameter dependence on VMinusPix.

11.2 Time Resolution of ATLASPix_IsoSimple

For the time resolution study of the ATLASPix_IsoSimple, the same correction steps are performed as for ATLASPix_Simple. The main difference between both sensor types is observed in the internal sensor delay (see Figure 11.5). The gradient along the row address is significantly smaller compared to the simple version. This could be caused by the CMOS comparator being able to switch faster, consequently reducing the delay. After the delay correction the deviation is less than a bin size of 2 ns. For the subsequent measurements, a high voltage of −60 V and a threshold level of 65 mV above the baseline is chosen.



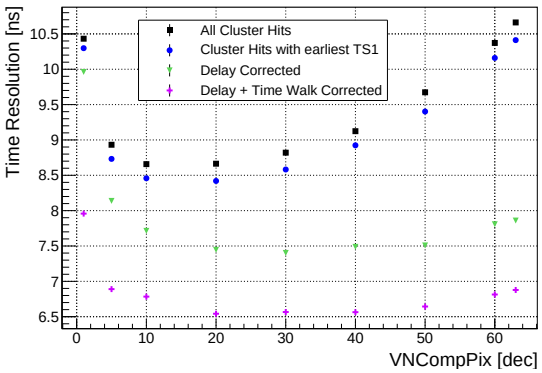
(a) Delay along the row address

(b) Corrected delay along the row address

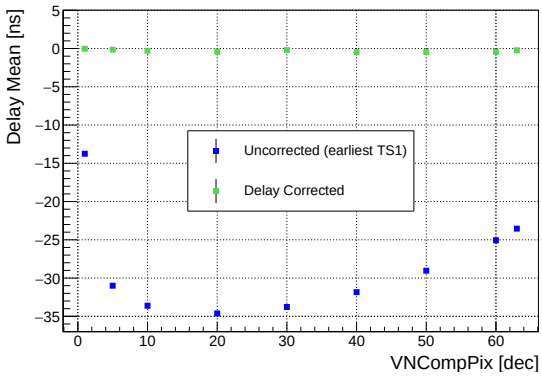
Figure 11.5: Delay correction for the ATLASPix_IsoSimple

VNCompPix

The time resolution as well as the delay mean improve up to a *VNCompPix* value of 20 (see Figure 11.6). For higher DAC values, the time resolution before corrections deteriorates, due to the increase of the delay mean. The delay and time walk corrected time resolution is stable at 6.5 ns up to a DAC value of 50. In comparison to ATLASPix_Simple a significantly better time resolution can be achieved, caused by the faster CMOS comparator and the consequently lower delay.
A *VNCompPix* value of 20 is recommended, providing a good trade-off between power consumption and time resolution. If the efficiency shows to be equal, a CMOS comparator design should be implemented in future generation, which provides a better uncorrected time resolution with respect to the ATLASPix_Simple.



(a) Time resolution versus VNCompPix

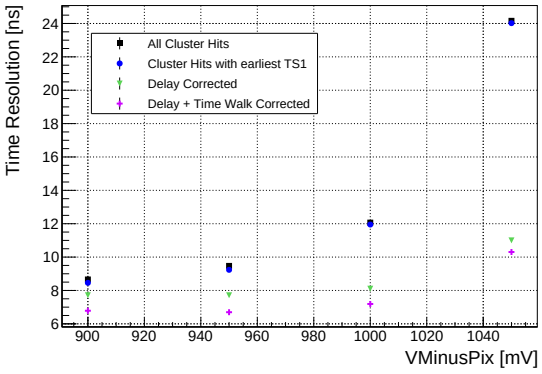


(b) Delay mean versus VNCompPix

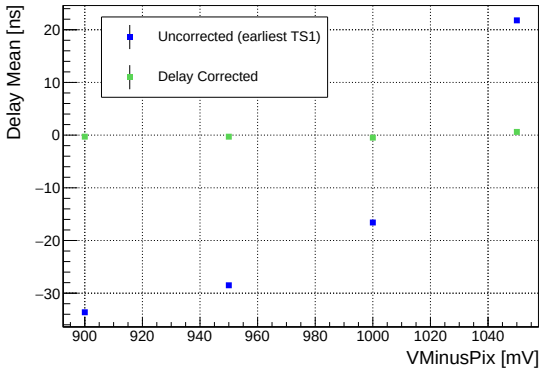
Figure 11.6: Time resolution study on VNCompPix.

VMinusPix

The influence of the line driver, which can be adjusted via *VMinusPix*, on the time resolution and delay mean is similar compared to ATLASPix_Simple (see Figure 11.7 and 10.4). The time resolution before corrections improves with lower voltage levels of *VMinusPix*, caused by a decrease of the delay mean. After delay correction, the time resolution is stable for *VMinusPix* smaller 1000 mV.
Since, higher activity regions (see section 11) in the pixel matrix are observed for lower voltage levels than 900 mV, this value is recommended for operation. If an improvement with more suitable settings for the receiver is found, perhaps even lower voltage levels can be considered.



(a) Time resolution versus VMinusPix

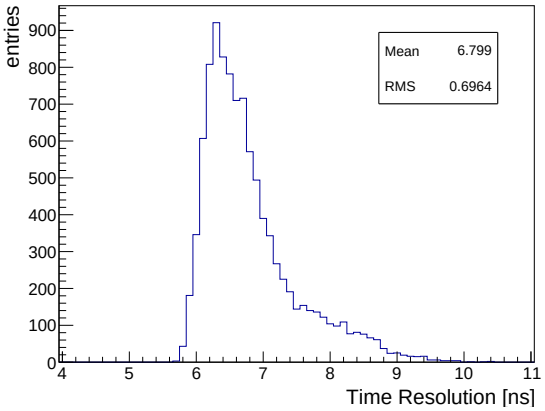


(b) Delay mean versus VMinusPix

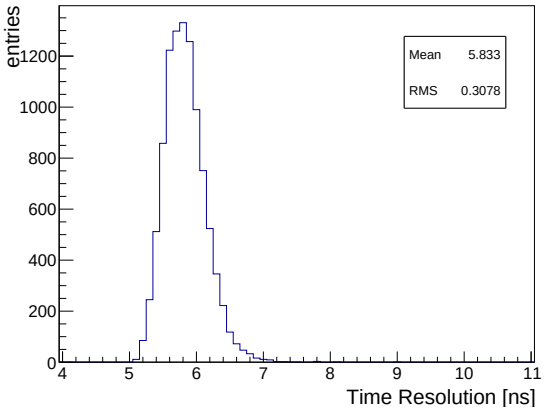
Figure 11.7: Time resolution study on VMinusPix.

Single Pixel Time Resolution

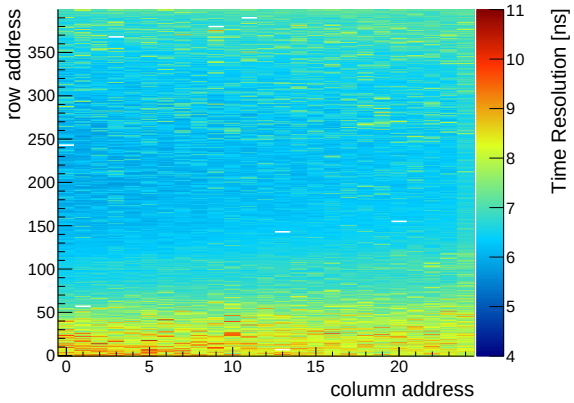
For this measurement the high voltage is increased to $-75\,\mathrm{V}$, which represents the upper limit for this sensor before reaching the breakdown domain. In addition, a *VNCompPix* value of 20 is chosen, according to the improved time resolution shown in section 11.2. Figure 11.8 displays the measurement result for the single pixel time resolution before and after time walk correction. Before time walk correction the mean time resolution is $(6.799 \pm 0.6964\,\mathrm{ns})$. The tail to higher time resolution is an effect of increased time walk, which is observed for pixels with a row address smaller 50. After time walk correction the time resolution map shows no regional dependence anymore and only pixel-to-pixel fluctuation can be observed. The time resolution improves to $(5.833 \pm 0.3078\,\mathrm{ns})$, which is similar to the single pixel time resolution after TWC of ATLASPix_Simple, see section 10.8. Albeit, the time resolution before TWC is significantly better. This is an effect of CMOS comparator, which switches faster and has a larger output amplitude. This enables a better signal transmission to the periphery cell, as its less prone to voltage level variations across the sensor.
The intrinsic time resolution, calculated according to equation 10.8, is about $(3.562 \pm 0.504\,\mathrm{ns})$. For future prototypes the time resolution can be improved by a faster signal transmission to the periphery cell, which decreases the internal delay and a higher bias voltage to decrease time walk. If the time stamp is sampled more precisely, this technology displays a promising future for particle tracking detectors.



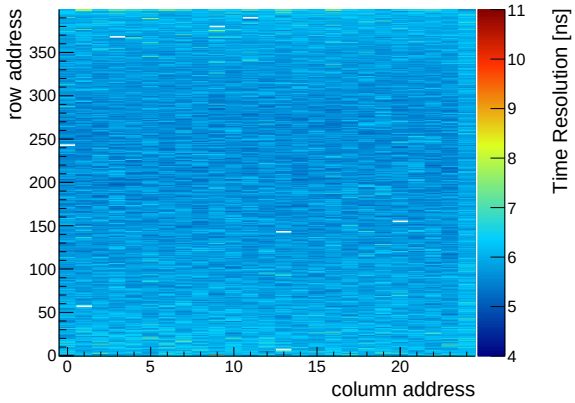
(a) Single pixel time resolution distribution before TWC



(b) Single pixel time resolution distribution after TWC



(c) Time resolution map before TWC



(d) Time resolution map after TWC

Figure 11.8: Single pixel time resolution study on sensor 1-54.

Part IV

Discussion

12 Summary and Discussion

Within the scope of this thesis, ATLASPix_Simple and ATLASPix_IsoSimple sensors are characterized using radioactive sources and charge injection as signal sources. The difference between both sensors is the in-pixel comparator. ATLASPix_Simple has a pure NMOS comparator design, whereas ATLASPix_IsoSimple features a CMOS comparator. To isolate the PMOS transistors of the CMOS comparator, an additional deep p-well is embedded within the deep n-well of the pixel.
The performance of the individual chip components is studied as function of the bias settings, which are adjustable via DACs. For this purpose, the pulse shape parameters of two available test outputs, called AmpOut and Hitbus, are investigated. The AmpOut is utilized to observe the performance of the amplification circuitry, whereas the Hitbus is the signal output after the comparator. In addition, the impact on the power consumption of each DAC is monitored. At the default settings (see Table A.1), the power consumption of ATLASPix_Simple amounts to approximately 166 mW.
The impact of the DAC settings on the pulse shape parameters is put into context with the time resolution of both sensors. The initial time resolution for optimized settings for ATLASPix_Simple is measured to be (11.78 ± 0.01) ns, whereas for ATLASPix_IsoSimple a time resolution of (8.66 ± 0.01) ns is measured. This is related to the faster CMOS comparator, which presents a significantly lower internal delay. To improve the initial time resolution several correction steps are implemented in the offline analysis. The first correction step is a cluster analysis, which is used to obtain its earliest time stamp of each hit cluster. With this correction the contribution of later hit time stamps associated to the same physical event are neglected. The corresponding time resolution improves slightly to (11.44 ± 0.01) ns for ATLASPix_Simple and (8.42 ± 0.01) ns for ATLASPix_IsoSimple. Two more effects deteriorating the time resolution are corrected for, the internal sensor delay and the time walk. The delay is an effect of varying signal line lengths and therefore shows a dependence on the row address. Furthermore, a dependence of the ToT on the row address is observed. Since no convincing evidence is found that the amplification differs from row address to row address, the ToT is corrected for the row address dependence. This in turn allows a more precise investigation of the time walk. After delay and time walk correction a time resolution of (7.25 ± 0.01) ns for ATLASPix_Simple and (6.54 ± 0.01) ns for ATLASPix_IsoSimple is achieved. Finally, the time resolution of single pixels is investigated. The mean of the corresponding single pixel time resolution distribution is taken as a measure for the time resolution achievable with the respective sensor technology. After time walk correction the results are (5.93 ± 0.27) ns for ATLASPix_Simple and (5.83 ± 0.31) ns for ATLASPix_IsoSimple. It has to be noted that the time resolution of the full sensor is limited by pixel-to-pixel variations. The threshold for each pixel can differ and an individual tuning was not performed. The main limitation of the time resolution is the precision of the time stamp sampling, which is 16 ns for both sensor types.

After subtracting the binning contribution of $16\,\mathrm{ns}/\sqrt{12}$, the intrinsic time resolution of both sensors is below 4 ns. This presents that this technology can fulfill the ATLAS requirements. Since ATLAS requires a good time resolution before offline corrections, the faster CMOS comparator is preferred over the NMOS design and should be pursued with the next prototypes.
Measurements at ambient temperatures below 20 °C displayed an increase of the noise rate at the default settings, which can be suppressed by higher current supplies for the CSA. At lower temperatures than 10 °C, the signal amplitude decreases and the steepness of the slew rates increases, which can be related to a shift of the transistor working points with the temperature. For each investigated temperature step the DAC related to the current supply of the CSA is adjusted for lower noise rate and the corresponding time resolution is observed to be stable. As a temperature dependence of the current reference circuitry is observed, a temperature stable design has to be implemented in the next prototypes.

12.1 Outlook

Since ATLASPix1 is a prototype, the insights from the measurement results can be used to improve the design of the next generations. The first step is a finer time stamp sampling, which gives rise to better time resolution, due to the lower binning contribution. Still some measurements remain for the complete characterization of ATLASPix1. The efficiency for the optimized setting of ATLASPix_Simple as well as the general efficiency of ATLASPix_IsoSimple have to be measured in a testbeam campaign. The influence of the ambient temperature on the amplification and noise rate has to be studied more intensively. The sources of the noise have to be identified. If they turn out to be common mode signals or an insufficient decoupling of the comparator transistors from the deep n-well, this can be corrected for in the design.
The next generation, ATLASPix3, is expected to operate at higher reverse bias voltages, which increases the width of the depletion zone and enhances the electric field. In this case, sensors with $80\,\Omega\,\mathrm{cm}$ substrate resistivity are considered to still be able to be thinned down to 50 µm without interfering with the depletion zone. Due to the higher electric field an even better time resolution can be expected.

Part V

Appendix

A Operation Settings

Dac name	DAC Value [dec]	DAC value [hex]
VNBiasPix	0	0x0
VPPix	20	0x14
VPPix2	0	0x0
VNFBPix	10	0xa
VPLoadPix	10	0xa
VNFollPix	10	0xa
VPFoll	20/0*	0x14/0x0*
BLResPix	10	0xa
VNCompPix	10	0xa
VNDACPix	0	0x0
VPBiasRec	30	0x1e
VNBiasRec	25	0x19
VNHB	63/0*	0x3f/0x0*
VPHB	63/0*	0x3f/0x0*
VNPEdge	10	0xa
VNVCO	13	0xd
VPVCO	12	0xc
VPPump	63	0x3f
Invert	0	0x0
VNDcl	40	0x28
VPDcl	10	0xa
VNDelDcl	40	0x28
VPDelDcl	40	0x28
VNDelDclMux	24	0x18
VPDelDclMux	24	0x18
VNLVDS	30	0x1e
VNLVDSDel	0	0x0
VNDelPreEmp	24	0x18
VPDelPreEmp	24	0x18
SelEx	0	0x0
SelSlow	0	0x0
EnablePll	1	0x1
Readout_reset_n	1	0x1
Serializer_reset_n	1	0x1
Aurora_reset_n	1	1
sendcounter	0	0x0
resetckdivend	15	0xf
maxcycend	63	0x3f
slowdownend	15	0xf
timerend	15	0xf
ckdivend	0	0x0
ckdivened2	7	0x7

Table A.1: Default DAC settings (* test output on/off).

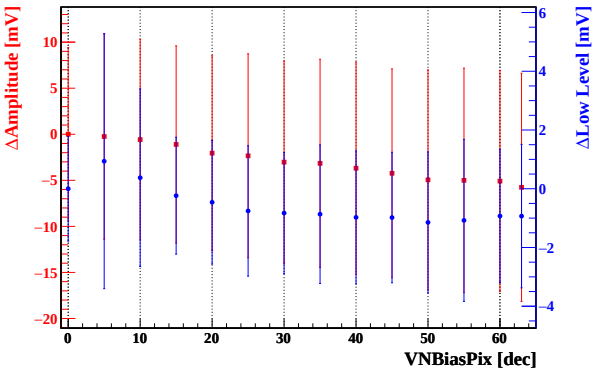
ID 1-11 (col./row)	ID 1-41 (col./row)	ID 1-21 (col./row)	ID 1-22 (col./row)	ID 1-38 (col./row)	ID 1-54 (col./row)
5/323	2/365	3/388	1/0	2/245	0/242
5/324	2/366	6/131	1/1	2/246	0/243
5/325	2/367	10/9	1/2	2/247	0/244
10/29	3/339	13/143	1/91	5/223	1/56
10/30	3/340	14/229	1/92	5/224	1/57
10/31	3/341	16/5	1/93	5/225	1/58
16/105	8/52	19/35	2/315	6/58	3/367
16/106	8/53	19/54	2/316	6/59	3/368
16/107	8/54	20/26	2/317	6/60	3/369
17/54	9/77	20/391	5/394	19/163	9/379
17/55	9/78	20/391	5/395	19/164	9/380
17/56	9/79		5/396	19/165	9/381
20/295	13/268		10/65		11/389
20/296	13/269		10/66		11/390
20/297	13/270		10/67		11/391
	19/385		17/10		13/6
	19/386		17/11		13/7
	19/387		17/12		13/8
			19/18		13/142
			19/19		13/143
			19/20		13/144
					20/154
					20/155
					20/156

Table A.2: Masked pixels for different sensors.

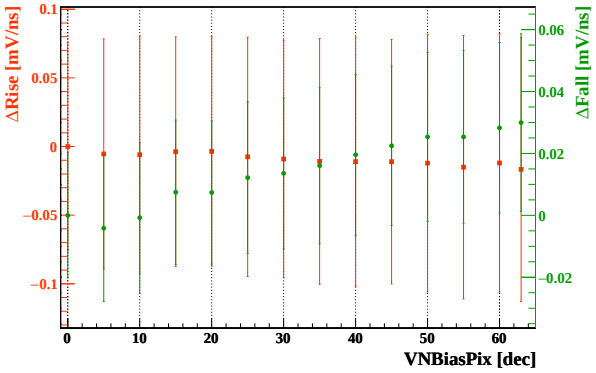
B Additional Measurements

Analog Measurements: VNBiasPix

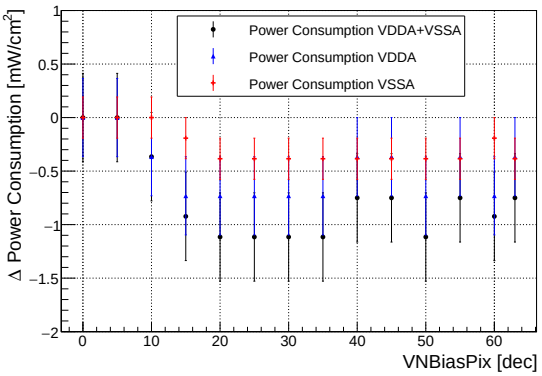
The DAC *VNBiasPix* has no significant impact on the pulse shape parameters and the power consumption according to Figure B.1. The amplitude decreases slightly, while the fall increases marginally with higher DAC values, but staying within the uncertainties. The rise and low level are stable over the entire operating range. All measurements are within the error range. In addition, an increase in noise was observed for larger *VNBiasPix* values than the default of 0.



(a) ΔAmplitude and ΔLow Level versus VNBiasPix



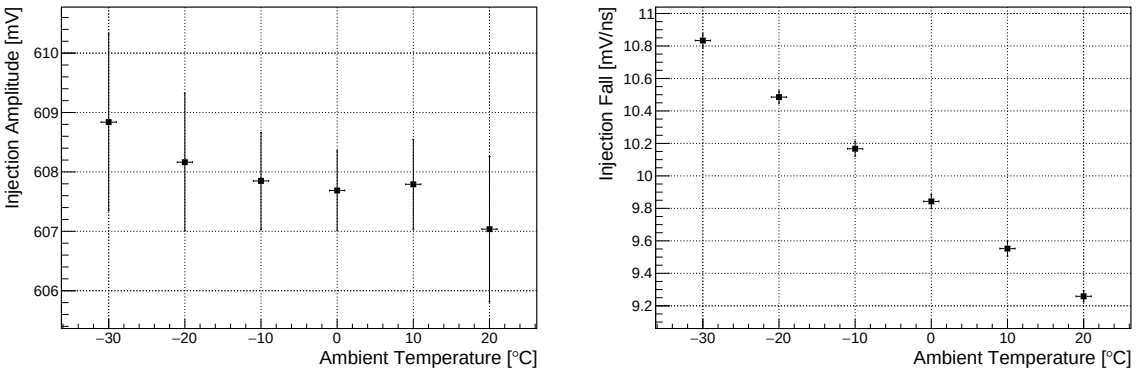
(b) ΔRise and ΔFall slew rates versus VNBiasPix



(c) ΔPower consumption versus VNBiasPix

Figure B.1: AmpOut pulse shape parameter and power consumption dependence on VNBiasPix with respect for the default value at VNBiasPix = 0

Temperature dependence on Injection

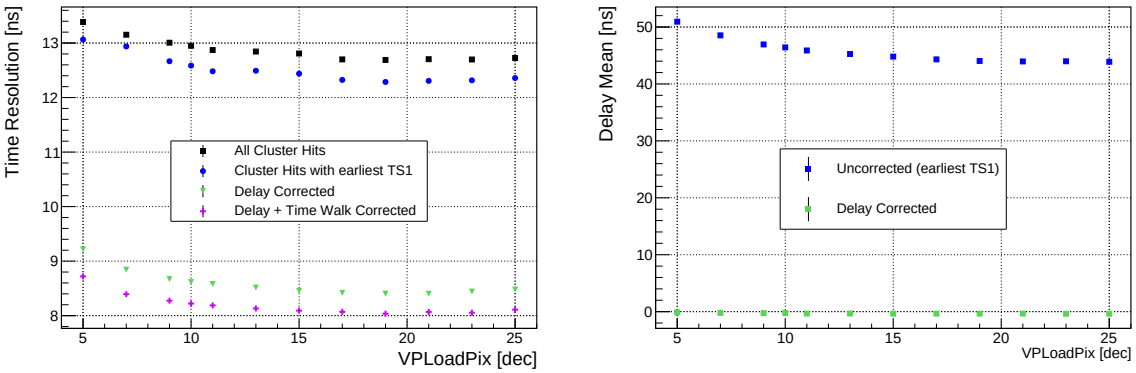


(a) Amplitude versus ambient temperature (b) Fall versus ambient temperature

Figure B.2: Injection parameter dependence on ambient temperature.

Time Resolution: VPLoadPix

All measured time resolutions improve up to *VPLoadPix* value of 10, subsequently saturating, see Figure B.3. A slight improvement still can be achieve for the delay and time walk corrected time resolution of about 8 ns, if an increase from the default DAC value of 10 to 15 is considered, albeit increasing the power consumption.

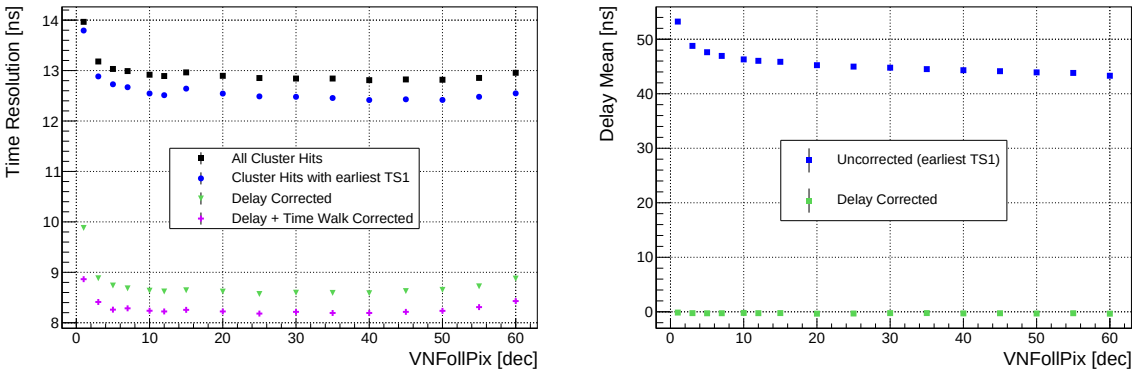


(a) Time resolution versus VPLoadPix. (b) Delay versus VPLoadPix.

Figure B.3: Time resolution study on VPLoadPix.

Time Resolution: VNFollPix

The uncorrected and corrected time resolution is stable for *VNFollPix* values larger 10, for smaller DAC values the amplifier pulse shape parameter decrease, causing the deterioration of the time resolution, see Figure B.4. The influence on the delay is according to time resolution and caused by the same effect. Together with the analog measurement results from section 9.7, a change from the default value of 10 is not recommended, since no significant improvement is observed and the power consumption increase linearly with higher *VNFollPix* values.



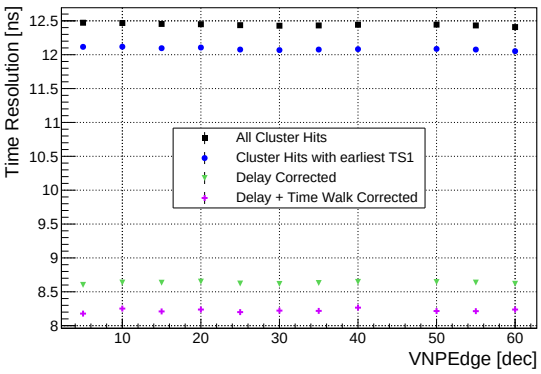
(a) Time resolution versus VNFollPix.

(b) Delay versus VNFollPix.

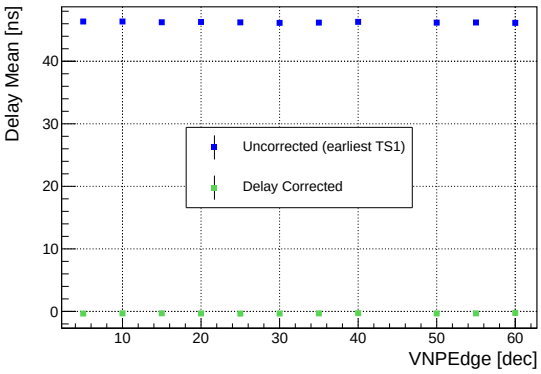
Figure B.4: Time resolution study on VNFollPix.

Time Resolution: VNPEdge

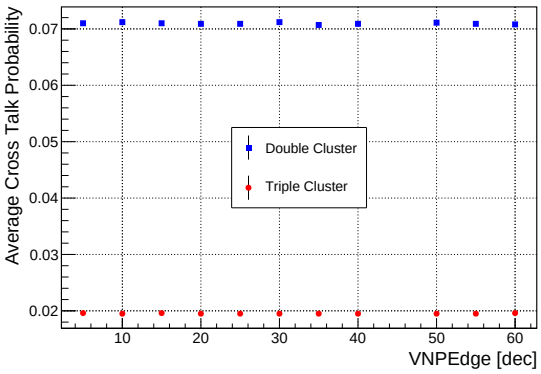
VNPEdge is the DAC to control the edge detector, which provides the last digitizing step in the readout chain. Since the Hitbus output is before the edge detector, no analog investigation could be done. In terms of time resolution, delay mean and cross talk no significant influence is observed. Since the ATLASPix1 is efficient for the default value of 10, a change of the DAC value is not recommended.



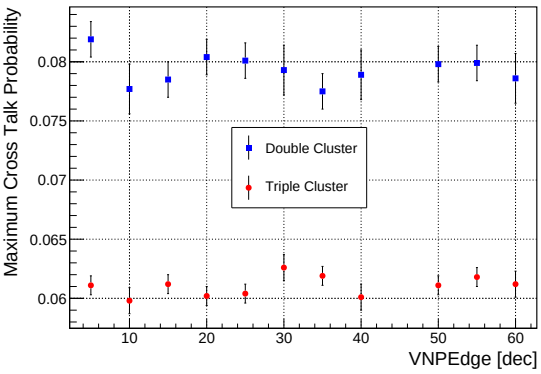
(a) Time resolution versus VNPEdge.



(b) Delay versus VNPEdge.



(c) Average cross talk probability versus VNPEdge.



(d) Maximum cross talk probability in a row versus VNPEdge.

Figure B.5: Time resolution study on VNPEdge.

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Acknowledgment

This master thesis is dedicated to all the people who have supported and encouraged me during the time of writing, especially my family. Without their support over all the years during my studies many things would not have been possible.

First and foremost, I would like to thank Prof. Schöning for giving my the opportunity to work on such an interesting and ground breaking topic with such capable and amazing people.

I like to thank Prof. Herrmann for being the second examiner of my master thesis.

This thesis would not have been possible in such a short time without the following persons: Heiko, Adrian, Sebastian, Lennart, Jan and Lars. The sharing of their expert knowledge and the stimulating and advancing discussion during the detailed proofreading make these results possible.

I would like to thank Lukas and Carlotta, with whom I share an apartment, for bearing me in this stressful time without complaining.

Last but not least, I would like to thank the staff in the workshop with whom I have worked. I would like to express my gratitude for the fact that they had to cope with some of the large workloads I caused with short completion times, which they have always mastered with great commitment.

Erklärung:

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 15.04.2019 .....