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A fast GEM HV analogue current readout system for the ALICE TPC upgrade at CERN LHC

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Abstract

Within this work, the system to control and monitor the GEM HV analogue current was developed for the ALICE TPC upgrade. The current on the GEM foils is proportional to the amount of back-drifting ions, which is relevant for the correction of the distorted electron drift paths. The software was designed as a Finite State Machine in order to control and monitor the execution flow of the system. Its network communication is enabled with an implemented Command Handler. The mean and RMS value of the current is being periodically published via DIM, in order to monitor the GEM currents. The used A-D Converters offers a resolution of better than 1 nA for sampling rates of up to 8 kHz. Performance studies together with noise measurements were conducted on two TPC-GEM sectors that are installed in the ALICE cavern. The system has shown excellent stability and reliability for the required continuous readout and monitoring of the space charge fluctuations on the GEM foils. Furthermore, it scales for the full system with 144 channels and will be deployed when constructing the upgrade TPC at CERN starting in 2019.

Zusammenfassung

Im Rahmen dieser Arbeit wurde das System für die Steuerung und Überwachung der GEM-hochspannungs-analogen Strommessung für das ALICE TPC Upgrade entwickelt. Der Strom an den GEM-Folien ist proportional zu der zurückdriftenden Ladung, die relevant für das Korrigieren der verzerrten Elekronendriftspuren ist. Die Software wurde als ein endlicher Zustandsautomat gestaltet, um die Ausführung des Systems zu überwachen und zu kontrollieren. Die entsprechende Netzwerk-Kommunikation findet mithilfe eines Command-Handlers statt. Um die GEM-Ströme nachzuverfolgen, wird deren Mittelwert und quadratisches Mittel periodisch über DIM publiziert. Bis zu einer Abtastrate von 8 kHz ermöglichen die gewählten A-D Wandler eine Auflösung von 1 nA. Sowohl Leistungstests als auch Rauschmessungen wurden an zwei TPC-GEM Sektoren, die in der ALICE-Kaverne installiert sind, durchgeführt. Das System funktioniert mit einem hohen Mass an Stabilität und Zuverlässigkeit für die geforderte kontinuierliche Aufgabe der Messung und Überwachung von Raumladungs-Fluktuationen an den GEM-Folien. Darüber hinaus ermöglicht es eine Skalierung auf das vollständige System mit 144 Messkanälen und es wird während der Konstruktion des TPC Upgrades am CERN in 2019 beginnend eingesetzt.

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1 Introduction

The ALICE (A Large Ion Collider Experiment) experiment is one of the four major experiments of the Large Hadron Collider (LHC) at CERN. Specifically, ALICE examines the Quark Gluon Plasma (QGP), a state of matter which is believed that existed just microseconds after the Big Bang. In this state the quarks and gluons are no longer confined. In particular, heavy-ion collisions at few TeV, which are generated from the LHC, allow the characterization of the QGP plus the investigation of the phase transition between the QGP and the hadronic matter. For tracking and identification of the particles that are produced after the QGP formation, ALICE is composed of several individual detectors. Specifically, it consists of a central barrel part, which measures hadrons, electrons, photons, and a forward muon spectrometer. The central part is embedded in a large solenoid magnet reused from the L3 experiment at the Large Electron-Positron Collider (LEP). From the inside out, the barrel contains an Inner Tracking System (ITS) of six planes of high-resolution silicon-technology based detectors, a cylindrical Time Projection Chamber (TPC), three

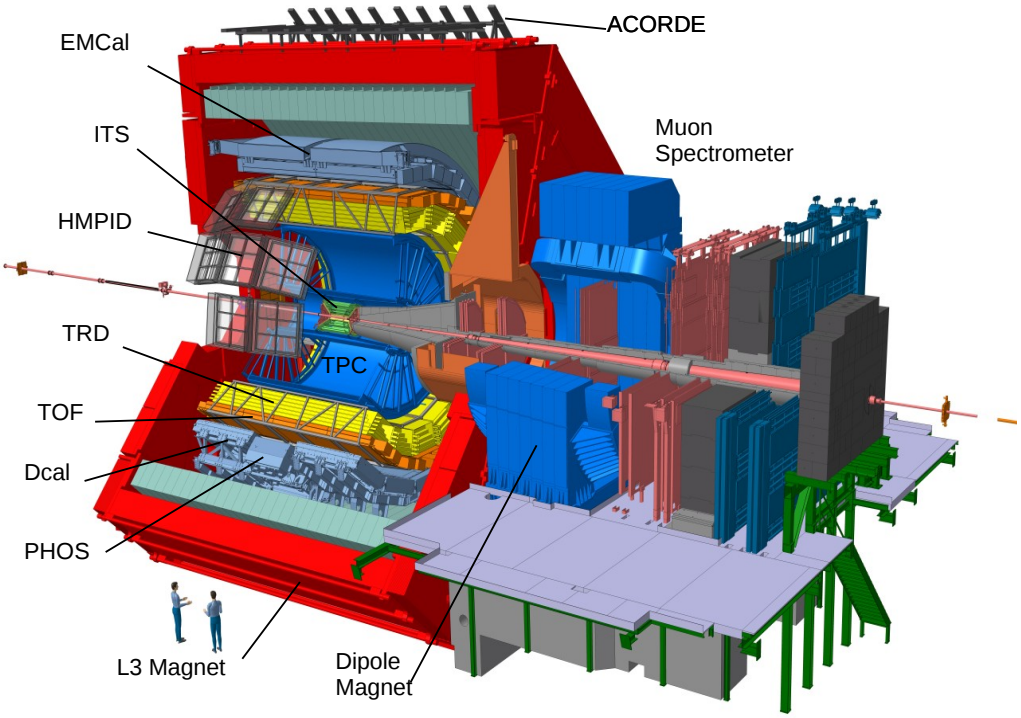

Figure 1.1: *Schematic view of the ALICE experiment at CERN and its main detectors [1].*

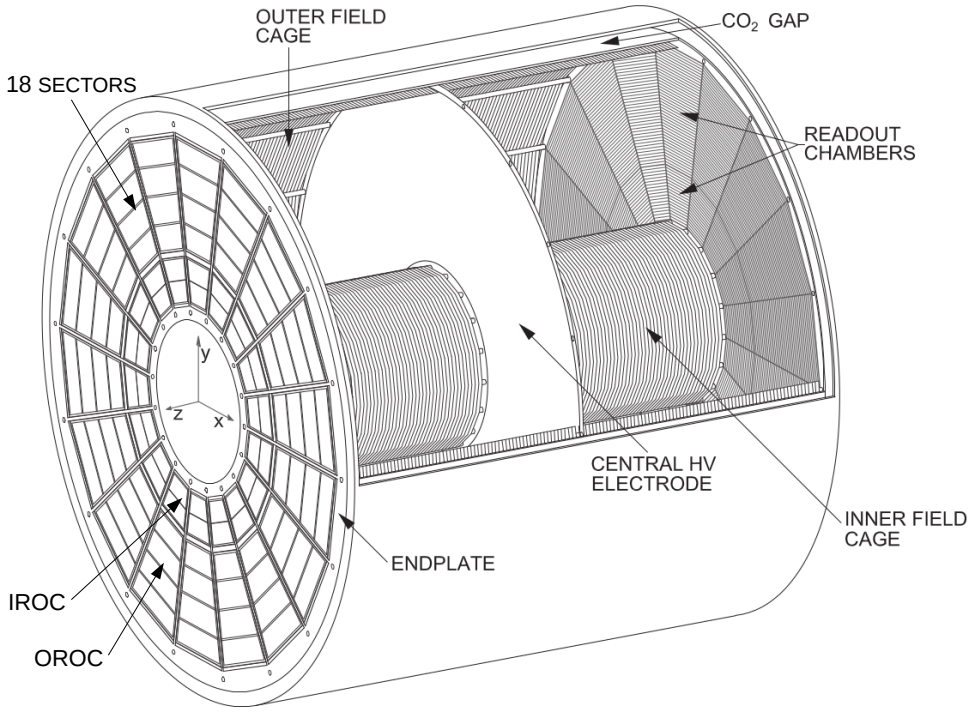

Figure 1.2: *Schematic view of the ALICE Time Projection Chamber [3].*

particle identification arrays of Time-Of-Flight (TOF), a High Momentum Particle Identification Detector (HMPID) and a Transition Radiation Detector (TRD), and three calorimeters the Photon Spectrometer (PHOS), the Electromagnetic Calorimeter (EMCal) and Di-jet Caloremeter (DCal). The forward muon arm consists of a complex arrangement of absorbers, a large dipole magnet, and several planes for tracking and triggering chambers. An array of scintillators (ACORDE) on top of the L3 magnet is used to trigger on cosmic rays. Figure 1.1 indicates the location of the various detector systems [2].

1.1 ALICE Time Projection Chamber

The main detector of ALICE for identification and tracking of particles is the TPC. Its volume, which is filled with a gas mixture (Ar-CO_2 in 2016 and Ne-CO_2-N_2 in 2017), is divided into two drift regions by a central electrode, as shown in Figure 1.2. Between the central cathode and the anode at the endplates, an electrical field of 400 V/cm is applied at each side. The electrons and ions, that are produced from the gas ionization of the actual particles, are drifting towards the endplates and the central electrode, respectively. The readout chambers are installed at the two endplates of the TPC and are divided into 18 sectors of trapezoidal shape. Because of the higher track density in the center, each sector is further segmented into the

Inner Read Out Chamber (IROC), with a higher pad-density, and the Outer Read Out Chamber (OROC).

Until now, the readout chambers consist of Multi-Wire Proportional Chambers (MWPC) with a gating grid operation. In brief, while the gating grid is open, the electrons can pass and get amplified by the strong electric field that is generated in the vicinity of the wires. Hence they produce a detectable signal on the readout-pads. The maximal drift time that the electrons need to reach the endplates is around 100 µs. However, for each electron that is produced during the amplification process, an additional ion is created. Because a part of these ion clouds is moving back, the electric field at the drift region can be locally affected. Thus, the electron trajectories are distorted throughout the entire drift and lead to deviations of up to 20 cm. In order to prevent ions from drifting back into the TPC drift volume, the gating grid is being closed for around 180 µs, i.e. the time until the ions are neutralized through the voltages that are applied on the wires. This gating operation leads to a total dead time of around 300 µs. As a result, the acquisition rate of the TPC readout system is limited to 3 kHz. The LHC upgrade in 2019/2020 will bring an increase of the Pb-Pb collision rate up to 50 kHz. This means that the TPC has to overcome the data rate limitation in order to profit of these much higher event rates. Using the MWPC without a gating grid would lead to massive drift-field distortions due to the ion back-flow, and would make precise track reconstruction impossible. To overcome this challenge, it was decided to replace the MWPCs with a Gas Electron Multiplier (GEM) system.

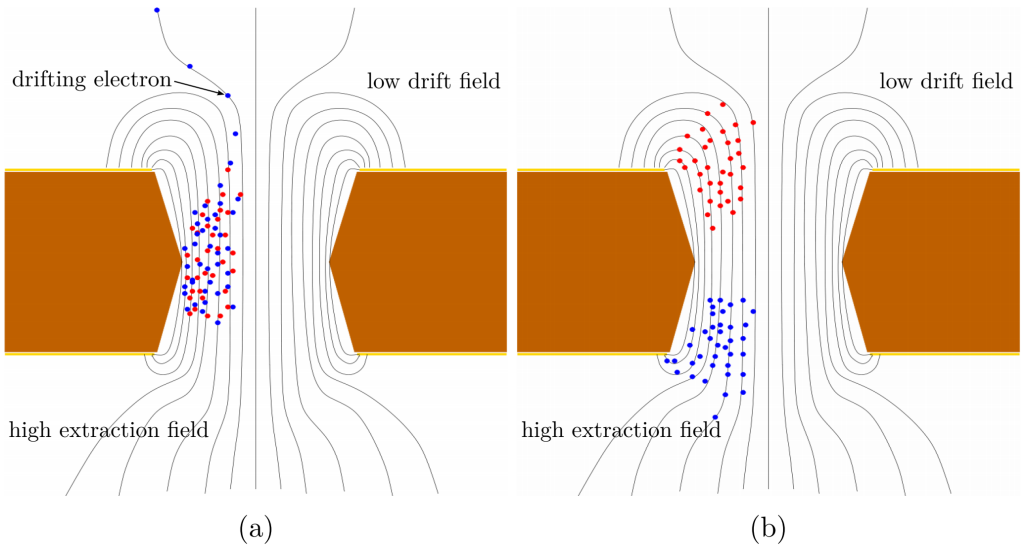

Figure 1.3: *Simulation of the Electric field at the GEM holes: (a) electrons (blue) are guided into the holes by the created field, where avalanches of electron-ion pairs are generated. (b) The asymmetric field configuration together with the small ion (red) mobility lead to efficient backflow suppression [4].*

1.2 Gas Electron Multipliers

The new readout system, which is currently in production, will use GEM foils for the electron amplification. Specifically, a GEM consist of a 50 μm thin insulating Polyimide foil covered by two 2–5 μm copper surfaces. The foils are etched, forming a dense hole-pattern. A potential difference between the copper sides leads to a strong electric field sufficient for avalanche creation, inside the holes. A certain amount of the created ions are following the field lines, due to their low mobility and thus are collected by the foil. Figure 1.3 shows the electric field at a GEM hole and the movement of the particles. The requirements in terms of sufficiently large gain and low ion backflow can be fulfilled by using a stack of foils with different amplification fields and hole-geometries. The upgraded ALICE TPC readout chamber will consist of 4 GEM foils combined in one stack. In addition, the OROC is further divided into OROC1, OROC2 and OROC3, due to GEM foil size limitations. The OROC stacks are shown in Figure 1.4. This stack configuration has shown to be ideal for the minimization of the field distortion in the drift-volume, as it leads to an effective gain of around 2000 and an ion backflow of 1%. This corresponds to 20 back-drifting ions for each electron that enters the amplification region. The electrons can flow continuously through the GEM foils for a continuous readout at the pad planes. However, this method produces a vast amount of data in time, which makes it impossible to store it for a later analysis. This necessitates online track reconstruction.

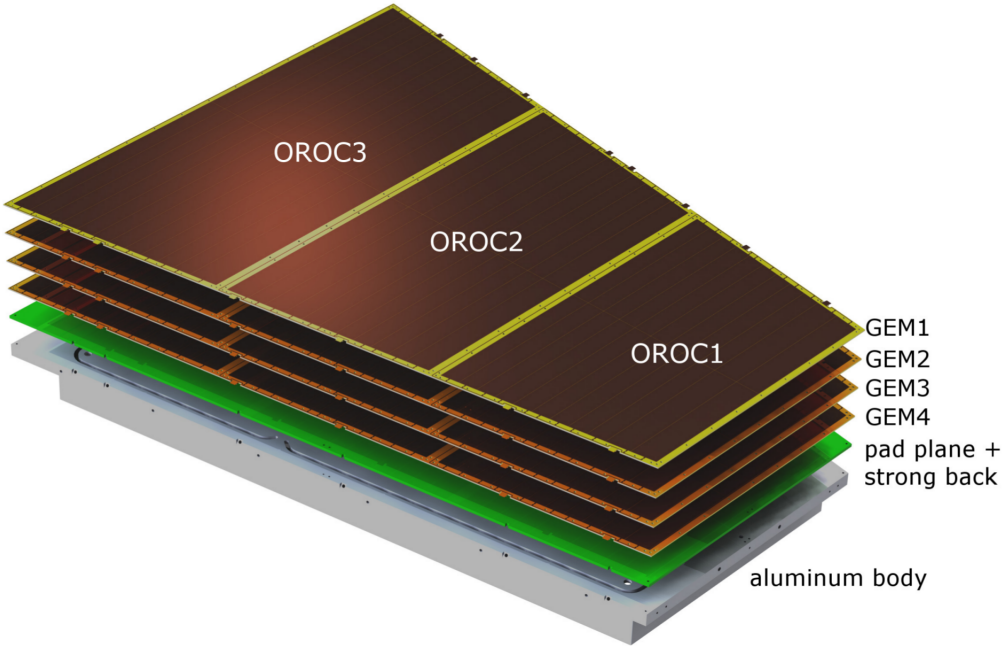

Figure 1.4: *Exploded view of the Outer Readout Chamber and its main components. The Inner Read Out Chamber consist, similarly of a single GEM stack [5].*

1.3 Readout Upgrade

The presence of space-charge distortions in the drift field due to backflow of ions from the amplification region poses a major challenge for the TPC reconstruction and calibration scheme. As mentioned before, due to the vast amount of data that comes from the continuous readout, the initial reconstruction steps, which contain finding and associating the clusters with tracks, need to be performed online. The idea is to base the space charge distortion correction on a scaled average space-charge density map, where the scale would be proportional to the ion density distributions in time and space [3]. In particular, by measuring the digital current after the amplification process with the plane pads, the ion backflow can be estimated. In this way, the space charge density map can be calibrated, which is relevant for the correction of the new measured incoming electron paths. Figure 1.5 indicates the pad plane below the GEM stack together with the ion backflow through the GEM foils. This method offers high granularity in space and time, but due to its complexity, e.g. in the data selection and compression process, it can lead to systematic errors or information loss.

Therefore a redundant and independent system was developed for the measurement of the ion backflow, which could contribute to the space-charge corrections. The special advantage of this method is that it determines the charge, which is locally produced by the gas amplification, by measuring the analogue current that passes through the GEM foils. This thesis is mainly dealing with the necessary software development for this alternative readout system and noise testing on the pre-production boards.

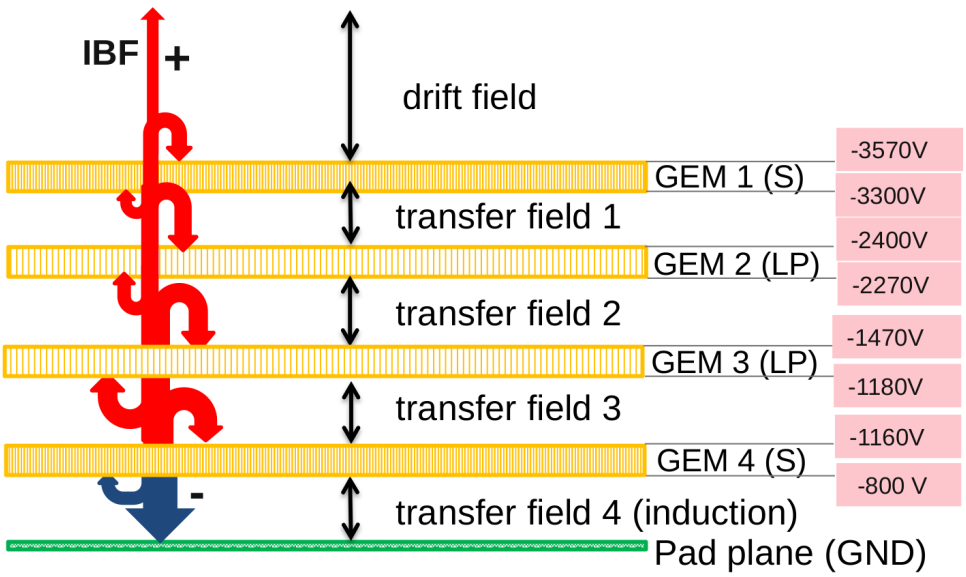

Figure 1.5: *Representation of ion backflow on the four GEM foils together with the applied voltages at each foil [6].*

In particular, each GEM foil is connected with two High-Voltage (HV) power lines (at GEM Top and GEM Bottom) as it is shown in Figure 1.5. This means that eight HV channels are supplying one stack. Additionally, because each sector consists of four stacks, the total number of HV supplies at each 18-sectors TPC-side is 576. Clearly, the largest space-charge can be found on the lowest GEM layer of the amplification process, namely the GEM 4. More specifically, as it can be seen in Figure 1.3(b), after the generation of avalanches of electron-ion pairs inside the GEM holes, most of the ions are follow the field lines towards the top GEM foil. On the other hand, only few electrons are collected on the bottom GEM foil, as they have a higher mobility compared to the ions. Therefore the current-meter system is set on the HV cable of the GEM 4 Top foil of each stack where the largest current occurs. In total

$$4\,(\text{Stacks}) \cdot 18\,(\text{Sectors}) \cdot 2\,(\text{sides}) = 144\,\text{channels}$$

are considered to be implemented in two crates at the Counting Room 4 (CR4), 80 m away from the ALICE apparatus.

The hardware which monitors the GEM current is also presented within this work. Moreover, this thesis follows with an extensive description of the software that was developed, in order to ensure the continuous readout and the control of the system via network. Therefore, the focus mainly lies on the design and deployment of the software, which is based on a Finite State Machine (FSM). Additionally, special importance is given to the format and features of the implemented commands. The various precision, functionality and stability tests which were carried out before deploying the software at CR4, are also presented.

2 Instrumentation

For the measurement of the current on the GEM 4 Top foil at each stack, a current-meter is set in series on the HV cable that supplies the foil. The system is free floating, i.e. it is not grounded, which leads to a relative potential of zero. The potential difference changes, only if current passes through the GEM foil. The system consists of a 10 kΩ resistor at the input, where the potential difference is being measured. Figure 2.1 shows the GEM current readout scheme. The voltage is digitized with an Analog-to-Digital Converter (ADC), which has an operating range of 0–100 µA and a signal resolution of 1 nA. The acquired data is sent through an insulator to a Field Programmable Gate Array (FPGA) for data collection and processing.

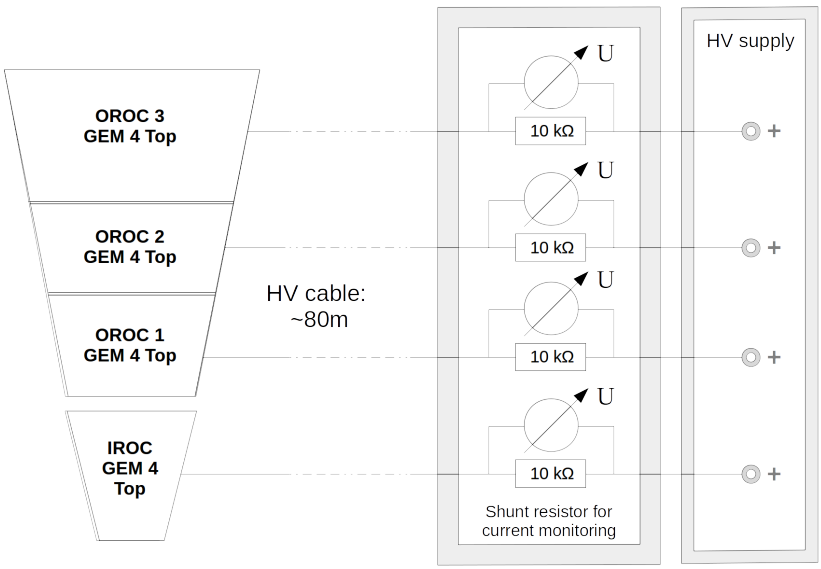

Figure 2.1: *GEM analogue current readout scheme.*

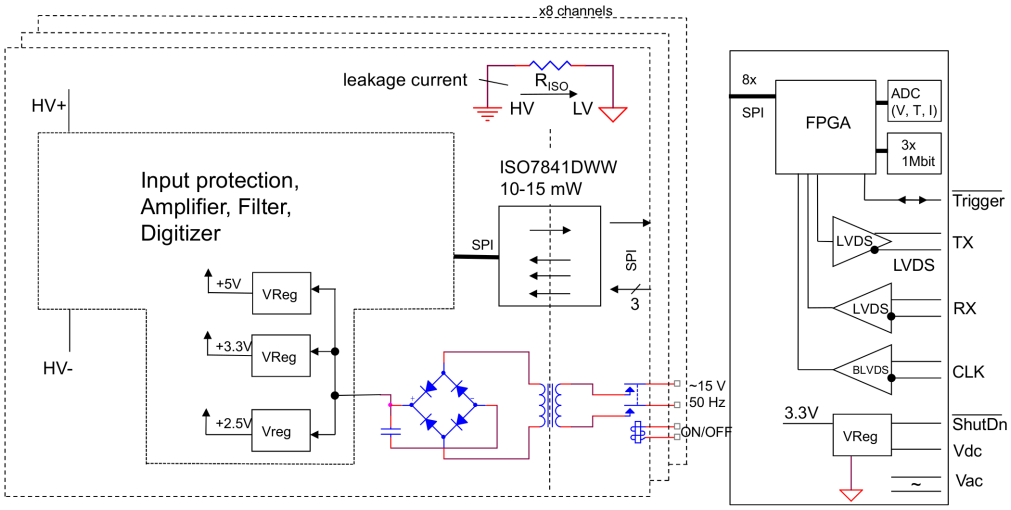

Figure 2.2: *Block diagram of the front-end board [7].*

2.1 Front-End Board

Figure 2.2 indicates the block diagram of the front-end readout board and Figure 2.3 shows a picture of the board, which was used at the Physikalisches Institut. The front-end board consists of eight channels, which are responsible for the GEM-current measurement at two TPC sectors. At the input, a feedback amplifier with gain 1, a so-called voltage follower, and a low pass analogue filter are used, in order to prevent the signal from being affected by the load and to attenuate the 30–40 kHz noise by the HV generator, respectively [7]. Afterwards, the voltage drop on a 10 kΩ input resistor is being digitized with the ADC, which can be converted into current by using Ohm's law:

$$I = \frac{V}{R}$$

As far as the power supply of the electronic components is concerned, three linear voltage regulator stages are implemented. A voltage regulator is an electronic device that receives a voltage signal and generates a more stable one, but with lower voltage magnitude. The discontinuous line, which is shown in Figure 2.3, indicates the separation of the High- and Low-Voltage regions. A transformer generating 15 V AC 50 Hz, is being used for the supply of the parts which lie in the HV region. Transformers are excellent insulators, but only operate with alternating current. Therefore, an additional diode-bridge rectifier is used in order to produce the same polarity for the supply of the circuit's components. Eight Transformers are implemented in total on every board, one for each channel. The digitized data that comes from the ADCs is sent to the FPGA through a digital insulator. The communication interface between the ADCs and the FPGA is realized by a Serial Peripheral Interface (SPI) bus, which is typically used for short distance communication in embedded systems. SPI is bi-directional, i.e. the communication can occur in both directions. On the other hand, the PC and the FPGA are communicating

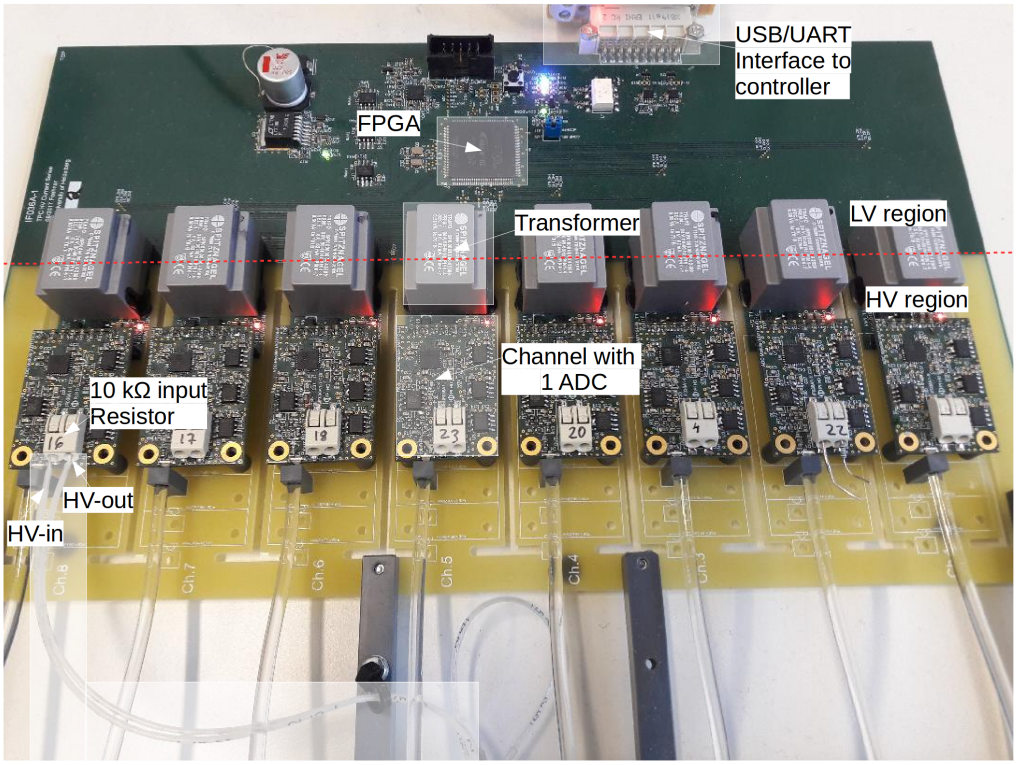

Figure 2.3: *Readout board at the Physikalisches Institut and its main components. Its dimensions are: 17x28* cm

with a USB cable through the backplane using a Universal Asynchronous Receiver-Transmitter (UART) protocol. The FPGA functionalities and tasks are described in section 2.3.

2.2 Analog-to-Digital Converter

ADCs are used for analogue data processing similar to this measurement, where a potential difference has to be determined. After sampling the signal with a reference clock, a digital number from 0 to $(2^N - 1)$ is assigned to each sampled voltage value, where N is the bit number of the ADC. In this way, the signal is converted from a continuous one to a discrete one. This process introduces the quantization error, which is defined as the difference between the sampled signal and its digital representation. The quantization error has a uniform distribution ranging from $-\mathrm{LSB}/2$ to $+\mathrm{LSB}/2$, where the Least-Significant-Bit (LSB) refers to the maximum quantization error. Thus, the RMS of the quantisation error can be derived as:

$$\mathrm{V_{qn}} = \sqrt{\frac{1}{\mathrm{LSB}} \int_{-\mathrm{LSB}/2}^{+\mathrm{LSB}/2} \mathrm{x^2 dx}} = \frac{\mathrm{LSB}}{\sqrt{12}}$$

In other words, quantization results in extra noise, the quantization noise, which is uniformly distributed with a standard deviation of LSB/$\sqrt{12}$ within the Nyquist band [8]. The Nyquist band is given for a sampling rate f_s, the frequency range from 0 to $f_s/2$, where $f_s/2$ is referred to as the Nyquist frequency f_N. A signal can only be sampled properly when it contains frequency components below the Nyquist frequency. The effects of improper sampling will be discussed in section 4.1.

In order to reduce the quantization noise in the frequency range of interest, a method called sigma-delta (Σ-Δ) modulation is being widely used in ADCs. Figure 2.4 is indicating the frequency spectrum for the filter operations during Σ-Δ modulation. In brief, the principle of the Σ-Δ modulation is based on the concepts of oversampling and noise shaping. First, the sampling rate is increased into a much higher sampling frequency, i.e. $K \cdot f_s$, where K is the oversampling ratio. In this way, the quantization noise remains LSB/$\sqrt{12}$, but the noise is now distributed over a wider bandwidth, in particular from 0 to $Kf_s/2$. The noise outside the frequency of interest can be removed by digital filtering operations, i.e. low pass filters which are described in section 4.1. In addition, the quantization errors are integrated by an Integrator (Sigma) and corrected by a Comparator (Delta) for many times using a Digital to Analog (DAC) feedback loop, which leads to a signal noise shaping. This means that the quantization noise is reduced in the area of interest and increased at higher frequencies [9].

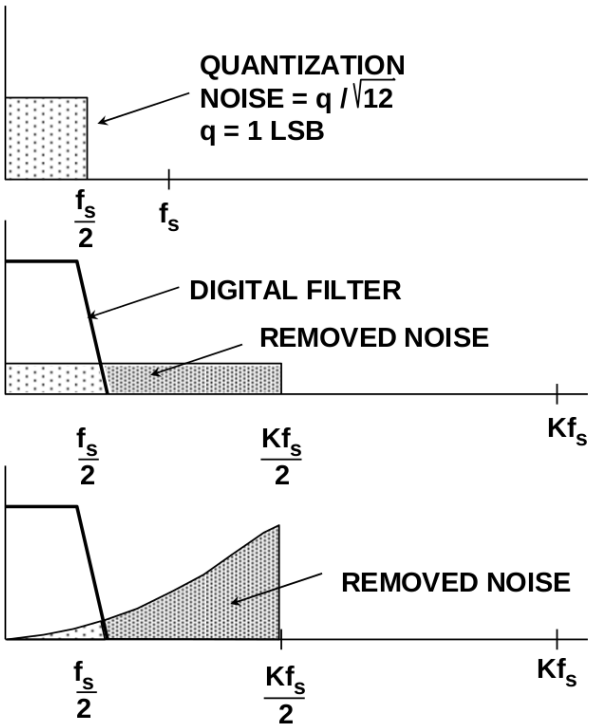

Figure 2.4: Σ-Δ *modulation for quantization noise reduction. Oversampling, digital filtering, and noise shaping are the main filter operations [9].*

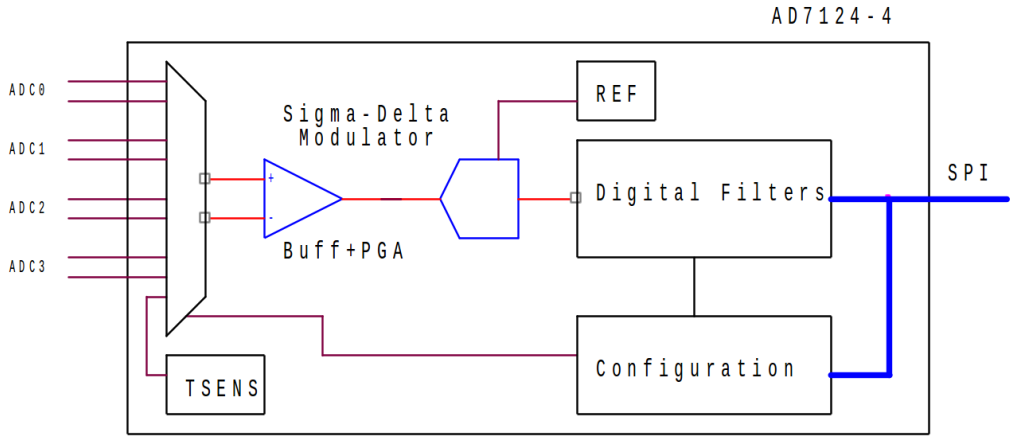

Figure 2.5: *Block diagram of the AD7124-4 [7].*

The selected ADC is the Analog Devices AD7124-4, which is a 24-bit Sigma-Delta ADC with a Programmable Gain Amplifier (PGA) and a reference voltage (V_{ref}) [10]. Its block diagram is shown in Figure 2.5. The PGA is amplifying the voltage difference at the input in order to increase the sensitivity of the ADC. Specifically, the multiplication-factor is set to 2, which is the same as to use a resistor of 20 kΩ instead of 10 kΩ. Furthermore, the V_{ref} of the AD7124 is 2.5 V. This means that the ADC converts the analogue input in correspondence to this isolated reference voltage, i.e. the output can vary from 0 to Vref. A 24-bit ADC can output 2^{24} possible digital values, which means that V_{ref} corresponds to 2^{24}. Moreover, the digital resolution, LSB, is equal to V_{ref} divided by the total number of possible outputs:

$$\mathrm{LSB} = \frac{2.5\,\mathrm{V}}{2^{24}} = 1.5 \times 10^{-7}\,\mathrm{V}$$

As only the current value is relevant for the ion backflow, the digital resolution can be calculated using the 10 kΩ resistor:

$$\mathrm{I_{Res}} = \frac{1.5 \times 10^{-7}\,\mathrm{V}}{10\,\mathrm{k\Omega}} = 15\,\mathrm{pA},$$

which is much more precise than the required precision of 1 nA.

2.3 Field Programmable Gate Array

In order to collect and to process the digital data of the eight ADCs, one FPGA is implemented on each board. FPGAs are integrated circuits which are re-programmable. This means, that in contrast to most application-specific integrated circuits, FPGAs doesn't have a fixed hardware structure and can be configured with new functionalities according to the experiment's needs. Moreover, a great advantage of FPGAs, over micro-controllers, is that they can process data at different input pins simultaneously. Like in this case, the FPGA processes the digital data from eight ADCs

at once. This FPGA has an internal flash memory, sufficient to store two design configurations. The first configuration is fixed and it is well working. The second one is for the development of the design and is updated frequently [7]. The FPGA design is shown in Figure 2.6. This diagram indicates the processing steps of the data. First of all, the ADC data passes through a filtering process. A three stage digital filter consists of three identical low-pass filters, which are set one after the other. The stage is configurable, which means that the number of filters can be selected during the configuration. A low-pass filter, as the name indicates, passes frequencies lower than a given cut-off frequency with little attenuation. For frequencies higher than this cut-off, the gain is proportional to 1/f, where f is the frequency. This frequency behavior is changing by chaining together two or more filters. An observation of the frequency behavior for different filter setting is presented in section 4.1. Furthermore, the readout rate can be configured through a decimation of the ADC sampling rate. The new readout rate is implemented by taking mean values and can obviously be only equal or lower than the ADC sampling rate. In order to observe simultaneously the GEM-current changes, it is preferred to output the mean:

$$\overline{x} = \frac{x_1 + x_2 + \cdots + x_n}{n}$$

and the RMS value:

$$x_{rms} = \sqrt{\frac{(x_1 - \overline{x})^2 + (x_2 - \overline{x})^2 + \cdots + (x_n - \overline{x})^2}{n}}$$

The RMS value gives precise information about the amplitude of an alternating signal. Therefore, in order to profit from the FPGA's programmable logic components potential, the relevant equations are implemented in it. The filtered ADC value is stored in the corresponding register and the RMS and mean value are continuously calculated. Instead of measuring the current at the ADC's input, it is also possible to measure the leakage current that passes from the LV to the HV side of the board, in order to test for instance if the insulation is still satisfactory. This can be done by directing the multiplexer (MUX) to the desired mode during the board's configuration.

An additional and important feature of the FPGA design is the ring buffers, which are used for the signal triggering. The system of this project is not using the triggering mode, but only focuses on the continuous real-time data acquisition. Therefore, the ring buffers will be discussed only briefly. At the top of the diagram, a large ring buffer can be seen, with a capacity of eight times 16 kilo-samples. The ADC data is passing continuously inside, rewriting the already written data after a constant time interval. At the point when the programmable threshold is reached, the last values around the trigger point are sent out. Moreover, a smaller buffer exists for continuously storing the mean and RMS data.

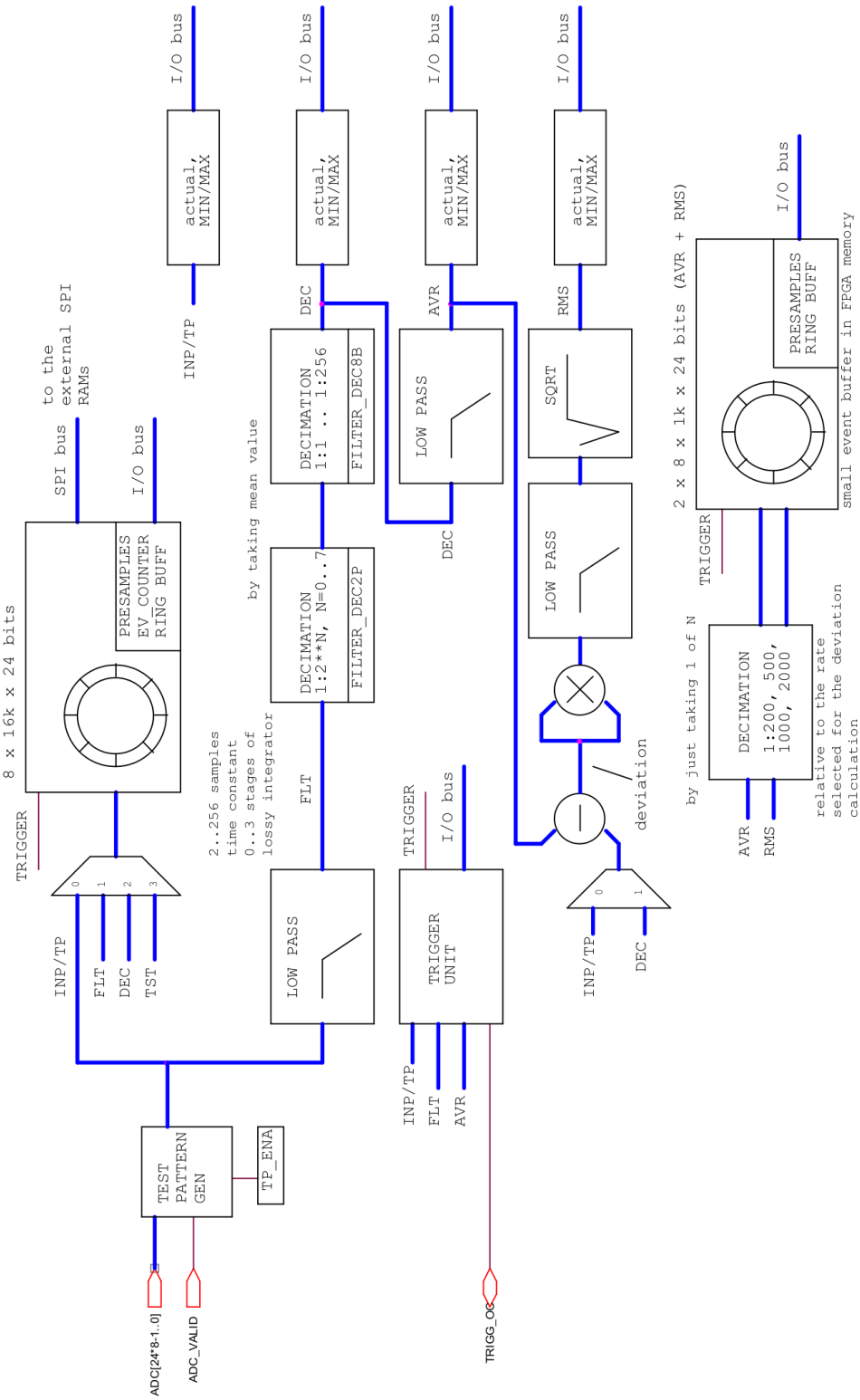

Figure 2.6: *Field Programmable Gate Array design [7].*

3 Control and Monitoring

For the initialization and the desired configuration of the board, a sequence of low-level functions has to be executed. For a continuous GEM current readout, a software code had to be developed that calls the corresponding functions. Moreover, a command handling tool had to be implemented for the control of the system, for instance, to modify the configuration during readout. The software is designed as an Finite State Machine which means, that it is structured into different states. This gives a clear view of the system current status and the possibility to progress from one state to the other only when fixed conditions are satisfied. Figure 3.1 indicates the GEM current system control and monitoring process. In order to control the meters and to monitor the GEM current from the Detector Control System (DCS), the Distribution Information Manager (DIM) is used to establish this communication. The GEM current is considered to be fed to the Data acquisition system for the online space charge distortion correction.

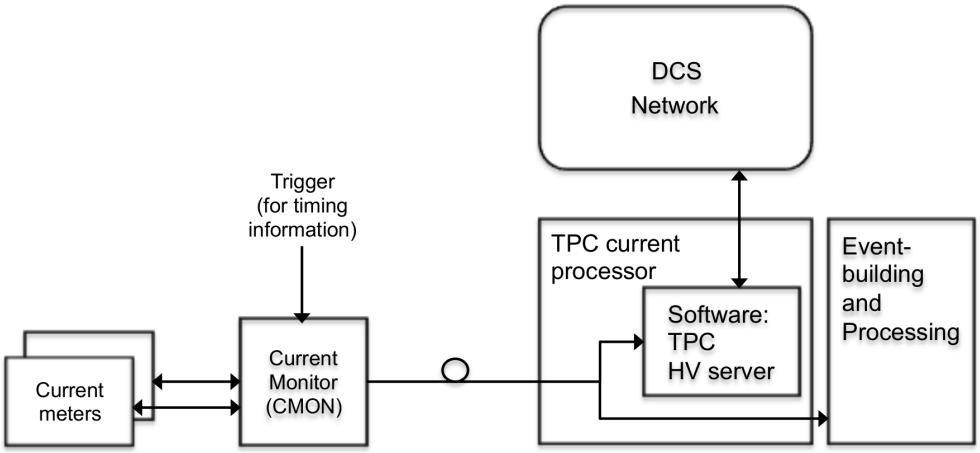

Figure 3.1: *Schematic showing the control and monitoring of the GEM current system [3].*

3.1 Distributed Information Management

DIM is a network communication tool which was developed at CERN in order to connect local devices to the supervisory layer [11]. The DIM system is based on a client/server paradigm, where at the beginning the server is registering its services, and the client is requesting for them. Services are all the parameters that need to be published, like measured values, or system status information. The services of

the relevant system are presented below:

Alive Evidence that the software is still running. In each reading period, this value is alternating between 0 and 1.

CurrentState Reflects the current FSM state of the system, which will be described in the next section. Its value can be from -1 to 3, i.e. State: *Error*, *Standby*, *Initialized*, *Ready*, *Mixed*.

UartMask Informs, through a hexadecimal number, which ADCs are configured and are operating.

Rms An eight-channel array which contains the continuously calculated RMS values of each channel.

AverageCurrent An eight-channel array which contains the continuously calculated average values of each channel.

LogService Indicates the latest software operation.

After a successful subscription, the server can send the data to the client at any time. Moreover, the DIM server can receive commands from the client, in order to make desired changes on the system. Therefore, the software is polling periodically, if any new command was received. Figure 3.2 shows the available services on the DIM client window.

3.2 Finite State Machine

An FSM is a software model that can be implemented with a software in order to control an execution flow. This model consists of a finite number of states and ensures that only one state can be active at the same time. Therefore, in order to perform the system's actions, the FSM has to change from one state to the other, which is called a transition. A transition can be accomplished in response to a corresponding client input or can happen automatically by the fulfillment of fixed conditions. A diagram of the relevant FSM states is shown in Figure 3.3. The different states are presented below:

Standby

This state is set as default when starting the program. Both the DIM server and its services are defined and the DIM commands can be executed. The commands and the associated arguments, which are used for the state transitions, are described in the next section.

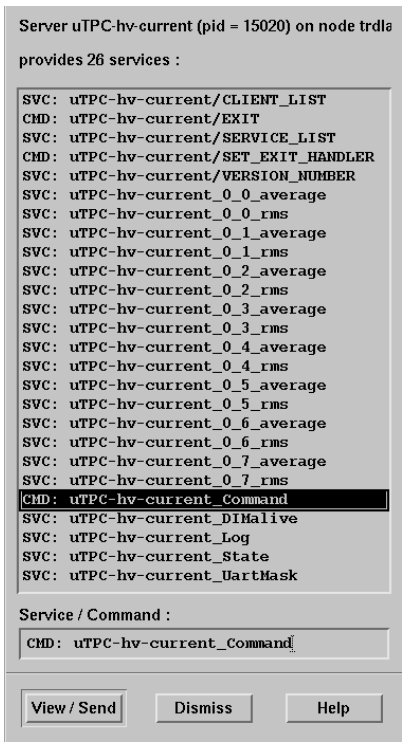

Figure 3.2: *DIM client window with the available DIM services. The command service enables the control of the board via network.*

Initialized

In the *Initialized* state, the UART communication is established. Furthermore, the FPGA design is loaded from the flash memory and its CPU is reset. The device is initialized and can from now on be configured as desired.

Ready

By moving into the *Ready* state, the system starts reading the RMS and average current values at a pre-set frequency. The digital output data is converted into units of nA and is published through DIM. Here it has to be noted that two separate frequencies are configurable. The first one is the sampling rate of the ADCs and the second one is the publishing rate via DIM. After each readout, the configuration of the FPGA is verified, i.e. the current configuration parameters are compared with those which were stored in the configuration process at the beginning. If any change occurs, the system moves to the *Error* state.

Error

The first case for a transition to the *Error* state is when the configuration has been modified by external parameters, for instance a single event upset, i.e. when an ionizing radiation flips a configuration register bit. However, the possibility that

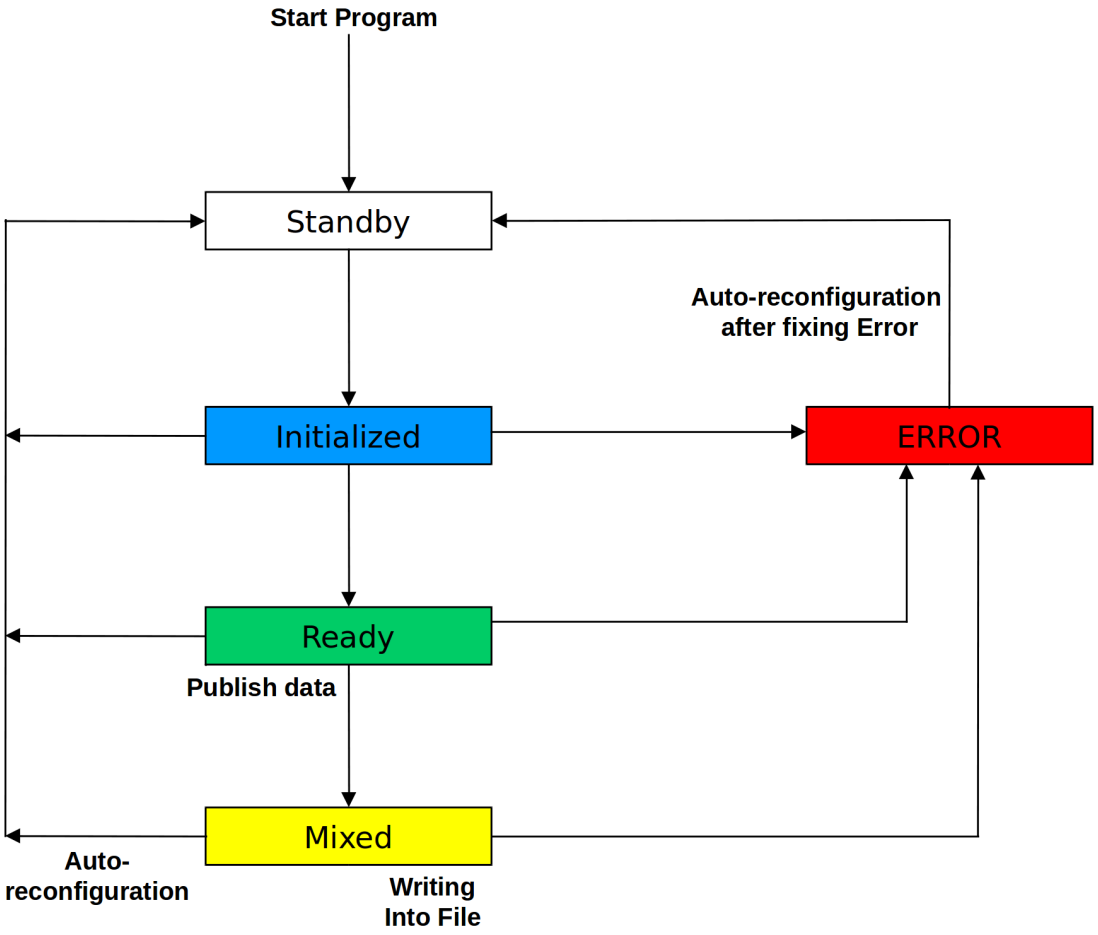

Figure 3.3: *Finite State Machine of the GEM-current readout system software.*

this can happen is very low, because the front-end board is placed 80 m away from the detector. Secondly, a shorter or longer system's power-off moves the system into the *Error* state. This is examined permanently in every state by checking the device validity. Lastly, by receiving a wrong byte from the ADC, i.e. not a typical value. The readout stops and the reconfiguration process is started. For all three cases, the system tries to return to the same state as before by executing the commands automatically using the buffered configuration parameters.

Mixed

The system has another readout mode, where the RMS and the average current publishing pauses, while the contiguous ADC values are read out and stored in a file for debugging purposes. Once this is done, the system automatically goes through the individual states using the configuration settings which were given at the beginning, until it reaches the *Ready* state and continues publishing the RMS and mean data.

3.3 Command Handler

A command handling tool was implemented in order to call the device's low-level functions and generally to control the system through DIM. Emphasis was placed on constructing only few compact commands, in order to decrease the complexity of the system. The system is able to recognize only a standard form of user commands. In the case of a misspelling or a wrong number of arguments, the command is being rejected providing feedback to the user for the correct use of the command. In addition to that, each argument input must be in the range of the accepted values and must have the correct type, e.g. integer or string. Any different type than expected is captured and the whole command is rejected. The reason behind this is that a continuous readout is required and any misusing of the low-level functions would lead to a wrong configuration or even worse to a program crash. The explicit form of the commands together with the state from where they can be called are listed in Table 3.1. They are presented below in the same order. If a command requires several arguments, then the arguments are hyphenated with a colon (:). Also, a sequence of commands can be executed at once, by appending several commands separated by a comma (,).

setVerbosity

The verbosity level, which must be an integer, represents how much amount of a software operation will be shown on the terminal and stored in log files. In order to adjust the information that is posted, each output-message of the software is categorized into three levels: DEBUG (Verbosity>2), INFO (Verbosity>1) and ERROR (Verbosity>0). By setting the verbosity level using this command, only the messages of interest can be seen. The default value is 2, in order to log only

Command	Arguments (in)	Example	Permitted
setVerbosity	verbosity level (int)	setVerbosity:3	all states
goStandby	none	goStandby	all states
goInitialized	none	goInitialized	Standby
goReady	multiplexer (int), sampling rate (Hz)	GoReady:1:1000	Initialized
setRead Frequency	frequency (Hz)	SetReadFrequency:8	all states
writing	ADC mask (hex), sampling rate (Hz), number of samples (int)	writing:0xFF:8000:10000	Ready

Table 3.1: *Structure of existing operational commands.*

the important messages. However, the system is running as daemon, which is a state that blocks any terminal output. For this reason, syslog, which is a standard for message logging, is used and implemented in this program. Depending on the verbosity level, the information or error messages are stored in log files and can be analyzed at a later time. Besides that, every software operation is published via DIM (LogService), in order to monitor the system from the DCS. This command can be executed from all FSM states.

goStandby

The system can be reset by sending this command. This brings the system to its initial status. In this state, no readout exist and only the transition to the *Initialized* state can occur.

goInitialized

This command starts the UART communication. Afterwards, the FPGA design is loaded from the internal flash memory and its CPU is reset. After these operations are successfully completed, the FSM moves from the *Standby* to the *Initialized* state and the device is ready to be configured.

goReady

The goReady command has two arguments and is mainly relevant for the configuration of the device. The first argument is directing the multiplexer, which was mentioned in section 2.3. For measuring the leakage current that passes through the board, the MUX parameter must be set to 2. On the other hand, in order to digi-

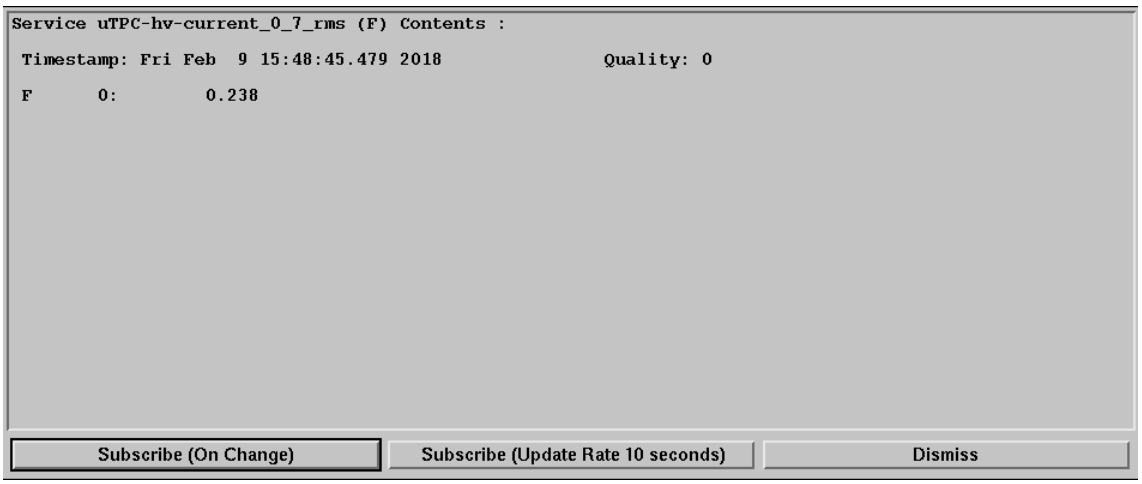

Figure 3.4: *Example of the DIM client display showing the RMS value in nA units.*

tize the voltage drop at the input resistor, which is relevant for the GEM-current, it should be set to 1.

The second command argument is the sampling rate of the ADC, which must also be an integer value. The maximum sampling rate is 16 kHz. Other possible sampling rates are 8, 4, 2, 1 kHz and any 16000/N, where N is an integer from 1 to 2047. As described before, the space-charge in the drift region of the TPC is fluctuating. These space-charge fluctuations require an update of the distortions maps in time intervals of 5–10 ms. This means that the current will be monitored with an ADC sampling rate at around 1 kHz.

In addition to that, the ADC can perform a self-calibration. The sampling rate is automatically reduced to its minimum (8 Hz) and the inputs are disconnected internally from the pins and connected to proper voltages in order to make the offset and gain correction. The sampling rate reduction occurs in order to have higher precision in the calibration [7].

Lastly, the configuration of the FPGA digital filters is performed. This is described in more detail in section 4.1 where noise measurements will be performed with different filter settings. After the execution of the low-level functions, the ADC and the FPGA are configured and the state changes to *Ready*. From then on, the ADC is digitizing with the given sampling rate and the FPGA is permanently calculating the RMS and the average current. These values are permanently published via DIM for monitoring the GEM current. An example of a DIM client display (did) for the RMS value in units of nA on the seventh channel of the board is shown in Figure 3.4.

setReadFrequncy

Its argument relates to the frequency with which the RMS and average value will be published via DIM. However, because DIM is a network communication tool, the publishing rate is limited. Presently, the default value of the publishing rate

is set to 8 Hz, but it can be adjusted if necessary. For this reason, an additional project, which is in progress, considers to feed these values directly to the ALICE Data acquisition system (DAQ) through optical fibres at a rate of 1 kHz for higher precision corrections [12]. Nevertheless, the communication with DIM is considered to be used in order to control and monitor the system. Indeed, it has already offered great benefits in diagnosing and monitoring of two TPC-GEM sectors installed in the ALICE cavern.

writing

In order to store a set of contiguous values for offline analysis, the writing command has to be called. In the case of using all eight ADCs, the maximum sampling rate is 2 kHz. Therefore, for measurements with higher sampling rates, the ADCs must be operated separately, for instance, two ADCs at a time. This is not the case for the continuous readout, as described above, where only 1 kHz is required.

Therefore, the first argument of the writing command is the 8-bit mask which defines which ADCs will be configured. This has to be given in hex form. By setting for example 0x80, only the last ADC will operate because in binary form it equals to b1000-0000. The maximum number of simultaneously operating ADCs for different sampling rates are eight ADCs at 2 kHz, four ADCs at 4 kHz, two ADCs at 8 kHz and only one ADC at 16 kHz. This is caused by the limited bandwidth of the presently used USB/UART interface in the controller card. This controller card is presently upgraded with an e-link interface which directly feeds into the GBTx chip [13] of the ALICE DAQ [12]. A single channel on the GBTx chip has a bandwidth of 80 Mbytes/s. This is more than sufficient for the current-monitoring system which will deliver 144 x 1 kHz x 4 Bytes = 0.576 Mbytes/s.

The second argument in the command is the sampling rate, represented again as an integer number. The last argument corresponds to the desired number of samples. The file is named after the date-time when the measurement took place. This command can be called only from the *Ready* state. The RMS and average value readout stops and the FSM moves to the *Mixed* state. After writing all the samples into the file, the system is being automatically reconfigured with the parameters which were initially given. This means, that the system moves to the *Ready* state and starts again the continuous readout as before.

GEM readout system at CERN

Figure 3.5 indicates the presently GEM readout system at CR4 at CERN. In particular, one crate can host eight readout boards with 8 channels each. Currently one board is set, in order to measure the GEM current through the HV cable of the two TPC sectors at ALICE. The microcontoller on the left of the picture enables the communication with the board through the backplane. The readout of the microcontroller from the PC take place with a USB interface, from where later the data is being published via network.

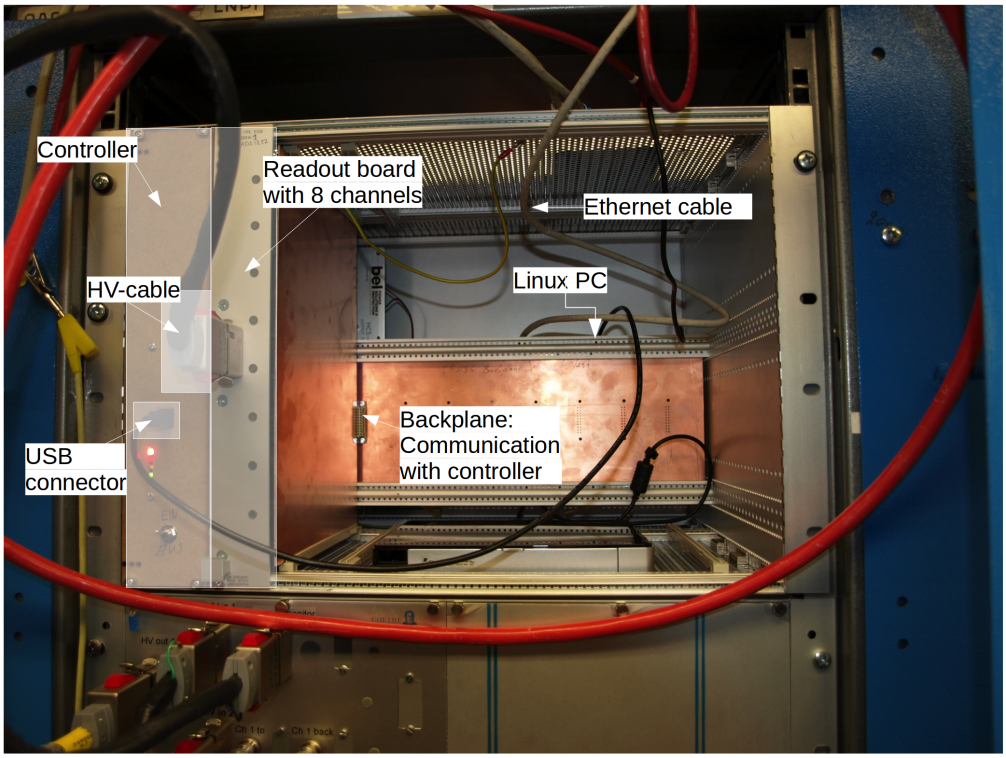

Figure 3.5: *GEM current readout system at Counting Room 4 and its main components.*

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4 Performance

After designing the program in accordance to the required functionalities which were previously presented, several measurements and tests were made in order to verify its performance capability. The graphical representation of the system's acquired data was made using ROOT, a powerful object-oriented data analysis package [14]. In particular, histogram drawing and Fourier transformation were performed, for the RMS calculation and the frequency spectrum study, respectively. As mentioned in section 2.3, the system includes digital filters, which were varied in order to observe their frequency behaviour. After ensuring the system's stability, the program was installed in CR4 and tested on the readout system which shown previously. Additional Fourier transformations were performed on data which was acquired at the two ALICE TPC sectors during proton-proton collisions.

4.1 Noise and Noise Filter

First of all the aliasing effect, which is important in the digitization area, is described since it can influence the signal of interest. The sampling theorem says that in order to sample properly a continuous signal, it must contain only frequency components below one half of the sampling rate, the so-called Nyquist frequency. Therefore, if signals above the Nyquist frequency are present, they will be aliased, which means, they will appear as new signals at frequencies below the Nyquist [15]. In general, for a signal frequency f and a sampling frequency f_s, the alias frequency f_a is equal to:

$$\mathrm{f_a} = |\mathrm{n} \cdot \mathrm{f_s} - \mathrm{f}|,$$

where n is an integer so that $\mathrm{n} \cdot \mathrm{f_s}$ is as close as possible to f. For example, with $\mathrm{f_s} = 16\,\mathrm{kHz}$, a frequency $\mathrm{f} = 20\,\mathrm{kHz}$ which is greater than the Nyquist frequency, $\mathrm{f_N} = \mathrm{f_s}/2 = 10\,\mathrm{kHz}$, will generate an alias frequency

$$\mathrm{f_a} = |16\,\mathrm{kHz} - 20\,\mathrm{kHz}| = 4\,\mathrm{kHz}.$$

Indeed, the GEM HV power supplies produces high-frequency noise above 20 kHz. In order to prevent this components aliasing into our digital signal, a low-pass analogue filter is set in front of the circuit. In addition, a three-stage digital filter is implemented in this FPGA, which provides flexibility for modifying the frequency components of the signal. This digital filter is designed with the same principle as an RC low-pass filter.

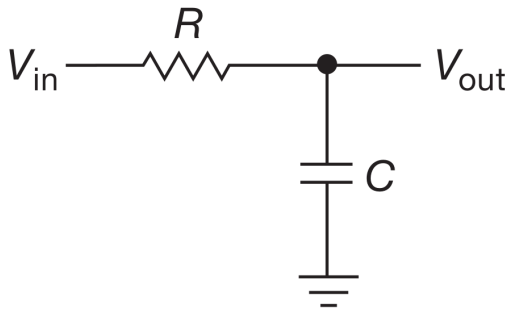

Figure 4.1: *RC low-pass filter [15].*

By combining resistors and capacitors, it is possible to make a frequency dependent voltage divider by taking the frequency dependence of the capacitor impedance:

$$\mathrm{Zc} = \frac{-\mathrm{j}}{\omega \cdot \mathrm{C}}$$

A low-pass filter is pictured in Figure 4.1. The complex Ohm's law gives:

$$\mathrm{I} = \frac{\mathrm{V_{in}}}{\mathrm{R} - \mathrm{j}/\omega \cdot \mathrm{C}} = \frac{\mathrm{V_{out}}}{-\mathrm{j}/\omega \cdot \mathrm{C}}$$

By further calculations, the amplitude of $\mathrm{V_{out}}$ can be written as a function of $\mathrm{V_{in}}$:

$$\mathrm{V_{out}} = \mathrm{V_{in}} \frac{2\pi \cdot \mathrm{f} \cdot \mathrm{R} \cdot \mathrm{C}}{(1 + (2\pi \cdot \mathrm{f} \cdot \mathrm{R} \cdot \mathrm{C})^2)^{1/2}},$$

where $f = \frac{1}{2\pi \cdot \omega}$. A characteristic reference point is the frequency where $\mathrm{V_{out}}$ has fallen by a factor of $\sqrt{2}$ of its maximum, which is ideally equal to $\mathrm{V_{in}}$, i.e. $\mathrm{V_{out}(f)} = \sqrt{2} \cdot \mathrm{V_{in}}$. This point corresponds to the cut-off frequency $\mathrm{f_c}$:

$$\mathrm{f_c} = \frac{1}{2\pi \cdot \mathrm{R} \cdot \mathrm{C}}.$$

This means that by varying the R and C values, the attenuation behaviour of the output can change correspondingly. Moreover, it can be referred to the time constant τ, of the filter which is equal to the product $R \cdot C$. The cut-off frequency can then be written as:

$$\mathrm{f_c} = \frac{1}{2\pi \cdot \tau}$$

Figure 4.2 indicates the frequency response of the RC filter. The cut-off frequency refers to the point where the output is equal to $\mathrm{V_{in}}/2$.

The digital filter of the processor can be configured with two parameters. The first one is the time-constant and the second one is the bypass parameter, which corresponds to the filter stage. Firstly, the time constant was set to 0.250 ms. Therefore, the cut-off frequency is equal to 636 Hz.

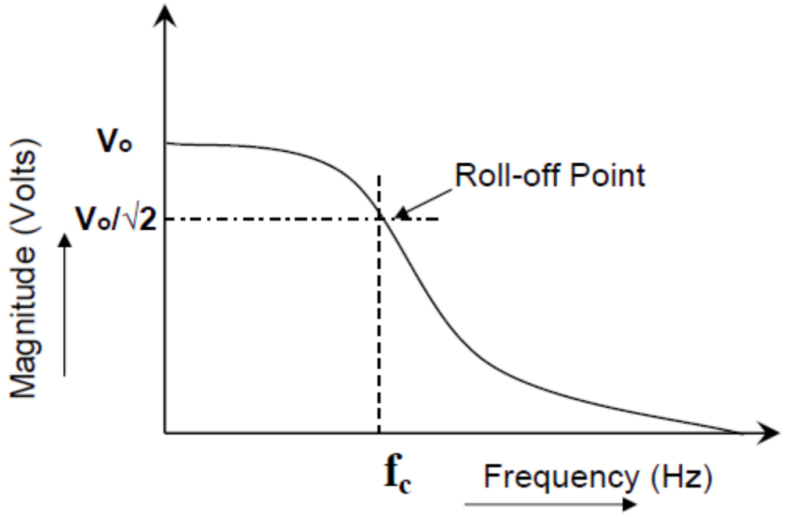

Figure 4.2: *Frequency response of the RC low-pass filter. At the cut-off frequency f_c, the value of V_{out} has decreased by a factor of $\sqrt{2}$ of its maximum [16].*

In order to test the system in the laboratory, a function generator was used. This device gives the possibility to generate desired periodic signals and even white noise signals with given peak-to-peak voltage value. White noise is a random signal which has equal intensity at all frequencies. This means that the frequency spectrum of white noise is flat. Two signals were generated and connected to the system's input, a sine wave of $\mathrm{f} = 636\,\mathrm{Hz}$ and $\mathrm{V_{pp}} = 1\,\mathrm{V}$ and a noise signal with $\mathrm{V_{pp}} = 1\,\mathrm{V}$. Next, raw data was recorded with an 8 kHz sampling frequency. In order to represent the input signal in the frequency domain, a ROOT macro file was written, for performing Fourier transformations. The continuous Fourier transform is defined as

$$\mathrm{F}(\omega) = \int_{-\infty}^{\infty} \mathrm{f(t)e^{-2\pi ikt}dt}.$$

Considering generalization to the case of a discrete function $f(t) \rightarrow f(t_n)$ by letting $\mathrm{f_n} \equiv \mathrm{f(t_n)}$, where $\mathrm{t_n} \equiv \mathrm{nT}$, with $\mathrm{n} = 0, 1, 2, ..., \mathrm{N}-1$, and T the sampling period, the discrete Fourier transform can be written as

$$\mathrm{F_k} = \sum_{\mathrm{n}=0}^{\mathrm{N}-1} \mathrm{f_n e^{-2\pi iknT}}.$$

The frequency spectrum that is obtained by performing discrete Fourier transformation on the acquired signal data can be seen in Figure 4.3. Both axes are in logarithmic scale. The x-axis values indicate the present frequencies up to 4 kHz, which is the Nyquist frequency. The y-axis values indicate how often certain frequencies appear, which is equivalent to the corresponding intensity. Hence, the intensity of two different frequency regions can be compared in order to follow the filter's frequency behaviour. The sine wave was used to reference the cut-off frequency. It

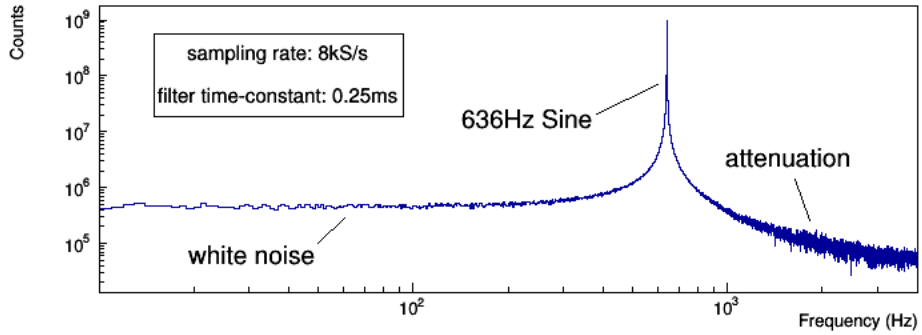

Figure 4.3: *Frequency spectrum of a filtered sine and white noise when a digital filter cut-off frequency of* 636 Hz *is applied.*

can be seen that the generated sine contains not only a single frequency, but has a finite bandwidth which is inevitable in real signals. Before the sine wave peak, i.e. before the cut-off frequency, the generated white noise signal is passing the filter unaffected and therefore a flat spectrum can be noticed. On the contrary, after the cut-off frequency, the noise is attenuating over the frequency due to the low-pass filter operation.

In order to increase the roll-off after the cut-off frequency, the processor consists of a chain of three identical low-pass filters. The stage can be adjusted by the second filter parameter. By setting the bypass parameter at 3, all three filters are bypassed, i.e. no filter is being used. On the other hand, setting it to 0, all three filters are active. The behaviour of applying a different number of filters was tested by sending a white noise signal with $V_{pp} = 1\,V$. Figure 4.4 is showing the frequency response both of one (black) and three (blue) filters. In this case, only the y-axis is in logarithmic scale. As before, the reduction of the signal power after the cut-off frequency can be recognized. An exponential function

$$y = \exp(\text{Constant} + \text{Slope} * x)$$

was fitted on both graphs in order to compare at their slopes. The fits were performed in the region around the cut-off frequency, i.e. 400–2000 Hz, where the steepest roll-off is expected. The fits appear as lines, due to the logarithmic scale of the y-axis. The slope with one filter is -6.5×10^{-5}, whereas the slope with three filters is -15.7×10^{-5}. Clearly, when applying all filters, the slope of the roll-off is increased. This is actually what usually is desired when a low-pass filter is applied. The roll-off slope should be steep, so the undesired signal should attenuate rapidly.

Lastly, the output noise produced by the AD7124-4 operation was determined for different sampling rates. In particular the output current, in the absence of any input signal, was measured for the possible sampling rates between 500 and 16 000 Hz. Its mean value together with its variation for the different frequencies is shown in Figure 4.5. For each sampling rate, the current is fluctuating around

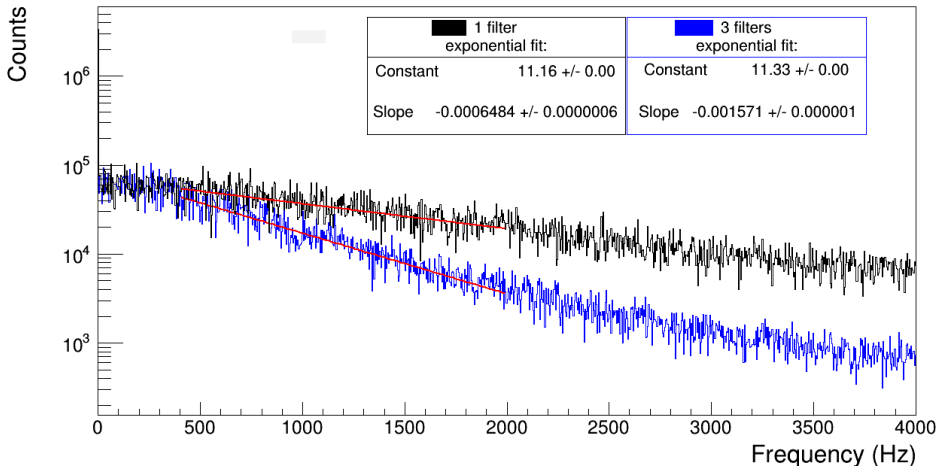

Figure 4.4: *Frequency spectrum of white noise signal when applying one (black) and three (blue) filters. Data fitted with the exponential function. The slope values are indicating that the roll-off is increasing when applying more filters.*

zero, as desired. However, for ADC operations with faster sampling processes, the fluctuations of the output value are expected to increase. This was also observed in the measurement. The RMS values are plotted separately in Figure 4.6. At a sampling rate of 16 kHz, the signal output shows a much higher RMS level. Because for the GEM-current monitoring where a resolution of 1 nA is required, the optimal sampling rate was found to be up to 8 kHz. Nevertheless, the RMS value that is calculated by the FPGA continuously is not stable for zero input, i.e. does not have a constant value. It can be seen, that the variation of the output RMS value is also greater for higher frequencies.

4.2 Stability Tests

In order to have a continuous readout of the analogue current on the GEM foils, the monitoring system must be stable. First, the stability was tested by installing the software at ALICE and carrying out a long-term readout. The data was being published through DIM with a rate of 8 Hz for more than six weeks while no error was observed. Secondly, the system's stability was tested by sending permanently new commands. In total, 1000 configurations were made and again not a single problem, misconfiguration occurred. Lastly, attention was paid to capture any error from external causes. For example, if the board power supply would stop for just a few milliseconds, the software will transition to the *Error* state, until it is able to communicate again with the device. In this case, the necessary reconfiguration steps are automatically executed in order to retrieve same status as before the power-off.

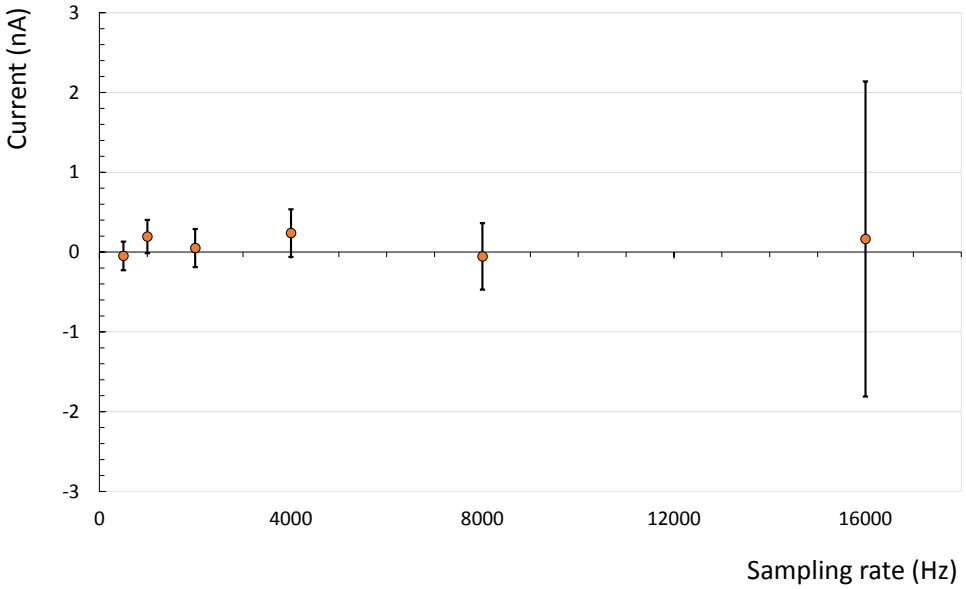

Figure 4.5: *ADC operation noise for the different possible sampling rates. Dots indicate the mean value at no input and the vertical bars represent the RMS values.*

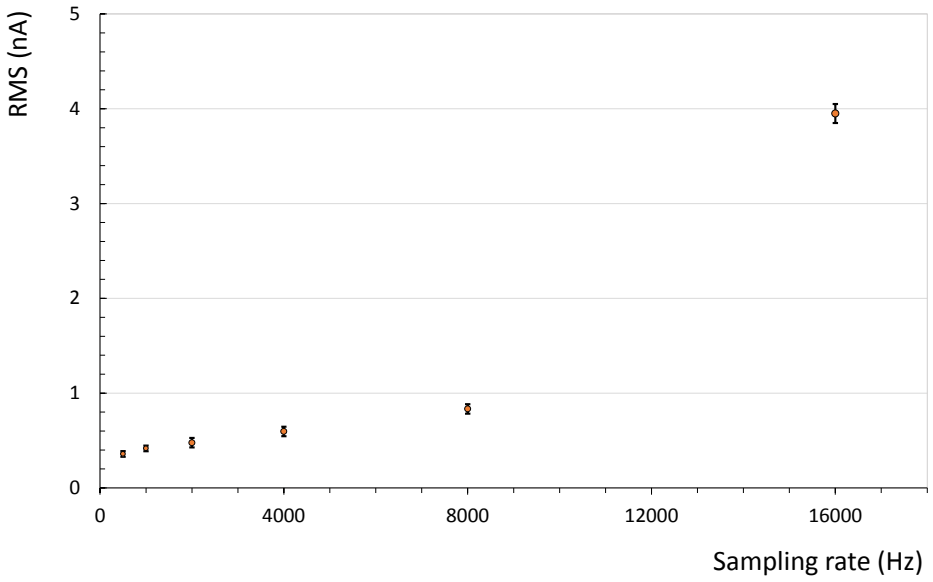

Figure 4.6: *RMS values for the different sampling rates. The ADC noise is increasing for higher sampling rates.*

4.3 Deployment at CERN

Eight GEM stacks have been already installed at two TPC readout chambers at ALICE. Furthermore, one board with eight channels is placed in CR4 since July 2017 in order to test its capability in measuring the analogue current on these GEM stacks. Firstly it was measured that by connecting only the board with the HV supplies, an RMS noise less than 1 nA is produced due the 80 meters long HV cable and circuit's noise. Moreover, the RMS value is increased up to 3 nA, when switching the power supplies on for the GEM operation.

During LHC proton-proton collisions at 190 kHz, the GEM current was recorded with a sampling frequency of 8 kHz. Indeed, a current of -94.76 nA was measured passing through the GEM4 top foil. Its corresponding RMS value was found to be 8.29 nA. These values are actually indicating that the current arises from the LHC beam, as even the RMS is greater than this, which is produced by the system itself. For the estimation of the space-charge fluctuations in the drift volume, the distortion map must be updated at 1 kHz with the mean value of the current. Furthermore, a Fourier transform was performed as before. Figure 4.7 shows the frequency domain of the acquired data. The spectrum indicates a general slight increase at the lower frequencies together with two bumps at 100 and 300 Hz, which can be probably traced to the structure of the beam collisions. Apart from that, the spectrum is mainly flat as desired. Most of the spikes that can be seen on the spectrum can be refereed to the higher harmonics of the frequency peaks at 50, 100 and 300 Hz. The 50 Hz power-line noise is unavoidable, but has low power compared to the power of the whole signal and therefore it is not greatly affecting the current measurements.

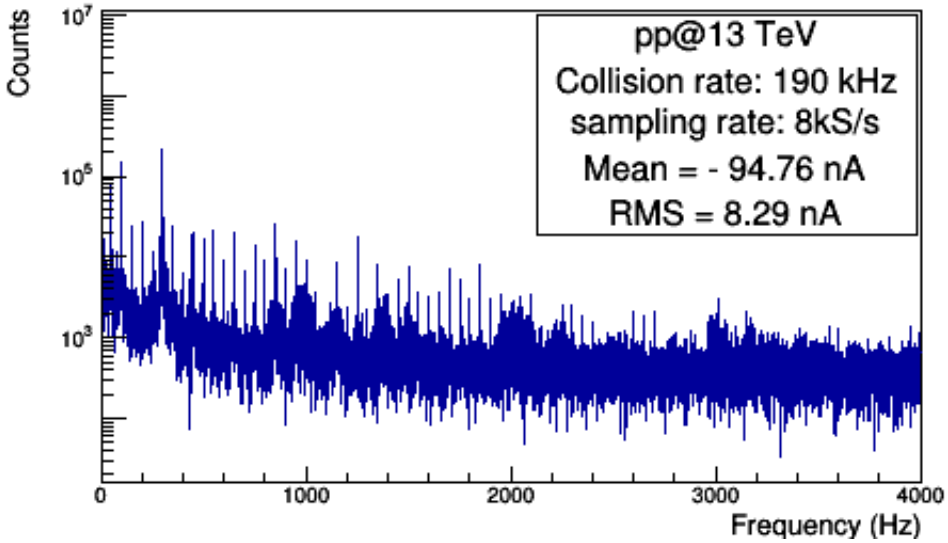

Figure 4.7: *Fourier Transformation of GEM current raw data acquired at ALICE during proton-proton collisions. The current was found to be (-95 ±8) nA.*

5 Conclusion

The TPC will be upgraded with an amplification and readout based on GEM technology in order to perform a continuous readout. For the online track reconstruction, the space-charge distortions which are caused by the ions that flow back into the drift region, must be determined.

This is considered to be done by measuring the analogue current on the GEM foils. Within this thesis, the software for the relevant system was developed in order to ensure a continuous readout. In particular, the software is designed as a finite state machine to control and monitor the execution flow. Moreover, a command-handler was implemented, which enables the communication with the system. The commands are structured in a standard form in order to avoid false configuration or crash of the program. The RMS and the average value of the GEM4 Top currents are digitized by the the FPGA continuously and being published via DIM, in order to monitor the GEM current. It was found that the deployed ADCs have a resolution of better than 1 nA with sampling rates of up to 8 kHz. However, due to the network communication via DIM, the data transfer of all channels is presently limited to 10 Hz. For this reason, an additional project, which is in progress, considers to transfer the data directly to DAQ through e-link communication at a rate of 1 kHz and more for higher precision corrections.

Furthermore, the system's stability and functionality was proven with long-term tests together with the different digital filter configuration tests. After installing the system at ALICE for measuring the analogue current on two TPC-GEM sectors, a Fourier transform was performed on acquired data during proton-proton collisions. In the lower frequency region, the beam fluctuations could be seen but apart from that, the frequency spectrum was found to be mainly flat.

The system offers a redundant possibility to reliably correct the space charge distortions and it is routinely used in the present setup. Furthermore, it scales for the full system with 144 channels in total and will be deployed when constructing the upgrade TPC in the ALICE clean room starting in 2019.

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I want to close this thesis by telling to my parents, my sister Elisavet, my brothers Constantinos and Lysandros, and my girlfriend Georgia, a big thank you, for being always there for me during my undergraduate studies, even if they were far away...

Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg,