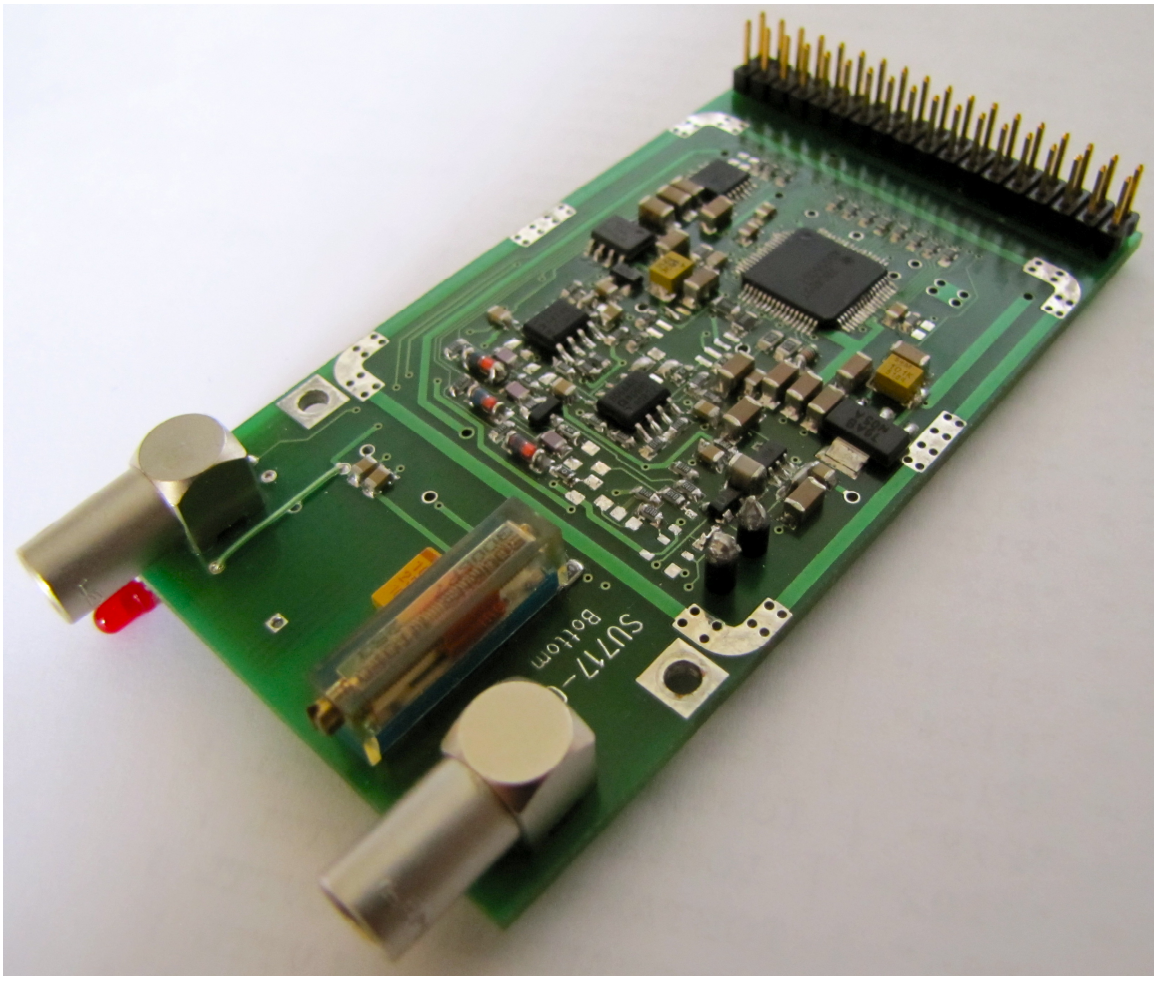
SU717: Ladungsempfindlicher ADC

Beschreibung

Das Modul besitzt einen schnellen analogen Integrator sowie einen 100 MHz ADC mit 14 Bit Auflösung.

Der Integrator wird mit einem Steuersignal entladen (Reset) und der Eingang mit zwei weiteren Steuersignalen kurzgeschlossen bzw. durchgeschaltet. Der Ruhestrom kann über ein Poti eingestellt werden.

Im weiteren gibt es einen Coax-TTL I/O sowie eine LED, die unabhängig betrieben werden.



Funktionen

Anzahl	Modul	FPGA Modul
1	Ladungsempfindlicher ADC (100MHz)	QDC
1	Digital IO (TTL)	DIO
1	Leuchtdiode	LED

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Steckerbelegung

Pin	Signal	Bedeutung
1	+ 5V	Spannungsversorgung
2	+5V	Spannungsversorgung
3	CLKout	Systemclock (100MHz) Rückführung
4	Reset	ADC Reset
5	D1	ADC Data
6	D0	ADC Data
7	D3	ADC Data
8	D2	ADC Data
9	D5	ADC Data
10	D4	ADC Data
11	D7	ADC Data
12	D6	ADC Data
13	D9	ADC Data
14	D8	ADC Data
15	D11	ADC Data
16	D10	ADC Data
17	D13	ADC Data
18	D12	ADC Data
19	SCLK	Serial Clock
20	OVR	ADC Overflow
21	SEN	Serial Enable
22	SDATA	Serial Data
23	CLK_n	ADC Clock negativ
24	CLK_p	ADC Clock positiv
25	EN1	TTL Output Enable (Low active)
26	OUT1	TTL Output
27	IN1	TTL Input
28	QRES	Integrator Reset
29		
30	QShort	Integrator Input Short
31	LD1	LED
32		
33		
34		
35	GND	Spannungsversorgung und Signalreferenz
36	GND	Spannungsversorgung und Signalreferenz

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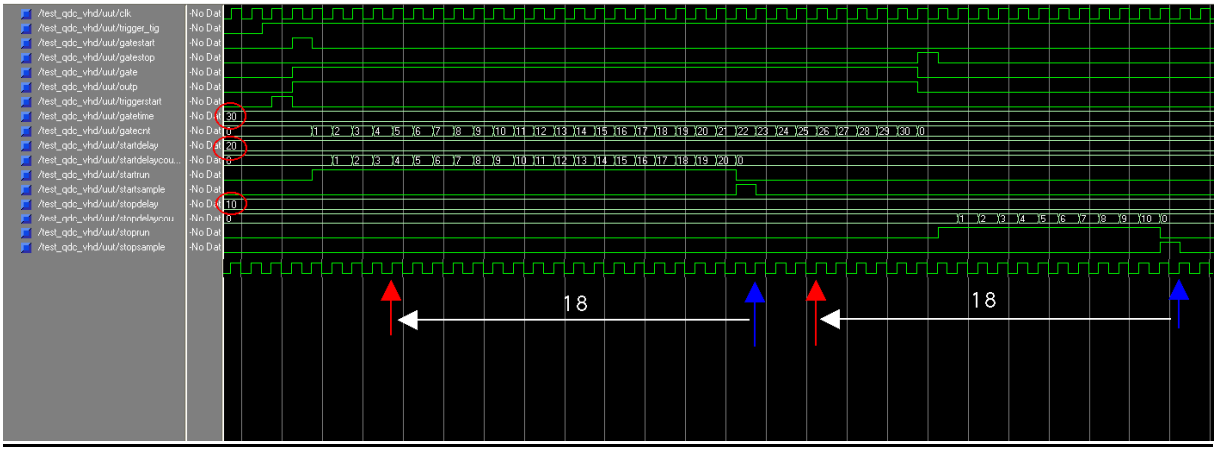
Timing



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Introduction

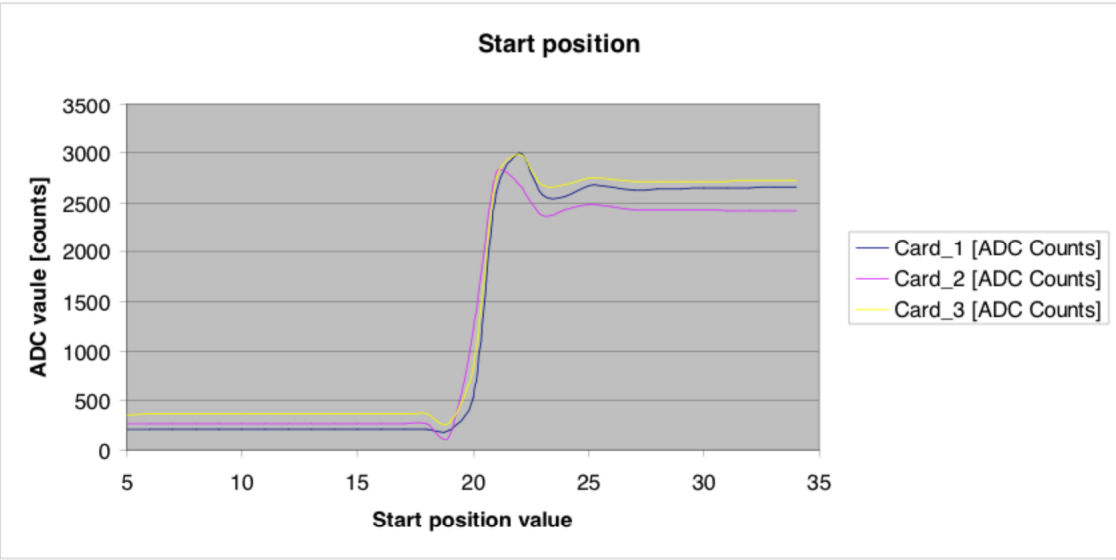
This document describes a test procedure of the system DL710-1 in conjunction with the three SU717-1 and one SU704-1 sub-modules for the Perkeo project. The aim of this test is the characterization of the SU717-1 sub-module for future analyses. The influence of several parameters in the results was analyzed.

Start position test

In this test the position where the QDC signal is stable after the gate is opened will be estimated. For this purpose the start position is modified from 10 to 30. An input signal is not necessary for this test. Each point will be acquired as a 512 samples vector with a frequency sample of 2 KHz, from this vector the mean value will be calculated. The parameters of the QDC are the following:

Start pos = 5 to 35
Stop pos = 15
Gate = 30 (300 ns)
Trigger frequency = 2 kHz

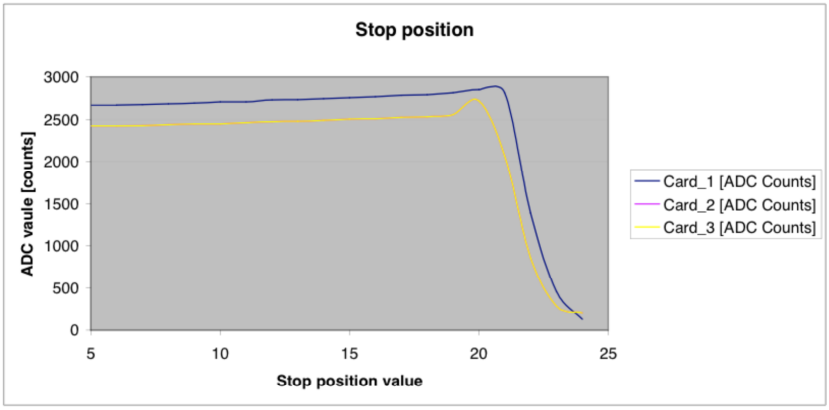
The graphic shows the mean value of the 512 samples vector for each start position.



Stop position test

In this test the last position where the QDC signal is stable before the gate is closed will be estimated. For this purpose the stop position is modified from 5 to 25. An input signal is not necessary for this test. The parameters of the QDC are the following:

Start pos = 23
Stop pos = 5 .. 25
Gate = 30 (300 ns)
Trigger frequency = 2 kHz



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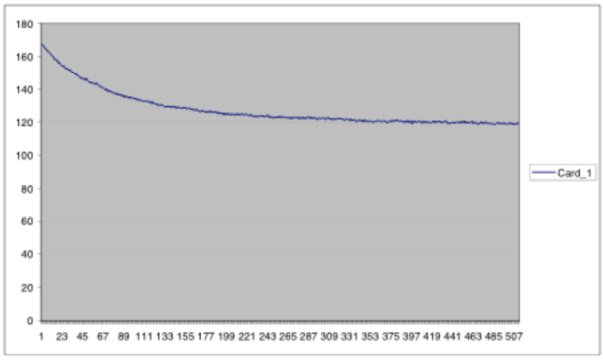
Stress test

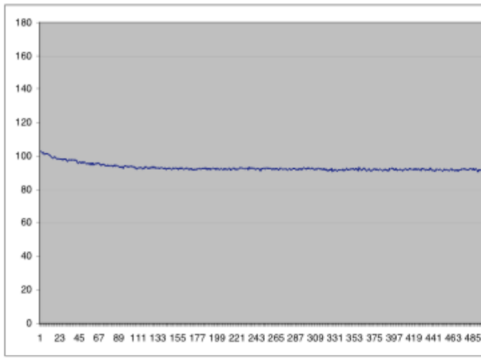
This test is made to calculate the noise and stability of the QDC system. An input signal is not necessary for this test. Each point will be acquired as a 512 samples vector with a frequency sample of 2 KHz, from this vector the mean value and deviation will be calculated. A histogram for all the points of all vectors is shown as well. The parameters of the QDC are the following:

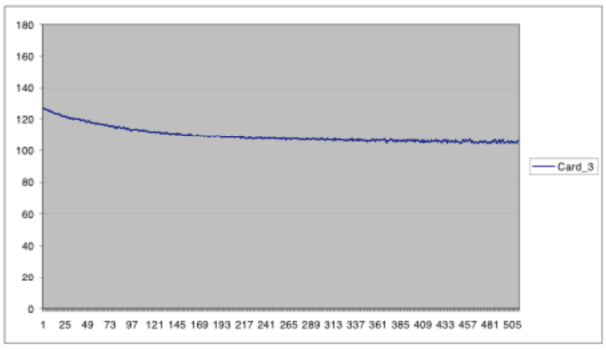
Start pos = 30
Stop pos = 15
Gate = 30 (300 ns)
Trigger frequency = 2 kHz

The test ran approximately 31 minutes and 1515 vectors were saved. Thus a new vector was saved each 1.22 seconds. The graphics show only 500 vectors for each sub-module.

→ Mean value







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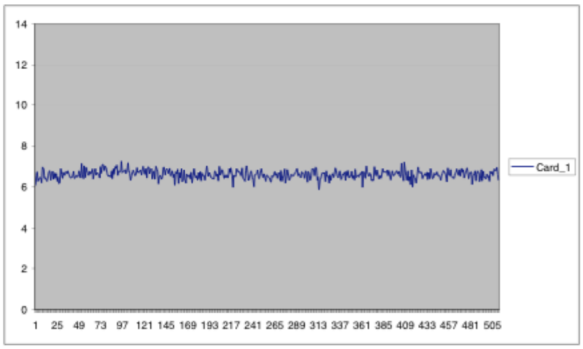
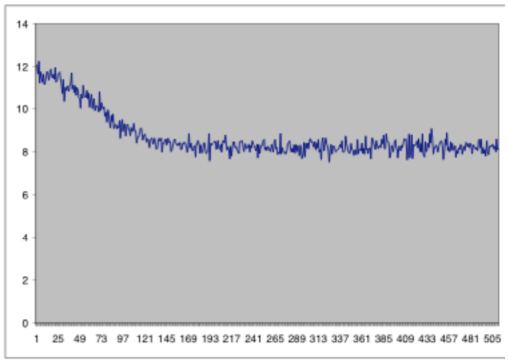
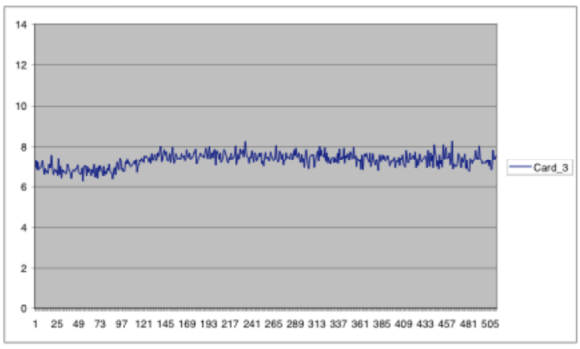
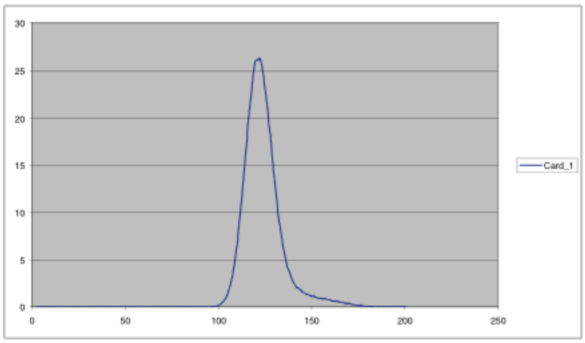
→ Deviation

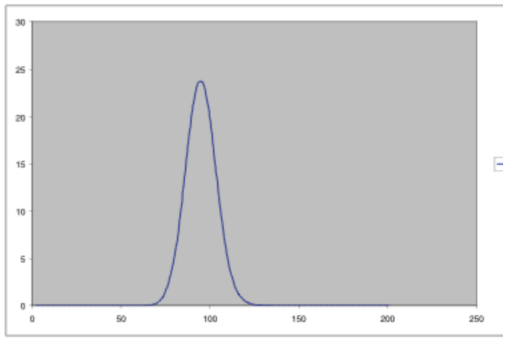


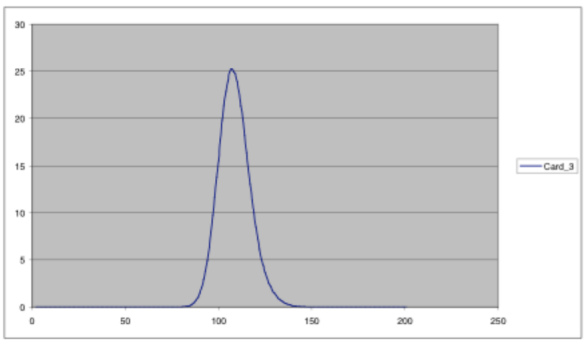




→ Histogram







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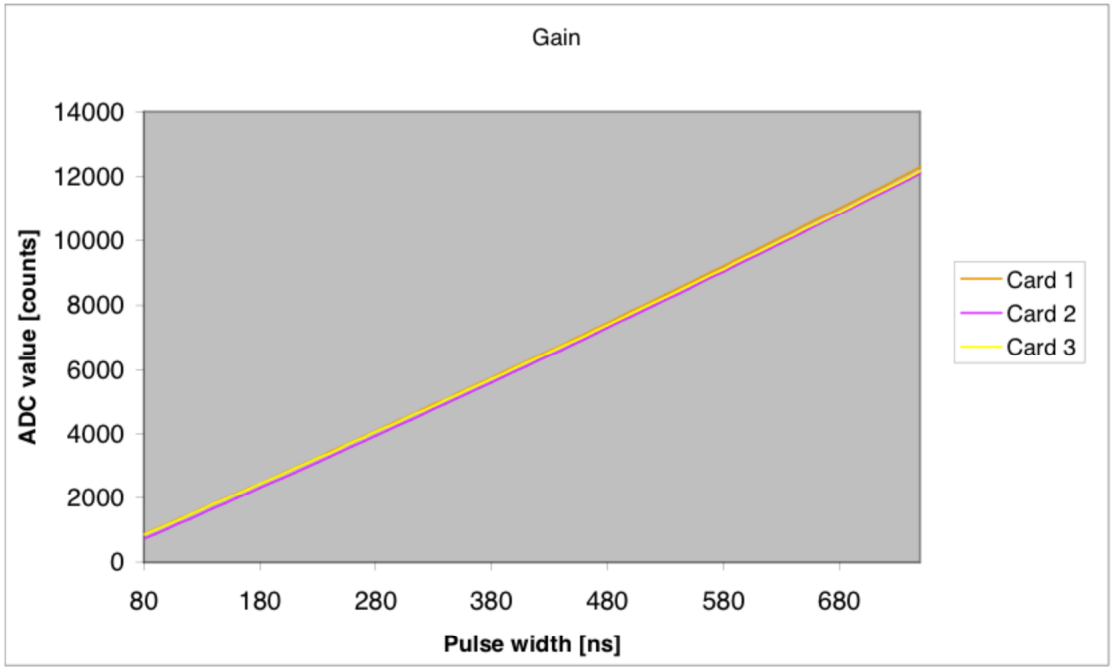
Gain test

To test the gain a pulse signal with a variable width is used. The parameters of the QDC are the following:

Start pos = 30
Stop pos = 15
Gate = 100 (1 us)
TTL pulse width = 1..100 (10 ns to 1 us)
Trigger frequency = 2 kHz

The test signal was created with the SU704 and it was attenuated with 50 dB, thus the QDC was not saturated.
The measurement consists of a 512 samples vector for each pulse width. This measurement was made for all sub-modules. In the following graphic the mean ADC Value of the 512 samples vector for the corresponding pulse width is shown.



If a regular curve fit is made (linear regression), the equations of the three sub-modules are approximately the same. The main difference is the offset of the curve (which can be adjusted with an external potentiometer), the gain is the same. The linearity of the curve is not so bad, because for all the curves the coefficient of determination (R2) is approximately 0.999.

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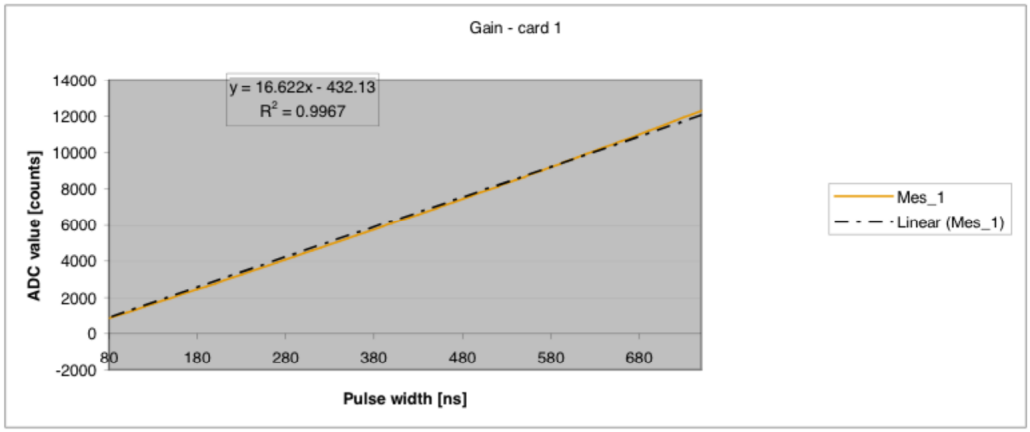

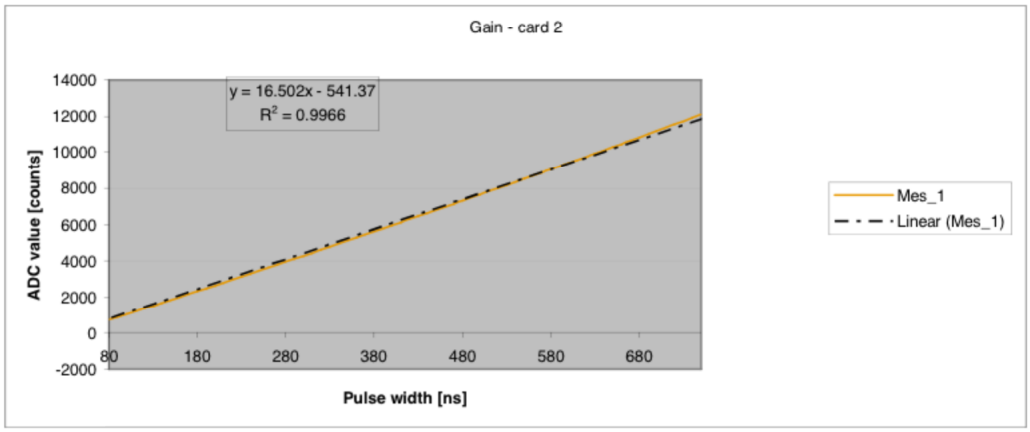

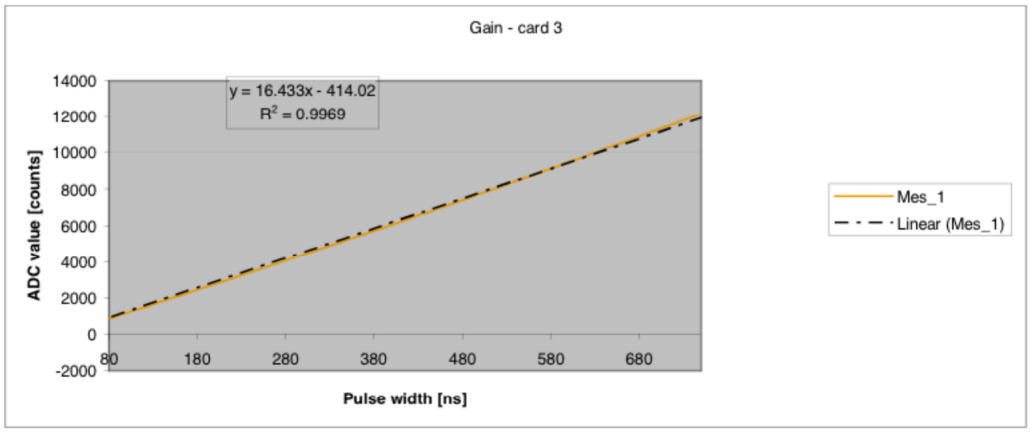

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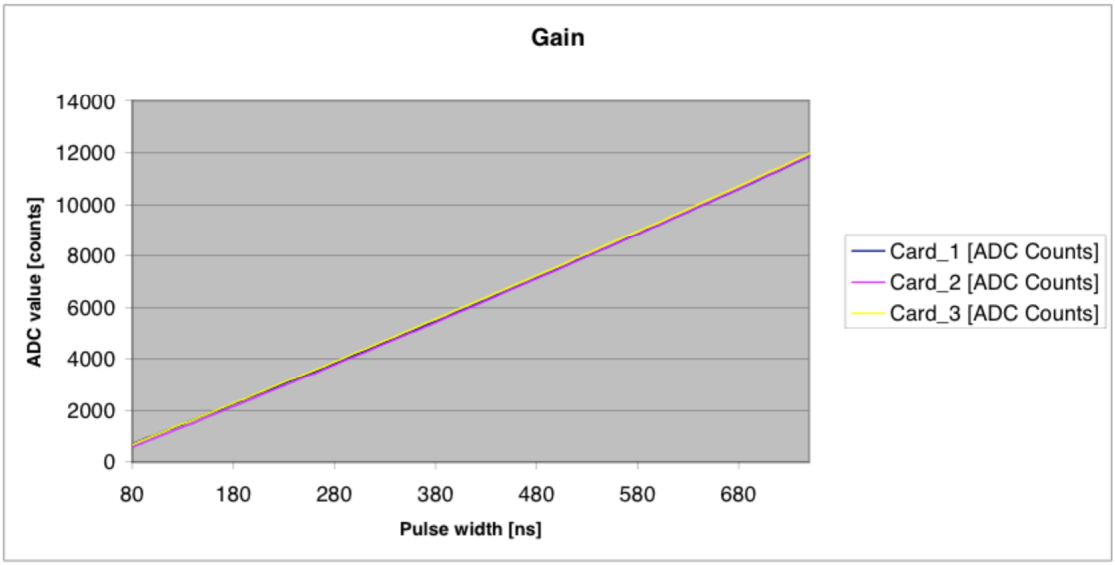
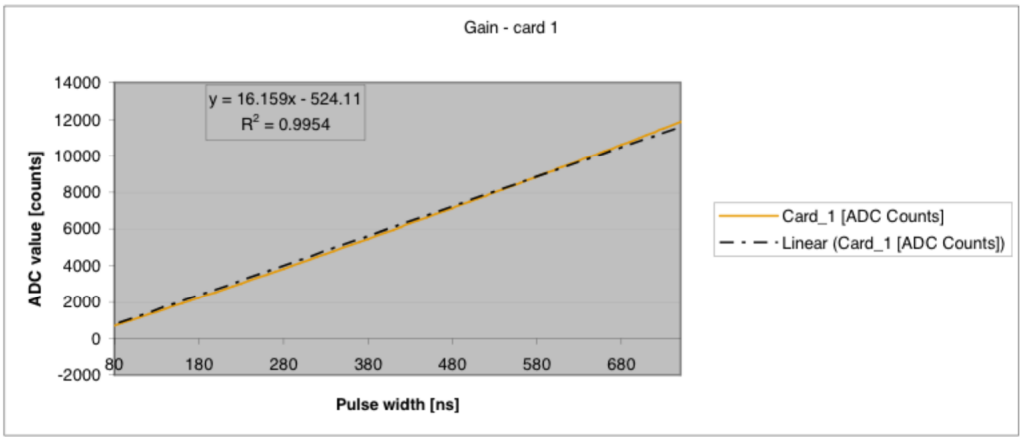
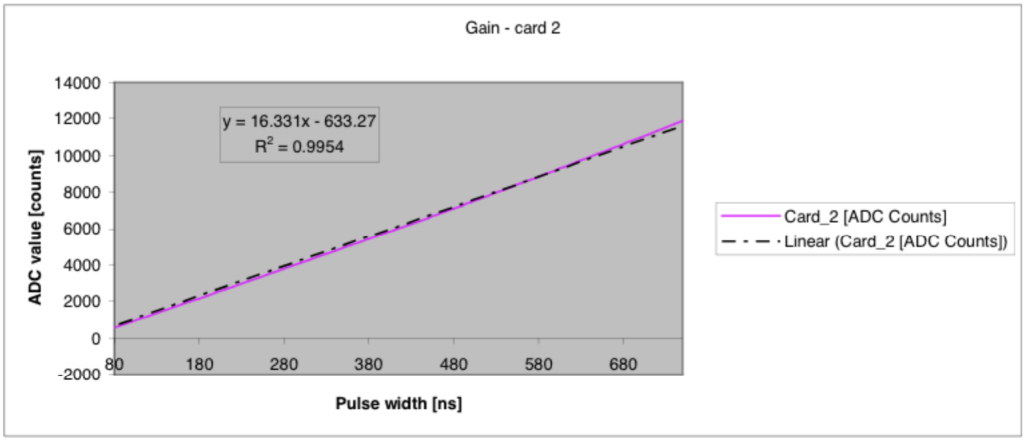
The same test was repeated a day after







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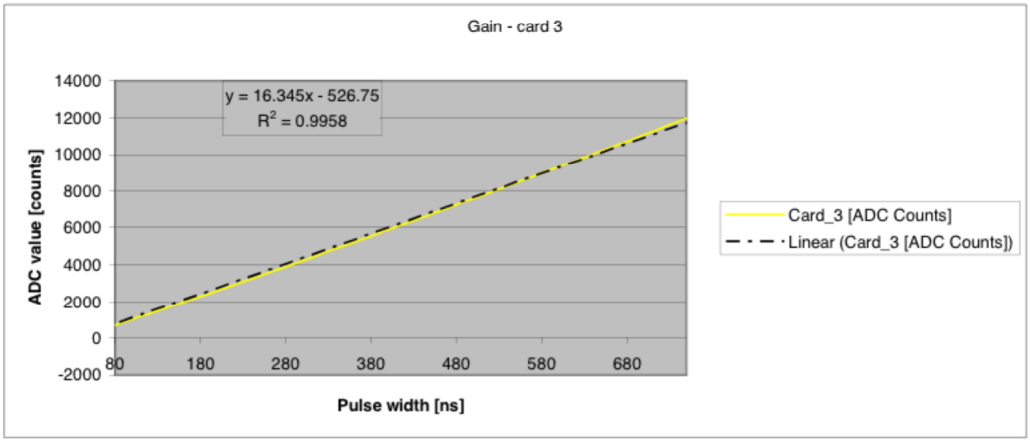

In the next tables are shown the gain for the two measurements and the error for each gain respect to the mean gain in % (mean value – gain / mean value x 100).

	Gain mes. 1	Error Gain mes. 1 (%)
Card 1	16.622	-0.623524426
Card 2	16.502	0.102911799
Card 3	16.433	0.520612628
Mean value	16.519	

	Gain mes. 2	Error Gain mes. 2 (%)
Card 1	16.169	0.69198485
Card 2	16.331	-0.302999283
Card 3	16.345	-0.388985567
Mean value	16.2816667	

The results show a different value of Gain, it is possible that this error is due to the used source (TTL output from SU704) or the temperature difference.

Conclusions

The system is strongly temperature dependant, but when the final temperature is achieved, the noise and gain remain constant.
The start position test shows that a start position larger than 25 units must be used to avoid the transient effects of the gate. The stop position must be 18 maximum.

It is important to set the same QDC parameters for all QDCs (start, stop, gate, offset, etc) to obtain the same gain.