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# **Design, Implementation and Commissioning of the Pretrigger System for the Transition Radiation Detector at the ALICE experiment of CERN**

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## **Design, Implementation and Commissioning of the Pretrigger System for the Transition Radiation Detector at the ALICE experiment**

The Transition Radiation Detector (TRD) in the ALICE experiment at the Large Hadron Collider (LHC) requires a trigger signal  $500ns$  after a collision had occurred. This is  $1\mu s$  before the first trigger decision by the ALICE experiment is made in the Central Trigger Processor. The design for the TRD pretrigger, using 88 analogue inputs from the V0 and T0 detector and interfacing an additional 576 digital inputs from TOF via an external unit, has been developed, implemented and successfully commissioned in the solenoid.

## **Entwurf, Aufbau und Inbetriebnahme des Pretrigger Systems für den Übergangsstrahlungsdetektor am ALICE Experiment**

Der Übergangsstrahlungsdetektor (TRD) im ALICE Experiment am CERN benötigt ein Trigger-Signal  $500ns$  nachdem eine Interaktion stattgefunden hat. Dies bedeutet  $1\mu s$  bevor die erste Trigger-Entscheidung des ALICE Experiments im Zentralen Trigger Prozessor (CTP) gefällt wurde. Das Design für den TRD Pretrigger benutzt 88 analoge Eingänge von den Detektoren V0 und T0. Zusätzlich wertet es 576 digitale Eingänge von TOF über eine externe Einheit aus. Der TRD Pretrigger wurde entwickelt, aufgebaut und erfolgreich im Magneten in Betrieb genommen.



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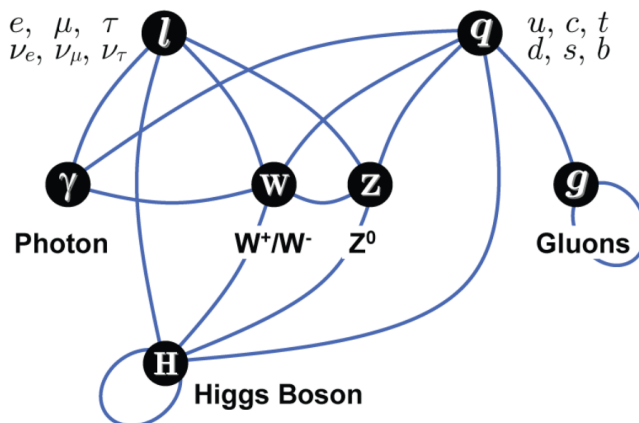
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# 1 Introduction

Since the beginning of human kind one aims to understand the nature of matter. Today the matter has been traced down to consist of molecules, atoms, nucleons and finally quarks and leptons. Along the discovery of smaller and smaller particles theories have been developed to describe the forces between them. Today we have the standard model. All matter consists of quarks and leptons. The exchange of bosons is the origin of forces. Strong interactions occur between quarks and gluons, where the gluons are the carrier of the strong force. Quantum chromodynamics (QCD) is the field theory describing the strong interactions.



**Figure 1.1:** The Standard model. The matter in nature consists of quarks and leptons. The forces are transmitted via the exchange of bosons. The Higgs boson has not been yet discovered.

**Deconfined Nuclear Matter** The asymptotic freedom states that the effective coupling constant of QCD, falls with increasing momentum transfer  $q^2$  or equivalent, with decreasing distance between particles. In a thermal medium, the characteristic momentum transfer between (nearly) massless particles is of the order of the temperature  $T$ , and thus the effective coupling between quarks and gluons must become weak when  $T$  grows large. The structure of nuclear matter at low temperatures, where it is composed of a multitude of hadronic particles, baryons and meson melt down to weakly interacting quarks and gluons, the quark-gluon plasma (QGP).

Our universe is expected to have been in such a plasma state  $10\mu s$  after the Big Bang. Today deconfined nuclear matter only exists in neutron stars, super novae explosions or artificially created in the laboratory.

Numerical solutions of QCD (Figure: 1.2) at net baryon chemical potential of zero predict that the transition from a hadronic gas to a quark-gluon plasma should occur at a temperature of approximately 170MeV. This value coincides with the limiting temperature of matter composed of hadrons first postulated by Hagedorn [2]. Below a critical temperature of 150MeV the created matter acts like a Hadron gas. The  $1/T^4$  proportionality as well as the absolute value can be explained similar to a Stefan Boltzmann gas of pions and nucleons [4]. Above the critical temperature this matter acts completely different. Between 170 MeV and 150 MeV the  $1/T^4$  proportionality of a hadron gas is violated. A sign for a phase transition like from liquid water

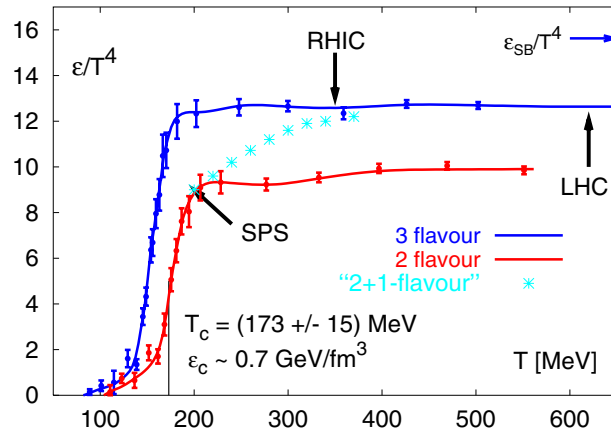


Figure 1.2: Lattice QCD calculation of the freeze out temperature of the QGP [1].

to steam. The hadrons melt to quarks and gluons increasing the number of degrees of freedom in the matter. After all matter melt the proportionality of a Stefan-Boltzmann gas is restored but at a much higher energy density due to the increased number of degrees of freedom. It is expected that chiral symmetry is recovered within the QGP [4] reducing the mass of the light quarks to their bare current mass [3].

The only way to create such a QGP in the laboratory is by colliding heavy nuclei such as Au or Pb at highest energies. Figure 1.3 shows experimental results for the chemical freeze out temperature at various baryo-chemical potentials. At the chemical freeze out the chemical equilibrium of the QGP is destroyed and the quarks and gluons begin to hadronize. An approximated phase diagram for baryon chemical potential not equal to zero can be calculated using the Bag Model, modelling the confinement of the QGP by introducing a vacuum pressure holding together nuclear matter [6].

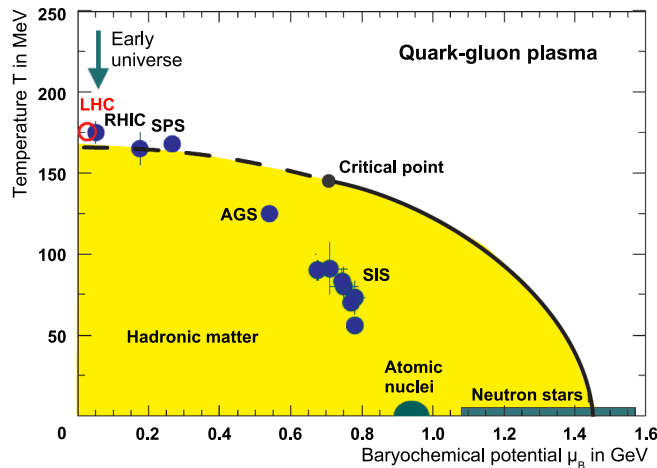


Figure 1.3: Phase diagram of strongly interacting matter [5].

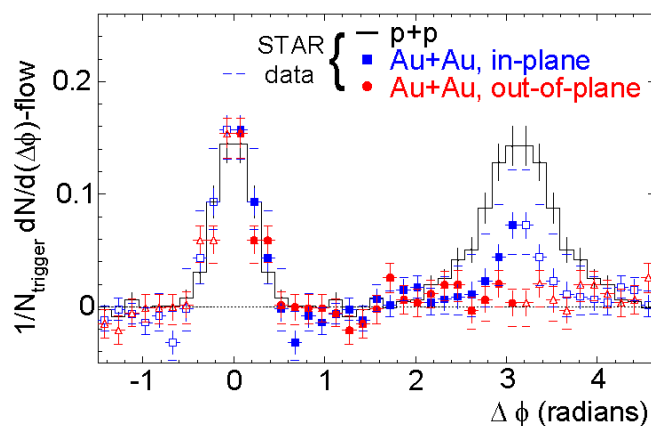
**The ALICE Experiment** The ALICE Experiment at the Large Hadron Collider (LHC) at CERN in Geneva is going to produce and investigate a QGP in heavy ion collisions. Two lead nuclei will be collided at a center of mass energy of 5.5 TeV per nucleon pair. The matter will be compressed

to a density of  $10^{10}$  times the density of normal baryonic matter and heated up in a fireball to more than  $2 \cdot 10^{12} K$ . At this stage the quarks and gluons will interact strongly. This strongly interacting quark gluon plasma (sQGP) has an expected lifetime of  $10^{-23} s$ . This is a significant difference to the weakly interacting quark gluon plasma (wQGP) as it has existed up to  $10 \mu s$  after the Big Bang at densities of 10 times the density of baryonic matter. The sQGP will give a opportunity to test the QCD in perturbative as well as non-perturbative regions.

The ALICE detector is laid-out to investigate the QGP. ALICE focuses rather on the exact reconstruction of particles in a high multiplicity environment over a large interval of momenta than on high event rates. Therefore a TPC is used as the main tracking device. Special attention was laid on electromagnetic probes since they can escape the QGP without any further interaction. Thus they give a pure insight into the QGP. The Transition Radiation Detector (TRD) is besides an electromagnetic calorimeter (PHOS) one of the main detector for these probes. The TRD is a tracking and trigger detector with electron identification located in the central barrel. It provides a hardware trigger for a certain invariant mass in the electron channel as well as a hardware trigger on tracks with a high transverse momentum.

**Heavy Flavour Physics** Heavy quarks (charm and bottom) are produced in the first perturbative interactions within a heavy ion collision. A later thermal production is negligible because of their high mass [3]. Also an annihilation of a heavy quark and its antiquark has no significant effect within a QGP [7]. Therefore the number of produced heavy quarks is constant during the expansion of the QGP. If thermalization is reached the heavy quarks will statistically move within the plasma. Two effects specific for a QGP determine the number of created quarkonia. At low energy the produced quarks are surrounded by gluons that shield their colour charge. Hence two heavy quarks do not form a meson by binding via the strong forces [9]. At higher energy more quarkonia is produced at the phase boundary due to statistical coalescence of abundant  $c$  and  $\bar{c}$  quarks [8]. At some point the increased probability for meson production compensates the colour charge shielding and the Meson production increases.

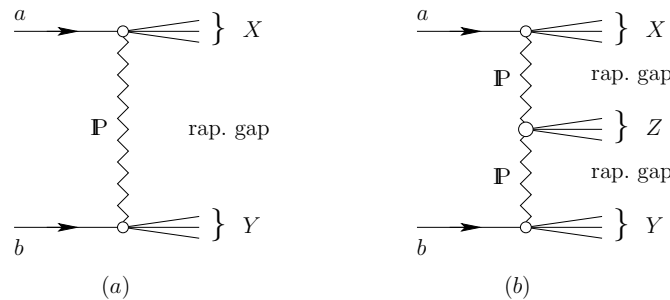
The TRD detector will be used to identify the  $J/\Psi$  and  $\Upsilon$  by their decay into a positron and electron pair. Both for offline analysis as well as for online triggering. The decrease of quarkonia production at low energies and the increase at high energies is a good proof for the existence and thermalization of the QGP phase of matter.



**Figure 1.4:** Jet quenching measured by STAR at RHIC [10].

**Jet Physics** The aim of the jet physics within ALICE is to understand the mechanisms of energy loss of particles travelling through the medium caused by QCD effects. High- $p_t$  partons produced in the initial stage of a heavy ion collision make multiple interactions inside the collision region prior to hadronisation. The energy of these partons is reduced by collisions with other partons as well as by induced gluon radiation. Figure 1.4 illustrates this energy loss as it was measured in STAR. If two nuclei do collide not fully central the reaction plane is defined by the two trajectories described by the centers of the nuclei. Star selected jets that either move within the reaction plane (in plane) or perpendicular (out-of-plan) to it by looking for trigger particles with high momenta. The backwards directed jet is more suppressed the longer the way through the medium is. Within  $pp$  collisions this jet quenching is not observed. The backwards jet has almost the same intensity as the forward one. Arguments that the jet quenching is caused by the structure of the Au itself have been enervated by d-Au collisions where no jet quenching has been observed. Because of the higher energy the cones of the jets in ALICE are more narrow and set itself more apart from the background [11], the TRD is able to detect online regions with high momenta particles and trigger on them [27].

**Diffractive Physics** QCD predicts the odderon, a particle consisting of three gluons with odd C parity and without (neither electric nor colour) charge. Thus it does neither irradiate pions nor photons [12]. The pommeron consisting of two gluons is its counterpart with even C parity. The Pommeron [13] was experimentally discovered 1990 [14]. The Pommeron as well as the Odderon increase the  $pp$  cross section [12]. The two pommerons can either undergo fusion and



**Figure 1.5:** p+p Interaction via a Pommeron exchange (a). Glueball creation via Pommeron fusion. This figure was taken from [13].

produce secondaries or one pommeron can interact directly with both p (see Fig. 1.5). A similar fusion process is also expected for the Odderon [15]. Up to now the modification of the cross section going along with the odderon channel has not been experimentally proven because of the large background originating from  $\gamma\gamma$  fusion. Using the TRD in the ALICE experiment it will be possible to suppress the background [16]. Also the  $\gamma\gamma$  fusion processes especially in Pb + Pb collisions are interesting of its own to probe the QED at strong fields [11]. Of special interest is the production of  $J/\Psi$  and  $\Upsilon$  mesons and its decay into a  $e^+$  and  $e^-$  pair, since in ALICE an efficient trigger using the TRD can thus grep 150000  $J/\Psi$  events as well as 400-1400  $\Upsilon$  events within a  $10^6$ s run with at 5% of the design luminosity of ALICE [11]. One common signature of these events is a rapidity gap [17]. In forward as well as in backward direction  $\frac{dn}{d\eta}$  is higher than at central rapidity. If the Odderon is not found one has to think if the modeling of the strong force by gluon exchange is the right way to describe QCD [12].

Within this thesis a trigger system has been developed, implemented, installed ,commissioned and successfully brought to first beam to provide a wake up signal to the TRD 500ns after the event, that is 1 $\mu$ s before the first ALICE wide trigger. The system has an input of 88 analog

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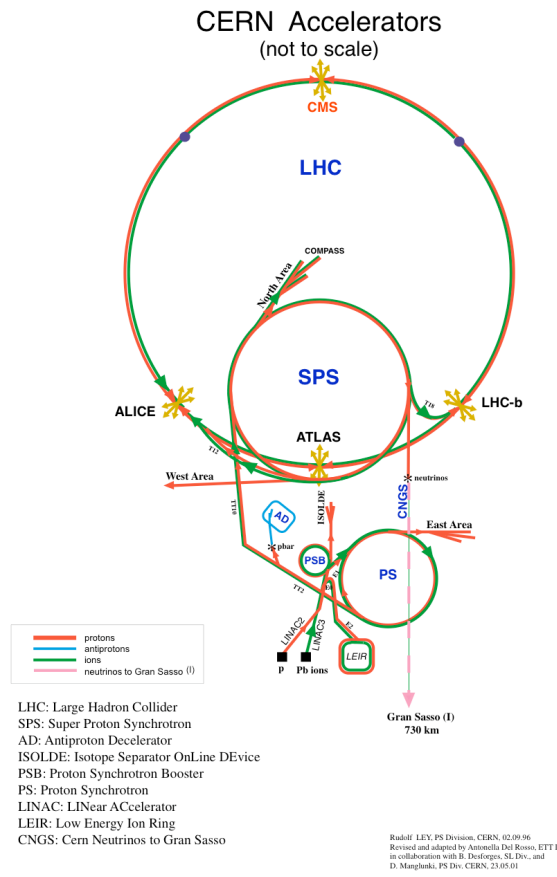
channels as well as 576 digital channels from the T0, V0 and TOF detector. It increases the effective gas volume of the TRD by 60% (Fig. 8.4(a)) necessary to achieve the trigger and tracking capabilities of the TRD. During this time also contributions to the commissioning of the TRD have been made (Chapters F, I, J, K).

The Thesis is summarized as follow. Chapter 2 describes the Accelerator facilities and the ALICE detector. Chapter 3 gives an overview on the TRD detector. Chapter 4 presents the considerations for the TRD pretrigger and the design for the TRD pretrigger derived from it. Chapter 5 is dedicated to the hardware and the services for the pretrigger. Chapter 6 summarizes the technical implementation of the design into the FPGAs. Chapter 7 introduces the software and DCS integration of the pretrigger system. Chapter 8 presents data from tests, cosmic runs and the first beam in the LHC.

# 2 LHC and ALICE

## 2.1 Large Hadron Collider

The large hadron collider is an accelerator located at the European Center for Nuclear Research (CERN) near Geneva. It has been designed to achieve center of mass energies for proton-proton collisions of up to 14 TeV and for Pb + Pb collisions of up to 5.5 TeV per nucleon pair. At 10:28 a.m. September 10th 2008 the first proton bunches with an energy of 450GeV circulated in the tunnel. Compared to the currently up to date accelerators Tevatron for  $p + \bar{p}$  collisions at 1.96 TeV and RHIC for Au - Au collisions at 0.2 TeV this will considerably extend the available energy and thus open the door for new physics. The LHC will not only open the door but also make it possible to do more precise measurements compared to previous experiments due to the high luminosity of  $10^{34} \frac{1}{cm^2 s}$  for  $p + p$  and  $10^{34} \frac{1}{cm^2 s}$  for Pb + Pb runs.



**Figure 2.1:** Schematic view of the accelerator complex of the LHC. This figure has been taken from [18]

The LHC is constructed as follow (see 2.1). The protons originate from a 90 kV duoplasmatron proton-source. In a first step they are accelerated to a kinetic energy of 50 MeV in the LINAC2 linear accelerator and passed to the multi ring booster synchrotron where they are accelerated

to 1.4 GeV. In the proton synchrotron (PS) the protons reach 26 GeV and are concentrated into bunches. The super proton synchrotron (SPS) accelerates up to 450 GeV and injects the beam into the LHC which to accelerates them up to 7 TeV. The LHC is a circular tunnel of 27 km circumference equipped with 1232 superconducting dipole magnets that are cooled down to 1.9 K by liquid helium and are able to provide a magnetic field of up to 8.3 T. The acceleration from 450 GeV to 7 TeV is done at P4 at the RF cavities. These cavities are distributed only over a distance of approximately 50 m. To keep the beam focused, 392 quadrupole magnets are distributed over the whole ring.

For lead lead runs an electron cyclotron resonance source provides the ions that are accelerated and bunched by a radio frequency quadrupole. Ions in the  $Pb^{27+}$  state are selected and accelerated up to 4.2 MeV/nucleon in the LINAC3 accelerator. Additional electrons are stripped by a carbon foil. A filter line ensures that only  $Pb^{54+}$  ions reach the Low Energy Ion Ring (LEIR) which accelerates them up to 72 MeV/nucleon. In a next step the ions are accelerated to 5.9 GeV/nucleon in the PS. When the ions are injected to the SPS they pass another foil that fully strips them to the  $Pb^{82+}$  state. The SPS further accelerates them up to 177 GeV/nucleon. The last step of acceleration is done in the LHC where the ions reach their final energy of 2.76 TeV/nucleon.

The LHC consists of two beam pipes within each single cryo-modules forming the LHC ring. It is possible to have a clockwise and counterclockwise proton beam at 7 TeV or a clockwise and counterclockwise lead beam at 2.76 TeV per nucleon. Both beam lines cross at 8 interaction points making the full kinetic energy of the LHC available for the experiments. There are four main experiments (ATLAS, CMS, LHCb and ALICE) at the LHC.

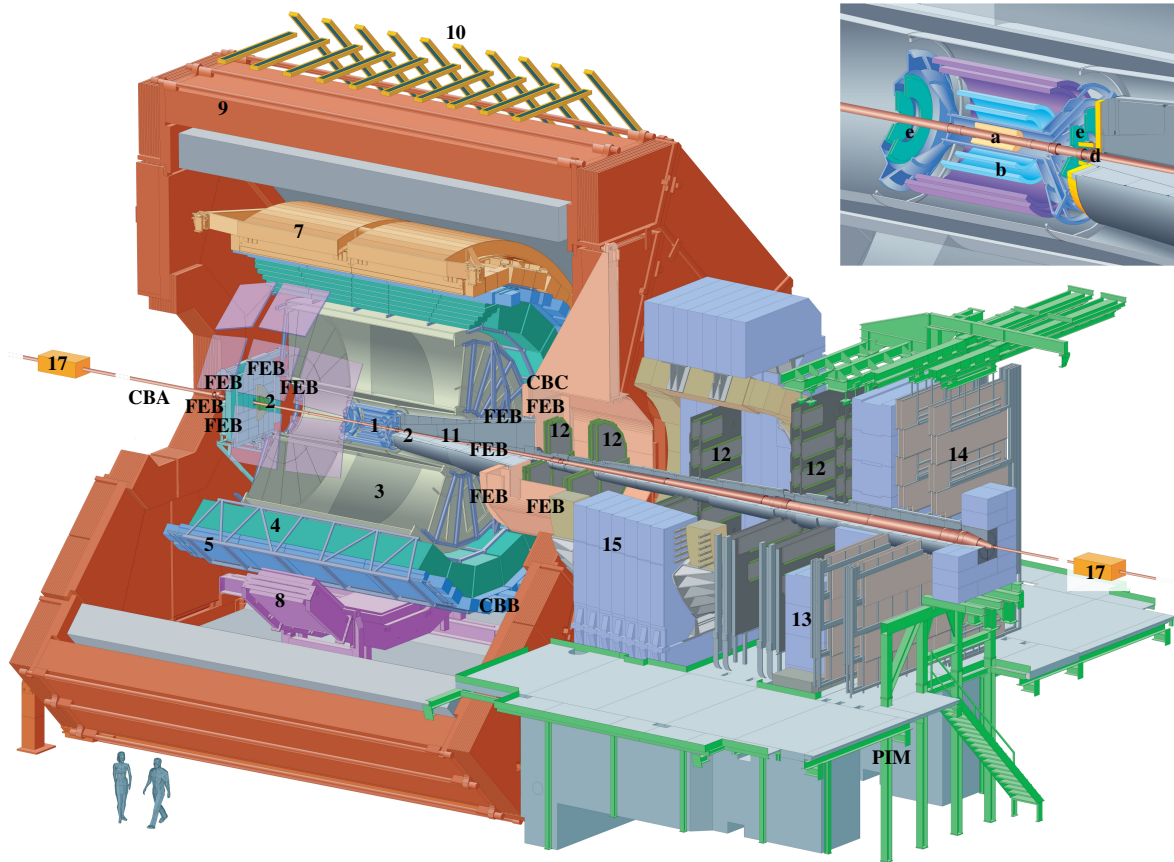
ATLAS and CMS are dedicated to search for the Higgs-Boson and to investigate theories beyond the standard model like supersymmetric particles and extra dimensions with complementary experimental approaches. The Higgs particle should be identified by reconstructing the final particles of different processes with Higgs production. Even if both detectors are general purpose detectors with large silicon inner tracking systems, hadronic and an electromagnetic calorimeters they are complementary. CMS has a two times higher magnetic field ( $B=3.8T$ ) resulting in a better momentum resolution, whereas the tracking efficiency is lower. The energy resolution in the CMS calorimeters is at least for lower energies much better than in ATLAS. However for higher energies it is more difficult to calibrate. Opposed to the Atlas electromagnetic calorimeter it is not able to do longitudinal tracking. Unique to the Atlas detector is the Transition Radiation Tracker making it possible to distinguish particles with different Lorentz-factor similar to the TRD in the ALICE experiment, but with a different technical realisation.

LHCb is dedicated to beauty physics, that is physics related to hadrons with a bottom quark or antiquark. The lifetime of these hadrons is typical long enough that it decays in the detector at a well distinguishable vertex. These decays have typical signatures like high momenta perpendicular to the direction of the original b quark among others which can be used for triggering and offline selection. Reconstructing and observing the original mesons and their oscillations one into another allows the measurement of CP violation. Since the particles of B meson decays mainly appear in the forward rapidity region, the LHCb detector is a single arm detector covering only the forward rapidity. It is equipped with three layers of trackers, RICH detectors for particle identification, a muon part for triggering and an electromagnetic as well as a hadronic calorimeter.

## 2.2 ALICE Detector

The ALICE experiment the dedicated experiment at the LHC for heavy ion physics. ALICE will identify and characterise the Quark Gluon Plasma (QGP). Instead of high event rates the experiment is optimized to precisely deal with track densities of up to  $\frac{dn}{d\eta} = 8000$  as expected for Pb+Pb collisions at LHC energies. In addition it covers a momentum region from 100 MeV/c up

to 100 GeV/c where it tracks and identifies particles. The following sub-detectors of the Alice experiment are hosted in the L3 solenoid providing a homogeneous magnetic field of 0.5 T.



**Figure 2.2:** Schematic view of the ALICE experiment. The figure shows the sub-detectors of the ALICE experiment (1: ITS; 2: FMD, T0, V0; 3: TPC; 4: TRD; 5: TOF; 6: HMPID; 7: EMCAL; 8: PHOS; 9: L3 - Magnet; 10: ACCORDE; 11: ABSORBER; 12: MUON TRACKING; 13: MUON WALL; 14: MUON TRIGGER; 15: DIPOLE MAGNET; 16: PMD; 17: ZDC). In addition the position of the individual parts of the TRD pretrigger system are marked (FEB, CBA, CBB, CBC and PIM). This figure has been taken from [19].

**Inner Tracking System** The inner tracking system (ITS) is located around the interaction point. Its six cylindrical layers of silicon detectors are placed between 4 cm and 44 cm from the collision point. The middle two layers are silicon strip detectors surrounded by a two layers of silicon drift detectors. The two layers silicon pixel detectors close to the center provide a very high spatial resolution of approximately  $12\mu\text{m}$ . This enables identification of D and B mesons by their decay vertex. Low momentum particles (below 100 MeV/c) are coiled up in the ITS and can thus be identified by their energy loss.

**Time Projection Chamber** The time projection chamber (TPC) is the largest detector in ALICE. Its field cage covers the radial space from 85 cm to 250 cm from the interaction point and has a total length of 5m. It is filled with a  $Ne/CO_2$  gas mixture. The TPC measures the momentum of charged particles, their vertex as well as their identity by their specific energy loss while passing the gas. Charged particles going through the gas free electrons along the trajectory by ionization. Due to a high voltage (up to 100 kV) between the cathode in the middle of the TPC and the cathode wires close to the end caps the electrons drift towards the anode wires. The



anode wires are located between the cathode wires and the pads of readout electronics on the end caps of the field cage. The electrons from the primary ionization produce avalanches of electrons in the vicinity of the anode wires. These avalanches induce a charge at the readout pads. The electronics samples this charge 500 to 1000 times within the drift time of  $88\mu s$ . Thus it is possible to get up to 160 three dimensional points of each trajectory. Two dimensions from the charge position on the readout pad plane and one from the drift time.

A grid at an alternating potential in front of the cathode plane prevents the ions from the avalanches to drift back into the drift region and thus destroy the calibration of the TPC. The grid is held at a potential corresponding to its position in the field cage for a typical readout time of  $90\mu s$  after the L1 trigger decision.

Drift time and the whole calibration is sensitive to the environmental temperature therefore the surrounded temperature is kept constant within 0.1K. Turbulences as they might occur from hot spots in other detectors are avoided to get a good position resolution. To achieve these goals, water cooled thermal shielding is mounted between the TPC and the TRD.

Because of the large amount of data the TPC electronics has a limited trigger rate of 200 Hz in Pb + Pb collisions. Therefore L1 trigger detectors like the TRD are used to limit the number of readouts of the TPC to the events interesting to physics.

**Transition Radiation Detector** The transition radiation detector is positioned around the TPC and identifies electrons with  $p_T > 1GeV/c$ . In addition it provides a trigger signal within  $6.9\mu s$  after a collision occurs. The TRD is described in more detail in chapter 3.

**Time of Flight** The momentum of a particle is calculated according to the radius of its trajectory in a magnetic field. By knowing the velocity of the particle the mass can be calculated. Together with the T0 detector very close to the interaction point the TOF detector is able to measure the flight time of a particle from the interaction point to its barrel at 3.5m radial within an accuracy of  $70ps$ . TOF identifies particles where the ITS and the TPC are not sufficient any more. TOF consists of 18 supermodules equipped with multigap resistive plate chambers. The TOF detector also provides input signals to the TRD pretrigger to cover the mid rapidity.

**High Momentum Particle Identification Detector** Particles moving faster than the speed of light in a medium produce Cerenkov radiation. The high momentum particle identification detector (HMPID) uses this light in combination with the ring imaging Cerenkov counters (RICH) method to identify hadrons at  $p_T > 1GeV/c$ . The detector consists of multiwire chambers and a radiator. The radiator is filled with liquid perfluorohexane ( $C_6F_{14}$ ). The Cerenkov light as well as the penetrating particles are detected by pads covered with CsI, a photosensitive material.

**Photon Spectrometer** The photon spectrometer (PHOS) consists of 17920 lead-tungsten crystals ( $PbWO_4$ ) located at mid rapidity at the bottom of ALICE 4.6m away from the interaction point. It provides photon energy measurement with a high spatial and energetic resolution. PHOS identifies neutral mesons by their two photon decay. To achieve the best energy resolution the crystals are cooled down to 248K by hydrofluoroether.

**V0** The V0 system consists of two scintillator plates placed around the beam axis on each side of the interaction point. Each scintillator plate is segmented into 4 rings and 8 sectors. Each segment is read out via a optical fiber and a photo multiplier tube. It delivers an online centrality trigger based on a threshold for the deposited energy. In addition it rejects beam gas events by their asymmetric signature. The V0 has a main contribution to the TRD pretrigger.

**T0** T0 consists of 12 Cerenkov radiators on each side of the interaction point. They are placed around the beampipe at  $-3.3 < \eta < -2.9$  and  $4.5 < \eta < 5$ . Each radiator is read out via a photomultiplier. The system has a trigger efficiency of about 50% for  $pp$  collisions and up to 100% for A + A collisions. The overall time resolution of the detector and electronics is better than 50ps ( $\sigma$ ). The signal is used by TOF to determine the time of interaction. In addition a  $\Delta t$  measurement between both sides provides the position of the interaction with a precision of 1.5 cm online. Furthermore the detector provides its signals to the TRD Pretrigger.

The following detectors are located outside the magnet.

**Muon arm** The Muon arm consists of a muon tracker and a muon trigger. It is located at forward rapidity  $-4.0 < \eta < -2.5$  outside the L3 magnet. The muons ( $\mu^+$  and  $\mu^-$ ) are separated from hadronic particles and photons by the big front absorber composed of several materials. Between the tracker (cathode strip chambers) and the trigger, an ion wall suppresses background and low energy muons. The momentum and the charge of the muons are determined with the large dipole magnet ( $B = 0.68T$ ). The muon arm identifies quarkonia such as  $J/\Psi$ ,  $\Psi'$ ,  $\Upsilon$  and  $\Upsilon'$  in their muon decay channel. Thus the physics program is partly complementary to the electron identification and tracking with the ITS, TPC and TRD in the central barrel.

**Accorde** Accorde is a set of scintillators located on top of the L3 magnet. It serves as a trigger detector during cosmic runs.

**Zero degree calorimeter** The two zero degree calorimeters are hadronic calorimeters located 116m from the interaction point at 0 degree relative to the LHC beam axis in the ALICE experiment. Thus spectator neutrons and protons from peripheral collisions are detected. Due to the long distance to the central trigger processor to ALICE, these detectors do not contribute to first (L0) trigger decision.

## 2.3 ALICE Trigger

Heavy Ion experiments as they are planned in ALICE have two special characteristics. First they produce a large number of tracks thus a huge amount of data, second the huge majority of interesting events are very rare events (e.g. 1 out of  $10^5$  for the occurrence of  $J/\Psi$  in the di-electron channel). To filter out the interesting events and to store them an efficient online processing chain has been installed. The chain is divided into 4 levels. L0 up to L2 are processed in hardware L3 is done in a computer cluster. If all three levels accept a collision it is permanently stored.

**Central trigger processor** The CTP is responsible for the first three ALICE wide trigger decisions L0 (arrives  $1.6\mu s$  after the event at the FEE), L1 (arrives  $8.1\mu s$  after the event at the FEE) and L2 (arrives  $80\mu s$  after the event at the FEE). The CTP is located in the C side racks under the muon arm. It consists of a Busy board, three trigger input boards and three main CTP boards (one for L0, L1 and L2), and 6 output boards. L0,L1 and L2 input boards as well as a so called switch board. The L0 and L1 input boards forward the 24 trigger signals to the main CTP boards where the trigger decision is formed. To extend the number of L0 inputs the switch board fans out the L0 trigger inputs. The switch board can be controlled via software from the ALICE Control Room (ACR). It is possible to change the available triggers from run to run.

Each detector has its individual Local Trigger Unit (LTU). The LTU is a VME module that operate either in standalone or global mode. In global mode it receives the trigger signals from the CTP and forwards them via the TTC fibers to the detector. In addition it receives the busy signals and returns them to the CTP. In standalone mode the functionality from the detector side

of view is the same. But the CTP is replaced by an LTU internal CTP emulator that can be configured by the detector. This mode is useful for debugging as well as for standalone runs. More information is available from [47]. The 24 detectors are dynamically partitioned into 6 completely independent clusters [20] and assigned to a trigger class. A trigger class is a configuration for a cluster, giving the conditions for a trigger. The CTP supports up to 50 trigger classes. Several trigger classes can be assigned to one cluster. Thus it is possible to trigger on different events with different rates and different detectors included. This increases the flexibility and efficiency of the ALICE experiment. A past-future-protection reduces the number of pile-up events. Pile-up events are events with tracks from several interactions. At each trigger level the trigger process can be stopped by a veto if more than a programmable threshold of events appeared in a programmable time window before the corresponding trigger level [20]. This is especially important for the TPC ( $88\mu s$  drift time) and the SDD ( $260\mu s$  drift time) to be able to reconstruct the event in an offline and in the an HLT analyses. The rate of each L0 input is downscaled by a programmable factor to reduce the overall trigger rate. In addition the trigger rate is downscaled if the buffer of the DAQ is getting full. A rare event logic [20] inhibits certain clusters from downscaling if the buffers at the DAQ are getting full. Since cluster triggering on rare events are excluded from this suppressing, this technology improves the statistics for rare events.

**High Level Trigger (HLT)** The HLT is a cluster of 8000 CPU cores located close to the experiment. It has direct access to the data from all detectors without having to go through the DAQ. By this it provides a full event reconstruction, used for the reconstruction of invariant masses as well as jets among others. Based on this it forms the last trigger decision in the hierarchy, for the ALICE experiment. The data is forwarded to the DAQ either as a direct copy of the event or as some modified event. Thus compressions as well as first filters, rejecting data from certain events or certain regions, are possible to reduce the amount of data. Typical processing times are 2s for a  $D^0$  HLT trigger [21] with  $dn/d\eta = 6000$ . This includes cluster finding, track reconstruction, vertex finder and  $D^0$  trigger using data from ITS. During the processing the data is buffered in the HLT and after that forwarded to the DAQ, thus latency is not that important as long as enough buffer and bandwidth is available. Besides from triggering, the HLT provides also online monitoring for various detectors.

**The TRD Pretrigger** The TRD Pretrigger is a low latency trigger system especially designed for the TRD. It produces a wake up signal necessary for the detector front end electronics  $1.1\mu s$  before the L0 of the CTP. Thus the visible drift region in the TRD data is enlarged from  $1.3\mu s$  to  $2\mu s$ . It is computed independently from the CTP. This trigger is based on a crude decision made of signals from T0, V0 and TOF. To reduce the latency due to cable and fibers, this system is distributed in several places inside the magnet close to the interaction point.

### 3 Transition Radiation Detector

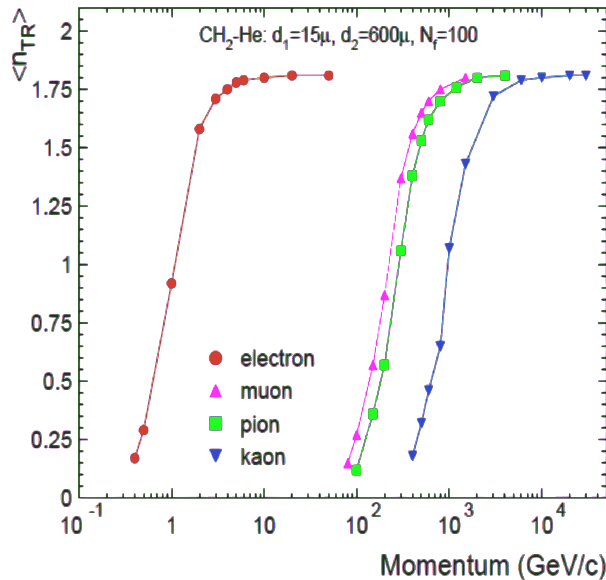
The Transition Radiation Detector (TRD) identifies electrons with high transverse momentum ( $p_T > 1\text{GeV}/c$ ). The electronic of the detector provides a fast trigger on electrons with  $p_T > 3\text{GeV}/c$  as well as a trigger on high  $p_T$  jets within  $6.9\mu\text{s}$  after the interaction.

#### 3.1 Detector Design

**Transition Radiation** Transition Radiation (TR) emerges when a charged particle passes the boundary between two media with different dielectric constants due to the changing electric field surrounding the particle. The integrated emitted energy per transition between a radiator medium and vacuum is [25]

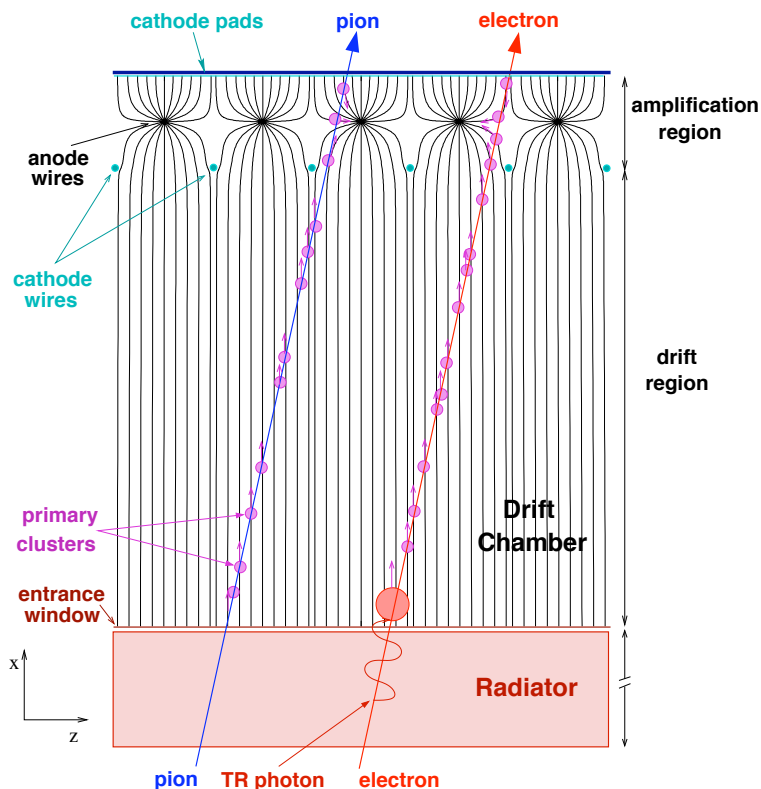
$$W_{TR} = \frac{1}{3}\alpha\omega_f\gamma$$

where  $\omega_f = 28.8\sqrt{\rho Z/A}\text{eV}$  is the plasma frequency of the material, with  $\alpha = 1/137$  the fine structure constant,  $Z$  the atomic number,  $A$  the atomic weight,  $\rho$  the density of the radiator. The characteristic of the particle crossing the detector is taken into account via its Lorentz factor  $\gamma = (1 - v^2/c^2)^{-0.5} = E/m$  where ( $\hbar = c = 1$ ). The emitted photons are well forward peaked within an angle of the order of  $1/\gamma$  and below the cutoff frequency  $\omega_c = \omega_f\gamma$ . For typical electron energies of 1 GeV to 10 GeV this results in soft X-Ray TR photons for polypropylene as detector material. Pions have a 273 times higher mass compared to electrons, such the  $\gamma$  is 273 times smaller for a given energy, making the TR of pions negligible. Due to the practical lack of a TR photon with a pion it can be distinguished from electrons with the same energy.



**Figure 3.1:** Transition Radiation. This figure shows the results of simulation for the number of produced transition radiation photons for electrons, pions and kaons at different momenta. The radiator corresponds to the radiator used in the ALICE TRD. Figure taken from [32].

**Functional Description** The TRD is sitting at mid rapidity between the TPC and the TOF barrel and covers a rapidity from  $|\eta| < 0.9$ . It is azimuthal divided into 18 supermodules. A supermodule consists of 5 stacks in longitudinal direction each divided in 6 chambers in radial direction. Each chamber is a multiwire - proportional chamber with 30mm drift and 7mm amplification region. The chambers have a width of 0.94 to 1.16 m and a length of 1.21 to 1.58 m. Drift- and amplification region are separated by a plane of wires, the cathode plane. Within the amplification region there is another plane of wires, the anode plane. The chamber is filled with a 85:15  $Xe/CO_2$  gas mixture. The gas volume is on the one side covered by a compound of Rohacell and polypropylene fiber mat and on the other side by a PCB with the  $6cm^2 - 7cm^2$  large readout pads. On top of this PCB a honeycomb structure covered by a carbon plate houses a part of the readout electronics. Figure 3.2 illustrates the functionality of the TRD. A charged



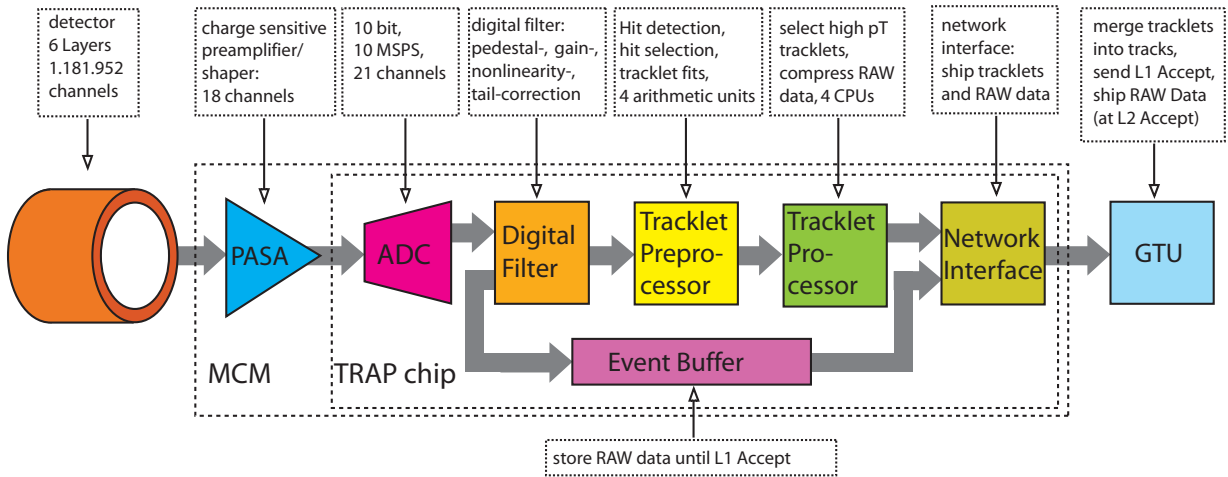
**Figure 3.2:** Principle of the ALICE TRD. The picture shows an intersection through a multi-wire proportional chamber of the ALICE TRD detector. Particles penetrating through the chamber produce primary electron clusters by ionizing the detector gas. The electron clusters drift along an electric field towards the anode wires where they produce avalanches of ions. These ions influence an electric charge in the read out electronics connected to the cathode pads. The appearance or absence of additional electron clusters caused by transition radiation photons emitted in the radiation by particles with  $\gamma > 1000$ , allows to distinguish between electrons and pions. The figure has been taken from [27].

particle coming from the interaction first penetrates the radiator. Only particles with a  $\gamma > 1000$ , typically electrons, will irradiate an X-ray photon in the direction of the particle momentum while passing the many transitions between polypropylene and air. The thickness of radiator is critical. On the one hand the probability to get a TR photon should be maximized on the other hand interference effects have to be kept low. Within the TRD a thickness of 4.8 cm has shown a maximum TR efficiency close to 100 %.

While passing the drift and amplification region the particle produces electron clusters by ionizing the detector gas. The TR X-ray photon is absorbed in the gas within the first centimeter after the radiator and thus produces additional electron clusters there. The cross section for

photons in gas is proportional to  $Z^4$  [26] therefore the expensive Xe noble gas with  $Z=54$  is used as detector gas. The electrons drift with a velocity of  $1.5 \frac{cm}{\mu s}$  with a typical electrical field between the entrance window (positive potential) and the cathode wires (ground potential) of  $0.7 \frac{kV}{cm}$  towards the anode wires (positive potential). The inhomogeneous electrical field between the cathode wires and anode wires accelerate the electrons. By further colliding with the gas atoms these electrons produce avalanches of electrons and positive ions around the anode wire. Thus a gas gain factor of  $5 \times 10^3 - 10^4$  is achieved [27]. The electrons are absorbed by the anode and the ions influence a charge at the cathode pads that is digitalized by the readout electronics. The Xe Ions are quenched by the  $CO_2$  fraction of the gas mixture. During the readout of one event mainly the avalanche ions in the vicinity of the anode wire accumulate, since the heavy ions have a low drift and diffusion velocity. Thus the quenching process is not that efficient. To compensate for this effect, the ion tail, an electronic filter called tail cancellation is applied in the read out electronics [29] [27] [28].

### 3.2 Readout Electronics

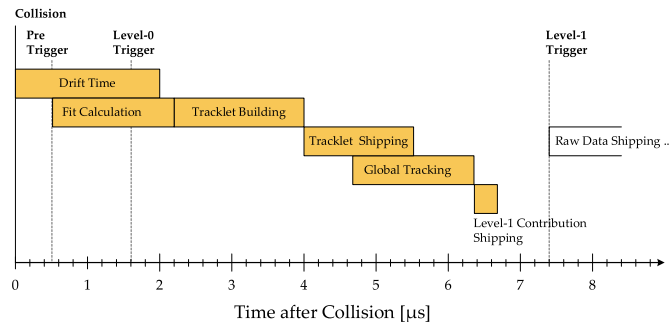


**Figure 3.3:** TRD readout chain. The Figure shows the readout chain of the TRD detector consisting out of the PASA, the TRAP Chip and the GTU. A multi wire proportional chamber influences charge into the PASA where it is amplified. The ADC in the TRAP chip digitalizes the signal. After signal filtering the tracklet (see text) is calculated and shipped to the GTU where the TRD L1 trigger contribution is generated. After a L1 accept from the ALICE trigger the ADC data is read out from a event buffer via the GTU. The PASA and the TRAP chip are combined in a MCM module. This figure has been taken from [33]

The read out electronics consists of two main parts. The Multi Chip Merger (MCM) located on the detector, it houses a preamplifier (PASA) as well as a digital part (TRAP chip) and the Global Tracking Unit (GTU) sitting in the C side racks (Fig. 3.3).

Each chamber is equipped with 6 to 8 readoutboards with each 17 to 18 MCMs making it possible to read out the 1.156 Million channels of the TRD detector. The signal from the pads is first amplified and shaped by the PASA and afterwards digitalized and processed in the TRAP chip. The TRAP chip compensates for several signal characteristics and builds the so called tracklets. A tracklet is basically a set of parameters, like slope, position and total charge, describing the trajectory of a particle in a chamber. A part of the tracklet calculation (Fit Calculation) is already done during the read out of the TRD [27]. The tracklets of a half chamber are collected and shipped via the ORI board and optical fibers to the GTU. After a L1 trigger the ADC values describing the detector signal are shipped to the GTU and afterwards forwarded to the ALICE Data Acquisition (DAQ) and the High Level Trigger (HLT).

Each chamber has a DCS board, a small linux pc, (Chapter 7.1) which monitors and configures the MCM via an ethernet connection to the control pc. In addition it receives the trigger and clock informations from the pretrigger system and distributes them to the MCM of each chamber.



**Figure 3.4:** Timing of the TRD readout chain. The figure shows the time budget of the individual steps necessary for a L1 trigger contribution of the TRD as well as the timing of the individual trigger levels. This is an updated figure adapted from [33]

To reduce the power consumption and thus the thermal heat the TRD detector is set into a standby mode in between the individual collisions. Furthermore the buffers in the filter stage of the Front End Electronics as shown in Chap. 3.2 are reduced as much as possible to keep the noise, heat and latency in the system to a absolute minimum. The noise disturbs the analog digital converters of the TRD electronics, the heat the TPC callibration and any latency introduced in this stage decreases the time for the L1 decision in the GTU. Depending on the adjustable delay of the filter stage the maximum latency of this stage is  $500ns$  to  $900ns$  [31].

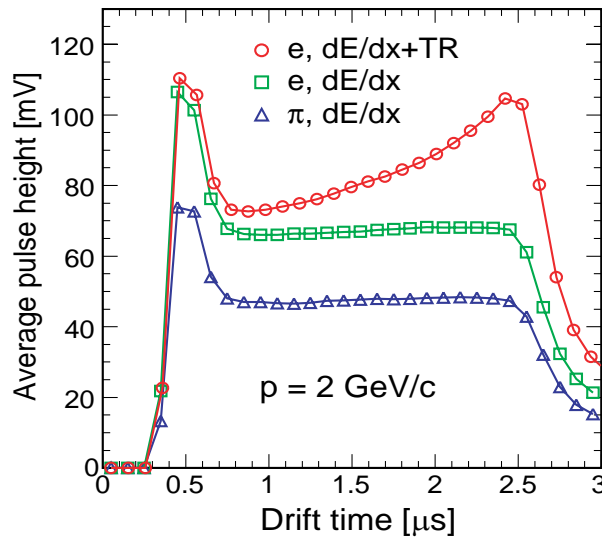
Figure 3.4 illustrates the timing of the TRD readout chain. The cathode pads of the TRD are continuously read out. Independent from any trigger the charge is amplified in the PASA, digitalized in the ADC and filtered in the Digital Filter (Fig. 3.3). From the point when the pretrigger signal arrives at the MCM  $500ns$  after the collision the data from the output of the digital filter is sequentially stored into the event buffer. In parallel to the read out of the TRD detector during the drift time and the storage of the raw data in the event buffer the Tracklet Preprocessor performs the fit calculations, like the accumulation of the charge or the determination of the slope, for the tracklet [27]. To reduce the noise on the ADC and the PASA the tracklet preprocessor is running at 10 Mhz. If a L0 trigger arrives at the MCMs within this period the TRAP chip proceeds, otherwise it stops after the fit calculations. After the drift time of the TRD the data is written into the event buffer and processed by the tracklet preprocessor until the pipeline consisting of ADC and digital filter is emptied. Afterwards the TRAP chip switches to 120 Mhz and evaluates the tracklet parameters for tracklets with high momenta or according to another programmable algorithm with the help of 4 CPUs. The evaluated tracklets are sent to the GTU. The GTU receives the tracklets of the whole TRD and matches together the tracklets(Global Tracking) from the individual chambers and calculates the TRD L1 trigger decision. Several trigger conditions can be requested. The total charge mode requires a minimum number of collected charge in a stack. This mode is used to purify the TOF trigger during cosmic data taking. Jets are selected by requesting a high momentum particle. Heavy particles decaying into  $e^+$  and  $e^-$  are selected by requesting two opposite tracks with a pulse height distribution identifying an electron and a total momentum roughly equivalent to the invariant mass of the heavy particle. The L1 trigger contribution is sent to the CTP  $6.9\mu s$  after the event. As soon as the MCMs get the L1 signal from the CTP they send the buffered raw data of the event via the same fibers like the tracklets to the GTU from where they are shipped to the ALICE DAQ and the HLT.

As established above only the electron clusters arriving at the event buffer after the pretrigger

signal are stored into the datastream. Thus any data, that has been amplified by the PASA more than the latency time of the ADC and the digital filter (typically 900 ns) before the pretrigger signal, are not stored into the data stream.

### 3.3 Particle Identification

Figure 3.5 shows a typical pulse height distribution, averaged over several particles. The curves have been recorded during a test beam where the electrons and pions have been separated by a Cerenkov and lead glass detector (Chapter J). The spectra consist of two or three parts. The first peak at around  $0.6\mu\text{s}$  is the amplification region of the pulse spectra. It is caused by the ionization of the penetrating particle in the amplification region between the cathode wires and the cathode pads. It is caused by electrons drifting from both sides towards the anode wire. The drift region of the pulse height spectra is the time ( $0.8\mu\text{s}$  to  $2.5\mu\text{s}$ ) when the electron clusters from the drift region are detected by the cathode pads. The exponential decay of the signal after the end of the drift time is an effect of the ion tail (Chapter 3.1). The electron clusters produced by the TR photons add up to the TR peak at  $2.5\mu\text{s}$ . The red curve shows the pulse height distribution for electrons including the TR peak. The green curve represents the energy loss of an electron without transition radiation. The blue curve is the energy loss of a pion. All signals are for  $p = 2\text{ GeV}/c$ . Within the TRD currently three methods are applied for the particle ID.



**Figure 3.5:** Electron and Pion separation in the TRD. The plot shows averaged pulse height spectra of electrons and pions penetrating the TRD detector. In addition to the energy deposit by ionization according to the Bethe-Bloch formular (green line) electrons produce ionization by the transition radiation photon. This plot has been taken from [27]

**The LQ Method** According to the Bethe Bloch formular the electrons have a larger over all energy loss than pions of the same momentum. In addition the electrons deposit the energy of the TR in the detector. By integrating the pulse height distribution over time the probability of being an electron or pion can be calculated. If 90 percent of the electrons should be correctly identified as electrons and all six layers of the detector are evaluated this method identifies 1 in 100 pions as electron [30].



**The LQX Method** The LQX Method is an extension to the LQ Method. It uses in addition to the total amount of energy also the position in the detector where the maximum energy has been deposited. In the pulse height spectra this corresponds to the timebin with the highest signal. For electrons this will most probably be near to the end of the drifttime whereas for pions the peak appears equally distributed over all timebins. The performance of this method is 15% to 30% better than the LQ method [30].

**Neural Networks** None of the methods described above takes the full information of the TRD signal into account that is the cluster distribution over the whole detector and not only the sum of it. In addition several other effects like overlapping charge clusters from two tracks are not taken into account. To take these effects into account a neural network approach is available [30]. A neural network is a piece of software that is trained with known samples, that is with pulse height distributions that are known to come from electrons or pions. The samples are fed into the system and the software will get a feedback according to whether its decision was right or wrong. These identified pulse height spectra are either extracted from detailed Monte Carlo simulations or real data with tagged particles (Chapter J). Within this phase the network adjusts its internal parameters. After the training phase the network will be able to correctly recognise samples to origin from electrons or pions with a certain probability. [30] has shown that this method misidentifies only 1 in 700 pions as electrons, given 6 layers and 90% electron efficiency. This method is only available in offline analyses and requires higher computing performance.

## 4 TRD Pretrigger

The TRD requires a wakeup signal at latest  $700ns$  after the interaction to achieve the full trigger, tracking and particle identification performance. The TRD pretrigger provides this wake up signal. In addition it performs a part of the trigger processing, that is blocking, forwarding, merging and reformatting of the trigger signals intended for for the TRD. In this chapter the pretrigger is presented within its functional context.

In the first section is described how the pretrigger signal influences the performance of the TRD detector. In the second section the technical requirements for the operation of the pretrigger system in the ALICE experiment are analyzed and documented. The third section presents the lookup table concept used to form the pretrigger decision. The last section shows how this concept is used to optimize the pretrigger signal for different types of collisions.

### 4.1 Motivation

The front end electronics of the TRD (chap. 3) can only record electron clusters from the gas volume, that arrive not earlier than  $900ns$  before the first trigger signal. The Alice Central Trigger Processor sends its L0 trigger  $1.1\mu s$  seconds after the event. After an additional  $450 ns$ , because of delays in fibers and cables, it arrives at the Front End Electronics (FEE) of the TRD. As described in chapter 3 the TRD has only a buffer of  $900ns$ . Using the L0 from the CTP and the full buffer of the TRAP chip would result in a pulse height spectrum without an amplification region, the first timebins of the drift-region and the starting point, indicating the time when the first electron cluster from the particle arrives at the anode wire ( $0.3\mu s$  in Fig. 3.5). As shown below these characteristics are essential to achieve the design specification of the TRD [27].

**Full Drift Region** The pretrigger signal extends the visible drift region in the TRD data from  $1.3\mu s$  to  $2\mu s$  at nominal drift voltage (Figure 8.4(a)). The enlarged trajectory of each particle makes the tracking more efficient, since the trajectories are better separated from clusters caused by noise. The exact curvature of a trajectory is calculated in offline analyses by a stochastic Kalman-filtering approach [27]. This fit is more precise the more points of a trajectory are available in the 3 dimensional space. Thus the momentum resolution in offline analyses is increased.

A lower drift voltage in the TRD is not an alternative to a pretrigger signal for recording a longer drift region. This would delay the calculation of a TRD L1 trigger decision. The TPC starts to read out its drift region after a L1 accept signal. Increasing the time interval between the event and the L1 decision would result in an effectively shorter active TPC volume.

**Calibration** The momentum and position resolution depends mainly on two factors. The accuracy of the position in the cathode pad plane (z-y accuracy) and the accuracy in the drift dimension perpendicular to it (x accuracy). The z-y accuracy is given by how precisely the charge is located on the readout pads by the MCMs. This accuracy gets worse with increasing drift time because of the ion tail as described in chap. 3. The TRAP can compensates for that by a continuous convolution of the ADC values with a correction function. For an offline tail cancellation the starting point of the pulse height spectra must be seen since otherwise no ion tail charge from the past is visible. The y-accuracy depends on a precise calibration of the drift velocity of the

ions. This is only possible if all ionization clusters from one particle trajectory are available. The pretrigger ensures that also the amplification region is seen. The calibration is explained in [29]. drift dimension is determined by drift velocity.

**TRD L1 Trigger Decision** One of the strength of the TRD is the capability to trigger on high  $p_T$  electrons. Of special interest is a  $J/\Psi$  and  $\Upsilon$  trigger (chap. 1). One of the decay channels is the di-electron channel. For this the tracking capabilities of the TRD and the electron identification are combined. As described above the pretrigger improves the tracking as well as the particle identification.

**Particle Identification** For offline analysis there are three established methods to identify a particle. LQ and LQX as well as approaches with neuronal networks. The different methods are briefly described in chap. 3. All these methods depend on the measurement of the energy deposit of a particle trajectory in the detector relative to the baseline. The LHC is able to provide a Pb + Pb collision every 100ns. At this rate the baseline drifts because of the ion tail with decay times of  $\tau_{short} = 0.1\mu s$  and  $\tau_{long} = 0.93\mu s$  [29]. This offset in the energy deposit of a previous triggered or not triggered events is reconstructed with the baseline indicated by the presamples before the signal of a particle trajectory (0 to 300ns in fig. 3.5). Depending on the multiplicity of an event two or more trajectories of particles lay that close to each other that they cannot be distinguished by the TRD readout electronics. The TRD TDR [27] calculates 10% overlap clusters at  $\frac{dn}{d\eta} = 500$  and 45% overlap clusters at  $\frac{dn}{d\eta} = 8000$ . The particle identification using neural networks taking the amplification region and the full drift region into account performs well under these conditions [38]. A neural network might recognize overlapping tracks by analyzing the amplification region. The TR peak of an electron might be detected by the comparisons of the pulse height in the first time bins of the drift region, where for sure no electron clusters from transition radiation are detected, to the pulse height at the end of the drift time [28].

The online particle identification for a L1 contribution of the TRD is based on the LQ as well as the LQX algorithm. The thresholds are applied in the GTU. Both methods depend on the energy deposit that is charge in the pulse height spectra in the detector. By taking the amplification region into account the total charge is larger making the statistical error smaller. This improves the quality of the particle identification for a L1 trigger

Both the amplification region and the first timebins of the drift region are only visible with a pretrigger signal.

## 4.2 Requirements

**Wake Up Signal Generation** The pretrigger sends a wake up signal (pretrigger signal) for all kinds of ALICE events, including also cosmic and ultra peripheral events, to the TRD 500ns after an event. This signal is as pure and efficient as possible (chap. A.1) to enrich the fraction of events where the TRD is taking data with a fully visible drift region (see chapter 4.1).

**Connection to the ALICE Wide Trigger** The pretrigger system has an L0 trigger input to the ALICE wide trigger (CTP). According to the CTP configuration this input is used as inverse veto in the TRD partition. Thus the detectors in the TRD partition, only receive an L0 trigger if the TRD is able to analyze the event for a L1 accept or reject. By this the maximum L0 bandwidth of these detectors is not unnecessarily narrowed. The pretrigger system has actually two inputs to the CTP. One for the pretrigger signal, the other one for a real L0 contribution of the pretrigger system based on information from V0,T0 and TOF. This information is different to

the information provided by the front end electronics of these detectors to the CTP [39] [40]. Therefore this L0 contribution may extend the trigger possibilities of ALICE.

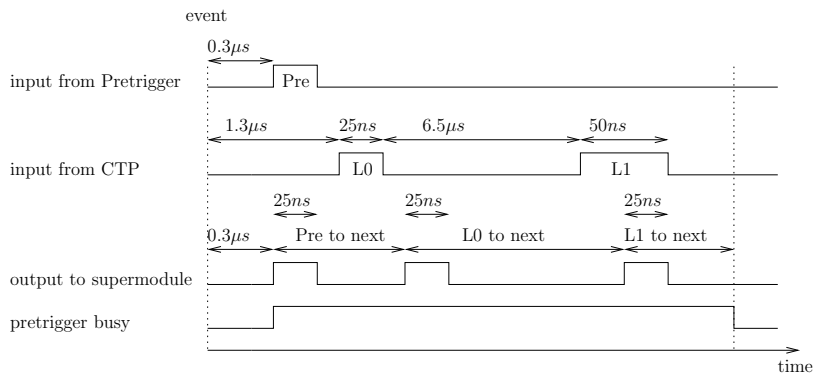
**Fail-Proof Design** The Pretrigger decision is formed by 13 primary plus 13 backup Spartan3 FPGAs. In addition it has a Virtex4 FPGA for the TOF connection as well as a Spartan3 FPGA for the CTP connection. The FPGAs are located inside the L3 magnet to reduce latency caused by long trigger cables. The location inside the magnet and close to the interaction point requires radiation and B-field proof hardware. Therefore the old and thus robust Spartan technology with its limitations has been chosen wherever possible. This technology has shown in tests of the T0 and V0 collaboration to be able to perform well under these conditions [32]. Since the System is essential for the operation of the TRD the critical parts have been designed redundantly. That is as a main and a backup system. The TOF signals are processed by a Virtex4 FPGA since no Spartan3 FPGA with enough IO pins is available. The Virtex family is not that radiation proof as the Spartan3 [33]. Therefore the system has to be operational without this FPGA. To achieve the required latency, the connection between the different components has been established using LVDS signals as well as optical fibers. Normal LVTTTL are not able to send signals with that high frequency over distances (3m to 15m) as it is required for the pretrigger system. In addition LVTTTL is not that noise resistant.

**Easy Configuration for Offline Tuning and Special Experimental Conditions.** The configuration of the pretrigger system consists of a set of numerical parameters for thresholds and lookuptable values that fully describe the trigger logic of the system. The hard coded logic is reduced to a minimum. Within Aliroot [34], the software simulation of ALICE, the pretrigger configuration can be optimized towards best purity and efficiency, using the largest possible parameter space determined by the pretrigger and detector hardware. The obtained configuration is uploaded afterwards to the hardware and used for real runs. By using a simulation approach as described above to find the pretrigger configuration the configuration can take conversation and absorption as well as detector specific response behaviour into account. An algorithm based on Darwin's idea of evolution to automatically optimize any configuration towards a CTP trigger configuration has been presented [35]. A similar idea is already realized within the configuration of FPGA and FPTAs [36]. The pretrigger is optimized within a run to react on different experimental conditions.

**Calibration and Monitoring Tools** The purity and efficiency of the pretrigger and its configuration towards the L0 of the CTP is directly measured in the pretrigger system. Additional counter to monitor the trigger activity for quality assurance as well as for the debugging of the interplay with the various trigger systems in ALICE. The quality of the pretrigger configuration is analyzed in depth by programmable counters searching for different trigger conditions (Chap. 6). The System is synchronized internally as well as in respect to the LHC collisions with rate measurement tools and timing analyzers (Chap. 7.3). The synchronization procedure is described in detail in Chap. E.

**Trigger Processing** The MCMs of the supermodule require a programmable but fixed timing of the Pre, L0, L1 sequence (Fig. 4.1). The timing of the MCMs is uploaded during the supermodule configuration at the start of a run [45]. Ideally the pretrigger system forms a trigger decision 300ns after the event and sends afterwards a L0 and L1 pulse to the TRD in the correct timing if the corresponding L0 and L1 is received from the CTP. The L1 pulse from the CTP is for historical reasons 50ns instead of 25ns wide. The trigger processing logic has to shrink this pulse to 25ns since a 50ns pulse is a reset for the supermodule [45]. All pretrigger pulses within the pretrigger

busy time (see 4.1) are not forwarded to the supermodule. Otherwise the MCMs go into an undefined state and must be reconfigured. For some L0 trigger the pretrigger is not able to provide a pretrigger. Not all L0 trigger detectors of ALICE are used for the pretrigger decision (Pre) since their latency is beyond  $150ns$ . In this case the L0 of the CTP is used as Pre and reused after the Pre\_to\_next time as L0, if the pretrigger system is set into the emergency mode (set register L0 as Pre en). Time critical commands for the MCMs like a synchronous reset are generated in the pretrigger and forwarded via the trigger fibers to the MCMs. The commands are described in [45]. The trigger processing is described in more detail in (chap. 6.3).



**Figure 4.1:** Processing of the CTP trigger signal in the Pretrigger

**Event by Event Monitoring** The pretrigger writes data related to the formation of the trigger decision for an event into the DAQ data stream. This data is used for offline analysis of the event [37] as well as for optimization of the pretrigger configuration. Trigger classes ( Chap. 4.3) leading to rejected events are removed from the lookuptables. Data from the CBA, CBC and CBB level (fig. 4.2) are recorded. This feature is intended for a later update.

### 4.3 Concept

To achieve all requirements the design of the hardware was strictly driven to achieve minimal latency and maximal possible flexibility. The latency requirements dictates the detectors as well as the topological structure of the hardware. Only the TOF, V0 and T0 detector provides a signal within  $150ns$  after the event. The trigger decision is formed by a set of consecutive lookuptables with trigger classes.

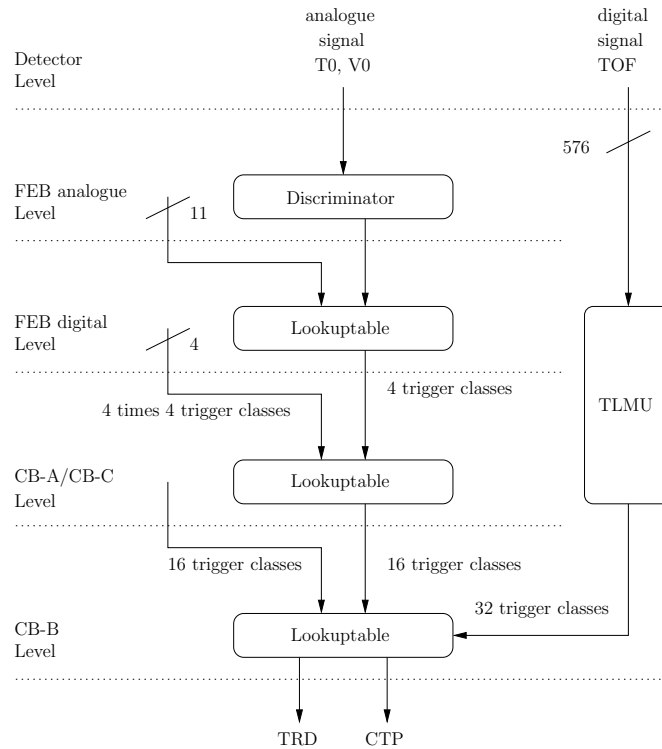
A lookup table implements any logic that can be formed out of its inputs. Every input configuration is available as an address of a memory. The stored information of an address defines the trigger class of an input configuration. (for an example see tab. 7.1). This trigger class, encoded in a number of bits, is the output of the lookuptable. Figure 4.2 illustrates how this concept of

input configuration	000	001	010	011	100	101	110	111
output trigger class	00	01	01	10	01	10	10	10

**Table 4.1:** LUT configuration implementing a minimum bias trigger requesting more than 1 hit in trigger class 1 and a minimum bias trigger requesting at least 1 hit in trigger class 2

lookuptables is implemented in the pretrigger. Each analogue signal (detector level) from a PMT from T0 or V0 is first discriminated (FEB analogue level). According to a programmable threshold a digital high or low is forwarded to a lookuptable (FEB digital level). This lookuptable assigns

the input of 8(V0 detector) or 12(T0 detector) discriminated channels into one out of four trigger classes. Five of the trigger classes of the FEB digital level are assigned to one out of 16 trigger classes by the lookuptable in the CBC alternatively CBA level. Parallel to the FEB digital and the CBA/CBC level the TLMU assigns 1 out of 32 trigger classes to the 576 digital input channels from TOF detector. The final trigger decision is formed in the CBB level. For a configurable set of trigger class configurations from the CBC level the CBA level as well as from TLMU a trigger is issued to the TRD alternatively the CTP. The trigger classes extend the possibilities to achieve



**Figure 4.2:** Processing of the CTP trigger signal in the Pretrigger. The pretrigger decision is formed on several levels. 88 analogue signals from the PMTs of V0 and T0 are discriminated. 12 lookuptables combine 8 to 12 detector inputs each to one out of four trigger classes in the FEB digital level. Two times 5 FEB trigger classes are combined to one out of 16 trigger classes from the CBA respectively CBC level. The lookuptable on the CBB level produces a pretrigger decision out of CBC, CBA and TOF information. This decision is forwarded to the TRD as well as to the CTP.

an efficient and pure pretrigger. The trigger decision in a level is not only based on a binary trigger decision in the preceding level but also on its characteristic encoded in the trigger classes.

## 4.4 Configurations

The pretrigger detects several characteristics of an event to enrich the efficiency and purity of the pretrigger signal compared to the L0 from the CTP and the physics events.

The overall TRD performance increases with the pretrigger efficiency as established in chap. 4.1. The pretrigger efficiency has also impact on the TRD L1 efficiency, since the tracklets (especially the charge parameter) calculated by the MCMs (Chapter 3.2) depend largely on the number of captured time bins of the drift region. So far only one set of thresholds is applied to the tracklets in the GTU for a L1 trigger decision. This is either optimized for tracklets taken with pretrigger or for signals without pretrigger.

The pretrigger signal has to be as pure as possible for the following reasons.

- Every pretrigger starts the fitsum calculation on the TRAP chip (Chapter 3.2) causing heat production of the MCMs. The TRD cooling system removes 50kW of heat. This might be exceeded by the MCM power consumption when operating continuously. The irradiated thermal power causes convection in the close to the TRD located TPC and thus decreases the spacial resolution of the TPC.
- The maximum pretrigger rate, that can be handled by the MCMs is limited to 300 kHz [28].
- Each pretrigger causes a TRD deadtime of about  $0.6\mu s$ . Events occurring in this time are not recorded by the TRD. Thus the efficiency is decreased.

The pretrigger signal is generated and purified by similar methods as they are used in the CTP. Technically these methods cannot be implemented in the same way as it is done by the detectors front end electronics for the L0 decision in the CTP because of hardware and timing limitations in the pretrigger system. In addition more detectors are available for an L0 decision in the CTP because of the larger latency of the L0 compared to the pretrigger signal. Nevertheless some approximate event analyses is possible.

**Minimum Bias Trigger** The most basic configuration sends a pretrigger as soon as the number of V0 and T0 segments firing within a collision exceeds a threshold. This trigger is implemented by the following lookuptable configuration. The FEBs categorize the number of firing detector segments into one out of four trigger classes (compare fig. 7.1) and report it to the lookuptable on the CBA/CBC level. The trigger classes from the FEBs are summed up in the CBA/CBC lookuptable and a trigger class corresponding to the total multiplicity of one side is reported to the CBB lookuptable. The CBB lookuptable fires a pretrigger if the sum of reported hits from CBA and CBC exceed a threshold.

**Centrality Trigger** Within heavy ion collisions the number of produced particles increases with the number of participating nucleons. Thus central collision, that is collisions with a small impact parameter, produce a higher number of particles than collisions with a larger impact parameter. For triggering on events with a certain impact parameter the total deposited charge in the V0 detector of an event has to be within a certain margin, since every charged particle crossing the V0 detector deposits energy into the scintillator. The pretrigger system is not able to integrate the analogue signals from the PMTs and has thus no direct information about the amount of energy deposited in the V0 detector. An approximation of the total charge of an event is given by the number of firing V0 sectors in combination with the height of the thresholds. A deviation of the coherence between multiplicity and impact parameter is given in App. A.3. The plot rate of events with the similar total multiplicity versus the total multiplicity (in arbitrary units) is measured by counting the events within a certain multiplicity class or obtained via simulations in Aliroot. With this plot the impact parameter of a multiplicity class is estimated (App. A.3).

**Rejection of Beam-gas Events** Beam-gas events are suppressed by tworequirements.

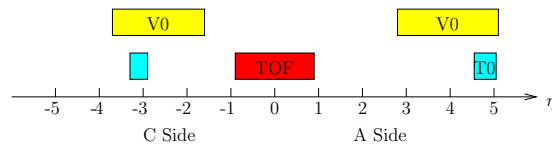
- Asymmetric event in V0
- Non coincident signals in the A and C side

Asymmetric events are detected in the CBC and CBA as well as in the CBB by the following lookuptable configuration. Each FEB categorizes an event in 2 multiplicity classes. If more than one FEB sends a different multiplicity class a no-trigger class is sent to the CBB otherwise a trigger class corresponding to the overall multiplicity of one side (A or C) is sent to the CBB.

The lookuptable of the CBB rejects the event if the multiplicity classes reported from CBC and CBA are not the same. Non coincident signals from CBC and CBA are rejected by the same mechanism in the lookuptable of the CBB.

**Rapidity Distribution Trigger** The multiplicity distribution in rapidity of an event is a signal for the underlying physics and is therefore used as trigger signature. Especially diffractive physics events as well as events where a QGP is generated have a characteristic multiplicity versus rapidity distribution. Figure 4.3 illustrates the rapidity coverage of the different detectors. A configuration of the CBB lookuptable requesting trigger classes with high multiplicity from CBC and CBA and low multiplicity classes from TLMU is sensitive for diffractive events (Chap. 1). Selecting events with similar multiplicity classes from TLMU and CBC and CBA triggers for events with a flat multiplicity versus rapidity distribution. This is a general signature for nuclear collisions with a large number of participants [22] [23]. Special triggers for ultra peripheral interactions [24]. request zero multiplicity on one side ( $1 < \eta < 5$  or  $-5 < \eta < -1$ ) and multiplicity unequal zero on the opposite site ( $-5 < \eta < -1$  or  $1 < \eta < 5$ ). This condition is matched by requesting a low multiplicity class from CBA and a high multiplicity class from CBC and vice versa.

Some of the trigger signatures can be reasonably combined by uploading the set union of two lookuptable configurations into the corresponding lookuptable.



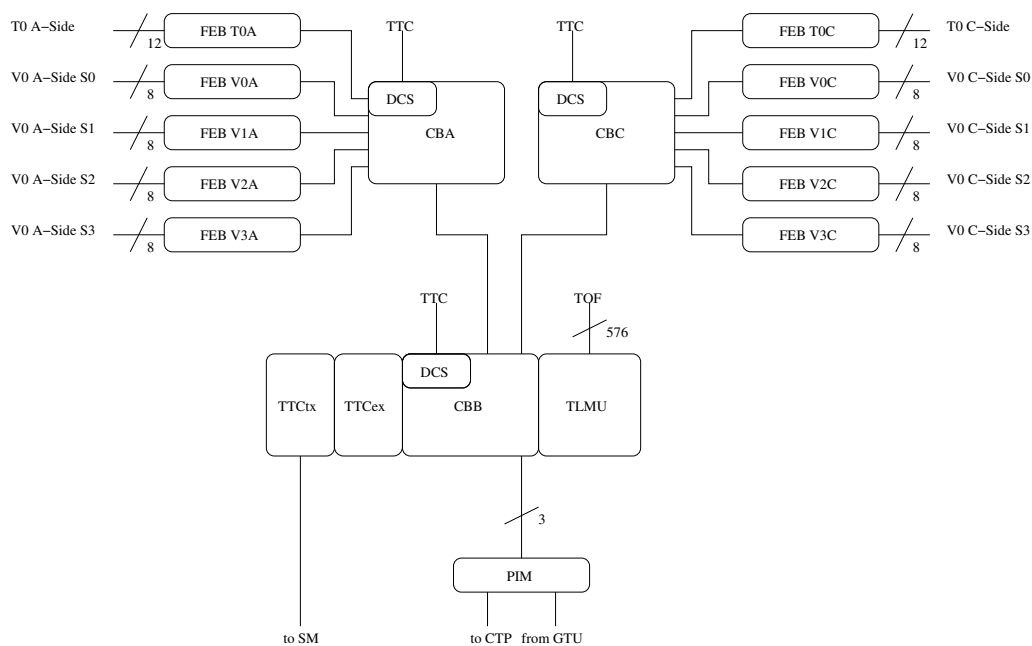
**Figure 4.3:** Pretrigger Detectors. Detectors connected to the pretrigger signal and their rapidity coverage.



# 5 Infrastructure Installation

## 5.1 Hardware

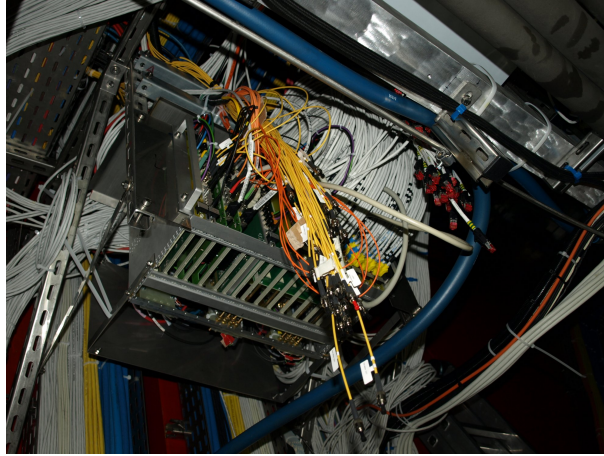
The Hardware of the pretrigger system consists of the following main parts.



**Figure 5.1:** Overview over CheshireCat the TRD pretrigger system. It shows the main parts and the connections used to generate the pretrigger decision.

- 3 Control Boxes (CBA, CBB, CBC)
- 10 Front End Boxes (FEBs)
- 1 Pretrigger Interface Module (PIM)

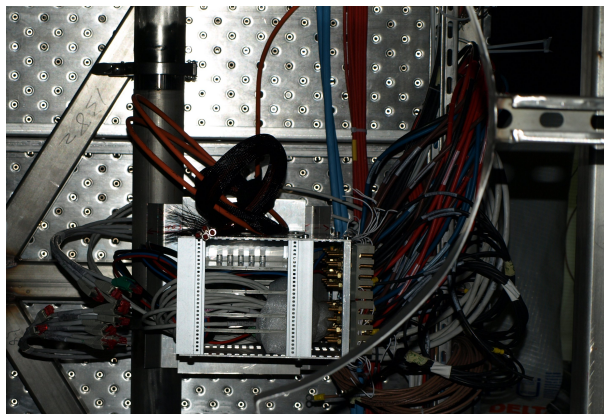
The CBB is the center of the system (Fig. 5.1). It is located in the L3 magnet at the outer most C side 3m under the beampipe. It receives inputs from CTP (via TTC), GTU (via PIM), CBA, CBB, CBC and the TOF and has outputs to the TRD as well as to the CTP. The CBA as well as the CBC receive inputs from five FEBs and have each one output to the CBB. The inputs from the detectors are first processed in the FEBs. The pretrigger is very critical for the operation of the TRD. Therefore all subcomponents except for the PIM and TLMU are redundant. If the primary system breaks the full functionality is taken over by the backup system. The TLMU part as well as the PIM part can operate with both systems. The connections between the main parts are done via optical multimode fibers or standard CAT6 Ethernet cables. CBA is located under the gangway of the miniframe in front of the V0 detector (pic. 6.5). CBC is on top of the muon absorber inside the L3 magnet. The PIM sits in a VME crate in the C-Side racks under the muon arm (Pic. 5.5). The CBB houses the following parts:



**Figure 5.2:** The CBB housing the TLMU and the CCUB. It is located below the C side of sector 12 in the magnet. The patch panel for the low voltage of the pretrigger systems on the C side is mounted in the back of the CBB.

- 2 CheshireCat Units (CCUB primary, CCUB backup)
- 1 TOF Logic Multiplicity Unit (TLMU)
- 2 TTCvi (TTCvi primary, TTCvi backup)
- 2 TTCex (TTCex primary, TTCex backup)
- 3 low voltage patch panels

The CCUB (Pic. G.1) is controlled and programmed by a DCS board (Chapter 7.1) via the scsn and jtag protocol. The scsn protocol is a serial communication used to configure the registers in the FPGA. The jtag is used to upload the firmware into the FPGAs. Logic related to the pretrigger decision is running on the CCUB-FPGA and the TLMU. The CCUB-FPGA interfaces the other parts of the pretrigger via the Motherboard or the adapter card. CCUB and TLMU are connected with a SCSI II cable via the adapter card. The TTCvi converts the ECL signals from the CCUB into the TTC protocol and distributes it via single mode fibers to the TRD. The TTCex is connected to the TTCvi and extends its number of optical outputs. The CBA (Pic. 5.3)

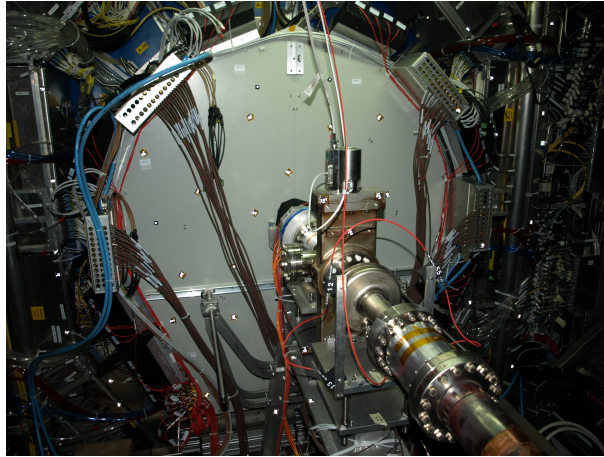


**Figure 5.3:** The CBA housing the CCUA. The patch panel for the low voltage of the pretrigger system on the A side is mounted in the back of the CB-A. The same box without a patch panel is mounted on top of the muon absorber on the C side.

as well as the CBC consist of:

- 2 CheshireCat Units (CCUA primary, CCUA backup for CBA and CCUC primary, CCUC backup for CBC)
- 2 low voltage patch panel (only CBA)

The CCUA and CCUC (Pic. G.1) are based on the same hardware than the CCUB, but with a different adapter card (Schematics [75]). The CCUA and CCUC have interfaces to the FEBs for trigger and SCSN. The FPGAs of the FEBs are programmed via a jtag chain (Schematics H.2) starting from the DCS board of the CCUA and CCUC. Each FEB (pic. 5.4) is built out of:



**Figure 5.4:** 4 FEBs for the V0 detector at the A side located around the beam pipe. All FEBs are built in the same way. The 4 FEBs for V0 C side are located around the muon absorber. The FEB for T0 on the C side is mounted on top of the muon absorber inside the magnet. The FEB for T0 on the A side is mounted below the beam pipe.

- 8 (V0) or 12 (T0) preamplifier cards
- 1 Front End Box Unit (FEBU) consisting out of a primary and a backup unit.

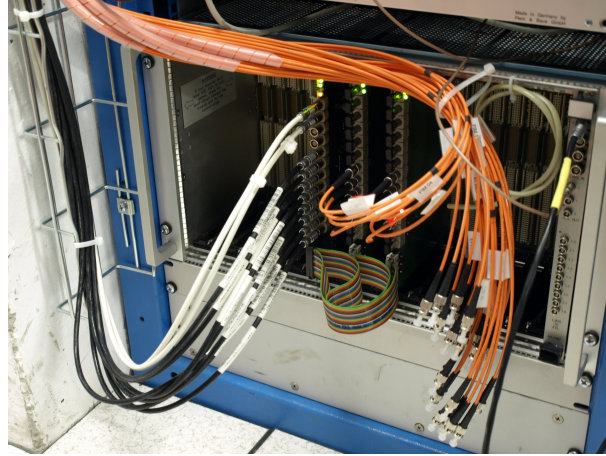
The preamplifiers are mounted on the main FEBU (Pic. G.2). They receive the analog signals from each PMT and forward the original as well as a 5 times amplified analog signals to the front end electronics of the detectors. The PIM (Pic. 5.5) consists out of the following hardware

- 2 Pretrigger Interface Optical Modules (PIMOPT primary/backup).
- 1 Pretrigger Interface FPGA Module (PIMFPGA).

Each PIMOPT connects to CBA, CBB and CBC with four multimode fibers. Three fiber in direction from the Control Box to the PIM for trigger respectively data transmission, one from the PIM module to the Control Box for busy transmission. The PIMFPGA has a connection to PIMOPT primary and PIMOPT backup via a ribbon cable. It also sends up to 8 trigger contributions (2008 two are used) to the CTP and receives two busy signals (a primary and a backup) from the GTU.

For more detail about the exact infrastructure see chapter H. For schematics of the board see chapter H and online documentation [75].

The main parts are powered by four Wiener power supplies [42] (ALIDCSWIE 093, ALIDCSWIE 094, ALIDCSWIE 095, ALIDCSWIE 096) with each 1 to 4 equipped channels (see H). The low voltage power is distributed to the individual pretrigger boxes at a patch panel behind the CBB and the CBA box. So far all FEBs of one detector at one side are connected together.



**Figure 5.5:** The PIM module in the VME crate in the C side racks under the muon arm. The orange fibers are the connection to the CBs. The two white LVDS cables are connected to the GTU busy. The black LVDS cables connect the TRD pretrigger system to the CTP of the ALICE experiment.

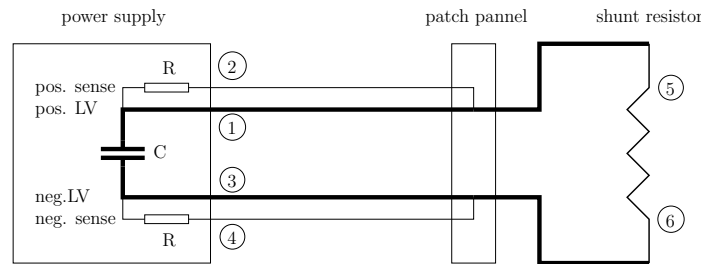
The primary and backup system of each FEB are connected to the same power line. The power line is split in front of the FEB into two connectors via a Y adapter. The ground of the V0 and T0 detector are connected together via the pretrigger system. If this influences any noise in T0 or V0 the FEBs are powered individually. In this case the non-equipped channels of the Wiener power supplies have to be equipped and the bridges at the CBA and CBB patch panel must be removed.

## 5.2 Tools

The following tools and methods have been used to test and install the pretrigger infrastructure as well as the TRD low voltage cables. By this the crimped and pulled cables as well as the mechanical connections on the patch panel have been checked.

**Frequency generators** After the installation of the low voltage cables of the TRD (14.4 km) and the pretrigger (4 km) system many cable labels have been removed or wrongly relabeled by the cable companies. The frequency generators have been used to efficiently find the corresponding ends of a cable within the racks and the detector. Each generator produces a rectangular signal with a unique frequency using a NE555 IC. The cables are marked by injecting a frequency into each cable. The grounds of the frequency generators are connected to the common ground of the ALICE detector. The cables are traced by measuring the frequency by a multimeter at the open end of the cable. By this method it was possible to trace many cables at once without being confused by cables permanently or by accident connected to the ground.

**Burn-in-test** Figure 5.6 illustrates the wiring of a low voltage channel. The power supply provides a ground free terminal voltage at point 1 and 3. This voltage is forwarded to the load at point 5 and 6 via the patch panel. The power supply is intended to provide a nominal voltage at the patch panel. It measures the voltage at the patch panel via the sense wires (point 2 and point 4). The terminal voltage is increased relative to the nominal voltage to compensate for the voltage drop because of the ohmic resistance of the power cable between the power supply and the patch panel. During commissioning of the TRD supermodules and the pretrigger system 5% of the cables have shown to be connected the wrong way for various reasons. To ensure the functionality of the low voltage infrastructure the burn in test has been developed. With it



**Figure 5.6:** Schematic view of the Burn-in-test to commission the low voltage cables. By applying a high current (2A to 50A) and measuring the voltage drop over the cables the polarity and connection of the individual cables have been tested.

a low voltage channel can be checked within 1 minute without any risk to the hardware. The power supplies are controlled via the commissioning PVSS panel providing direct access to the monitoring and configuration of all TRD Wiener power supplies. The following steps have to be performed:

- connect the shunt resistor instead of the hardware as load
- apply voltage to the channel (PVSS).
- check voltage drop between terminal voltage and sense voltage (PVSS). This indicates a not broken sense wire as well as a not broken power cable between power supply and patch panel.
- check for the same polarity of sense and terminal voltage (PVSS). This indicates a correct mapping of the sense wires to the power cables.
- check for a voltage drop between sense and load voltage (PVSS, Multimeter). This indicates that the shunt resistor is connected to the correct channel.
- check for correct polarity of the load voltage (Multimeter). This indicates that the cables between the patch panel and the load are not swapped.
- check for comparable values in all measurements. This checks for loose cable connections.

Table 5.1 shows typical measurement values. Terminal as well as sense voltage are measured

cable	$U_{nominal}[V]$	$I[A]$	$U_{terminal}[V]$	$U_{sense}[V]$	$U_{load}[V]$
SM17A1.8L23	1.000	47.117	1.222	1.007	0.985
PTLV-1-1-3/4	3.000	2.856	3.556	3.004	2.739

**Table 5.1:** Reference values for the Burn-In-Test. SM17A1.8L23 is a low voltage cable for the TRD supermodule. PTLV-1-1-3/4 a low voltage cable for the pretrigger.

with the PVSS panel of the low voltage channel. The voltage drop over the load is measured with a multimeter. The shunt resistor for the TRD low voltage channels is a V4A lot (Picture G.9). The pretrigger channels have been tested with a 5W power resistor. A test of the cables by connecting the one end of the cable to ground and check at the other cable end with a multimeter for continuity between ground and cable does not give meaningful results because of the capacities and resistors in the power supply (see fig. 5.6).

**LVDS converter** For the TRD standalone cosmic run in April 08 (Chap. 8.3) and during commissioning, especially the TOF part and the CTP interface, it was necessary to have a low noise LVDS to TTL and TTL to LVDS converter. A small board with a LVDS to TTL and a TTL to LVDS converter IC as well as some voltage regulators and jumpers to select different configurations has been built (pic. G.6 and pic. G.7. The board is equipped with the most common connectors as they are used in the pretrigger system. Also some ECL to TTL and TTL to ECL IC have been mounted. For long runs or tests the board can be mounted in a normal VME crate for low noise and ground free operation a battery adapter board for two 9V batteries has been designed, that can be used instead of a VME crate.

## 6 Implementation

In this chapter the technical implementation of the pretrigger concept is described. The commands for the operation of the pretrigger system are summarized in App. D.

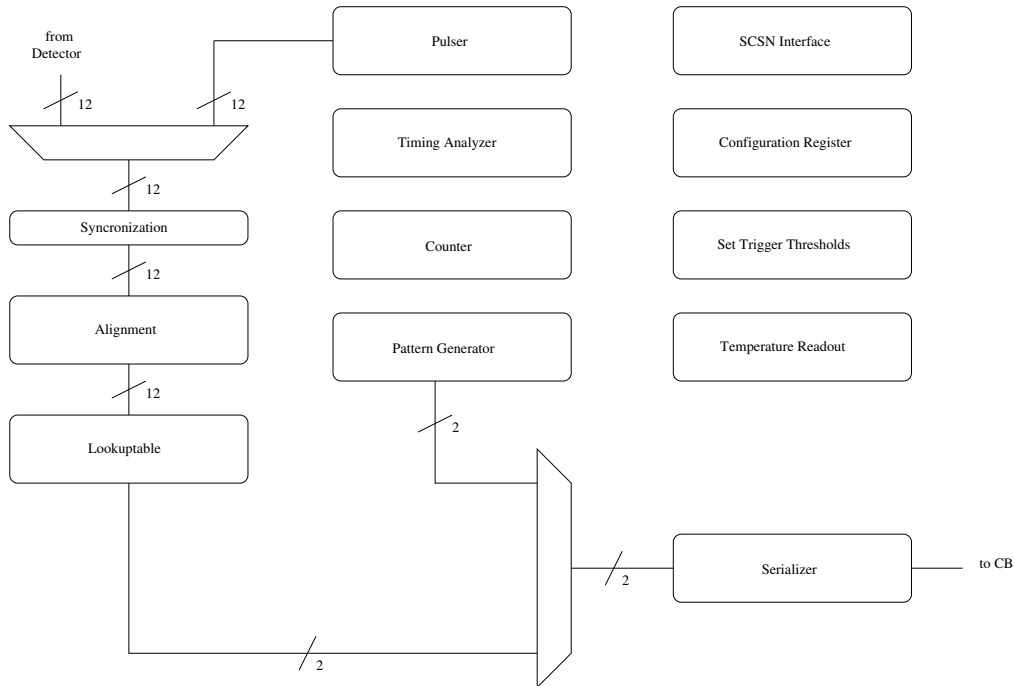
The TRD pretrigger system makes the trigger decision in three steps (see Fig. 4.2 and Fig. 5.1.

1. First the direct analog signals from the PMTs are collected in different front end boxes (FEB). There they are discriminated to digital signals and reduced to two bits according to a freely programmable trigger algorithm.
2. In the second stage the two bit signals of all FEBs of one side are reduced to a 4 Bit signal in the control box A (CBA), control box C (CBC) respectively, that is sent to the central control box B (CBB). The algorithm for this reduction is again freely programmable. In parallel to the V0 and T0 pretrigger a 8 Bit event classification is calculated in the TOF logic multiplicity unit (TLMU) based on the inputs from the TOF detector.
3. The final trigger decision is formed in the CBB. Here the signals from TLMU and from CBA and CBC are combined to a wakeup signal, called pretrigger, for the TRD detector as well as to a L0 that is sent to the CTP.

The whole trigger system is controlled via 2x3 DCS boards that are located on the control boxes. The DCS boards get via a TTC fiber the clock and trigger signals from the CTP. The FEBs are controlled by the DCSs boards on CBA and CBC. In addition the CBB formats the CTP signals so that it can be combined with the wakeup signal and be sent to the TRD. The electrical trigger signal is converted to the optical trigger signal for the TRD by the TTCex and multiplied by the TTCtx if necessary. The interface to the CTP and GTU is established by the PIM module.

### 6.1 Front End Boxes

Figure 6.1 shows the logical design of the Front End Boxes (FEBs). The analog signals from a detector are first digitized by a comparator IC. The comparator sends a one to the FPGA if the analog signal is above a reference voltage and a zero if it is below. The reference voltage of each comparators is set individually via a Digital to Analog Converter (DAC) using the Set Trigger Thresholds module based on [43]. The thresholds are only changed if the DET update register is high. Each digital detector input has two modes. The normal mode, where the inputs are forwarded to the synchronizer and the pulser mode. In the pulser mode a signal with a configurable frequency is used instead of the detector input. By switching to pulser mode while disabling the pulser an individual input is masked out. The synchronizer latches the digital signals into the 160 Mhz clock domain of the FEB box and makes sure that every signal from a PMT is only valid for one bunch crossing. So signals can be seen in the corresponding event and do not give fake triggers in the next event. This module is described in more detail in Chap. 6.5. After synchronization the different signals are delayed between 0 and 31 160 Mhz clock cycles. On the hardware side this is a chain of registers through which the signal is passed. According to the configured delay the output is connected to a certain register output in the chain via a multiplexer. For the less delayed signal this multiplexer has a fastpath logic, that prevents this signal from having to go through all logic stages of the multiplexer. Thus the combinatorial path is reduced



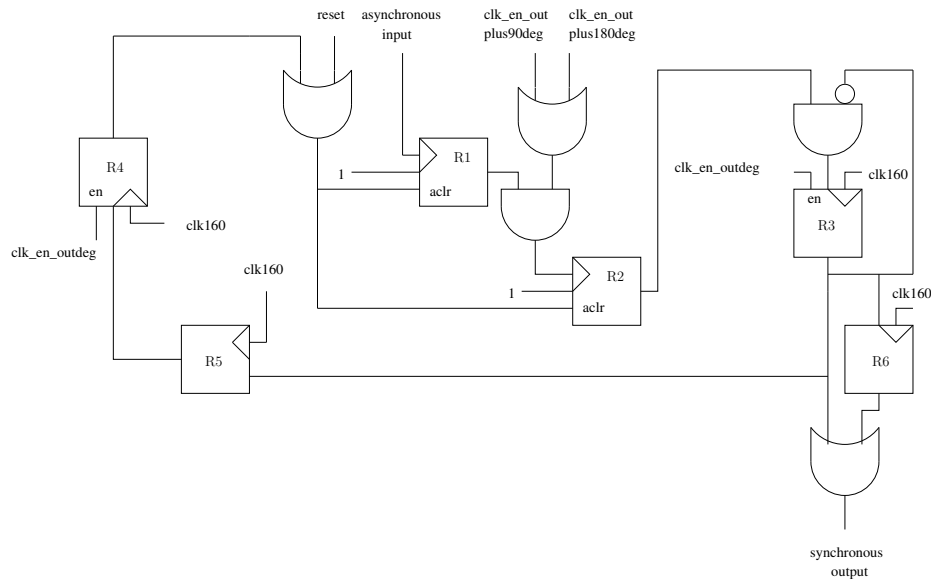
**Figure 6.1:** Logical function of the Front End Box. Discriminated signals coming from the detector are first synchronized and aligned. Afterwards a lookup table sends a trigger decision to the CBA or CBC, via a serializer, multiplexing two bits into one line. Several signals can be monitored by a counter or a timing analyzer. Counter, timing analyzer, thresholds, configuration registers and the temperature are controlled and read via an scsn interface. The input and output can be driven by a pulser or pattern generator alternatively.

to a minimum. The input of the lookuptable is given to the address port of a memory. Each possible trigger configuration is thus mapped to a location in this memory. Whenever a certain trigger configuration appears the corresponding location in the memory is sent to the serializer. By programming the content of the memory each possible trigger logic can be implemented. A description how to do this in software is described in Chap. 7.3. Alternatively to the two bits from the lookup table two bits from a register are sent to the serializer. This is used for debugging and alignment Chap. E. The serializer multiplexes both bits with 80 Mhz into the trigger line to the CB. Logically it gives the most significant bit (MSB) to the output when the 40 Mhz clock from the input is high and the least significant bit to the trigger line if this clock is low. Giving a 40 Mhz clock to the select input of a multiplexer does not work reliably since the synthesis and implementation tools get confused about the timing. Thus the select input of the multiplexer is driven by the LSB of a 80 Mhz counter. For monitoring the temperature inside the box a temperature sensor IC is implemented on the FEB board. It is read out via the temperature readout module based on [43]. For monitoring and aligning a timing analyzer 6.5 as well as a counter for several signals are implemented. The configuration registers defining the operation parameters as well as the monitoring read out of the FEB is done via the scsn interface (see 6.5 and B.5). For addresses, meaning and valid values of the scsn communication to the FEB see App. D.

**Synchronization** The Synchronizer prevents the registers of the FPGA from not accepting signals, but starting to oscillate. This can happen if the input from a detector changes within the setup and hold time or if the pulse width is smaller than  $25ns$  (an example is given in B.2). According to [44] the sum of the setup and hold times for Spartan3 FPGAs is  $2.79ns$ . The input is sampled with a period of  $6.25ns$  to reduce latency. Comparing both numbers and assuming randomly

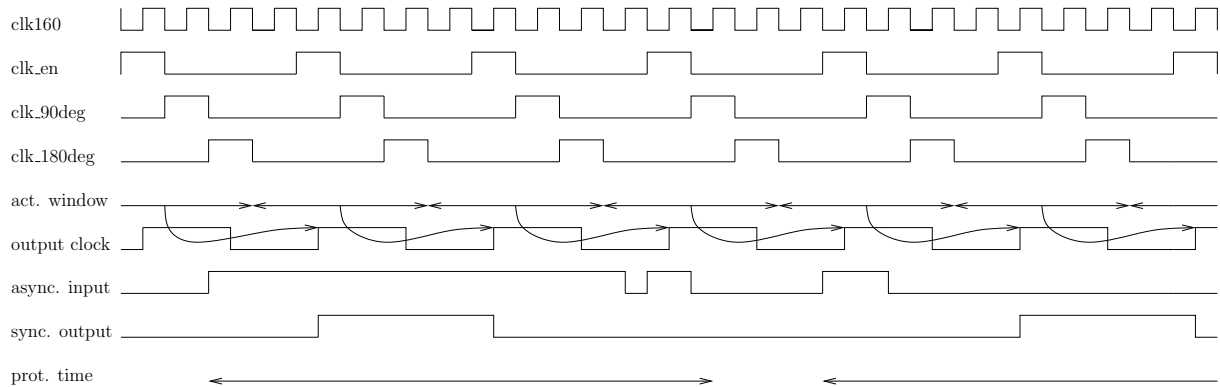


distributed signals this would mean having an unstable FPGA caused by 44% of the signals what is unacceptable. In addition the synchronizer reduces the input noise rate by introducing a protection time after an accepted input from a detector. The synchronizer works as follow (see



**Figure 6.2:** Logical function of the synchronizer module. An asynchronous signal is safely synchronized via the clock input of a register. Any rising edge in the asynchronous signal, arriving out of the protection time, produces a 25ns long pulse in the synchronous output. For a timing diagram see Fig. 6.3.

Fig. 6.2). A asynchronous signal is given to the clock input of a register. Whenever a rising edge appears in the input line, that is it changes from zero to one, the register (R1) connected to the input line latches the one on its input to its output. The forwarding to the clock input of the second register (R2) is only enabled if it is guaranteed that the signal will not change at the input of the output register within its setup and hold times. Otherwise it is stored in the R1 register. The signal on the synchronous output shapes itself to a pulse of the length of one output clock cycle (see Fig. 6.3) via a feedback to the input of the output register (R3). In addition this pulse is delayed by the protection time register and used to reset the input registers. Therefore no trigger is accepted in the input registers within the next two output clock cycles following the rising edge of a signal at the synchronous output. This time is increased by adding another delay register (R5). This 50ns are approximately the decay time of the PMT signal of V0 and T0 and prevent the system thus from trigger due to noise. This happens if the noise adds to a decaying signal and thus brings it over the threshold. Hence an additional not physics related trigger is rejected. The time window for coincidence measurements is increased by 25ns by adding another register R6 and an OR into the circuit. Thus the synchronous output fires for an additional 25ns increasing the probability of a coincidence with another signal. The timing diagram in Fig. 6.3 illustrates the function of the module. Clk160 is derived from the 40Mhz LHC clock in a DCM (App. B.1). It is in a constant phase to the LHC 40 Mhz clock. The clk\_en\_outdeg signals mark different phases of the output clock. They are produced with a falling edge counter in the 160 Mhz domain (for more detail see documented vhdl code on the accompanying CDROM). The asynchronous input signal is the signal the comparator IC produces out of the analog signals of the PMTs from V0 and T0. The synchronous output is within the clock domain of the FEB and is used for further trigger processing. The output clock is not a real signal but a signal introduced for illustration. It is a clock that has a rising edge whenever clk\_en\_outdeg is high. Whenever a signal appears on the asynchronous input line its first rising edge falls into a certain acceptance window (Fig. 6.3). The Synchronizer shapes or extend the signal to a one output clock cycle (if R6 is present to two



**Figure 6.3:** The synchronous output delivers safely a 4 clk160 cycles long pulse for each rising edge appearing at the asynchronous input at any time. During the protection time following a pulse at the synchronous output no rising edges are accepted at the asynchronous input. The pulse at the synchronous output is delivered at the rising edge of the output clock following the acceptance window time interval in which the rising edge of the input occurred.

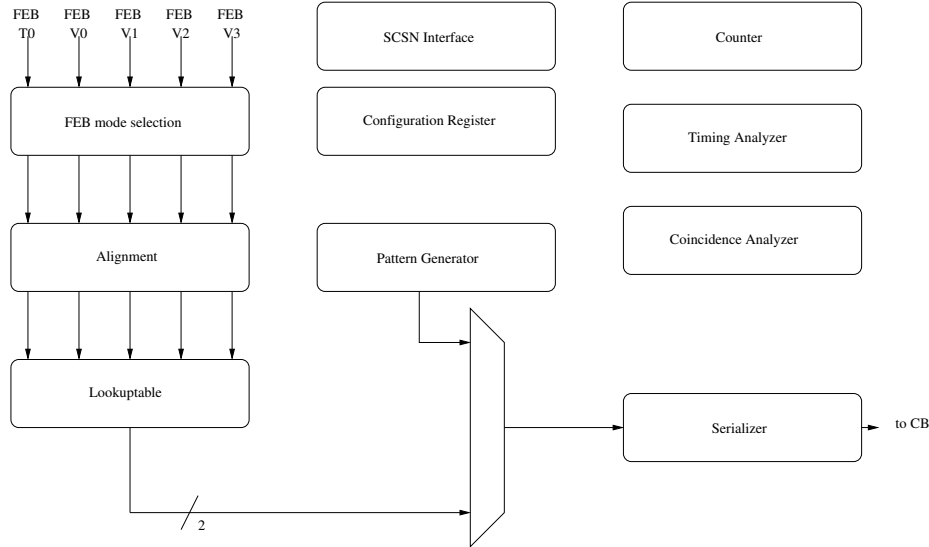
clock cycles, see above) and gives it to its synchronous output at the next output clock rising edge preceding this acceptance window. After a signal on the asynchronous input until two clock cycles after the rising edge of the synchronous output signal all input signals are ignored. To do a first step of alignment without having to delay the signal the acceptance window and the output clock can be shifted relative to the LHC clock, that is relative to the signals from a physics event on the asynchronous input line (see set input sampling phase in App. D).

**Fine Delay** The signal is shifted in units smaller than  $6.25ns$  by slightly changing the trigger threshold (5 units do not affect the calibration see Chap. 8.2), since the analogue signals of a PMT is not rectangular (compare Fig. 8.1). An alternative is the fine delay module (OR-delay) found in the project on the CDROM.

## 6.2 Control Box A and C

The Control Box A-Side (CBA) as well as the Control Box C-Side (CBC) combine the trigger decisions from the five FEB boxes of one side to one trigger decision of four bit sent to the CBB.

**The FEB Control Logic** The connection to the FEB is established using normal Ethernet cables. from the four logical lines three are for data sending from the CB to the FEB and one is the back channel from the FEB to the CB. The upstream line propagate a 40 Mhz clock, a SCSN upstream and a Selector line. A high Selector line indicates that the corresponding FEB box is in the configuration mode. Now the back channel is used as SCSN back channel and forwarded to the SCSN master on the DCS board. If the selector line is low the back channel is used as trigger input and forwarded to the alignment logic. If the SCSN upstream line is set to high while the selector line is low this issues a reset on the FEB. The logic to change the mode and mapping of the Ethernet cable to the FEB is implemented in the FEB mode selection module. To configure a FEB, that is to send scsn commands to it, the FEB has to be selected by setting the selection register to the corresponding value (see select FEB to configure in D) or to zero for normal trigger operation. The module will then route the four physical lines of the Ethernet cable. If a FEB is in configuration mode it can be configured using the FEB\_write and FEB\_read commands of the control software. If a box is in trigger mode a reset is issued by setting the corresponding reset register of this box (FEB reset).



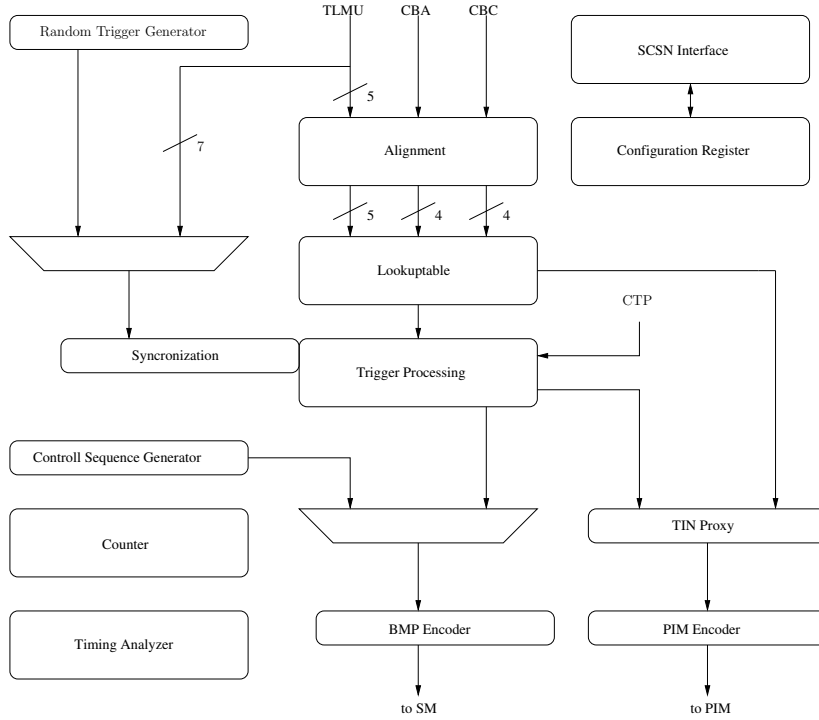
**Figure 6.4:** Logical function of CBA and CBC. The signals from five FEBs are aligned and a 4 bit trigger decision from the lookuptable is multiplexed into one line by the serializer and forwarded to the CBB. The system is configured by the configuration registers. Several signals (see App. D) are monitored by a timing analyzer and some counters. For synchronization the serializer uses a defined pattern. The whole system is controlled, configured and read out via an scsn interface.

**Alignment** If in trigger mode the signals from the FEBs are passed to the alignment logic. Here the signal is latched with a rising or falling edge (pattern sync edge sel). The period of the sampling clock is  $12.5ns$ . The signals of the FEB and the sampling clock have a fixed phase relation, since they origin from the same 40 Mhz LHC clock. Changes of the signal within the combined setup and hold time of  $2.79ns$  of the Spartan3 FPGA [44] are thus avoided by either latching with the rising or the falling edge of the CBA/C sampling clock. Like in the FEB alignment module a delay chain with fastpath logic is implemented. It delays the signal between 0 and 31 160 Mhz clock cycles. To get the right value for the delay all signals arriving at the lookuptable are monitored using the timing analyzer. The procedure to find the right latching edge and the right delay is described in E.

**Lookuptable** Within the Lookuptable module the inputs from the FEBs are parallelized and mapped to the address port of a RAM cell of the FPGA. The overall mapping of the two bits send by each FEB boxes and the address input of the lookuptable is summarized in table 7.1. The 4 bit output of the lookuptable is forwarded to the serializer and afterwards transmitted via a fiber to the CCB. Since the input to the laser diode driver is AC coupled (see schematics [75]) the output of the serializer should have a large AC component. Therefore the lookuptable should be programmed in a way that signals with a high DC component like “0000” and “1111” are avoided. Because of a heat problem on the printed circuit board (PCB) it is not recommended to transmit 4 but only 2 different bits. Up to a update of the PCB bit 1 and 2 as well as bit 3 and 4 must have the same value. This reduces the frequency and make the transmission working with less than 1 wrong bit in  $10^{10}$  bits. To cool down the laser transmitters some copper tape has been soldered to the pins of the transmitters. The serializer maps the four output bits of a lookup table into one 40 Mhz cycle. The MSB of the output appears within the first  $6.25ns$  after a rising edge, the second significant bit within the second  $6.25ns$  and so on. The counter module counts the number of 40Mhz clock cycles in which a signal carries a logic one. The monitored signals and the corresponding counter are documented in App. D.

**Coincidence Analyzer** To determine the contribution of individual FEBs to the output of the lookuptable a coincidence analyzer logic is implemented. It detects and counts 25 different conditions. A condition can be either the simple occurrence of a certain bit pattern on one of the 5 FEB inputs of the lookuptable or the occurrence of a specific bit pattern on one of the 5 FEB inputs in conjunction with the occurrence of another specific bit pattern in the output of the lookuptable. While forming this coincidence the delay of the lookuptable is compensated.

### 6.3 Control Box Bottom



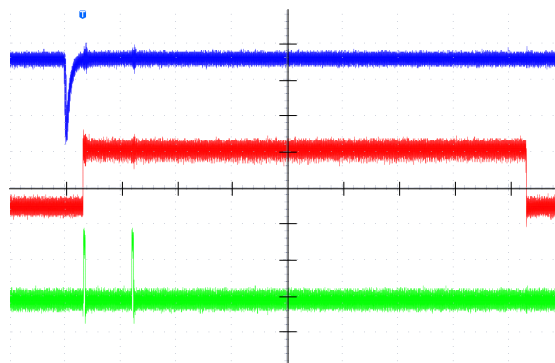
**Figure 6.5:** Logical function of the CBB

**Overview** The Control Box Bottom (CBB) is the central part of the pretrigger system. It receives the trigger inputs from the CTP and the different subsystems of the pretrigger. Namely the TOF system, the V0 and T0 system as well as a busy signal from the GTU via the PIM module. The CTP signals come encoded via the TTC fiber on the DCS board where they are decoded with the TTCrx IC and some logic on the hardware. The CBB FPGA receives four signals from the DCS board.

- LHC 40.08Mhz clock.
- A ready signal (RUNRUN) that is high after a start of run trigger and low after an end of run trigger. It thus indicates a ongoing run implying that the TRD is ready to receive triggers, since this SoR trigger is only enabled by the ALICE DCS if all detectors, participating in a certain run, signalize that they are configured and ready for data taking.
- The A-Channel line transmits the L0 and L1 trigger. On the DCS board this line is called L1accept.

- The B-Channel transmitting the L2accept as well as trigger messages encoded in a protocol. The B-Channel line is currently neither used by the TRD FEE electronics on the detector nor by the pretrigger.

The input from TLMU, CBA and CBC are first aligned in the same way as in the CBs and afterwards forwarded to the lookuptable. In the lookuptable module the signals from CBA and CBC are parallelized and connected to the address port of a RAM block like in the CB (Chap. 6.2). The mapping of the trigger output of the CBs to the address inputs of the CBB lookuptable is documented in Tab. 7.1. The lookuptable of the CBB has two outputs. The MSB of each address is forwarded to the TIN proxy. The TIN proxy, the interface module to the CTP, is described below. The LSB of the CBB lookuptable output can be used as pretrigger signal in the trigger processing logic. Alternatively one of the 8 Bits from TLMU can be forwarded to the pretrigger input of the trigger processing logic via a synchronizer as described in Chap. 6.1. The trigger input from TLMU via the synchronizer is especially foreseen for cosmic runs. It allows to implement asynchronous logic forming a coincidence in the TLMU without having to care about setup and hold time problematics. The pretrigger signal as well as the L0 signal is forwarded to the CTP according to the configuration (for setting the configuration see D). In production runs the CTP only proceeds in the trigger sequence of the TRD cluster if the TRD has its full power, that is if the detector has been waken by the pretrigger. The connection to the CTP is partly established via optical fibers therefore the signals are manchester encoded (see Chap.6.4). To reduce latency the whole design runs at 160 Mhz derived from the 40 Mhz LHC clock with a DCM (App. B.1). CTP signals and trigger signal from the other parts of the pretrigger system are  $25ns$  long corresponding to 40 Mhz. To be able to process these signals, that is to define the rising edge of the 40 Mhz clock, a clock enable logic has been implemented in each FPGA. This logic marks four different phases in the 40 Mhz clock. This idea is illustrated in Fig. 6.3. These enable signals are generated in a central module and distributed over the FPGA via clock networks to ensure the timing even though the large fan out of these signals. In addition to this the enable signals have been registered. More technical details are documented in the vhdl code. Practically this has the following advantages. The processing time by the whole system is reduced by a factor of four since a four time faster clock is used for the pipelining. In addition it is possible to gain up to another  $18ns$  in each of the three decision steps by shifting the clock instead of having to delay all signals to align them to the fixed phase of the 40 Mhz clock. To get the full advantage of this feature it is only important to first align the latest arriving signal by using the clock shift parameter instead of the delay parameter.



**Figure 6.6:** Function of the trigger processing unit in a L1 reject scenario (Oscilloscope Screen Shot  $t = 800ns/div$   $U = 2V/div$ ); blue: photomultiplier signal; red: busy signal; green: trigger signal for TRD.

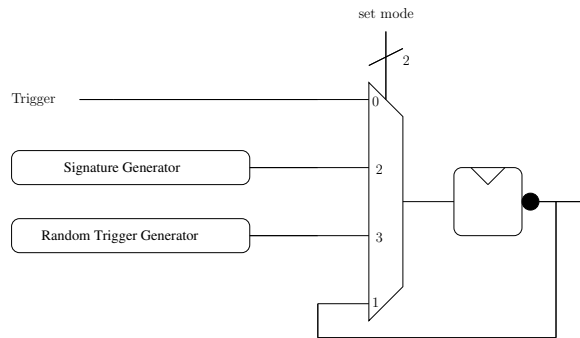
**The Trigger Processing and Busy Logic** The function of the trigger processing module is illustrated in fig. 4.2 and fig. 6.6. It merges the pretrigger, the L0 and the L1 trigger, takes care about the correct format and timing of the trigger sequence and blocks triggers under certain conditions. Blocking triggers protects the TRD front end electronics [45] during the read out. A pretrigger, a  $25ns$  pulse, from the lookuptable or from the synchronizer is forwarded as fast as possible to the bmp encoder. Such a pretrigger immediately invokes a busy signal that prevents further pretriggers to be sent to the supermodule. The logic keeps the busy high and waits for a L0 from the CTP for a configurable time `pre_to_next` (App. D). Whenever a L0 arrives within that `pre_to_next` it is forwarded after the `pre_to_next` as L0 puls to the SM and the busy signal is kept high for the configurable `L0_to_next`. If a L1 puls arrives within that period it is shortened to a  $25ns$  pulse which is sent to the SM after the `L0_to_next` time. After a L1 the busy signal stays high for a configurable time (`L1_to_next`). This is intended as temporary solution to prevent pretrigger from being sent to the SM while the GTU is reading out the MCMs on the detector. The busy signal is also kept high if the ready signal from the DCS board (Chap. 7.1) is low as well as if the GTU sends a busy signal to the CBB via the PIM module. This contribution to the CBB internal trigger blocking is disabled and enabled via the configuration registers. The ready busy and the GTU busy are intended to be the final busy control mechanisms. The GTU busy prevents pretriggers to the SM during readout. The ready busy ensure that no pretriggers arrive at the SM when it is not configured. To compensate for the propagation time of the GTU busy to the CBB box the `L1_to_next_time` must be set to 25 cycles. While writing this text the work for the GTU busy on the GTU side is in progress, but has not finished. If the L0 autogen and L1 autogen registers (see D) are set the L0 and L1 trigger is generated internally independent from the L0 and L1 issued by the CTP. The L0 from the CTP is forwarded to the Pretrigger input if the L0 as Pre en register is set. This enables an emergency trigger mode. At least for the beginning it is not expected that the configuration of the pretrigger system reaches 100 % efficiency. There will be L0 signals from the CTP without a preceding pretrigger. In this case the L0 from the CTP is used as pretrigger and as L0. The necessary delay and L0 puls splitting is automatically done within the trigger processing logic. In this mode the signals from the TRD will not show an amplification region (Fig. 8.4(a)) but at least some timebins are captured for those events. This mode is also useful if the detectors for the pretrigger (V0, T0 and TOF) are out of service, or if the pretrigger hardware for those detectors (FEB) have problems and therefore a reliable decision for the pretrigger pulse is not possible. In addition to the trigger signal processing this module also provides two benchmark counters that show how good the current pretrigger configuration, that is the adjustment of the thresholds and the values in the lookuptable are.

- Pretrigger without L0
- L0 without pretrigger

The first benchmark counter counts the number of pretrigger without a following L0 from the CTP (unnecessary pretriggers). If this number is high this indicates that the TRD starts the fit calculation for the tracklets (Chap. 3.2) too often. Thus the power and corresponding to it the heat production of the detector is too high. Since every pretrigger implies a dead time of TRD this scenario also leads to a reduced efficiency. That is there are events where the TRD does not participate or if the emergency pretrigger is enabled the pulse high spectra has no amplification region. This benchmark is implemented by storing the pretrigger puls in a register. If this register is not set to zero within the Pre to next time by a L0 from the CTP the register increases the counter and resets itself afterwards. The second benchmark counts the L0 events where the pretrigger has not fired. This signals gives direct information about the pretrigger efficiency relative to the CTP L0. The counter is increased whenever a L0 from the CTP arrives out of a pre to next busy time. Using these two signals and the total number of events it is

possible to calculate the purity and efficiency (App. A.1) of the pretrigger relative to the CTP L0. The control sequence generator is intended to send control signals, like a reset, simultaneous to all MCMs of the TRD detector. The sequence consists of 8 successive 40 Mhz pulses [45] and are programmed via a configuration register. As soon as the start sequence signal changes from zero to one the 8 bits appear sequentially on the trigger line with the MSB first. After the sequence has been sent for one time the trigger line is set to zero. Several counters and a timing analyzer are implemented for debugging and adjusting the signals. The mapping is documented in App. D.

**Random trigger generator** The random trigger generator provides random trigger pulses with an adjustable rate at the TLMU input. This rate is changed by changing the random trigger threshold value. The random pulses are generated as follow. A FIFO puffer with an XOR feedback generate equally distributed pseudo random numbers [46]. If one of these numbers are larger than the threshold a pulse is generated. Thus the higher the threshold the lower the rate. The random trigger is used instead of the TLMU as input to the synchronizer of the CBB if sel synchronizer input is set to 7.

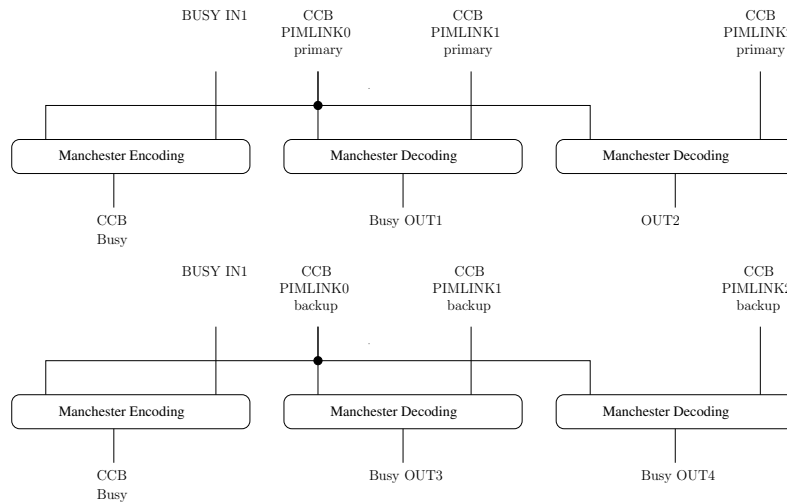


**Figure 6.7:** Logical Function of the TIN Proxy

**TIN Proxy** The TIN Proxy module is for the connection to the CTP via the PIM module. It provides four different modes. In mode 0 it forwards the L0 contribution of the TRD to the CTP in inverse logic. That is a trigger is indicated by a low signal and a idle line by a high signal. Mode 1 is for the synchronization with the CTP. In this mode a toggling signal with a period of 50 ns is sent. Mode 2 sends a signature according to [47] that identifies a input line to the CTP. The last mode, mode 3 sends pseudo random trigger pulses with an adjustable rate in the same way than the random trigger generator (see above). The basic control of the TIN Proxy is done by setting the control registers. This is either done with the ./CheshireCat software or a DIM server ( 7.3).

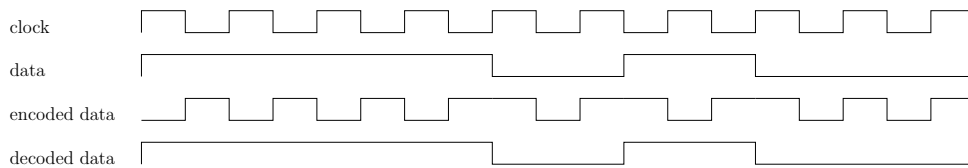
**The TOF Logic Multiplicity Module** The TOF Logic Multiplicity Module (TLMU) has a hard coded logic for the 576 inputs from TOF. It implements the cosmic logic as defined in Tab. 8.1. For debugging 16 Bit counters for the individual channels are implemented. They are controlled using the ./CheshireCat FEB\_write commands (Chap. 7.3). Within this thesis the TLMU implementation carried out by [48] was supported. In productive runs the TLMU measures the multiplicity of an event in the central rapidity region [48] and provides this information as a five bit signal (TLMU multiplicity bits) registered to the LHC clock to the CBB lookuptable for the final trigger decision. Since the cosmic output of the TLMU is not synchronized it is passed through the synchronizer of the CBB before it is used as pretrigger to avoid setup and hold time problematics similar to the FEBs (Chap. 6.1). By setting the values of sel synchronizer input the trigger from the cosmic logic or one of the five multiplicity bits from TLMUis used as pretrigger.

## 6.4 Pretrigger Interface Module



**Figure 6.8:** Logical function of the Pretrigger Interface Module (PIM). The busy signals from the GTU are Manchester encoded and sent to the CBB. The encoded trigger signals from the CBB are decoded and forwarded as LVDS signals to the CTP.

Since LVDS is not capable to transmit signals at a high bit rate over a long distance the connection between the CBB and the PIM module are realized via multimode fibers. Only the last meters of the CCB to CTP connection are normal LVDS. The used laser transmitter and receiver combination requires an AC coupled input for optimal performance (Schematics [75]). To transmit signals with large DC component, these signals are converted into signals with an AC component. The PIM module as shown in Fig. 6.8 decodes the trigger signals sent and encoded by the CBB backup and primary system and forwards them as LVDS signal to the CTP. In addition it encodes the busy signal from the GTU and transmits it to the CBB primary as well as to the CBB backup system. To have a low latency the manchester encoding is used [49]. This encoding is illustrated in Fig. 6.9. The encoded signal for the transmission over the optical line is generated by making the logical XOR of the clock and the data signal in the CBB. The clock and the encoded signal (both DC free signals) are transmitted to the receiver. There another XOR between both signals recovers the original data.

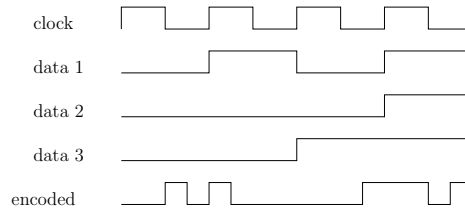


**Figure 6.9:** Principle of the DC free Manchester Protocol. A data signal is encoded into a AC signal by an XOR with the clock. The data signal is received by an XOR between the clock and the encoded signal.

**6 Bit CB to PIM Protocol** The 6 Bit CBB to PIM protocol is intended to be used as soon as the event by event monitoring (see chapter 4.2) is implemented. In this case the three fibers from each CBA, CBB and CBC must transmit 6 bit to the PIM module. These bits are either recorded in the DAQ data stream via a not yet built GTU interface or forwarded as trigger contributions to the CTP. The 6 Bit encoder module works as follow. The first fiber between CBB and PIM transmits a 40 Mhz clock signal. The second and third each a 160 Mhz signal that carries 3 data

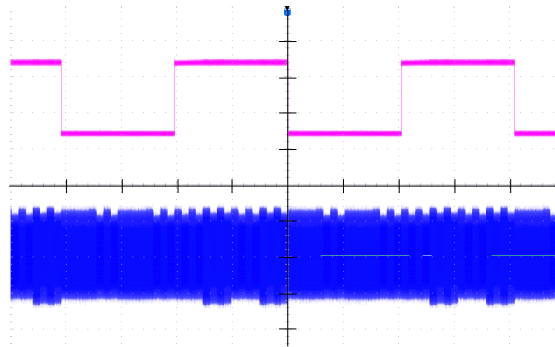


bit encoded in 4 bit. The data bits 0,1 and 2 are mapped to the encoded bits 0,1 and 3, bit 2 is a stuffing bit. The stuffing bit is only high if all data bits are low or if a reset is sent. Thus all signal have a sufficient AC component to be transmitted via the fiber. If all of the three fibers have a 80 Mhz clock this indicates a reset. More technical documentation can be found inside the VHDL code. The protocol is illustrated in Figure 6.10. The protocol was successfully tested



**Figure 6.10:** Principle of the 6 Bit serial code. A stuffing bit ensures the AC part of the signal.

within a test setup. Each of the 6 channels was connected to a rectangular signal with a unique period. To reset the DCM in the PIM module in the beginning a reset signal was sent. 6.11 shows one decoded signal, as well as one encoded signal.



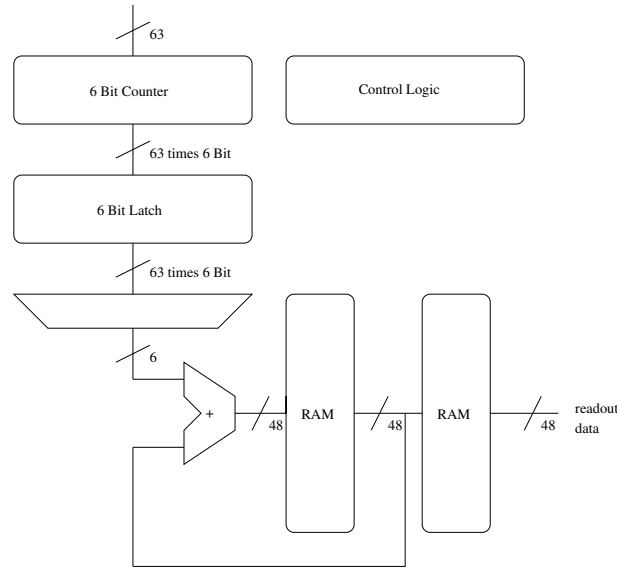
**Figure 6.11:** The 6Bit PIM decoder. (Oscilloscope Screen Shot  $t = 100\mu\text{s}/\text{div}$   $U_{\text{blue}} = 2\text{V}/\text{div}$   $U_{\text{purple}} = 1\text{V}/\text{div}$ ) (blue: encoded signal with 3 Bits; purple: one decoded Bit)

## 6.5 Common modules

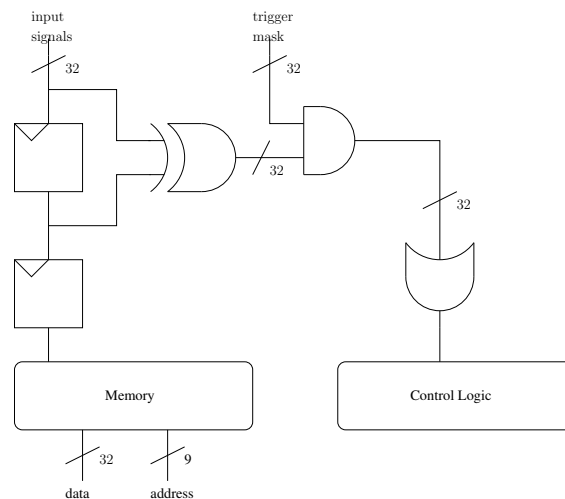
These modules are used several times in the pretrigger system in a slightly adapted manner.

**RAM Counter** The RAM counter module provides 63 different 48 Bit counters operating at 40 Mhz. The counters can be read out quasi simultaneously. An implementation in normal cells would fill the small FPGAs of the FEB by 80 percent and the FPGA of a CCU by 30 percent. Therefore the module uses the RAM blocks of the Spartan3. This reduces the number of occupied slices by a factor of 7 compared to an implementation without RAM blocks. The module increases a counter whenever the corresponding counter enable input is high during a rising edge of the 40 Mhz clock. The counter enable inputs are phase adjusted by some logic. Therefore each 25ns puls is safely counted no matter whether its rising edge comes at 90, 180, 270 or 0 degrees compared to the 40 Mhz clock. This logic is described in more detail in the source code. Figure 6.12 illustrates the function of the RAM counter. Each of the 63 counter enable inputs are first connected to the enable input of a 6 Bit counter. The value of all of these 6 Bit counters are continuously and simultaneously copied to a 6 bit latch of its own. After copying the counter values the latches are sequentially read out and each value is added to the counter value up to the previous copying

process stored in the RAM block and the sum is stored back in the RAM block. Whenever the control logic receives a rising edge (register counter readout req see App. D), that is a change of the signal from zero to one, it copies all data to the second stage of RAM. From there it is read out via scsn. Fig. B.1 shows a simulation of a readout cycle. The control logic also ensures that all necessary registers and RAM blocks are set to zero when the counter module receives a reset (register counter reset is high). After a readout process has finished the readout done register is high. It is automatically set to zero if a readout is requested.



**Figure 6.12:** Logical function of the RAM counter. 62 6 Bit Counter increase if the input is high during the rising edge of the clock. The values of these counters are stored every 64 clock cycles in a latch. After that the 6 Bit counters are reset. Within the next 64 cycles the counter values are sequentially added to the old counter values in the memory. Thus 63 48 bit counters are realized. If the control logic receives a readout request the counter values are stored into a second memory from where they are read out via scsn.



**Figure 6.13:** Logical function of the timing analyzer. If one of the input signals within the trigger mask changes, the control logic invokes a storage of the signals into a memory for the next 512 clock cycles.

**Timing Analyzer** The timing analyzer is a kind of logic analyzer. It records 512 samples of each input signals with a resolution of  $160\text{MHz}$  that is one sample every  $6.25\text{ns}$ . The timing analyzer

is self triggering. As soon as one of the 32 input signals that have been marked with the trigger pattern change and the analyzer is activated the recording to the memory starts. The analyzer done register (Chap. D) is set to one when the timing analyzer has recorded data. A changing signal is detected by making the logical XOR of the input and output of a register. See Fig. 6.13. To see some time in the past the signal is delayed by a register chain after the trigger detection. Activating the trigger, setting the trigger mask and reading out the timing analyzer is done with the `./CheshireCat` command (see Chap. 7.3). Figure 7.2 shows a captured event. The timing analyzer in the FEBs have only 16 inputs because of the lack of FPGA capacity. To avoid timing problems these analyzers only have one input that can trigger. This input is outside the module fanned out. Therefore the user will see no difference compared the timing analyzers in CB and CBB as described above, except for the fact that there will be less presamples in the output.

**SCSN interface** For the configuration of the individual components of the pretrigger the VHDL design of the scsn slave module from the MCMs has been adapted and ported to the Spartan FPGAs. Thus it is possible to use the same scsn hard and software on the DCS board as for the supermodules. Some minor changes have been made on

## 7 Slow Control

This chapter describes the low level control of the pretrigger using special hard and software. The first section presents the DCS board, the ssh interface to the pretrigger. The second section describes how the DCS board interfaces the pretrigger hardware. The third section shows the software running on the DCS board to control the pretrigger system. The last section is dedicated to the pretrigger control in the ALICE experiment.

### 7.1 DCS Board

The pretrigger system houses 3 primary plus 3 backup DCS boards (Fig. 5.1) in the CBB, CBA and CBC. A DCS board (Schematics [50]) is a small Linux PC with a Ethernet, Jtag and SCSN (Chap. B.5) interface. The Arm processor running at 160 Mhz as well as the driver hardware are implemented in an Altera Excalibur device. The driver hardware is realized in the CPLD of the Excalibur and has been modified within this work (Chap. C.1). The Linux operation system is loaded from a flash device and uses 256MBit of SDRAM as user memory and temporary disk space. The console based Linux system is fully equipped with a ssh server, a network file system client and standard Linux tools from the busy box [51] among others. Additional software is written in normal C or C++ and compiled using the arm-gcc [52] compiler. The board has special hard and software mechanisms for protection against functional errors because of radiation [53]. In addition this DCS boards receive the LHC clock and trigger signals from the CTP via an optical single mode fiber (TTC network). The DCS board generates a ready signal out of the trigger information from the CTP indicating if a run is ongoing. These signals are provided as LVDS signals to the CCU-FPGAs of the pretrigger.

### 7.2 Hardware Interface

The interface to the pretrigger hardware is established using the scsn (App. B.5) device driver on the DCS board. The scsn device file (/dev/scsn1) provides direct access to the bus master hardware on the CPLD of the DCS board. The software implements a scsn\_write(devicename, deviceport, slave, address, data) and a scsn\_read(devicename, deviceport, slave, address, \*returned.data) function based on the frame concept as defined in [53]. Each scsn master has 4 different ports, corresponding to 4 different physical scsn rings in the TRD. The pretrigger uses ring 0 to access CB and CCB and ring 1 to access FEBs and CBTOF. The rings are selected by writing an integer to the /dev/scsn1 device. Bit 17 and 16 select the ring 0 to 3 and bit 31 is the magic bit indicating a portselect writing command. The slave parameter indicates the position of the scsn device in the scsn chain, which should be addressed with a command. In the pretrigger system there is only one device in each chain. So this parameter is always one. Address is the address of the register that should be accessed. Data and \*data\_returned are the send and returned data in the frame format. They are constructed and analyzed before and after every read and write to check if a command was successfully executed on the scsn device. The whole software is completely independent from the libtrd, the library used to control the Trap Chip on the TRD, since it is too much specialized and follows a completely different design approach.

Each DCS board on the CBs and the CCB has a jtag master device implemented on the CPLD of the DCS board. The out and input lines of the jtag master has been multiplied within different ports with a multiplexer to adapt to the different jtag mappings of the pretrigger system. Selecting a jtag port can be done with 'echo x > /dev/jtagse1', where x is the number of the port. The architecture of the jtagmux is documented in (Chapter C.1). The jtag hard and software has been implemented on the DCS board to be fully compatible with the infrastructure on the TRD and is part of the ipkg branch of the DCS board. It has been committed to the officially DCS board repository [54] and is fully included in the ipkg branch starting from revision 307. The upload of the \*.xsvf files produced by the Makefile of each FPGA design (see accompanying CD) is done by './playxsvf -t /dev/jtagfeb Design.xsvf'. The jtagfeb device driver for the jtag master is in [54]. It has to replace the standard jtag driver to be able to cope with the long jtag lines in the pretrigger system. The PIM module is a standalone module without a DCS board. The best way to upload a design to the flash is to make a flash memory file using impact, a program included in the Xilinx ISE. The flash memory file can easily be uploaded using the xilprog program and a programming cable.

## 7.3 Software

```
alidcsdcb0904:/dcsnfs/pretrigger $ ./CheshireCat
CheshireCat the ALICE TRD Pretrigger
Controll programm by SZ

Read the manual on the DCS-Board for more informations about the function of the
registers

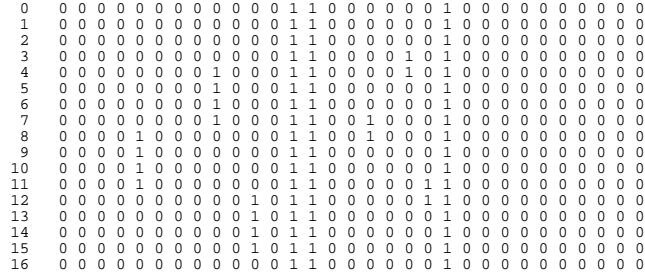
CB_reset
CB_write <reg_addr> <value>
CBTOF_read <reg_addr>
CB_read_many <start_addr> <end_addr>
CCB_LUT_config_min_bias
CBC_LUT_config_min_bias
FEB_reset
FEB_write <reg_addr> <value>
FEB_read <reg_addr>
FEB_read_many <start_addr> <end_addr>
FEB_LUT_config_min_bias
FEB_LUT_config_sync
CB_analyzer_read
FEB_analyzer_read
```

**Figure 7.1:** Functions implemented in the pretrigger control software.

**Functionality** Figure 7.1 shows the different functions that are currently implemented in the software. The functions are called via the CheshireCat software (./CheshireCat <function name> <parameter 1><parameter 2>). CB\_reset and FEB\_reset send a reset to the CB or FEB respectively. This reset is only a software reset. For the FEBs there is also a hardware reset (see appendix), which is the preferred way to reset the FEBs. CB\_read, FEB\_read, CB\_write and FEB\_write can read and write individual registers on the hardware. The meaning and possible values for the registers are documented in the appendix. The read\_many functions print the datum of several consecutive register addresses. The timing analyzer can be read out using the FEB\_analyzer\_read and CB\_analyzer\_read functions. A screenshot and explanation can be found in (Figure 7.2). The CCB has from the scsn side of view the same architecture than a CB. Therefore it can be controlled like a CB. The same applies for FEB and CBTOF.

**Programming the LUT table** The configuration of the lookuptable, that is the trigger logic of the system is programmed by setting all memory locations of all lookup tables to a value defined by the configuration.

This can hardly be performed using a bash script. The processing time is in the order of several minutes and therefore not suitable for the configuration before a run. The current configuration is done by some hard encoded functions into the control software. This way of configuration



**Figure 7.2:** The internal timing analyzer. Each row corresponds to a 6.25ns long timebin. The columns from right to left represent the signal on channel 0 to 31 and the timebin counter. The trigger mask was set to a change on channel 27.

takes well below 10 seconds. To have nevertheless the opportunity to optimize the configuration from run to run a DCS board compilation environment is being installed on a computers accessible from the pit. The configuration is done by looping over all possible lookuptable addresses. The memory location defining the type of trigger for each address is determined by analyzing the binary representation of its address. The analysis is done with the bit operators of C and the onecount function in the CheshireCat software. An example is given by CCB\_LUT\_config\_min\_bias, CBC\_LUT\_config\_min\_bias and FEB\_LUT\_config\_min\_bias that implement a minimum bias trigger on the system. The FEB\_LUT\_config\_sync programmes the lookuptable of the FEB to send a trigger if and only if a signal comes from the DET 0 input. This is used to synchronize the connection between FEB and CB (Chap. E).

Bit of LUT	FEB	CBA/C	CBTOF
0	DET(0)	FEB T0(0)	CBA(0)
1	DET(1)	FEB T0(1)	CBA(1)
2	DET(2)	FEB V0S0(0)	CBA(2)
3	DET(3)	FEB V0S0(1)	CBA(3)
4	DET(4)	FEB V0S1(0)	CBC(0)
5	DET(5)	FEB V0S1(1)	CBC(1)
6	DET(6)	FEB V0S2(0)	CBC(2)
7	DET(7)	FEB V0S2(1)	CBC(3)
8	DET(8)	FEB V0S3(0)	TTU(0)
9	DET(9)	FEB V0S3(1)	TTU(1)
10	DET(10)	'0'	TTU(2)
11	DET(11)	'0'	TTU(3)
12	'0'	'0'	TTU(4)

**Table 7.1:** Mapping of the inputs of the different lookup tables in the pretrigger system.

**Trigger Interface Proxy DIM Server** The ALICE trigger group requests a Trigger INterface proxy running on any hardware with a connection to the CTP [55]. The TIN proxy is described in (Chap. 6.3). The DIM server provides a interface for the CTP to remotely change the mode of each line between toggling(for synchronization), signature(for line identification), random trigger(for connectivity test) and normal trigger mode. The TIN proxy for the TRD pretrigger is implemented on base of a the TIN proxy of the SPD. The server as well as a client for testing are on the accompanying CDROM.

## 7.4 DCS Integration

The shifter controls the pretrigger via PVSS [56], a software providing a graphical interface to the control and monitoring of the detector. It is the standard software for all LHC experiments. PVSS provides an interface to a finite state machine(FSM) called SMI++. The FSM receives a command describing the desired mode of the detector (OFF, BEAM.TUNING,CONFIGURED, READY and some intermediate states) from the ALICE experiment control system (ECS) or a local shifter and sends afterwards the configuration commands to the different subsystems. In addition it monitors the status of the subsystems. In case of an error the shifter can take action and change the parameters, reboot or switch off individual parts of the subsystem until an expert can recover it. The communication between PVSS and the subsystem is done via DIM. DIM is a network protocol developed for the previous LEP experiment at CERN. It is based on a client server architecture. The server is part of the subsystem while the client belongs to the controlling system. The client can either query the value of parameters describing the status of the subsystem or send command to the server via a so called command channel.

Currently the LV of the pretrigger is controlled via the infrastructure tree of the TRD FSM [57] and is permanently switched on. The configuration for registers of FPGAs is done via configuraton scrips. These scripts run remotely `./CheshireCat` (Chap. 7.3) and DCS board commands on the pretrigger DCS boards via ssh. The connection to PVSS is done via DIM. A DIM server receives names of scripts to execute and executes them [58].

Four main configuration flavours exist. The scripts are found in `/home/trd/scripts` of workernode 5.

- `pretrig_config_TOF_as_pre` this mode uses the TLMU input as pretrigger. If no Pre was produced to a L0 the GTU reads out an empty event.
- `pretrig_config_TOF_and_L0_as_pre` this mode uses the TLMU input or a L0 of the CTP as pretrigger for events where no pretrigger is fired. Events without a Pre have no amplification region in the data. (Figure 8.4(a)). The Pre is forwarded as L0 to the CTP.
- `pretrig_config_random` A Pre is randomly produced with 10 kHz and forwarded to the CTP as L0. It is intended for debugging if no TOF is available.
- `pretrig_config_full_seq` The L0 L1 sequence from the CTP is extended to a Pre L0 L1 sequence to the TRD. This mode is used for runs triggered by other detectors than TOF.

Besides from this several sub flavours for testing and optimization exist.

A more sophisticated control allowing more states and also publishing the status of the pretrigger is under way [59]. It is based on a pretrigger final state machine daemon (PTFSMD) running on a workernode and 3 plus 3 DIM servers running on the DCS boards of the pretrigger. The DIM servers execute `scsn-command-files`, defining the values of certain registers, as well as readout and publish the individual counter values. The `scsn-command-files` are stored in a unique nfs filesystem mounted by all pretrigger DCS boards. The PTFSMD has a xml file defining the configuration within the different PVSS states in units of `scsn-command-files`. The pretrigger control has been implemented in collaboration with the corresponding experts for the PVSS and the detector.

## 8 Commissioning

This chapter describes the commissioning of the pretrigger in the ALICE experiment. The latency of the system was measured in the laboratory to 280ns. The pretrigger was installed and calibrated. Cosmic runs with an external scintillator and with TOF have shown the performance gain for the TRD in combination with the pretrigger. During the LHC startup the pretrigger system was successfully used as beam monitoring device in ALICE.

### 8.1 Latency

A test system of the pretrigger consisting out of a FEB the CBC and a CCU from the CBB has been set up and synchronized internally (Chap. E). A minimal bias trigger requesting at least one signal not equal to zero at one input of the FEB has been loaded as configuration to the lookuptables of the FEB, the CBC and the CBB CCU. A pulser signal, similar to a PMT signal, has been applied to one input of the FEB with a frequency of 1 kHz. Figure 8.1 shows the result of the latency measurement of the pretrigger system. The yellow signal is the emulated signal of a photomultiplier. This signal has no phase correlation with the clock from the trigger. It is discriminated and synchronized into the trigger clock domain within the FEB (Chap. 6.1). The signal is processed in the LUT of the FEB and forwarded to the CB. After another processing it is forwarded to the CBB - CCU (blue signal). In the trigger processing module of the CBB (Chap. 6.3) the trigger sequence for the supermodule is formed (purple line). The latency from the center of a PMT pulse to the rising edge of the output of the supermodule signal including 2 times 2.5m multimode fiber and 2.5m Ethernet cable is 280ns.

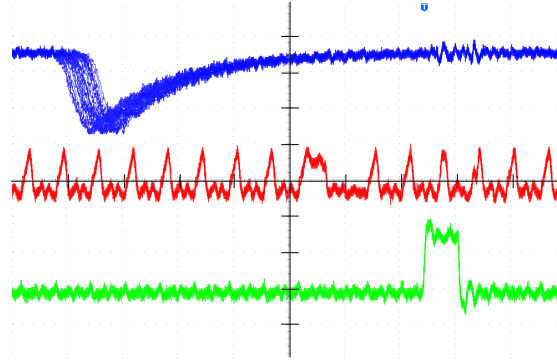
The jitter of exactly 25ns in the PMT signal demonstrates the functionality of the synchronizer circuit. All signals within one acceptance window are processed in the same way as shown by the output of the CB as well as the CCB.

The Figure 8.1 shows that the synchronizer circuit fake trigger probability is smaller than  $10^{-3}$ . The oscilloscope is triggering on the output of the CBC box (blue line). There was no CB box trigger event without a PMT puls within the luminosity time of the oscilloscope (1s). The PMT signal (yellow line ) always shows a puls and never a zero line. This measurement was repeated with oscilloscope luminosities of up to (300s) corresponding to a fake trigger probability of smaller than  $10^{-5}$  without finding any fake trigger.

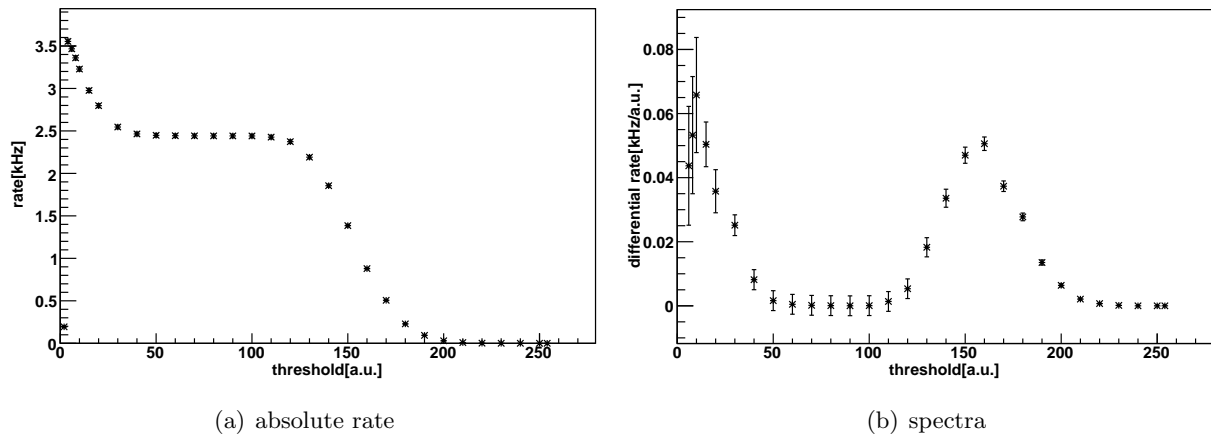
### 8.2 Calibration

For determining the correct values for the thresholds a light pulser was connected to the V0 detector. This LED gave flashes with 2.44 kHz and an intensity equivalent to a minimal ionizing particle [60]. On the pretrigger side a rate measurement with different thresholds was performed. The rate was calculated using the clock counter which is implemented in every Front End Box, thus the time measurement was precise to 25ns. As error the statistical error was taken into account. With the first plot it is possible to determine the dark rate for a given threshold by subtracting the nominal pulser rate of 2.44 kHz from the measured rate. When operating in the threshold region between 40 and 110 this is below 100 Hz.





**Figure 8.1:** Trigger latency between the input of the FEB and the output of the CCB (Oscilloscope Screen Shot  $t = 40ns/div$   $U = 2V/div$ ). 2.5 m Ethernet Cable has been used between FEB and CB and 2.5 m fiber between CB and CCB. yellow: PMT, blue: output of FEB, purple output of CCB



**Figure 8.2:** Pulse rate and spectra of V0 A side Sector 0 channel 5 with a 2.44 kHz pulser and nominal HV at the photomultiplier of the V0 detector

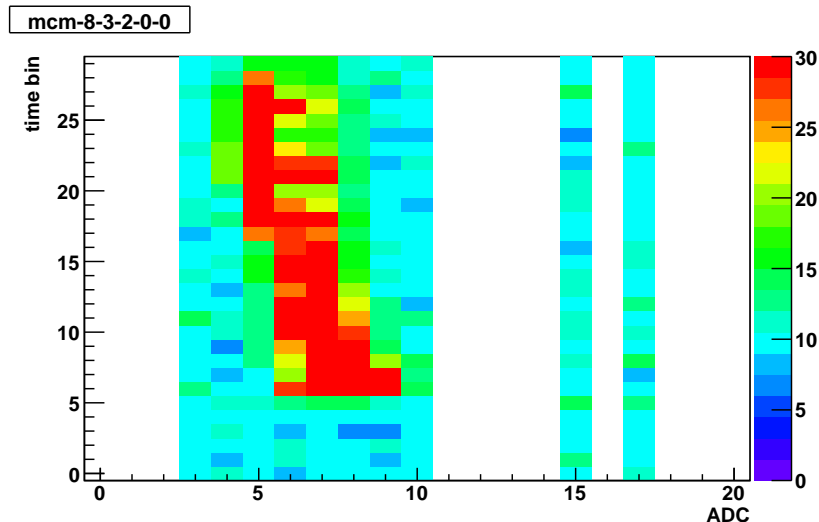
Figure 8.2 shows the pulse spectra obtained from Fig. 8.2 by differentiating. The figure is composed by two components. The first is the noise from PMTs. It is related to the first peak at the threshold of 10 and is almost zero at thresholds larger than 50. The second component is the Gauss distribution around threshold 160 and is caused by the light pulser. This component is zero for thresholds smaller than 90. By choosing a threshold between 50 and 90 the signal has 100 percent purity and 100 percent efficiency. Everything from the noise component is rejected, but nothing from the signal of a minimum ionizing particle. The decreasing rate with thresholds below 10 is an effect of the protection time of the synchronizer circuit in the FPGA (Chap. 6.1).

The second component is not always visible for every PMT, since it is at higher thresholds. In this case a noise free and 100 percent efficient signal is obtained by setting the thresholds to a value 10 units higher than the threshold where the noise component vanishes or to the maximum value.

Since the commissioning of V0 and T0 has not been finished in August 08 no complete analyzes of the optimal parameters of the threshold has been done so far. The DCS board scripts for the measurement as well as the root files for the analysis and the measurements are on the accompanying CDROM.

### 8.3 Cosmic Run with Scintillator

In March 2008 the pretrigger system was tested using an external scintillator placed on top of the supermodule in Sector 8 in the spaceframe at in the pit of point 2 of the LHC. The scintillator plane was perpendicular to the cathode plane of the TRD chambers. The signal from the scintillator (Picture G.3) was fed into a preliminary version of CBB processed like a TOF signal and forwarded to the supermodule and the CTP. The supermodule was running in a autotrigger mode, that is it generated L0 and L1 internally. The GTU was triggered by the CTP. With this configuration 4 to 5 presamples have been recorded. For further infromation see [35].



**Figure 8.3:** MCM readout showing presamples. Triggered with an external scintillator connected to the pretrigger. ADC is the number of the readout pad of one MCM. It corresponds to the position of the signal. The colour indicates the collected charge. The y-axis indicates the time. One timebin corresponds to  $100ns$ . Plot by Sylvester Radomski.

### 8.4 Cosmic Run with TOF

In the Cosmic run that stated in August 2008 the TOF was used as Pretrigger for cosmic events.

**Setup** TOF was providing signals directly from the detector in the Magnet to the CBTOF Module. There the coincidence trigger decision as described in Tab. 8.1 was evaluated and forwarded as Pretrigger to the CBB. There it is synchronized to the clock and forwarded as pretrigger to the TRD as well as to the CTP. The CTP invoked afterwards a full trigger sequence in the TRD partition which was forwarded to the GTU and to the TRD via the CBB. Typically also the TPC was part of the TRD cluster. The Supermodule configuration used the full internal buffer as well as the cross talk filter as an additional buffer. In total there have been  $900ns$  buffer.

**Pulse Height Spectra** As specified in [73] the CTP waits for L0 contributions up to  $800ns$ . According to [72] the CTP needs another  $300ns$  for a trigger decision. Assuming  $40m$  of fiber between the CTP and the Central Control Box of the Pretrigger results in a delay of  $200ns$ . According to [62] another  $300ns$  latency for the propagation between the Central Control Box and the DCS-board of the supermodule have to be added. Thus in Figure 8.4(a) the L0 trigger from the CTP comes  $1.6\mu s$  after the event. That is at timebin 20. Thus most of the drift time of a particle can not be seen by using only the L0 trigger from the CTP (Fig. 8.4(b)). As Figure 8.4(a) shows it was possible to get 20 more samples by using the full buffer of the MCMs, 9 Samples, and

LTMU configuration of the pretrigger in run 62274

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((S0A OR S0C OR S17A OR S17C) AND
(S7A OR S7C OR S8A OR S8C OR S9A OR S9C OR S10A OR S10C)) OR
((S1A OR S1C OR S16A OR S16C) AND (S8A OR S8C OR S9A OR S9C)) OR
(S0A OR S0C OR S17A OR S17C OR S8A OR S8C OR S9A OR S9C)

---



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**Table 8.1:** TOF configurations used during the cosmic run 2008. Each supermodule of TOF (S0 to S17) is segmented into four quadrants. Two on the A side two on the C side. One quadrant of each side provides inputs to the TLMU. The configuration is based on [61] with later extensions. It basically implements a coincidence trigger of two TOF quadrants.

the Pretrigger system, 11 samples. In the current configuration where a maximum of 24 Samples are used this is the main fraction. Subtracting the 900ns of the buffer from the beginning of the puls high distribution in Figure 8.4(a) the latency of the pretrigger signal from the event to the front end electronics can be estimated to 500ns. See also Fig. 3.4.

trigger statistics run 62274

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clock cycles	484655078043
deadtime cycles	5266391
number of Pre to TRD	18159
number of L0 from CTP	16832
number of L1 from CTP	436
number of Pre from TLMU	35410
number of L0 without Pre	0
number of Pre without L0	2755
duration of run (in s)	12116
relative deadtime of TRD (in %)	0.00108
Pre rate at TRD (in Hz)	1.49876
L0 rate from CTP (in Hz)	1.38923
L1 rate from CTP (in Hz)	0.03599
trigger rate from LTMU (in Hz)	2.92258
Pre efficiency to L0 (in %)	100
Pre purity to L0 (in %)	83.63

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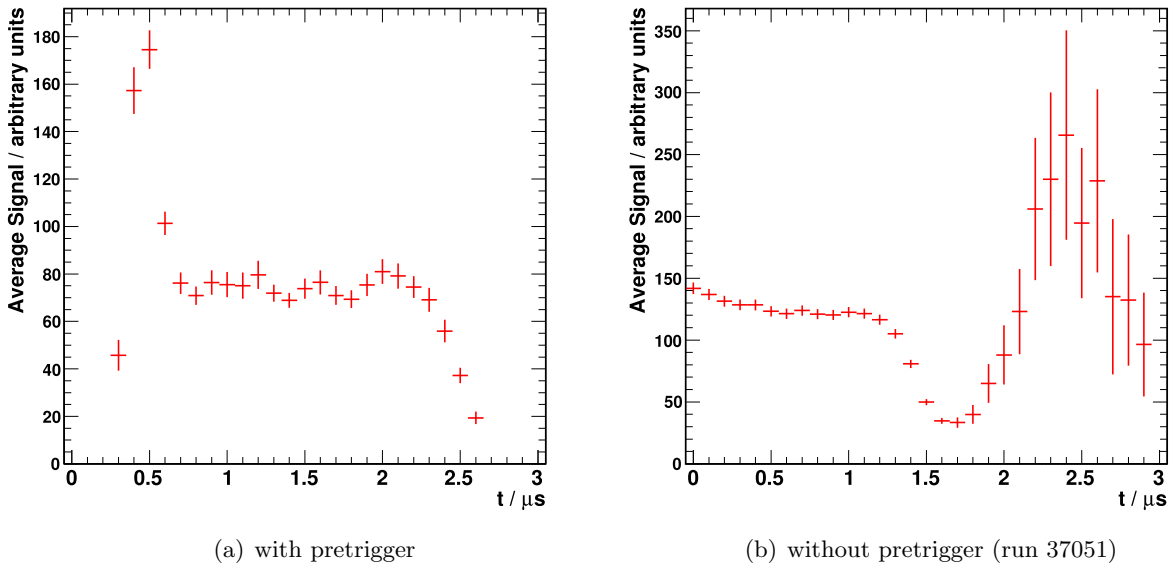


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**Table 8.2:** Trigger statistics of run cosmic 62274 from 20:45 until 23:13 obtained with the pretrigger.CTP configuration: TRD by TOF trigger class; L1 by TRD.

**Trigger Statistics** Table 8.2 shows the trigger statistics of the cosmic run 62274. The trigger rate of 2.922 from LTMU fits into the picture of the cosmic rate of 6 Hz for full TOF acceptance Hz as calculated in [61] and the rate of 8 Hz as measured by TOF [63]. The rate of the TLMU is decreased compared to TOF measurement since only half of the TOF modules had an interface to the TLMU. Also the TOF configuration has a different trigger condition. The multigap resistive plates of TOF have a dark rate of 0.2 Hz per  $cm^2$  [63] this result in fake triggers increasing the 6 Hz real cosmic rate to 8 Hz measured rate.

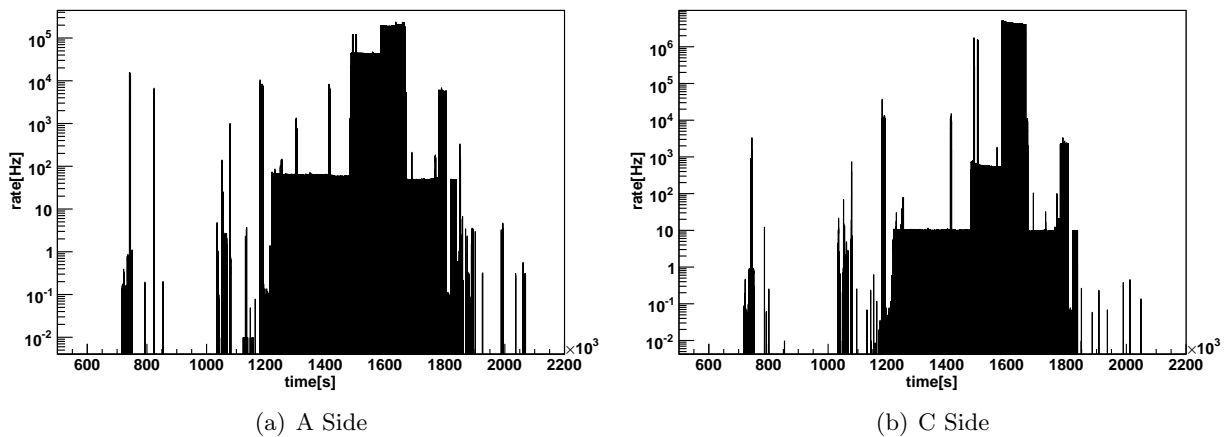
The pretrigger has the expected 100% efficiency since the TRD pretrigger was the only L0 trigger in the TRD cluster in the CTP. Any value apart from 100% would indicate a noisy connection between the CBB and the CTP. Only 48% respectively 51% of the LTMU trigger have been accepted by the CTP and the trigger processing logic forwarding the Pre to the TRD. This is expected because of the past-future protection of the CTP and the pretrigger busy in the trigger



**Figure 8.4:** Pulsheight distribution in the TRD detector with and without a pretrigger signal. The data has been taken in the cosmic run April 2008. The noise in the run without pretrigger is still under investigation. One explanation might be that the autotrig configuration of the supermodule, starts the digitalization at high clock speeds too early. Thus noise might be induced into the PASA.

processing logic alternatively. The 84% purity of the Pre is well above the 51%. This indicates that sometimes more than one event are registered by the TLMU within the pre to next time of  $550\text{ns}$ . The TRD received less Pre from the TLMU than L0 that have been exclusively triggered by the LTMU received from the CTP. The number of Pre forwarded to the TRD is different than the number of L0 received from the CTP. Even if both have been triggered by the same input from TLMU. This is caused by the different deadtime of the trigger processing logic in the pretrigger system and the past-future protection in the CTP. The low rate for the L1 trigger algorithm [64] is still under investigation.

**Random Trigger as Pretrigger** While TOF was not available a relatively high 10 kHz random trigger was used as pretrigger and L0 input to the CTP in combination with a L1 decision from TRD. The hope was to get through the high pretrigger and L0 rate by accident a suitable pretrigger for a cosmic event. The TPC was excluded in this run since it cannot deal with such high L0 rates. The maximum pretrigger rate until the TRAP chips of the TRD front end electronics crash have experimentally been defined to 20 kHz. Within a 10 minute run no L1 accept was received. The expected cosmic rate with this random pretrigger is calculated as follows. For a pretrigger being useful and fitting to the thresholds of the L1 trigger (see [64]) the cosmic has to penetrate the detector within a  $500\text{ns}$  time window starting  $650\text{ns}$  before the pretrigger (Chapter 3.2). With 10kHz pretrigger rate 0.5% of the time is suitable for a cosmic event. The real cosmic rate of 6 Hz is thus reduced to 0.03 Hz. Taking the L1 efficiency of 1.23% (using 8.2 and assuming 100% LTMU efficiency) the rate is furthermore reduced to 0.00036 Hz. That is one detected cosmic in 45 minutes. A random trigger is thus no alternative, also for heavy ion collisions, to a physics motivated pretrigger.



**Figure 8.5:** Beam activity at Point 2 during LHC commissioning. Total particle rate from V0 A side and V0 C side. 1033600s corresponds to 10th September 2008 1000. One measurement per 100s. The detected particles are mainly from beam-gas interactions. The spikes come from lost or dumped beam next to the ALICE detector. The A side has a higher rate than the C side, since the V0 C side detector is partly protected from beam-gas events by the muon absorber.

## 8.5 Beam Monitoring

The TRD Pretrigger System was used together with the V0 detector to monitor the beam activity at Point 2 during LHC commissioning. All other gas detectors including TRD have been in a safety mode not taking any data. The results are presented at Fig. 8.5(a) and Fig.8.5(b). The plot shows the accumulated rate of the V0 detector for both sides. The rates are influenced by beam-gas interactions as well as by particles produced while the beam was dumped. All spikes before 1033600s are caused by injection tests from the SPS to the LHC. After that the number of bunches injected into the LHC and the beam circulation time increased. Thus the baseline rate increased. The spikes result from beam dumping or beam loss around the ALICE experiment. In general the rate at the C side is lower, since many beam-gas events have been absorbed by the muon absorber and other detector, while the beam-gas particles on the A side could penetrate through the V0 detector from both sides. In addition the V0C has roughly 10% smaller active area. But this alone does not explain for the base rate difference of a factor of 10 between V0 A-side and V0 C-side.

## 9 Summary and Outlook

The Transition Radiation Detector (TRD) in the ALICE experiment at the Large Hadron Collider (LHC) of CERN requires a trigger signal 500ns after an event, that is 1μs before the first trigger decision by the ALICE experiment. The design for this pretrigger, using 88 analogue inputs from the V0 and T0 detector and interfacing an additional 576 digital input from TOF via an external unit, has been developed and implemented in the L3-magnet of the ALICE experiment. The information is processed by 27 FPGAs, mounted at a distance of 1.5m to 4.5m around the interaction point, plus 1 additional FPGA. The pretrigger system was successfully commissioned during several data taking periods with ALICE using cosmic events and a first circulating proton beam at LHC injection energy in Sep. 2008.

Trigger signals have been provided to the Central Trigger Processor of ALICE. The system is highly flexible to account for different physics conditions in  $pp$  and Pb + Pb collisions by the implementation of lookup tables. A more sophisticated DCS controlled system, providing graphical interfaces and a finite state machine for user friendly operation is under development [59]. As a next step the trigger must be implemented into the offline framework of the ALICE experiment for efficiency calculations and optimization.

With the system presently available, successful data taking with the Transition Radiation Detector is expected for the upcoming LHC run with  $pp$  collisions at  $\sqrt{s} = 10TeV$  scheduled for spring 2009.

# A Variables for Trigger Characterization

## A.1 Purity and Efficiency

Efficiency and Purity are quantities for the quality of a trigger. Efficiency is defined as

$$\xi = \frac{N_{found}}{N_{avail}}$$

. Where  $N_{found}$  is the number of events that have been correctly triggered and  $N_{avail}$  is the number of physics events that should have been identified by the trigger. Purity is defined as

$$\chi = \frac{N_{total}}{N_{avail}}$$

. Where  $N_{total}$  is the total number of event fired by a trigger. This include correctly identified and fired triggers as well as triggers that have misidentified an event. Whenever a read out electronics is triggered this goes along with a period in which the electronics cannot receive any trigger. This time is called deadtime. If the purity is getting low the total deadtime increases. By this physics events, appearing in the deadtime, cannot be triggered. Thus the efficiency is decreased.

## A.2 Rapidity and Multiplicity

**Rapidity** is a Lorentz invariant concept to describe the velocity component of a particle along the beam direction. It can be added like velocities in non relativistic physics. The pseudo rapidity is more suitable for the experiment, since it is mass independent. For high momentum of the particles  $E = \sqrt{p^2c^2 + m^2c^4} \rightarrow E = pc$  both values are equivalent.

$$y := \frac{1}{2} \ln\left(\frac{E + p_z c}{E - p_z c}\right) \approx \frac{1}{2} \ln\left(\frac{p + p_z}{p - p_z}\right) = \frac{1}{2} \ln\left(\frac{1 + \cos(\theta)}{1 - \cos(\theta)}\right) = -\ln\left(\tan\left(\frac{\theta}{2}\right)\right) := \eta$$

Where  $z$  is the direction of the beam line and  $\theta$  the angle between the particle the interaction point and the beam line.

**Multiplicity** is the number of particles per unit rapidity  $dN/dy$ . For Non-identified particles the number of particles per pseudo rapidity  $dN/d\eta$  is used instead.

## A.3 Centrality

Centrality describes how much overlap two colliding particles have in a collision. Within theory this is parametrized by the impact parameter defined as the minimal distance of the center of two nuclei within a collision. In the experiment the total multiplicity of an event is determined by the number of binary collisions. A binary collision is defined as the collision between two nucleons. Thus the total multiplicity is higher for more central events. The events are classified into centrality classes by their total multiplicity. The centrality class  $x\%$  to  $y\%$  contains the  $y$  percent of all events with the largest total multiplicity without the  $x$  percent of all events having

the largest total multiplicity. The maximum impact parameter  $b_c$  for the  $x\%$  of the events with the largest multiplicity is obtained by solving

$$x = \frac{\int_0^{b_c} \frac{d\sigma_{in}(b')}{db'} db'}{\sigma_{in}}$$

where  $\frac{d\sigma_{in}(b')}{db'}$  is the differential cross section and  $\sigma_{in}$  the total inelastic cross section. By this the interval of impact parameters of a certain trigger class is calculated.



## B Technology

### B.1 FPGA

A Field Programmable Gate Array (FPGA) is a logical electric device producing digital output according to digital input and a certain logic. This logic is programmable with the programming language vhdl among others.

Internally a FPGA is built out of cells, connection networks and more specialized devices. Each cell consists out of a lookuptable with a preceding register. The lookuptables have typically 2 to 4 inputs and one output. The principle is the same as it is used in the pretrigger. The individual inputs and outputs of the cells, the specialized devices and the inputs and outputs of the FPGA chip itself are connected among each other by activating the transistors of the specific connection. The number of cells, their speed as well as the number of available devices depend on the type of FPGA. XILINX FGPA's have typically at least one Delayed Clock Manager (DCM) special device as well as 4 or more memory blocks with 16 kBit capacity. A DCM increases the quality of a clock signal (duty cycle correction, clock delay compensation on the FPGA and shaping of the edges). It also provides clock signals with higher or lower frequencies. A hardware logic was implemented into the FPGA by the following steps.

1. Program the design in VHDL
2. Generate a programming file for the FPGA
3. Simulate and verify the functionality of the design
4. Verify the functionality of the design by doing measurements on the hardware

For the first three steps the XILINX development environment ISE 9.2 has been used for the Spartan FGPA's. The Excalibur from Altera on the DCS board has been changed using the Quartus 4.2 software from Altera.

Figure B.2 shows the trigger processing logic within the development. The random pulses and the missing busy signal on the left side are caused by oscillating registers because of mismatched setup and hold times. On the right side these problems are solved by optimizing the design as well as the synthesis. Problems with setup and hold times have been quite common with the pretrigger since the hardware is running on its speed limit to reduce the latency.

### B.2 LVDS

Low Voltage Differential Signal (LVDS) is a standard for signal transmission on the hardware level. Receiver and transmitter are connected via two cables. On the receiver side the two cables are connected by a  $100\Omega$  resistor. The transmitter drives a current from nominal  $+ - 350mA$  through the resistor in the receiver. A signal change changes the direction of the current. The potentials of the cables are typical 1.05V and 1.40V. Thus a high signal is indicated by a voltage drop of  $350mV$  at the receiver side while a low signal is indicated by a voltage drop of  $-350mV$ . Since LVDS signals transmit their information via current they are more resistant against external distortions. This is the hardware protocol used for standard Ethernet connections in the computer.

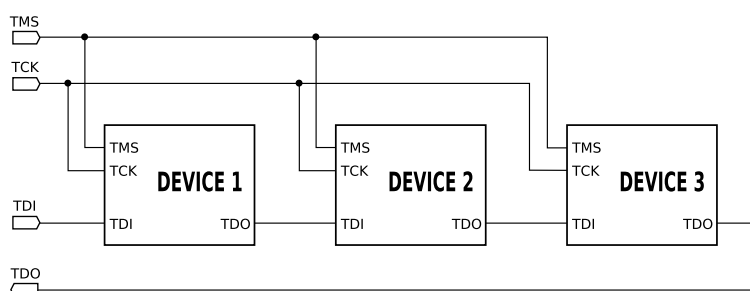


## B.3 ECL

Emitter Coupled Logic (ECL) is a standard for signal transmission on the hardware level. The output of an ECL device provides a high current source or a low current source to the input of an ECL device depending on the logical level that is transmitted. The current is drawn between a potential of  $0V$  on the transmitter and  $-5.2V$  on the receiver. The hardware is implemented using emitter transistor circuits. ECL has switching time down to  $200ps$ .

## B.4 JTAG

JTAG describes a hardware protocol for writing and reading data to a chain of devices requiring 4 lines per device. It was especially developed to configure and debug integrated circuits. Figure B.3 illustrates the principle of the jtag bus.



**Figure B.3:** Principle of the jtag bus. The TMS, TCK, TDI and TDO lines are connected to a jtag master device configuring the devices (DEVICE 1, DEVICE 2 and DEVICE 3). The graphic was taken from [74]

Four lines TMS, TCK, TDI and TDO are connected to the jtag master device. The clock line TCK provides the clock of the master device to all jtag slaves in the chain. The jtag master device injects the data to the chain via the TDI port of the first device. All devices forward the input of their TDI via an internal shift register driven by TCK to their TDO. The last device returns the data, that now also contains the read back values, to the jtag master device. The devices process or manipulate the data in the shift register according to the state of their internal jtag final state machine (FSM). This FSM changes its state with each rising edge of TCK. The next state is always determined by the level of the TMS device. By knowing the type, number and sequence of devices in the chain the jtag master injects data in a way that every device in the chain obtains data specific to it.

Each DCS board (Chap. 7.1) has a jtag master device. This device is addressed via the `/dev/jtag` device. For the pretrigger this device has to be replaced by the `/dev/jtagfeb` device because of the long jtag cables. A \*.bin file from the XILINX ISE (see above) is uploaded to the FPGA via the DCS board by the following steps:

1. use the Xilinx tool ISE to generate a mydesign.bit file
2. use the Xilinx tool impact to generate a \*.svf file out of the \*.bit file
 

```
echo 'setmode -bscan
naddDevice -p 1 -file mydesign.bit
nsetCable -port svf -file
mydesign.svf
nProgram -p 1 -defaultVersion 0
nquit' > impact_input;
Xilinx92i/bin/lin/impact -batch impact_input
```

 If more then one device is in the chain repeat the addDevice and Program commmands

3. use the Xilinx tool impact to generate a mydesign.xsvf file for the DCS board (make sure you use the here specified parameters)  

```
echo 'svf2xsvf -d -fpga -rlen 128 -i mydesign.svf -o mydesign.xsvf  
nquit' > impact_input;  
Xilinx92i/bin/lin/impact -batch impact_input
```
4. change the jtag kernel driver on the DCS board  

```
rmmod jtag; insmod jtagfeb.o
```
5. select the correct port of the jtag master device  

```
echo 'x' > /dev/jtagssel (Chap. C.1)
```
6. copy the file on the DCS board and upload it via the jtag master device  

```
./playxsvf -t /dev/jtagfeb mydesign.xsvf
```

To check the jtag chain the jtag command [53] on the DCS board might be used.

## B.5 SCSN

The slow control serial network is a standard protocol used in the TRD detector to control and configure the MCMs [69]. The protocol is designed to be reliable and scalable. SCSN is a ring protocol, meaning all devices have one data in and one data out line that are sequentially connected to each other. The ring is closed via the master device that is connected with its output to the data input line of the first device in the chain and with its data input to the output line of the last device in the chain. The master is implemented in the DCS board and can send packages containing a register address, a datum and a hop counter into the ring. The first slave receives the package from the master, decreases the hop counter and forwards it afterwards to the next slave in the chain. Whenever a slave receives a package with the hop counter value of zero it extracts the address and the datum from the package and forwards them to its electronics. When a slave has extracted a package it indicates this by setting a bit in the package and sends the package back into the chain to the next slave. The package goes through the chain and comes back to the master. By checking the content of the package and the processing bit the master can check if the package has arrived correctly at the electronics of the slave. For redundancy each slave is connected to the next slave or the master via two lines. If one line is broken it can be replaced by the backup line. This mechanism is software controlled for more details see [53].

## B.6 DIM

DIM is a protocol for the control and supervision of devices in a Ethernet network. It was developed for the LEP experiment at CERN. Each device is running a DIM server. This server publishes different services. Each service is a number or a string indicating a status of the device. In addition the DIM server provides command channels for receiving commands to control the device. DIM clients, programs to control the DIM devices, receive the data from the DIM devices and send commands via the command channel to them. If the devices register itself to a DIMDNS server running on a computer in the network the DIMDID software provides access to all services and command channels. A more detailed description can be found [70].

# C DCS Board Update

## C.1 Firmware

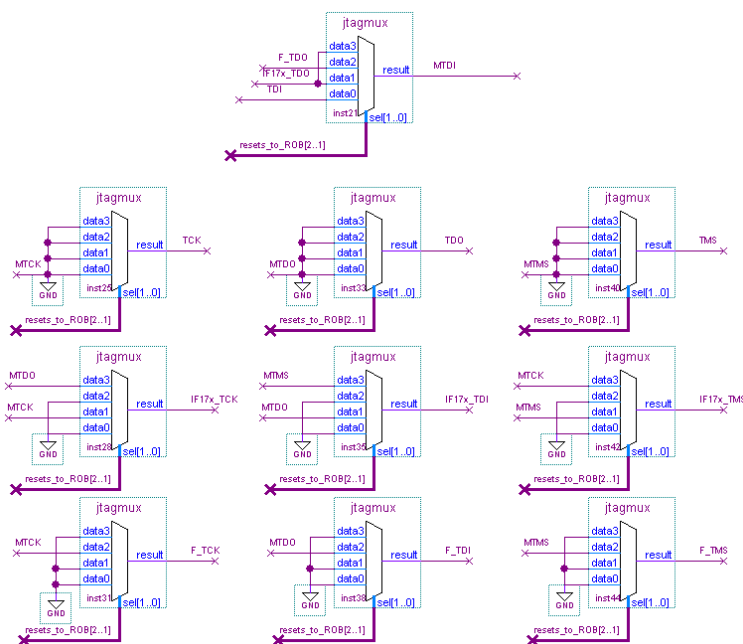


Figure C.1: The multiplexer of the jtagline on the DCS board.

The jtag output of the DCS board jtag master is multiplexed into four lines to meet the different jtag topologies for the pretrigger system. The master provides the lines MTDS, MTDO, MTCK, MTDI.

1. Line 0 (data0) is the standard line. It is for a jtag connection between two DCS boards. This is used to recover DCS boards from a total breakdown. This redundancy is used among the DCS boards in the supermodule as well as between the primary and backup DCS board of one control box of the pretrigger.
2. Line 1 (data1) is forwarded to the FEBS at CBA and CBC and connected to TLMU at the CBB. This line has the right line mapping to access the TLMU.
3. Line 2 (data2) accesses the jtag lines connected to CBA, CBB and CBC FPGAs.
4. Line 3 (data3) is forwarded to the FEBS at CBA and CBC and connected to TLMU at the CBB. This line has the right line mapping to access the FEBS.

## **C.2 Kernel Driver**

The jtag multiplexer is controlled via the `/dev/jtagsel` device on the DCS board. The `jtagsel` device is a subdevice of the `/dev/resetrob` device. The common driver of both devices has the major number 124. Minor number 0 is dedicated to `/dev/resetrob` and minor number 1 accesses the `/dev/jtagsel` device. The code for the driver is in the DCS board repository [54] folder `resetrob`. A different jtag line is selected via `echo 'x' > /dev/jtagsel` where `x` is a number between 0 and 3 identifying the jtagline (Fig. C.1).

# D CheshireCat Manual

This chapter summarizes the commands for the pretrigger configuration. All commands are executed via the command `./CheshireCat <command>` on the DCS boards of the pretrigger system.

## D.1 Control Box B

### TIN proxy no x = 0..5

set mode CTP inputs	CB_write 20+x 0..3	0 normal mode 1 toggling mode 2 send signature (83+x) 3 send random trigger
read mode CTP inputs	CB_read 20+x	
random trigger threshold	CB_write 30+x	0.. 2147483648

### Synchronizing the inputs

#### CB A

set latching edge	CB_write 200 0..1
set delay	CB_write 201 0..31
rate measurement	CB_read 202

#### CB C

set latching edge	CB_write 210 0..1
set delay	CB_write 211 0..31
rate measurement	CB_read 212

#### T0

set latching edge	CB_write 220 0..1
set delay	CB_write 221 0..31
rate measurement	CB_read 202

#### T1

set latching edge	CB_write 230 0..1
set delay	CB_write 231 0..31
rate measurement	CB_read 232

#### T2

set latching edge	CB_write 240 0..1
set delay	CB_write 241 0..31
rate measurement	CB_read 242

<b>T3</b>	
set latching edge	CB_write 250 0..1
set delay	CB_write 251 0..31
rate measurement	CB_read 252
<b>T4</b>	
set latching edge	CB_write 260 0..1
set delay	CB_write 261 0..31
rate measurement	CB_read 262
<b>T5</b>	
set latching edge	CB_write 270 0..1
set delay	CB_write 271 0..31
rate measurement	CB_read 272
<b>T6</b>	
set latching edge	CB_write 280 0..1
set delay	CB_write 281 0..31
rate measurement	CB_read 282
<b>T7</b>	
set latching edge	CB_write 290 0..1
set delay	CB_write 291 0..31
rate measurement	CB_read 292
<b>GTU Busy</b>	
first edge sel	CB_write 303 0..1
xor clk phase	CB_write 304 0..1
set latching edge	CB_write 300 0..1
set delay	CB_write 301 0..31
rate measurement	CB_read 302
<b>timing analyzer</b>	
clear timing analyzer	CB_write 600 1..0
set trigger pattern	CB_write 602 0..65535
active timing analyze	CB_write 601 1..0
read timing analyze	CB_read 16384 ... 16895
	CB_analyzer_read
done timing analyze	CB_read 603
<b>Trigger processing</b>	
TOF signal to scintil	CB_write 130 0..7
clk TTCex shifts	CB_write 99 0..3
disable GTU BUSY	CB_write 399 0..1
disable SOR EOR busy	CB_write 499 0..1
scintillator en	CB_write 100 0..1
LUT as pre en	CB_write 101 0..1
CTP as pretrig en	CB_write 102 0..1



L0 en	CB_write 103 0..1	
L1 en	CB_write 104 0..1	
LUT L0 to CTP en	CB_write 120 0..1	
scintillator to CTP en	CB_write 121 0..1	
Pre from LUT to CTP en	CB_write 122 0..1	
Software trig to CTP en	CB_write 123 0..1	
pre to next cycles	CB_write 106 1..65536	
L0 to next cycles	CB_write 107 0..65536	set to (desired rising'edge to rising'edge time) minus 3
L1 to next cycles	CB_write 108 0..65536	set to 0 (minimal L1-rising'edge to next pre-rising'edge = 2) set to (minimal L1_rising'edge to next pre-rising'edge) minus 4
L0 autogen	CB_write 109 0..1	
L1 autogen	CB_write 110 0..1	
B channel disable	CB_write 48 0..1	
TTCex clk disable	CB_write 49 0..1	
LUT L0 en	CB_write 120 0..1	
pre as L0 en	CB_write 121 0..1	
dissable trigger to SM	CB_write 199 0..1	
software trigger en	CB_write 105 0..1	
software trigger start	CB_write 350 0/1	
software trigger pattern	CB_write 351 0..255	
sel synchronizer inptut	CB_write 130	0..5: TLMU mult. bits 6: cosmic 7: random trigger
random trigger thresh.	CB_write 0..2147483348	

### Trigger Logic

write data to LUT	CB_write 32768..40959 0..3
read data from LUT	CB_read 32768..40959

### counter module

reset counters	CB_write 50 0..1	
start readout	CB_write 51 0/1	
readout done	CB_read 52	
get low bits	CB_read 6400+no	
get high bits	CB_read 12800+no	0: clock counter 1: pulses to SM 2: dead time 3: pre pulses 4: L0 from CTP 5: L1 from CTP 6: L0 by the LUT 7: not TIN to CTP Pre 8: pattern match cb a 9: pattern match cb c 10: pattern match tof

11: trigger synchronizer  
 12: trigger to SM  
 13: LUT pre  
 14: missing pre  
 15: unnecessary pre  
 28..16: LUT monitoring(12..0)  
 62..29: zero signal(62..29)

match pattern cb a           CB\_write 800 0..15  
 match pattern cb c           CB\_write 810 0..15  
 match pattern tof            CB\_write 820 0..31

## D.2 Control Box A and C

reset CB                      CB\_reset

### FEB input controls

#### T0

pattern sync edge sel        CB\_write 350 0..1  
 pattern sync set delay      CB\_write 351 0..31  
 pattern sync edge rate      CB\_read 352  
 disable FEB input          CB\_write 353 0..1

#### V0

pattern sync edge sel        CB\_write 310 0..1  
 pattern sync set delay      CB\_write 311 0..31  
 pattern sync edge rate      CB\_read 312  
 disabled FEB input         CB\_write 313 0..1

#### V1

pattern sync edge sel        CB\_write 320 0..1  
 pattern sync set delay      CB\_write 321 0..31  
 pattern sync edge rate      CB\_read 322  
 disable FEB input          CB\_write 323 0..1

#### V2

pattern sync edge sel        CB\_write 330 0..1  
 pattern sync set delay      CB\_write 331 0..31  
 pattern sync edge rate      CB\_read 332  
 disable FEB input          CB\_write 333 0..1

#### V3

pattern sync edge sel        CB\_write 340 0..1  
 pattern sync set delay      CB\_write 341 0..31  
 pattern sync edge rate      CB\_read 342  
 disable FEB input          CB\_write 343 0..1

### LUT configuration

LUT data in signal           CB\_write 32768..33791 0..15  
 LUT data out signal         CB\_read 32768..33791 0..15

### pattern generator output to CCB

fiber output pattern mode    CB\_write 360 0/1  
 fiber output pattern         CB\_write 361 0..15

### coincidence analyzer

analyzer pattern sel input   CB\_write 500+(10\*x) 0..4  
 analyzer pattern in         CB\_write 501+(10\*x) 0..3  
 analyzer pattern out         CB\_write 502+(10\*x) 0..15  
 analyzer pattern coinz en     CB\_write 503+(10\*x) 0..1

counter no: x = 1..25  
 inp 0 = T0; inp 1 = V0; inp 2 = V1;  
 inp 3 = V2; inp 4 = V3

### timing analyzer

clear timing analyzer        CB\_write 600 1..0  
 set trigger pattern         CB\_write 602 0..65535  
 active timing analyze        CB\_write 601 1..0  
 read timing analyze         CB\_read 16384 ... 16895  
                               CB\_analyzer\_read  
 done timing analyze         CB\_read 603

### counter readout

counter reset                CB\_write 50 0..1  
 counter readout req         CB\_write 51 0..1  
 counter readout done         CB\_read 52  
 counter value low            CB\_read 6400+(0..62)  
 counter value high          CB\_read 12800+(0..62)

0: clock  
 1..24: analyzer(1..24)  
 25..26: zero  
 27..28: T0 parallized(0..1)  
 29..30: V0 parallized(0..1)  
 31..32: V1 parallized(0..1)  
 33..34: V2 parallized(0..1)  
 35..36: V3 parallized(0..1)  
 37..41: zero  
 42..45: bits to CCB  
 46..62: zero

### FEB controll

select jtag line             echo '3' > /dev/jtagsel  
 load design                 ./playxsvf -t /dev/jtagfeb  
                               febfpga.xsvf

select FEB to configure	CB_write 999 0..7	5 for T0 FEB 1 for V0 FEB 2 for V1 FEB 3 for V2 FEB 4 for V3 FEB 0,6,7 normal trigger operation there is no trigger while configuration reset work only in trigger mode
T0 FEB reset	CB_write 450 0..1	
V0 FEB reset	CB_write 410 0..1	
V1 FEB reset	CB_write 420 0..1	
V2 FEB reset	CB_write 430 0..1	
V3 FEB reset	CB_write 440 0..1	

### D.3 Front End Boxes

#### LUT configuration

LUT data in signal	FEB_write 32768..36863 0..3
LUT data out signal	FEB_read 32768..36863
select outphase	FEB_write 99 0..3

#### Output to CB

fiber output pattern en	FEB_write 360 0/1
fiber output pattern	FEB_write 361 0..15

#### timing analyzer

clear timing analyzer	FEB_write 600 1..0
set trigger pattern	FEB_write 601 0..65535
active timing analyze	FEB_write 602 1..0
read timing analyze	FEB_read 16384 ... 16895
	FEB_analyzer_read
done timing analyze	FEB_read 603

#### counter readout

counter reset	FEB_write 50 0..1
counter readout	FEB_write 51 0/1
counter readout done	FEB_read 52
counter value low	FEB_read 6400+(0..62)
counter value high	FEB_read 12800+(0..62)

0: clock  
1..12: DET sync signal(0..11)  
13: trigger paralell(0)  
14: trigger paralell(1)  
62..15: zero

**set trigger thresholds**

DET update	FEB_write 799 0..1
DET threshold(0)	FEB_write 700 0..255
DET threshold(1)	FEB_write 701 0..255
DET threshold(2)	FEB_write 702 0..255
DET threshold(3)	FEB_write 703 0..255
DET threshold(4)	FEB_write 704 0..255
DET threshold(5)	FEB_write 705 0..255
DET threshold(6)	FEB_write 706 0..255
DET threshold(7)	FEB_write 707 0..255
DET threshold(8)	FEB_write 708 0..255
DET threshold(9)	FEB_write 709 0..255
DET threshold(10)	FEB_write 710 0..255
DET threshold(11)	FEB_write 711 0..255

**set input delays**

DET delay(0)	FEB_write 2200 0..255
DET delay(1)	FEB_write 2201 0..255
DET delay(2)	FEB_write 2202 0..255
DET delay(3)	FEB_write 2203 0..255
DET delay(4)	FEB_write 2204 0..255
DET delay(5)	FEB_write 2205 0..255
DET delay(6)	FEB_write 2206 0..255
DET delay(7)	FEB_write 2207 0..255
DET delay(8)	FEB_write 2208 0..255
DET delay(9)	FEB_write 2209 0..255
DET delay(10)	FEB_write 2210 0..255
DET delay(11)	FEB_write 2211 0..255

**set input sampling phase**

DET phase reg signal(0)	FEB_write 2100 0..3
DET phase reg signal(1)	FEB_write 2101 0..3
DET phase reg signal(2)	FEB_write 2102 0..3
DET phase reg signal(3)	FEB_write 2103 0..3
DET phase reg signal(4)	FEB_write 2104 0..3
DET phase reg signal(5)	FEB_write 2105 0..3
DET phase reg signal(6)	FEB_write 2106 0..3
DET phase reg signal(7)	FEB_write 2107 0..3
DET phase reg signal(8)	FEB_write 2108 0..3
DET phase reg signal(9)	FEB_write 2109 0..3
DET phase reg signal(10)	FEB_write 2110 0..3
DET phase reg signal(11)	FEB_write 2111 0..3

**input pulser**

pulser mode(0)	FEB_write 2300 0..1
pulser en	FEB_write 2500 0..1
pulser pause after puls(0)	FEB_write 2400 0..255
pulser mode(1)	FEB_write 2301 0..1
pulser en(1)	FEB_write 2501 0..1
pulser pause after puls(1)	FEB_write 2401 0..255
pulser mode(2)	FEB_write 2302 0..1
pulser en(2)	FEB_write 2502 0..1
pulser pause after puls(2)	FEB_write 2402 0..255
pulser mode(3)	FEB_write 2303 0..1
pulser en(3)	FEB_write 2503 0..1
pulser pause after puls(3)	FEB_write 2403 0..255
pulser mode(4)	FEB_write 2304 0..1
pulser en(4)	FEB_write 2504 0..1
pulser pause after puls(4)	FEB_write 2404 0..255
pulser mode(5)	FEB_write 2305 0..1
pulser en(5)	FEB_write 2505 0..1
pulser pause after puls(5)	FEB_write 2405 0..255
pulser mode(6)	FEB_write 2306 0..1
pulser en(6)	FEB_write 2506 0..1
pulser pause after puls(6)	FEB_write 2406 0..255
pulser mode(7)	FEB_write 2307 0..1
pulser en(7)	FEB_write 2507 0..1
pulser pause after puls(7)	FEB_write 2407 0..255
pulser mode(8)	FEB_write 2308 0..1
pulser en(8)	FEB_write 2508 0..1
pulser pause after puls(8)	FEB_write 2408 0..255
pulser mode(9)	FEB_write 2309 0..1
pulser en(9)	FEB_write 2509 0..1
pulser pause after puls(9)	FEB_write 2409 0..255
pulser mode(10)	FEB_write 2310 0..1
pulser en(10)	FEB_write 2510 0..1
pulser pause after puls(10)	FEB_write 2410 0..255
pulser mode(11)	FEB_write 2311 0..1
pulser en(11)	FEB_write 2511 0..1
pulser pause after puls(11)	FEB_write 2411 0..255

### temperature readout

temperature readout	FEB_read 1000	values 0..16383
---------------------	---------------	-----------------

## E Synchronization of the Pretrigger System

The pretrigger system is synchronized and made operational by the following steps. The x values depend on the specific part. The values can be found in the appendix. A @FEB command is executed by setting the FEB box at the CB to which it is connected to configuration mode (./CheshireCat CB\_write 999 1..5) and executing it at the CB. Load the designs

- cd /dcsnfs/pretrigger
- switch to the jtag driver for long cables (rmmod jtag; insmod jtagfeb.o)
- load CCB (@CCB ./playxsvf -t /dev/jtagfeb cbtofhans.xsvf)
- load CB (@CB echo '2' > /dev/jtagsel; ./playxsvf -t /dev/jtagfeb cbcfpga.xsvf)
- load FEB (@CBC echo '3' > /dev/jtagsel; ./playxsvf -t /dev/jtagfeb febfpga\_chain.xsvf)

Synchronize the pretrigger system internally Synchronize a FEB to a CB.

- set FEB to configuration mode (@CB ./CheshireCat CB\_write 999 1..5)
- FEB inputs to pulser (@FEB ./FEB\_sync.sh)
- Disable all pulser except for no 0 (@FEB ./FEB\_sync.sh)
- Set pulser\_period no 0 to 15 (@FEB ./FEB\_sync.sh)
- Configure LUT to forward inputs from input 0 as 1 to CB (@FEB ./FEB\_sync.sh)
- @FEB check trigger paralell(0) increases and trigger paralell(1) stays equal (use FEB\_counter\_readout.sh)
- set FEB to trigger sending (@CB ./CheshireCat CB\_write 999 0)
- toggle latching edge (@CB CB\_write 3x0 0/1) of the FEB if pattern\_sync\_edge\_rate of the FEB (./CheshireCat CB\_read 3x2) is not constant.
- add pattern\_sync\_delay (@CB CB\_wirte 3x1 ) if x\_paralized\_signal(0) does not increase or x\_paralized\_signal(1) increases (@FEB ./FEB\_counter\_readout.sh).

synchronize a CB to the CCB

- send synchronization pattern to the CCB (@CB ./CheshireCat CB\_write 361 1; ./CheshireCat CB\_wirte 361 3)
- change latching edge (@CCB ./CheshireCat CB\_write 2x0 1/0) if rate\_measurement (@CCB ./CheshireCat CB\_read 2x2) is not constant
- send alignment pattern to the CCB (@CB ./CheshireCat CB\_wirte 361 1; ./ChehsireCat CB\_write 361 4)
- configure alignment pattern detection at CCB (@CCB ./CheshireCat CB\_write 8x0 4)

- add delay (@CCB ./CheshireCat CB\_wirte 2x1 0..31) if match\_pattern\_cb\_x(1) signal does not increase like clock\_counter

Synchronizing to the beam.

- request a low luminosity run
- check the status of V0 and T0 detectors
- set FEB to configuration mode (@CB ./CheshireCat CB\_write 999 x)
- adjust sampling phase (@FEB ./CheshireCat CB\_wirte 210x 0..4) if not sufficient the delay in steps of 4(@FEB ./CheshireCat CB\_write 220x 0..3) of the detector inputs. All signals must be coincident. Use the timing analyzer to check (@FEB ./CheshireCat FEB\_analyzer\_readout).
- set the FEBs to a minimum bias trigger (@FEB ./CheshireCat FEB\_LUT\_config\_min\_bias)
- set all FEBs to trigger mode (@CB ./CheshireCat CB\_write 999 0)
- synchronize the FEBs at a CB: add pattern\_sync\_delay (@CB ./CheshireCat CB\_write 3x0 0/1) in steps of 4 if FEBs are not aligned (@CB ./CheshireCat analyzer\_readout)
- set all CBs to trigger mode (@CB ./CheshireCat CB\_wirte 360 0)
- synchronize the CBs at CCB: add pattern\_sync\_delay (@CCB ./CheshireCat 2x1 0..31). All signals must be coincident. Use the timing analyzer to check (@CCB ./CheshireCat FEB\_analyzer\_readout).

According to Chap. 6 the latency is reduced by shifting the clock domain instead of delaying a signal.



## **F Shifters Manual Cosmic Run Dec 2007**

Within this thesis a temporary trigger setup for the ALICE cosmic run in December 2007 has been built on the DCS-board FPGA. This design only provided an delayed L0 as pretrigger. The MCMs of the TRD produced the L0 and L1 automatically.

# Operate TRD (Pre)Trigger in Cosmic Run Dec07

Stefan Zimmer

December 4, 2007

## 1 Overview

This system should work. Normaly you don't need to do anything with it.

The way of trigger signals: CTP(Central Trigger Processor) - LTU(Local Trigger Unit) - Pretrigger - Supermodule

The CTP gets signals from all detectors and makes the first trigger decision. For cosmic run it will mainly use Accorde (the scintillators on top of the magnet).

In cosmic run the Pretrigger only passes the trigger signal to the Supermodules. In real experiment it has to produce a wake up signal for TRD before the first trigger of CTP so that TRD can contribute to the trigger decision. For this the pretrigger has direct connection to inner detectors (V0 and T0).

Log into the PCs in the Alice Control Room (ACR) and to the computers in the Working rooms next to it:

user:trd pw:xxx In case of problems call Stefan: 162860 from any CERN phone.

## 2 How to operate

### 2.1 Switch on/off Pretrigger Power

```
ssh -X trd@alitrdown005 pw:xxx  
/home/trd/pretrigger/pt-monitor
```

right click to switch on/off reference values:

ch0	ch1	ch2	ch3	ch4	ch5
7V	7V	5V	5V	7V	7V
5.7A	0.3A	-0.1A	0.1A	-0.1A	0.1A

### 2.2 Operate the LTU (our Acces to the Central Trigger (CTP))

```
ssh -X trd@alidcscom026 pw:xxx  
vmecrate trd click: Configuration  
click: setGLOBAL - get Triggers from CTP  
click: setSTANDALONE - enable CTP Emulator
```

### 2.3 Configure Pretrigger

```
ssh root@alitrddcbpt05 pw:xxx [dcs0028]  
reconf  
This does not reset the counters
```

## 3 Diagnostics

### 3.1 Does the Pretrigger System gets Triggers from CTP?

```
ssh root@alitrddcbpt05 pw:xxx [dcs0028]  
ttxrx_regs e  
Look at event counter:  
L0 signal makes 1 event  
L1 signal makes 2 events
```

L2a makes no event

### 3.2 Does the Supermodule get Triggers?

```
ssh root@alitrddcb0801 pw:xxx [logs into Supermodule 08 on stack 0 and layer 1]
ttxrx_regs e
look at event counters; for current DB config every L0 Trigger makes one event. All other trigger pulses (L1, L2a) are suppressed
```

### 3.3 Is TRD busy?

What does the busy signal means? If the TRD detector cannot record more data, since the memory is full, it sends a busy signal to the CTP. If the CTP recives a busy signal from any detector it stops sending triggers. That means if the TRD sends a busy signal to CTP all other detectors get no triggers. Thus they will not be able to record any data.

```
ssh -X trd@alidcscom026 pw:xxx
vmecrate trd
click: scope Signals
click: B
click: LTU Busy (output) (our busy is produced by GTU)
If the B has a red background we are busy
```

If slash has a blue background: click to update display.

### 3.4 How to send a Trigger Sequence to all Supermodules?

```
ssh -X trd@alidcscom026 pw:xxx [LTU]
vmecrate trd
Click: Configuration - setSTANDALONE
Click: CTP Emulator
Click: Sequence select select: L2a.seq
Click: Load Sequence
Click: start emulation (configure emulator)
```

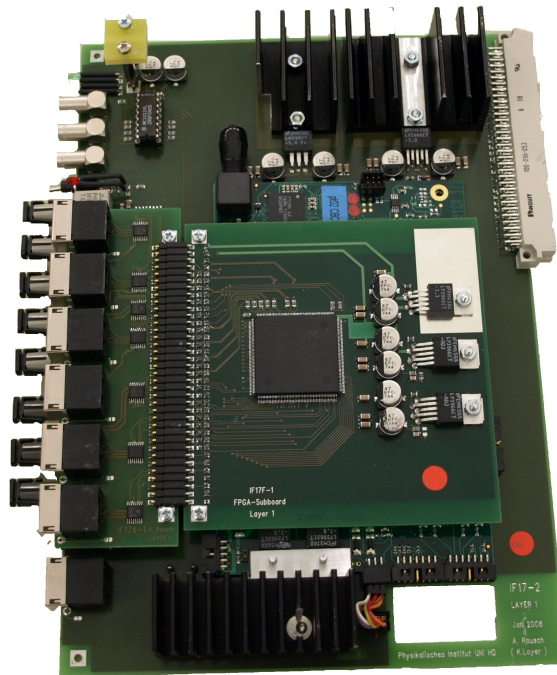
Set: #of signals 1

Click: Generate SW 'start signal(s)

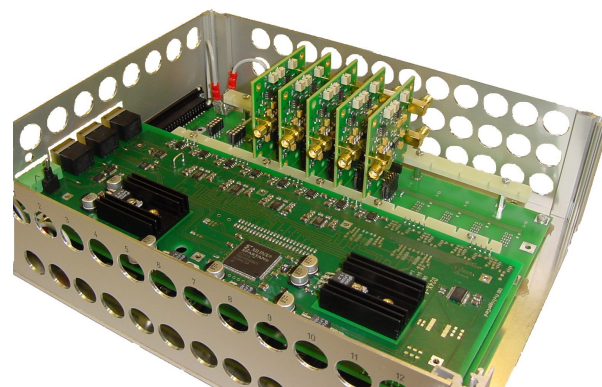
Now you send a whole trigger sequence (3 pulses equals 3 event) to the pretrigger. In current configuration you send so one puls (equals one event) to the SM.

Don't forget to set the LTU in global mode again (setGLOBAL in Configuration menu) to participate in the normal run.

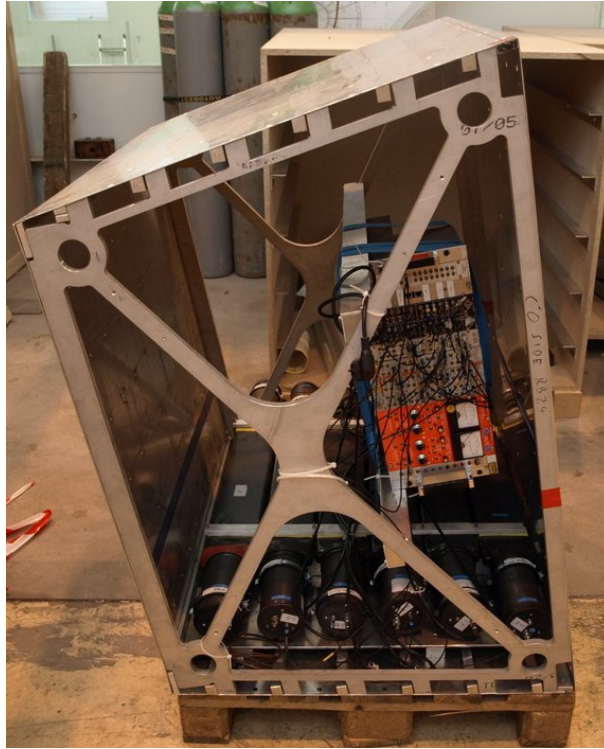
## G Pictures



**Figure G.1:** Pretrigger mother board (PMB) with detector control board (DCS board) and the Cheshirecat unit (CCU-FPGA) mounted on top of the PMB . Six of these CheshireCat Unit (CCU) are used within the 3 control boxes (CBA, CBB, CBC)



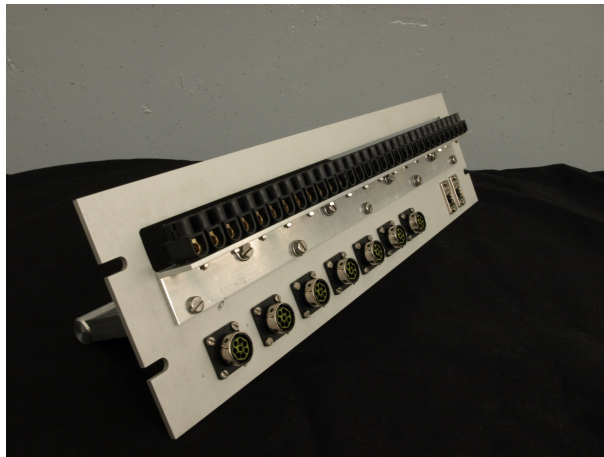
**Figure G.2:** One FEBU housed in an opened FEB with 5 preamplifier. The unit consists out of a primary system (large board) and a backup system(mounted board). 10 of these FEBU build the pretrigger interface to the V0 and T0 detector.



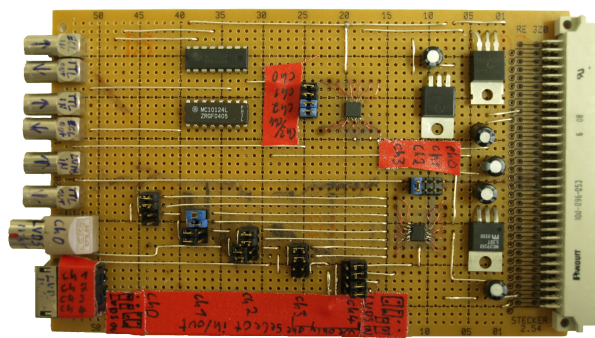
**Figure G.3:** Scintillator mockup used within the cosmic run April 08. The trigger is formed via a coincidence of two scintillators on top of each other in the bottom side. Mokuup construction by mechanical workshop. Scintillator installation Minjung Kweon.



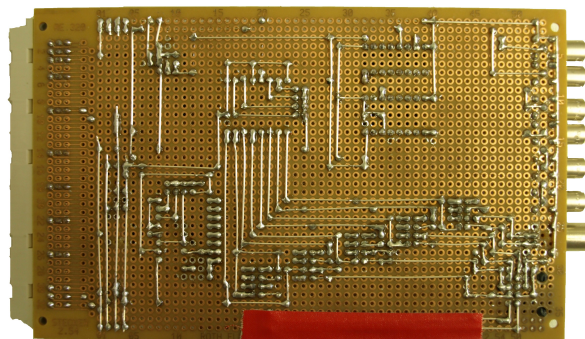
**Figure G.4:** The ALICE TRD as it was presented at opening days at CERN in April 2008. On the right side: Opened TRD multiwire proportional chamber. Center right: One out of 18 TRD supermodules partly equipped with chambers. Center Left: TRD chambers with mounted front end electronics (Readout boards equipped with MCMs) performing the gas leak test (see K). Left behind the cabin: Place and electronics for supermodule testing and the pretrigger development.



**Figure G.5:** Patch panel for the pretrigger low voltage and Ethernet connection to the miniframe.



**Figure G.6:** VME card for LVDS to TTL and TTL to LVDS conversion. Also some ECL to TTL and TTL to ECL converter are mounted. The jumper configure the operation. Top view.



**Figure G.7:** LVDS to TTL converter board bottom view.



**Figure G.8:** Frequency generators. At one end of a cable a unique frequency is feed into each cable of the bunch. On the other side of the bunch the cables are identified via a frequency measurement with an multimeter between cable and ground.



**Figure G.9:** Shunt resistor for the supermodule burn in test (Chap. 5.2). Bended V4A steel from Hornbach. High currents cause measurable voltage drops also over thick copper cables. This voltage drop has been used to efficiently check various connections in the low voltage cabling.



# H Schematics of the Infrastructure

This chapter outlines the overall signal cables as well as the low voltage infrastructure of the pretrigger system.

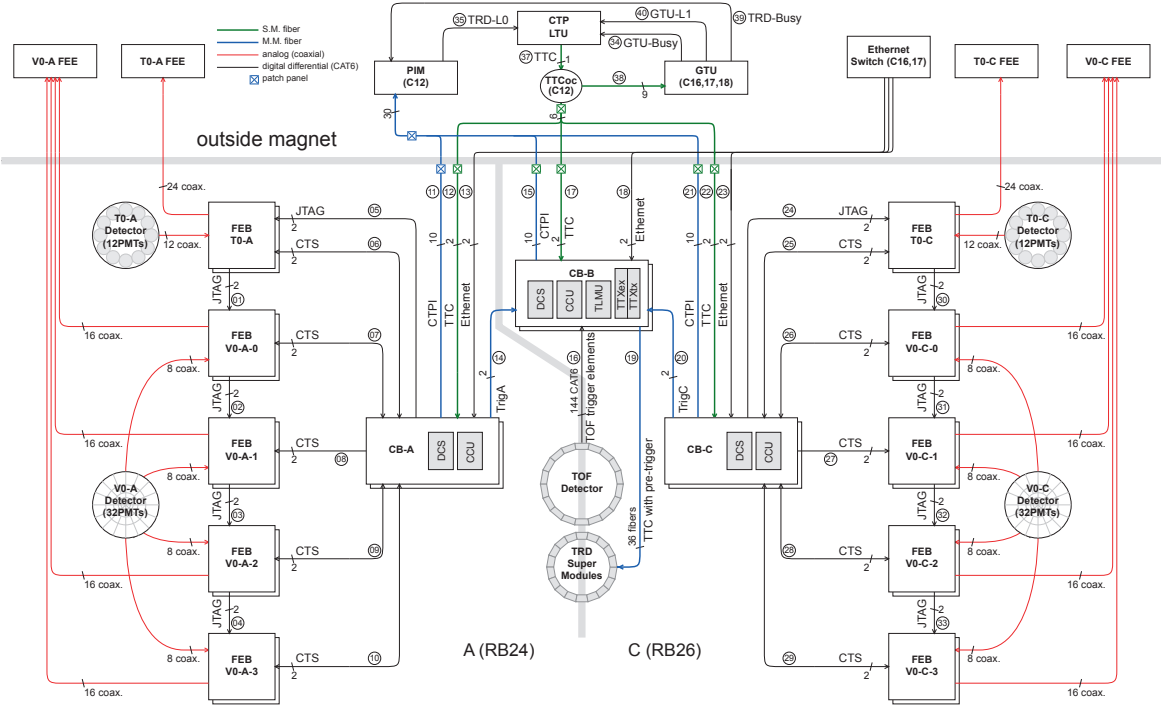


Figure H.1: Signal cable of the pretrigger system.

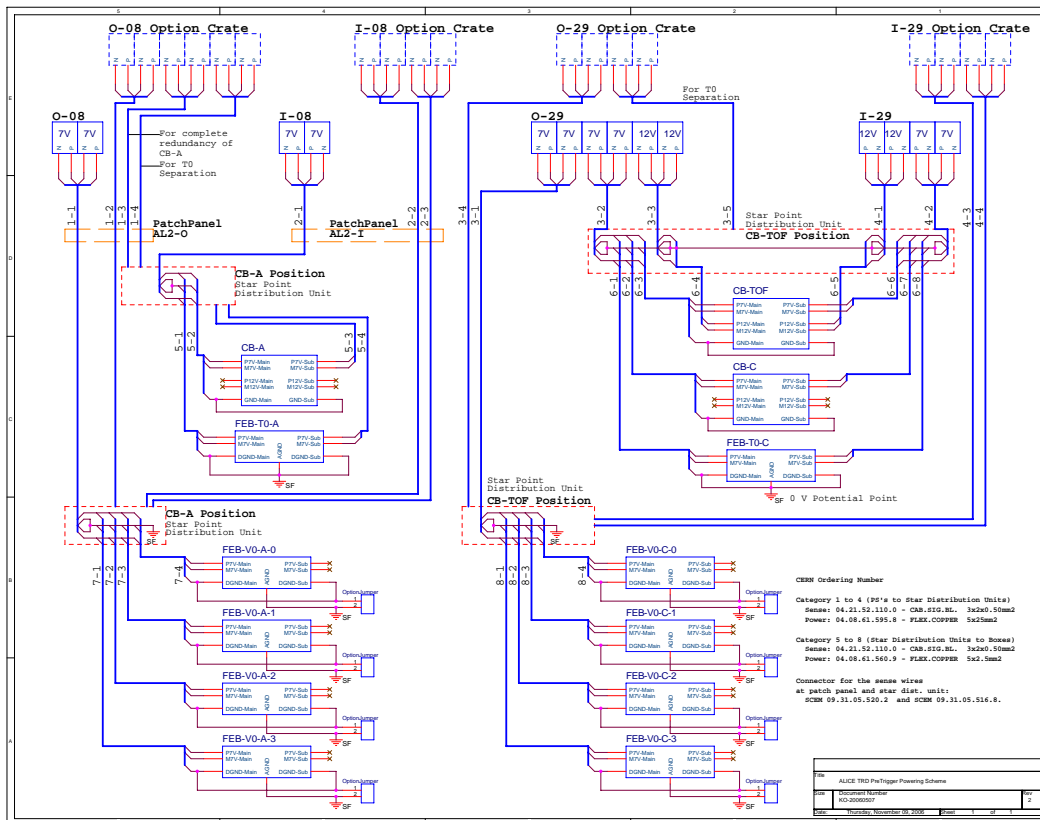


Figure H.2: Low Voltage Services of the pretrigger system.

# I HeidelbergHouse Booking System

The HeidelbergHouse Booking System [67] helps to administrate the house of the TRD group in StGenis. It is an internet web page written in php and html with an underlying mysql database and connection to a email server.

Whenever a person is looking for a room at CERN she/he asks for a room by marking a room on the days she/he wants to stay in the house. After he has authenticated himself by her/his email address and a password the room owner, responsible for one room, receives an email from the booking system with the request. The room owner follows the link and selects if she/he wants to approve or disapprove the request. After the room owner has authenticated with her/his password the owner and the person who has requested the room get an email from the system indicating the status of the room. Simultaneously the status is displayed on the webpage. If the room owner requests her/his room the request is automatically the confirmation. By this procedure the room owner, typically a person with a project at CERN, is privileged. Whenever she/he needs a room he does not accept a request and uses the room for himself. In addition the system summarizes the costs a person has to pay for utilities(1 Euro per day) and displays it on a private page for every registered user. The user is asked to put the money into the house cash and to receipt the payment by clicking a button on the page. This is done on mutual trust, but a log is kept in the database.

select year:  select month:  select day:

day	date	couch	jail	jura	leman	piano	tent	wonderland
Sunday	2008-05-25	<input type="checkbox"/> book	<input type="checkbox"/> book	OB	jkl	SZ	<input type="checkbox"/> book	<input type="checkbox"/> book
Monday	2008-05-26	<input type="checkbox"/> book	KS	OB	jkl	SZ	<input type="checkbox"/> book	MJ
Tuesday	2008-05-27	<input type="checkbox"/> book	KS	OB	jkl	SZ	<input type="checkbox"/> book	MJ
Wednesday	2008-05-28	<input type="checkbox"/> book	KS	OB	jkl	SZ	<input type="checkbox"/> book	MJ
Thursday	2008-05-29	<input type="checkbox"/> book	<input type="checkbox"/> book	OB	jkl	SZ	<input type="checkbox"/> book	MJ
Friday	2008-05-30	<input type="checkbox"/> book	OB	PC	jkl	SZ	<input type="checkbox"/> book	MJ
Saturday	2008-05-31	<input type="checkbox"/> book	OB	PC	jkl	SZ	<input type="checkbox"/> book	<input type="checkbox"/> book
Sunday	2008-06-01	<input type="checkbox"/> book	OB	PC	jkl	SZ	<input type="checkbox"/> book	MJ
Monday	2008-06-02	<input type="checkbox"/> book	RG	PC	jkl	MJ	SZ	OB
Tuesday	2008-06-03	<input type="checkbox"/> book	RG	PC	jkl	fer	SZ	MJ
Wednesday	2008-06-04	<input type="checkbox"/> book	<input type="checkbox"/> book	PC	jkl	fer	<input type="checkbox"/> book	MJ
Thursday	2008-06-05	<input type="checkbox"/> book	<input type="checkbox"/> book	PC	jkl	<input type="checkbox"/> book	<input type="checkbox"/> book	MJ
Friday	2008-06-06	<input type="checkbox"/> book	<input type="checkbox"/> book	PC	jkl	<input type="checkbox"/> book	<input type="checkbox"/> book	MJ
Saturday	2008-06-07	<input type="checkbox"/> book	PC	KK	SV	<input type="checkbox"/> book	<input type="checkbox"/> book	<input type="checkbox"/> book
Sunday	2008-06-08	<input type="checkbox"/> book	PC	KK	<input type="checkbox"/> book	<input type="checkbox"/> book	<input type="checkbox"/> book	<input type="checkbox"/> book
Monday	2008-06-09	<input type="checkbox"/> book	SV	KK	jkl	<input type="checkbox"/> book	<input type="checkbox"/> book	MJ

booking means: you get the room on that day you book after 1 p.m. and have to leave it the next day before 12 a.m.

I do a working trip

[persons behind the initials](#)

color code of the initials:

grey: you asked for the room, but the roomowner has not approved your booking so far.

red: the room is reserved for you, but you have not paid so far

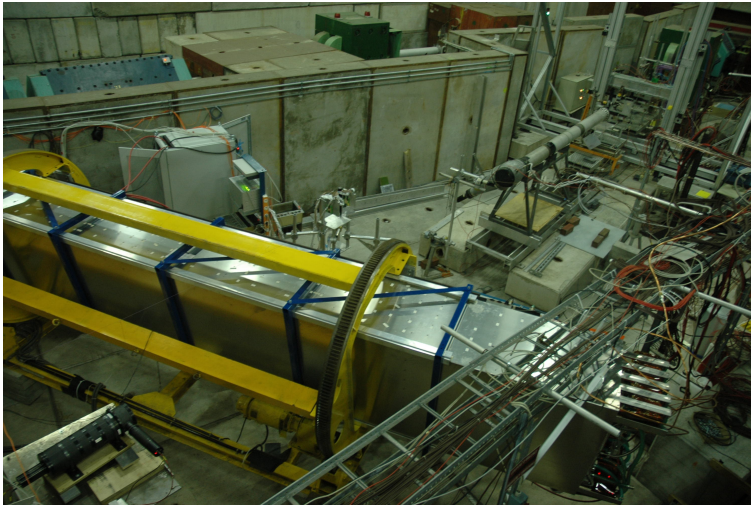
black: everything is ok. You paid and you are allowed to go into the room

[back to heidelberghouse page](#)

Figure I.1: Webshot from the HeidelbergHouse booking page.

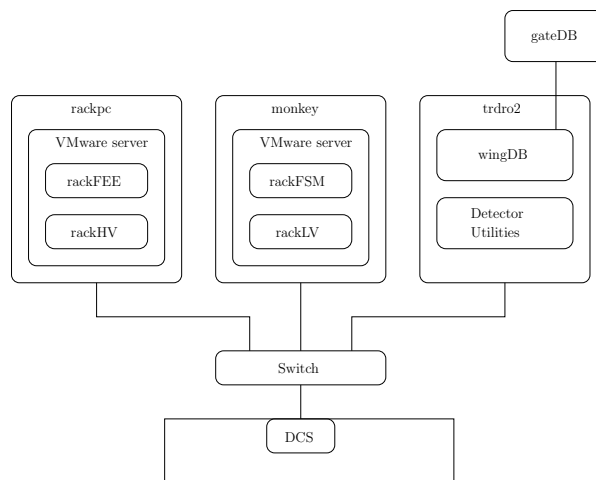
## J Test Beam

Figure J.1 shows the TRD in the test beam in November 2007. The aim of this testbeam was to show the functionality of the TRD as well as to get reference data for the electron and pion separation <sup>3</sup>.



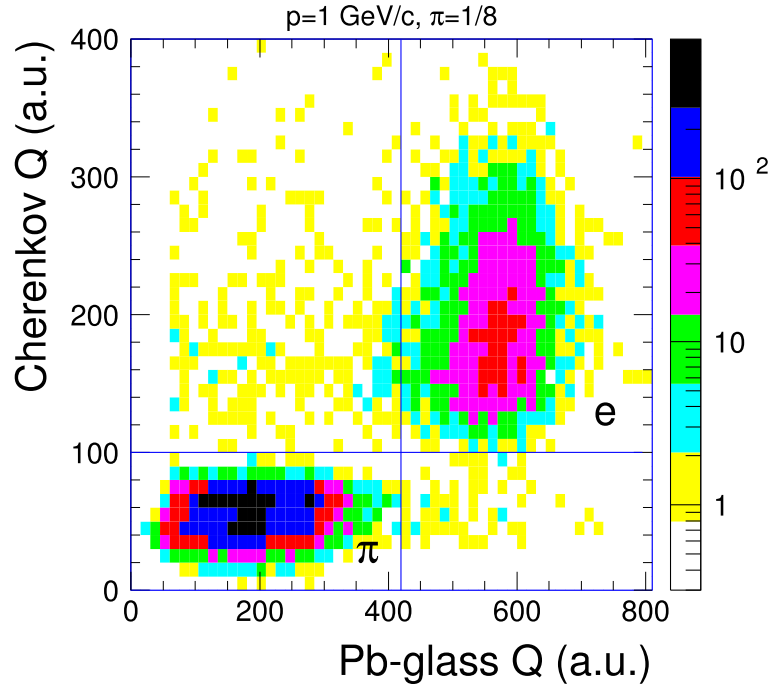
**Figure J.1:** TRD detector in the test beam.

The setup was established at the SPS at CERN (Chap. 2.1) at beamline T10 [68]. The proton beam from the SPS was dumped by a target and the secondary particles were forwarded by an optical system of magnets. to the experimental zone T10 where the TRD was irradiated with these particles. The momentum of the particles at T10 were defined by the magnetic field of the optical system. As trigger for the detector a scintillator was used.



**Figure J.2:** Computer infrastructure for the test beam Nov2007. The same setup is now used in the cleanroom at CERN. A similar one in the laboratory in Heidelberg.

To identify the particles as electrons or pions the particles passed first to the TRD through a Cerenkov detector filled with atmospheric air. After passing the TRD they were detected by a lead glass calorimeter. In addition to this a silicon detector for beam position and culmination monitoring was used. The TRD was running at this time with a  $Xe/CO_2$  gas mixture. According to the Frank-Tamm formula the irradiated Cerenkov radiation increases with the speed of a particle. Thus electrons deposit more energy in the Cerenkov detector than pions at a given momentum.



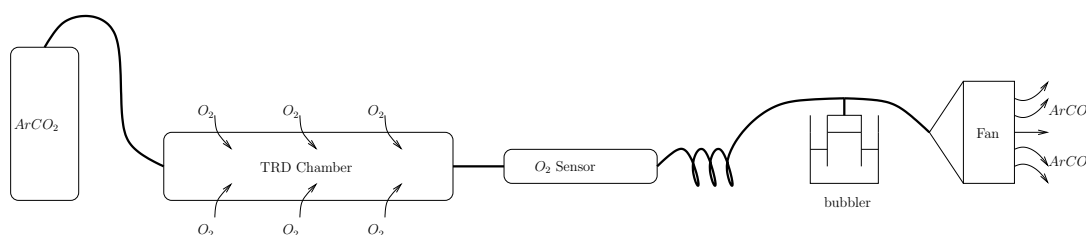
**Figure J.3:** Electron and Pion separation in a testbeam using a lead glass and a Cerenkov detector. The axes show the charge measured by the photomultiplier of each detector. The incident electrons and pions had a momentum of 1 GeV/c. 1 out of 8 pions have been an electron. The plot was taken from [27].

Since the pions are not fully stopped in the calorimeter they do not deposit as much energy as the electrons in the calorimeter. Both phenomena give a clear TRD independent signature for electrons and pions J.3 what is used for the optimization of various particle identification algorithms (see 3). The data have been used to train neural networks among others. The computer infrastructure controls the TRD (high voltage, low voltage, temperature, status of the front end electronics) and configures the TRD based on data from the detector construction. The detector construction data is centrally stored from all detector construction places in the gateDB a postgresql database running in Heidelberg. From there the gate2wing script [66] extracts the data and builds a configuration for the TRD front end electronics which is locally stored in the wingDB. The wingDB is based on the database engine from ORACLE. All PVSS projects for the detector control are installed on virtual windows PCs hosted by two VMWARE servers (Fig. J.2). More details are documented in the TRD Software Wiki [66]. Within this thesis the computer infrastructure for the TRD has been set up one time at CERN for the testbeam and one time in Heidelberg for DCS development. In addition help to the general installation of the testbeam setup has been provided. PVSS and the PVSS projects were installed and set up by the corresponding experts. The computer infrastructure from the testbeam is reused for TRD supermodule testing at CERN (see [58]). In addition several shifts have been taken as shifter and shift leader during the test beam. During the test beam it has been realized that the chambers of the TRD have not been totally leak tight. If the detector gas had an under pressure compared

to the surrounding atmosphere,  $O_2$  from the atmosphere contaminated the detector gas. Since the electrons from the ionization process of the penetrating particle attached to the  $O_2$  the pulse height spectra was destroyed. Especially the peak from the transition radiation 3 was lost because these electrons have the longest drift time through the detector gas. If the detector gas had an overpressure of 0.1 mbar the attachment was gone. The  $O_2$  from the atmosphere could not flow into the chambers any more since now the detector gas ( $Xe/CO_2$ ) was flowing from the chambers to the atmosphere. This mode was suitable for the test beam, but it cannot be used for the long run of TRD in ALICE since Xe is a very expensive gas. One bottle of 50 l with 200 bar costs around 50 000 CHF.

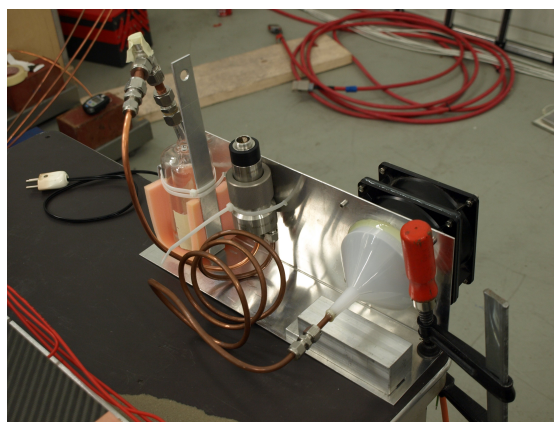
## K Sensitive Leak Test for Gas Chambers

During the testbeam it was realized that the methods used to test the gas tightness of the TRD chambers were not precise enough. Within this thesis a new more sensitive method to test the tightness of chambers has been proposed and a first prototype has been built together with the group.



**Figure K.1:** Setup for the gas leak test of a TRD Chamber. The fan produces an under-pressure in the chamber, thus the oxygen from the atmosphere goes through a leak of the chamber. The oxygen meter is sensitive up to 4ppm, therefore also very small leaks can be detected.

Figure K.1 illustrates the principle of the sensitive leak test. The chamber is flushed with  $ArCO_2$  gas at a low flow of 20l/h. Two computer fans pull the  $ArCO_2$  out. Thus the chamber reaches an under pressure compared to the surrounding atmosphere of 1mbar. The under pressure is monitored with a bubbler. If a chamber has a leak  $O_2$  from the atmosphere flows into the chamber, that is detected by the  $O_2$  sensor. A coil out of copper pipe between the bubbler and the sensor prevents  $O_2$  from back diffusion through the fans to the  $O_2$  sensor. According to the  $O_2$  content in the  $ArCO_2$  the leak rate of a chamber is calculated [58]. Typical values for a tight chamber are 50ppm oxygen. Typical Oxygen meters as they are used within detector construction have a error of about 4ppm. Figure K.2 shows the first prototype of the setup. Later compressors have been used instead of the computer fans. The test is now used at all camber production and testing locations. The chambers are reglued as long as the Xe leakrate of a supermodule is below 3l/h at atmospheric pressure for a working TRD supermodule [65].



**Figure K.2:** Prototype of the under pressure leaktest for the TRD chambers

# L Content of the CDROM

- VHDL code of the pretrigger system
- DCS-board Software of the pretrigger system
- DCS-board updates
- Scripts for the calibration, operation and synchronization of the pretrigger
- Calibration data files taken with the pretrigger
- Root Macros to evaluate the data files
- Vhdl code of the DCS-board as it was used in the Cosmic Run December 2007
- Copy of the TRD Software Wiki documentation for the computer infrastructure of the TRD detector
- HeidelbergHouse Management System; database files and webpage files



# Bibliography

- [1] F. Karsch, Lattice QCD at high temperature and density, Lect. Notes Phys., vol. 583, pp. 209, 2002.
- [2] R. Hagedorn, Nuovo Cim. Suppl. 3 (1965) 147.
- [3] X. Zhu et al., Phys. Lett. B647 (2007) 366.
- [4] P. Braun-Munzinger, J. Wambach, Physik, Extreme Materie Journal 5(2006) 10.
- [5] C.-Y. Wong, Introduction to High-Energy Heavy-Ion Collisions, World Scientific Publishing Co. Pte. Ltd, 1994.
- [6] S. Hands, The Phase Diagram of QCD, arXiv:physics/0105022v1.
- [7] A. Andronic et al., Nucl. Phys. A789 (2007) 334.
- [8] P. Braun-Munzinger and J. Stachel, Nucl. Phys. A690 (2001) 119c.
- [9] H. Satz, Colour deconfinement in nuclear collisions, Rept. Prog. Phys., vol. 63, p. 1511, 2000.
- [10] J. Adams et al., Experimental and theoretical challenges in the search for the quark gluon plasma: The STAR collaboration's critical assessment of the evidence from RHIC. collisions, Nucl. Phys., vol. A757, pp. 102, 2005.
- [11] Alice physical performance report.
- [12] J.LU, L. ZHOU, W. MA and X. HE, Quark, Gluon, Odderon Contributions to Total Cross Section of Proton-Proton Elastic Scattering at High Energies, Commun. Theor. Phys. (Beijing, China) 49 (2008) pp. 207 c Chinese Physical Society.
- [13] A. Donnachie, H. G. Dosch, O. Nachtmann, The missing Odderon, hep-ph/0508196v1.
- [14] O.Nachtmann, Pomeron Physics and QCD, arXiv:hep-ph/0312279v1.
- [15] R.Schicker, Low mass diffractive systems at LHC, Crimea 2007 Conference Proceedings.
- [16] R.Schicker, The ALICE detector and trigger strategy for diffractive and electromagnetic processes, arXiv:0807.1472v1.
- [17] V.P. Goncalves and M.V.T.Machado, Diffractive photoproduction of heavy quarks in hadronic collisions, PHYSICAL REVIEW D 75, 031502(R) (2007).
- [18] D. Manglunki, PS Div. CERN (2001). <http://ps-div.web.cern.ch/ps-div/PS/complex/accelerators.pdf>.
- [19] ALICE Collaboration, <http://aliceinfo.cern.ch/Public/en/Chapter2/Chap2Experiment-en.html>.

- [20] E. Evans et al., The ALICE central trigger system, Real. Time Conference, 2005. 14th IEEE-NPSS, ISBN: 0-7803-9183-7
- [21] ALICE: Physics performance report, volume II, J. Phys. G 32 (2006) 1295-2040.
- [22] Jean-Yves Ollitrault, Relativistic hydrodynamics for heavy-ion collisions, arXiv:0708.2433v2.
- [23] R. Kuiper and G. Wolschin, From RHIC to LHC: A Relativistic Diffusion Approach, Brazilian Journal of Physics, vol. 37, no. 2C, June, 2007.
- [24] J. Nystrand, Photon-Induced Physics with Heavy-Ion Beams in ALICE, arXiv:0807.0366v1.
- [25] Dolgoshein, B. Transition, Radiation Detectors, Nuclear Instruments and Methods in Physics Research A, 326, page 434-469, 1992.
- [26] W. Demtröder Experimentalphysik 3 2. Auflage, Springer.
- [27] ALICE transition-radiation detector : Technical Design Report, CERN-LHCC-2001-021.
- [28] T. Dietel, personal communication, University of Münster.
- [29] Lippmann et al. Position Reconstruction in Drift Chambers operated with Xe, CO<sub>2</sub>(15%), arXiv:physics/0511233v1.
- [30] A. Wilk, Elektron-Pion-Separation im ALICE TRD, Diploma Thesis University of Muenster.
- [31] V. Angelov, personal communication, KIP University of Heidelberg.
- [32] Ken Oyama personal communication.
- [33] F. Rettig, Entwicklung der optischen Ausleseketten für den ALICE-Übergangsstrahlungsdetektor am LHC (CERN), Diploma Thesis, KIP University of Heidelberg.
- [34] ALICE Off-line Project, <http://aliceinfo.cern.ch/Offline/>.
- [35] S. Zimmer Pretrigger Status, TRD comprehensive meeting 2008 Hauenstein <http://indico.cern.ch/contributionDisplay.py?contribId=11&confId=35522>.
- [36] <http://wwwasic.kip.uni-heidelberg.de/asicnew/vision/home/>.
- [37] R. Schicker, TRD comprehensive meeting 2008.
- [38] A. Wilk, personal communication, University of Münster.
- [39] ALICE TDR Forward Multiplicity Detectors.
- [40] ALICE TDR TOF.
- [41] A. Rausch, K. Layer, Electronic Schematics and Mechanical Construction of the Pretrigger [www.physi.uni-heidelberg.de/~rausch/](http://www.physi.uni-heidelberg.de/~rausch/).
- [42] D. Emschermann, TRD Hardware Homepage, [www.physi.uni-heidelberg.de/~demscher](http://www.physi.uni-heidelberg.de/~demscher).
- [43] M. De Gaspari, PhD, Physikalisches Institut University of Heidelberg, in preparation.
- [44] Spartan 3 Datasheet [www.xilinx.com](http://www.xilinx.com).

- 
- [45] V. Angelov, TRAP Manual, KIP Uni Heidelberg.
- [46] Spartan User Guide [www.xilinx.com](http://www.xilinx.com).
- [47] ALICE Central Trigger Processor <http://epweb2.ph.bham.ac.uk/user/pedja/alice/>.
- [48] R. Schicker, TLMU Documentation, Physikalisches Institut University of Heidelberg.
- [49] T. Ludwig, Betriebssysteme und Netzwerke, Script, Institut für Informatik, University of Heidelberg.
- [50] DCS board, KIP University of Heidelberg <http://www.kip.uni-heidelberg.de/ti/DCS-Board/current/>.
- [51] BUSYBOX, [www.busybox.net](http://www.busybox.net).
- [52] , GNUARM <http://www.gnuarm.com/>.
- [53] , T.Krawutschke, Phd, University of Köln.
- [54] , DCS board software, <https://www.kip.uni-heidelberg.de/repos/TI/DCSboard/trunk/>.
- [55] , TIN Proxy, <http://epweb2.ph.bham.ac.uk/user/jusko/>.
- [56] , PVSS at CERN <http://itcobe.web.cern.ch/itcobe/Services/Pvss/>.
- [57] , J. Mercardo, PhD, Physikalisches Institut University of Heidelberg, in preparation.
- [58] , J. Klein, Diploma Thesis, Physikalisches Institut University of Heidelberg, in preparation.
- [59] , S. Schmiederer, Diploma Thesis, Physikalisches Institut University of Heidelberg, in preparation.
- [60] , A.Sandoval, personal communication, Instituto de Ciencias Nucleares Universidad Nacional Autonoma de Mexico UNAM.
- [61] , M. Kwaeon, TRD commissioning meeting 2008.
- [62] , S. Zimmer, TRD Status Meeting GSI April 2008.
- [63] , E. Scapparone, TOF and cosmic ray trigger, <http://indico.cern.ch/getFile.py/access?subContId=3\&contribId=6\&resId=1\&materialId=slides\&confId=26364>.
- [64] , F. Rettig, TRD commissioning meeting 2008.
- [65] , C. Schmitt, TRD commissioning meeting 2008.
- [66] TRD Software Wiki, [https://wiki.kip.uni-heidelberg.de/ti/TRD/index.php/Main\\_Page](https://wiki.kip.uni-heidelberg.de/ti/TRD/index.php/Main_Page).
- [67] HeidelbergHouse Webpage, <http://www.physi.uni-heidelberg.de/~szimmer/>.
- [68] SPS T10 beamline, <http://gatignon.web.cern.ch/gatignon/EastArea/#t10>.
- [69] R.Gareus, Slow Control - Serial Network and its implementation for the. Transition Radiation Detector, Diploma Thesis KIP University of Heidelberg.
- [70] CERN DIM, <http://dim.web.cern.ch/dim/>.

- [71] , \with<http://indico.cern.ch/materialDisplay.py?materialId\=slides\&confId=36951>.
- [72] ALICE CTP Homepage, [http://www.ep.ph.bham.ac.uk/user/pedja/alice/ctp\\\_preliminary\\\_02.ps](http://www.ep.ph.bham.ac.uk/user/pedja/alice/ctp\_preliminary\_02.ps).
- [73] ALICE CTP FEE Requirements,[http://epweb2.ph.bham.ac.uk/user/pedja/alice/ctp/ctp\\\_time.htm](http://epweb2.ph.bham.ac.uk/user/pedja/alice/ctp/ctp\_time.htm).
- [74] Wikipedia, [www.wikipedia.de](http://www.wikipedia.de)
- [75] Schematics of the pretrigger system, <http://www.physi.uni-heidelberg.de/~rausch>.

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## Erklärung

Ich versichere, dass ich diese Arbeit selbständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 20.10.2008

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Stefan Zimmer