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Characterisation of

High Voltage Monolithic Active Pixel Sensors

for the Mu3e Experiment

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Charakterisierung von monolithischen aktiven Pixel-Sensoren in Hochspannungs-Technologie für das Mu3e-Experiment:

Das Standardmodell der Teilchenphysik beschreibt die Elementarteilchen und ihre Wechselwirkungen erstaunlich gut. Jedoch entstehen Theorien jenseits des Standardmodells, da es noch viele offene Fragen gibt.
Das Mu3e-Experiment sucht nach dem Leptonenzahl-verletzenden Zerfall $\mu^+ \rightarrow e^+e^-e^+$, der im Standardmodell stark unterdrückt ist. Deshalb wäre eine Beobachtung dieses Zerfalls ein klarer Hinweis auf neue Physik.
Der Detektor muss für hohe Myonen-Zerfallsraten ausgelegt sein und minimale Vielfachstreuung bewirken um die geplante Sensitivität von $< 10^{-16}$ zu erreichen. Daher werden monolithische aktive Pixel-Sensoren in Hochspannungs-Technologie (HV-MAPS) verwendet. Dies sind neuartige dünne Silizium-Pixel-Sensoren, bei denen die Sensor- und Ausleseelektronik auf dem selben Chip sitzen. Aufgrund der angelegten Hochspannung haben sie eine schnelle Ladungssammlung und können gedünnt werden.
In dieser Masterarbeit wurden HV-MAPS mit Photonen, β-Strahlung und Elektronen bei mehreren Strahltests getestet. Das Signal-Rausch-Verhältnis wurde für verschiedene Temperaturen über Raumtemperatur ermittelt. Dabei wurden Signal-Rausch-Verhältnisse von über 21 gemessen.
Die Effizienz des Mupix4-Prototyps, die aus den Strahltest-Daten berechnet wurde, ist $> 99{,}5\%$ und die Zeitauflösung ist mit einem Wert von 17 ns auch hervorragend.
Außerdem wurden das erste Mal gedünnte Sensoren getestet und sie zeigen gute Betriebseigenschaften.

Characterisation of High Voltage Monolithic Active Pixel Sensors for the Mu3e Experiment:

The Standard Model of particle physics describes the elementary particles of matter and their interactions surprisingly well. However, theories beyond the Standard Model arise because there are many open questions.
The Mu3e experiment searches for the lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ which is highly suppressed in the Standard Model. Therefore, the observation of this decay would be a clear hint for new physics.
The tracking detector has to deal with high muon decay rates and must have minimal multiple scattering in order to achieve the targeted sensitivity of $< 10^{-16}$. Hence, High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are used. These are novel thin silicon pixel sensors where sensor and readout electronics are on the same chip. Due to the applied high voltage they have a fast charge collection and can be thinned.
In this Master thesis HV-MAPS were tested with photons, β-radiation and electrons at several testbeams. The signal-to-noise ratio has been determined for different temperatures above room temperature and signal-to-noise ratios above 21 were measured.
The efficiency of the MuPix4 prototype, determined from testbeam data, is $> 99.5\%$ and the timing resolution has also an excellent value of 17 ns.
In addition, thinned chips have been tested for the first time and show good performance.

Contents

Part I

Introduction

1 Introduction

The Standard Model of particle physics describes all known particles and their interactions surprisingly well. Although the Standard Model has not been disproved yet, it cannot be the final theory because there are many open questions. The gravitation for example is not part of the Standard Model and it cannot explain the large asymmetry between matter and antimatter in the universe [Gri11]. Therefore, searches for theories beyond the Standard model are performed.

The Mu3e experiment searches for the lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$, which is highly suppressed in the Standard Model. The observation of this rare decay would be a clear hint for new physics beyond the Standard Model.

The requirements of the detector are very high because high muon decay rates of 10^9 muons per second are necessary to achieve the target sensitivity of $< 10^{-16}$ in a reasonable time. The detector must have a high momentum and vertex resolution for background suppression. Therefore, thinned High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are used to reduce multiple scattering.

HV-MAPS are based on a charge collecting diode which is operated with high voltage and have a thin depletion zone. Therefore, the charge collection time is short and the chips can be thinned. In addition the sensor and readout electronics are on the same chip so that the material is further reduced. This leads to low multiple scattering which in turn results in a good momentum resolution of the detector. The momentum resolution at the low momenta of the decay electrons of (10 - 53) MeV is dominated by multiple scattering.

In this Master thesis also thinned HV-MAPS prototypes are examined.

2 Theory

In the Standard Model of particle physics lepton flavour has to be conserved. However, neutral leptons, the neutrinos, can change from one flavour into another in a Standard Model extension. Therefore the search for charged lepton flavour violating processes like the decay $\mu^+ \rightarrow e^+e^-e^+$ is ongoing.

This chapter introduces the Standard Model of particle physics and lepton flavour violating muon decays.

2.1 Standard Model of Particle Physics

The Standard Model of particle physics is a theory that describes the elementary particles of matter and their interactions [Gri11]. There are two types of particles: six quarks and six leptons (and their antiparticles). Both the quarks and the leptons are fermions and are grouped in pairs (see figure 2.1).

The first quark generation is composed of the up quark u and the down quark d, the second generation consists of the charm quark c and the strange quark s, and the third generation of the top quark t and the bottom quark b.

The first lepton generation is composed of the negatively charged electron e^- and the neutral electron neutrino ν_e, the second generation consists of the muon μ^- and the muon neutrino ν_μ and the third generation of the tau τ^- and the tau neutrino ν_τ. The lepton flavour numbers of the three generations are L_e, L_μ and L_τ. In the Standard Model the lepton flavour numbers are conserved.

The gauge bosons mediate the interactions between these particles. The gluon is the force carrier of the strong force, the photon γ is the force carrier of the electromagnetic force and the W^+, W^- and Z^0 bosons are the force carriers of the weak force. The gravitation is not part of the Standard Model up to now.

The experiments CMS and ATLAS at the Large Hadron Collider (LHC) at CERN found a scalar, neutral particle with a mass of (125 - 126) $\mathrm{GeV/c^2}$ which is most likely the Higgs boson [Hig12] which was predicted to generate the mass of the W^+, W^- and Z^0 bosons (Higgs mechanism).

Neutrino oscillations, during which one neutrino flavour is changed into another, are lepton flavour violating and have been observed [F$^+$98, A$^+$01, E$^+$03]. It can be incorporated into an extended Standard Model. Because of that, neutrinos must have a small but non-zero mass.

The Standard Model can quite successfully describe all known particles and their interactions but there are still many unanswered questions. The Standard Model cannot explain the large asymmetry between matter and antimatter in the universe. Nor it can explain why there are three generations of elementary particles although all matter around us, namely the atoms, is only made of up and down quarks and electrons.

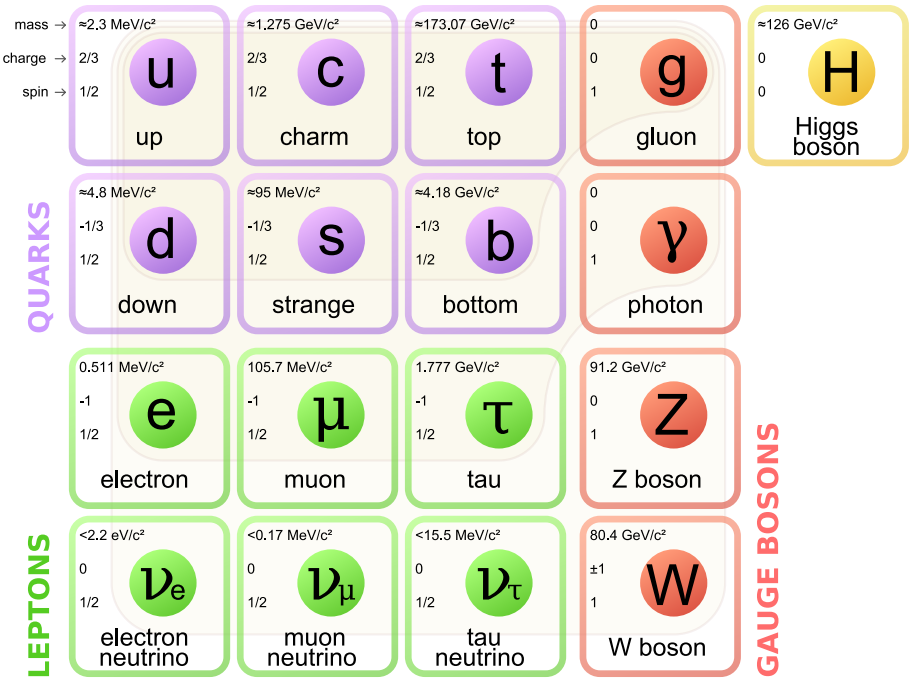


Figure 2.1: Elementary particles of the Standard Model [sta14].

2.2 Lepton Flavour Violating Muon Decays

The lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ is possible in the extended Standard Model via neutrino mixing (see figure 2.2). Due to the heavy mass of the W^+ ($m_w = 80.4\,\mathrm{GeV/c^2}$) and the very small difference of squared masses of the neutrinos ($\approx 10\,\mathrm{meV}$), the factor $\left(\frac{\Delta m_\nu^2}{m_W^2}\right)^2$ is very small and therefore this decay is heavily suppressed ($\mathrm{BR} < 10^{-54}$).

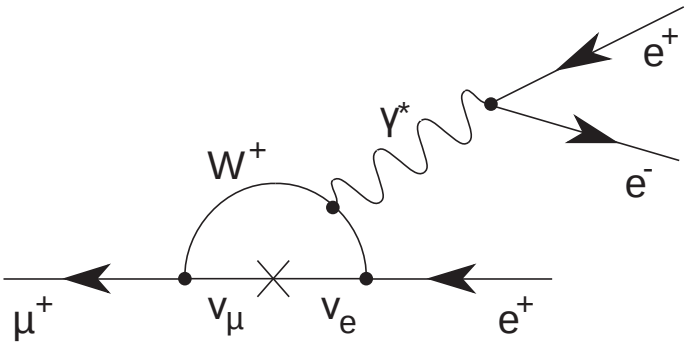
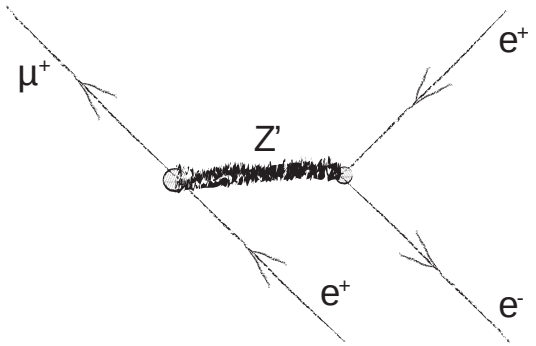
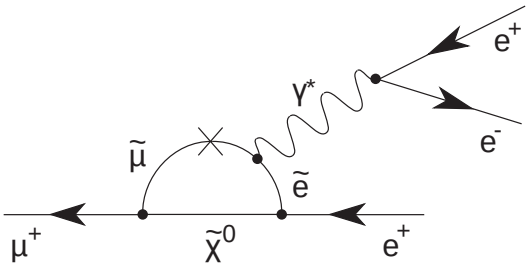


Figure 2.2: Feynman diagram of the lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ via neutrino oscillations.

If the decay $\mu^+ \rightarrow e^+e^-e^+$ is observed, this will be a clear hint for new physics beyond the Standard Model.



(a) $\mu^+ \rightarrow e^+e^-e^+$ mediated by a Z'



(b) $\mu^+ \rightarrow e^+e^-e^+$ with SUSY particles

Figure 2.3: Feynman diagrams of the decay $\mu^+ \rightarrow e^+e^-e^+$ with beyond Standard Model processes.

There are many new models which allow charged lepton flavour violation by means of new, heavy particles. Lepton flavour violating processes could be possible by adding new particles that can couple to both the electron and the muon at tree-level (see figure 2.3a). This particle could be a new Z boson and models with extra dimensions [CN05] predict such processes. In these models the lepton flavour violating decays are suppressed because of the high mass of these new particles. Lepton flavour violating decays at loop-level that have a higher branching ratio than the extended Standard Model decay with neutrino mixing, are possible if the neutrinos and the W boson are replaced by supersymmetric (SUSY) particles (see figure 2.3b). The superpartners of leptons are called sleptons and are bosons. Since SUSY particles have not been observed yet, they are expected to have high masses [Gri11]. Hence, their mass differences could be larger and therefore the branching ratio of the decay $\mu^+ \rightarrow e^+e^-e^+$ would be higher.

To be able to compare the new physics mass scale between the decays $\mu^+ \to e^+e^-e^+$ and $\mu^+ \to e^+\gamma$ a simplified Lagrangian function can be chosen [dG09]:

$$\mathscr{L}_{LFV} = \frac{m_\mu}{(\kappa+1)\Lambda^2}\overline{\mu_R}\sigma^{\mu\nu}e_L F_{\mu\nu} + \frac{\kappa}{(\kappa+1)\Lambda^2}(\overline{\mu_L}\gamma^\mu e_L)(\overline{e_L}\gamma_\mu e_L) \tag{2.1}$$

Λ is the common mass scale and κ is the amplitude ratio between the left and the right term. The left term describes dipole coupling (loop-level decays), the right term describes a contact interaction with left-left vector coupling (tree-level decays). Loop-level decays dominate at low κ and the tree-level decays dominate at high κ. In figure 2.4 it can be seen that the Mu3e experiment has to be two orders of magnitude better in sensitivity than the MEG experiment to be able to go beyond the accessible mass scale.

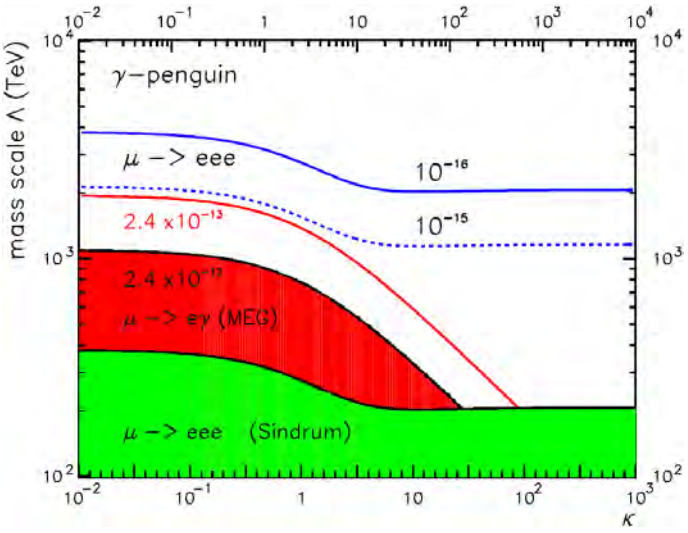


Figure 2.4: The expected branching ratios and the current experimental limits for the experiments SINDRUM, MEG and Mu3e [B$^+$12b].

3 Mu3e Experiment

The Mu3e experiment searches for the lepton flavour violating, and thus in the Standard Model forbidden, decay $\mu^+ \to e^+e^-e^+$ with a targeted sensitivity of $< 10^{-16}$ [B$^+$12b], which is four orders of magnitude better than the previous SINDRUM experiment [B$^+$88].

In order to reach such a high sensitivity in a reasonable time, high muon decay rates of 10^9 muons per second are needed. This leads to several requirements for the detector.

3.1 Current Experimental Situation

3.1.1 SINDRUM Experiment

The SINDRUM experiment was running from 1983 to 1986 at the Paul Scherrer Institute (PSI) in Switzerland and searched for the decay $\mu^+ \to e^+e^-e^+$. Since no signal event for this decay was found, they set the limit on the branching ratio to BR$(\mu^+ \to e^+e^-e^+) < 10^{-12}$ at 90 % CL [B$^+$88]. The detector consists of five concentric multiwire proportional chambers (MWPC) and a cylindrical array of 64 scintillation counters arranged in a homogeneous magnetic field of 0.33 T.

3.1.2 MEG Experiment

The MEG experiment is running since 2008 at PSI and searches for the decay $\mu^+ \to e^+\gamma$. Since no signal was found up to now, they set the limit of the branching ratio to BR$(\mu^+ \to e^+\gamma) < 5.7 \cdot 10^{-13}$ at 90 % CL [A$^+$13]. The detector consists of drift chambers, timing counters inside a gradient magnetic field and a photon detector. The MEG experiment will analyse more data taken in te last two years and are currently upgrading the detector in order to achieve an even better sensitivity of $6 \cdot 10^{-14}$ [BCC$^+$13].

3.2 Muon Decays

The muon has a mass of $105.659\,\mathrm{MeV/c^2}$ and a mean lifetime of $2.197\,\mu\mathrm{s}$ [B$^+$12a]. Due to its low mass and charge conservation, the muon can only decay into electrons, neutrinos and photons. The muon most likely decays via the lepton flavour conserving decay $\mu^- \to e^-\nu_\mu\overline{\nu}_e$ with a branching ratio of almost $100\,\%$ [B$^+$12a]. The muon also decays into $\mu^- \to e^-\gamma\nu_\mu\overline{\nu}_e$ with a branching ratio of $1.4 \cdot 10^{-2}$ and $\mu^- \to e^-e^+e^-\nu_\mu\overline{\nu}_e$ with a branching ratio of $3.4 \cdot 10^{-5}$ [B$^+$12a]. Because of the very low rate of the signal decay $\mu^+ \to e^+e^-e^+$, this background has to be suppressed.

3.2.1 The Decay $\mu^+ \to e^+e^-e^+$

All three decay particles of the $\mu^+ \to e^+e^-e^+$ decay come from the same vertex and are coincident in time. The total energy of the decay particles have to be equal to the mass of the antimuon:

$$E_{tot} = \sum_{i=1}^{3} E_i = m_\mu c^2 \tag{3.1}$$

So, the energy of the positrons and the electron can be 53 MeV at most, which is equivalent to half of the muon mass. If the antimuon decays after it has been stopped, the vector sum of the momenta of the decay particles vanishes:

$$|\vec{p}_{tot}| = \left|\sum_{i=1}^{3} \vec{p}_i\right| = 0 \tag{3.2}$$

These facts can be used to distinguish the signal decay from the background.

3.2.2 Backgrounds

There are two types of background: the internal conversion background and the accidental background.

Internal Conversion Background

The Standard Model decay with internal conversion $\mu^+ \to e^+e^-e^+\nu_e\overline{\nu}_\mu$ (BR $= 3.4 \cdot 10^{-5}$ [B$^+$12a]) is the most serious background for the Mu3e experiment because the decay particles are coincident in time and originate from the same vertex. The Feynman diagram is shown in figure 3.1. However, the neutrinos cannot be detected in the detector and this

energy loss can be used to reduce this background. Therefore, the Mu3e detector needs a very good energy and momentum resolution. In order for the Mu3e experiment to reach a sensitivity of 10^{-16}, a momentum resolution of the sum of the two positrons and the electron momenta of below 1 MeV is needed (see figure 3.2).

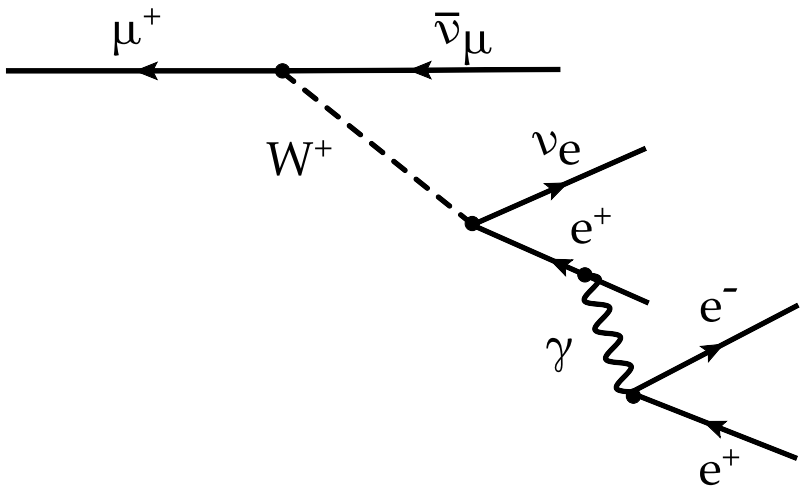


Figure 3.1: Feynman diagram of the internal conversion decay $\mu^+ \to e^+e^-e^+\nu_e\overline{\nu}_\mu$.

Accidental Background

A coincidence of particles from different processes could mimic the signal event. Positrons of two Michel decays and an electron from another decay superimposed can look like a signal decay (see figure 3.3). This electron can for example come from Bhabha scattering, a muon decay with internal conversion, photon conversion or could be a positron that is identified as an electron. Photon conversions can be reduced by minimising the detector material. Since the accidental background is neither coincident in time nor has one common vertex nor meet energy and momentum conservation it can be suppressed by a very good vertex, momentum and time resolution of the detector. The detector must in any case have as little material as possible to reduce multiple scattering.

3.3 Muon Beam and Target

Since a high antimuon rate is required to reach the aimed sensitivity, the Mu3e experiment will be operated at PSI in Switzerland which runs the world's most intense proton beam with up to 2.4 mA of 590 MeV/c protons [PSI14]. For a first low intensity phase, the existing πE5 beamline will be used. This beamline can supply a rate of up to $1 \cdot 10^8$

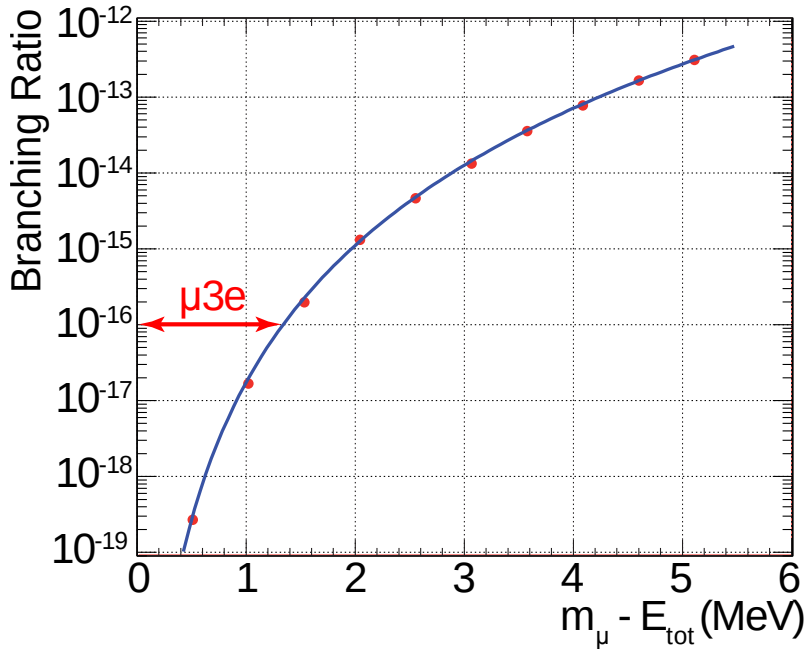


Figure 3.2: Effective branching ratio for the decay $\mu^+ \rightarrow e^+e^-e^+\nu_e\overline{\nu}_\mu$ as a function of the energy of the neutrinos [DK09].

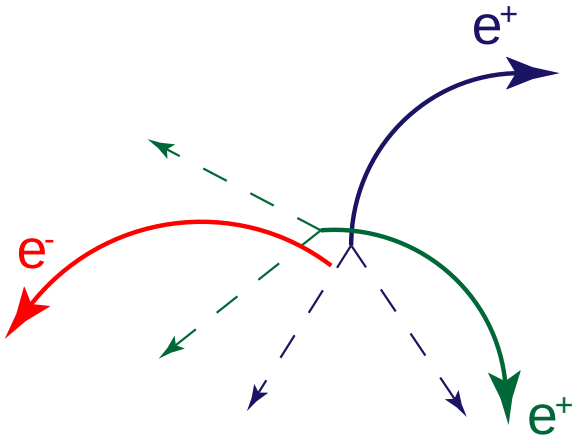


Figure 3.3: Accidental background from two Michel decays and an electron, the dashed lines represent the neutrinos.

muons/s [B$^+$12b]. In order to reach the planned sensitivity of 10^{16} in reasonable time a muon rate of $2 \cdot 10^9$ muons/s is required. Therefore a new, more intense beamline has to be built. The Swiss Spallation Neutron Source (SINQ) at PSI generates a large amount of antimuons and a secondary beamline exploiting these muons is under study [B$^+$12b].

In the Mu3e detector, the muon beam is stopped by a hollow double cone target, which is made of aluminium (see figure 3.4). The front part of the target is 30 µm thick and the back part is 80 µm thick. The target has a total length of 100 mm and a diameter of 20 mm.

3.4 Detector Design

The detector design is shown in figure 3.4. The final detector will have an additional recurl station on both sides, so that the whole detector will have a length of about 2 m.

3.4.1 Tracking Detector

The detector is placed in a 1 T magnetic field so that the momenta of the electrons and positrons can be measured by the curvature of their tracks. The trajectories of the particles are measured by pairs of inner and outer pixel layers. The high vertex resolution is achieved by the inner pixel layers which is very close to the target where the antimuons are stopped. The good momentum resolution is obtained by measuring the bending of recurling tracks in the recurl stations and by reducing the detector material and hence multiple scattering. The pixels of these sensors will have a size of $(80 \times 80)\,\mu\text{m}^2$ and therefore, the whole detector will have about 280 million pixels. The pixel sensors can be thinned down to 50 µm (see chapter 4) so that the radiation length of one layer is $\text{X}/\text{X}_0 \leq 0.1\,\%$. In addition the support structure and the readout cable will be made of 25 µm thin Kapton® foil onto which the pixel sensors will be glued and wire bonded. Furthermore, the detector will be cooled with gaseous helium. This reduces the deflection of the positrons and electrons traversing the detector material (multiple scattering) which is limiting the momentum resolution. The RMS of the scattering angle

$$\Theta_{RMS} = \frac{13.6\,\text{MeV}}{\beta c p}\sqrt{\frac{x}{X_0}}\left(1 + 0.038\,\ln\left(\frac{x}{X_0}\right)\right) \tag{3.3}$$

(see [B$^+$12a]) shows that the multiple scattering is larger for particles with low momentum p which is the case for the Mu3e experiment. β/c is the velocity of the positrons and the

electrons. Multiple scattering can be reduced by reducing the traversed material x and by using materials with high radiation lengths X_0.

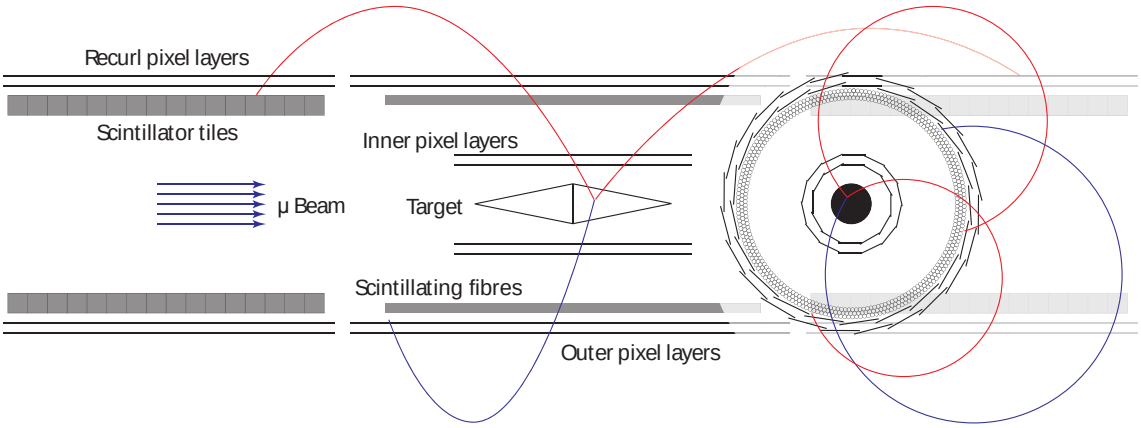


Figure 3.4: Schematic side view of the Mu3e detector with the first recurl station and overlayed transverse view.

(a) Most inner pixel layer prototype of the detector (b) Prototype of a segment of an outer pixel layer

Figure 3.5: Prototypes of the Mu3e pixel detector made of Kapton®; instead of pixel sensors 50 µm glass plates are used.

3.4.2 Timing Detector

The good timing resolution is accomplished by scintillating fibres and scintillating tile detectors. The fibres will be placed inside the central outer double pixel layers and the tiles will be placed at the recurl stations outside the active detector volume close to the beam pipe. The tiles can be bigger than the fibres because multiple scattering is no problem there (see figure 3.4). The scintillating fibres are expected to have a time resolution of less than 1 ns and the scintillating tiles are expected to have a time resolution of (0.1 - 0.2) ns.

4 HV-MAPS

The Mu3e experiment uses High Voltage Monolithic Active Pixel Sensors (HV-MAPS) for the tracking detector. These sensors were developed by Ivan Perić [Per12a, PKF11, PT10, Per07]. These special silicon sensors have the advantages that they are fast and have only little material. Monolithic Active Pixel Sensors (MAPS) have sensor and read-out electronics on the same chip and therefore a small material budget because no extra readout chip and no extra bump bonds are needed.

HV-MAPS can be implemented in an inexpensive commercial high-voltage CMOS process which is highly available. Every pixel is implemented as a smart diode, that means that the pixel electronics, e. g. the charge sensitive amplifier (CSA), is placed inside a high voltage n-well. These n-wells are on a p-doped substrate (see figure 4.1). This n-well to p-substrate diode is operated in reverse direction such that the n-well is the charge collecting electrode. Incoming particles ionise the atoms in the depletion zone. In contrast to MAPS, HV-MAPS collect this charge via drift because of high bias voltages of over 50 V. The time of the charge collection is then reduced to less than 1 ns [Aug12] and charge recombination is strongly reduced. Since the depletion zone is about 9 µm [Per07] the HV-MAPS can be thinned down to 50 µm. Thus the material in the detector can further be reduced to minimise multiple scattering.

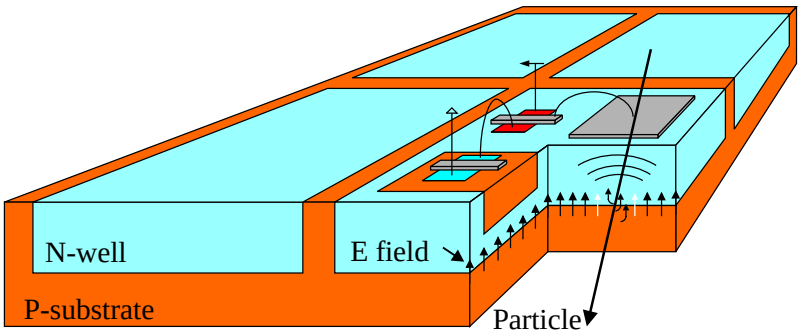


Figure 4.1: Sketch of four HV-MAPS pixels [Per07].

Part II

MuPix Prototypes

5 MuPix2

The MuPix2 chip is the second HV-MAPS prototype for the Mu3e experiment designed by Ivan Perić (see [Per12a]). The MuPix2 chip has already been intensely characterised in [Aug12] and [Per12b]. Before measurements for the MuPix3 and the newest prototype MuPix4 were done, the MuPix2 chip was tested in this thesis. Also a thinned MuPix2 chip was tested (see section 8.3).

5.1 Setup

5.1.1 The Chip

The MuPix2 chip has a size of $(1.8 \times 2.5)\,\mathrm{mm}^2$, its pixel matrix consists of 42×36 pixels and each pixel has a size of $(39 \times 30)\,\mu\mathrm{m}^2$. Therefore the chip has an active area of $1.77\,\mathrm{mm}^2$. In table 5.1 all MuPix prototypes but the MuPix1 are compared.

Incoming particles ionise the atoms in the depletion zone and this charge is collected by the pixels. The sensor diode is connected to the charge sensitive amplifier (CSA) via a capacitor because the amount of charge is very small (see figure 5.1). This sensor signal can be imitated by the injection capacitor for test purposes. Every pixel is connected to this injection. There is a digital processing unit (DPU) for every pixel. The comparator in the DPU compares the pixel signal with an adjustable threshold and generates an output signal that is as long as the pixel signal is above the threshold (time over threshold, ToT). Every pixel has in addition to that global threshold a DAC (digital to analogue converter) that adds a voltage to this threshold to even out pixel variations. This DAC is called TDAC.

The MuPix2 chip can be read out in the hit-flag mode or in the ToT mode, i. e. either the whole pixel matrix of the chip can be read out or the output signal of a selected single pixel can be analysed. The hit-flag mode gives only the information whether a pixel was hit and the signal was above the threshold. Every pixel is read out whether it registered a hit or not. The ToT mode gives in addition the time how long the signal of this pixel was above the threshold (time over threshold, ToT). While the chip is read out in the hit-

flag mode by the FPGA board, simultaneously the ToT signal of one single pixel can be measured via a probe on an oscilloscope.

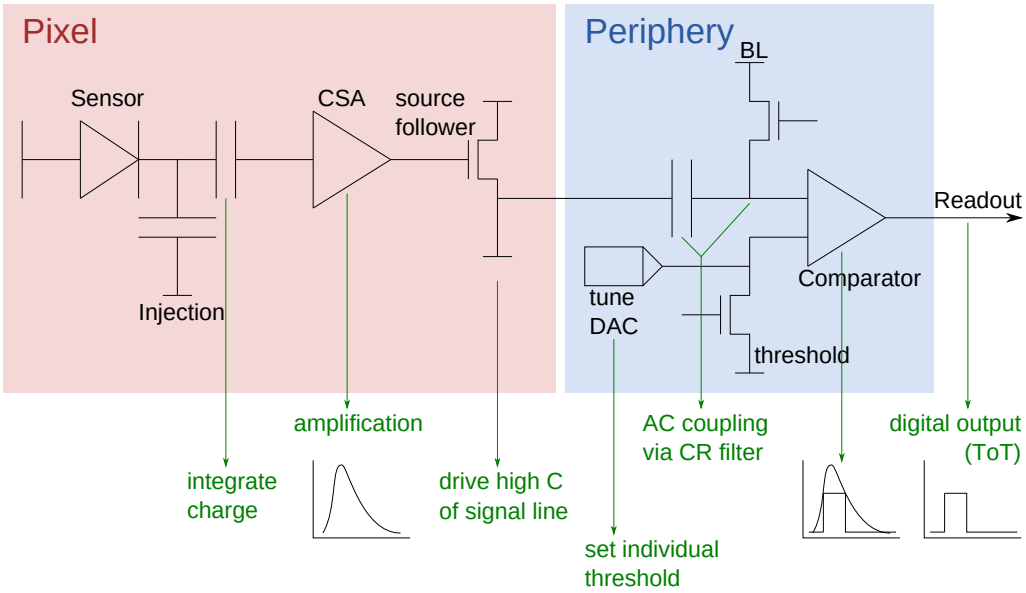


Figure 5.1: Electronics of all MuPix prototypes inside each pixel and on the chip periphery. The voltages that can be changed are marked in green. [Per12b]

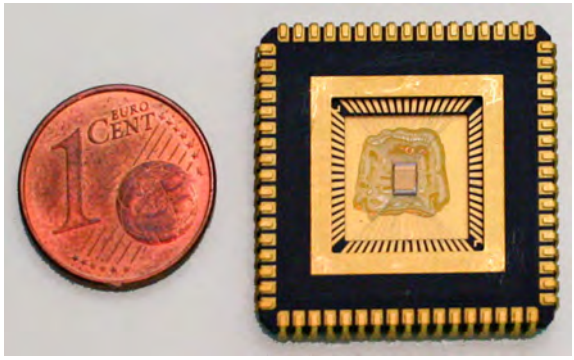


Figure 5.2: Picture of a MuPix2 chip.

5.1.2 The Hardware

The test setup consists of a PCB with a socket for the chip and a FPGA board (Uxibo, see [uxi14]) that is connected via a ribbon cable to the PCB and via a USB cable to a computer. The chip is glued and wire bonded on a chip carrier that can be placed in the socket of the PCB (see figure 5.3). The FPGA is controlled via a C++ programme and can set the voltage of the threshold and the injection generated on the PCB. In addition

chip	pixels	pixel size	chip size	active area	ToT signal
MuPix2	42×36	$(39 \times 30)\,\mu m^2$	$(1.8 \times 2.5)\,mm^2$	$1.77\,mm^2$	positive
MuPix3	32×40	$(92 \times 80)\ \mu m^2$	$(4 \times 5)\,mm^2$	$9.42\,mm^2$	positive
MuPix4	32×40	$(92 \times 80)\,\mu m^2$	$(4 \times 5)\,mm^2$	$9.42\,mm^2$	negative
MuPix6	32×40	$(103 \times 80)\,\mu m^2$	$(4.4 \times 5)\,mm^2$	$10.55\,mm^2$	negative

Table 5.1: Comparison of the MuPix prototypes, note that the MuPix6 prototype is the fifth HV-MAPS prototype for the Mu3e experiment.

the readout sequence can be started. The readout mode is chosen by switching a jumper at the test PCB.

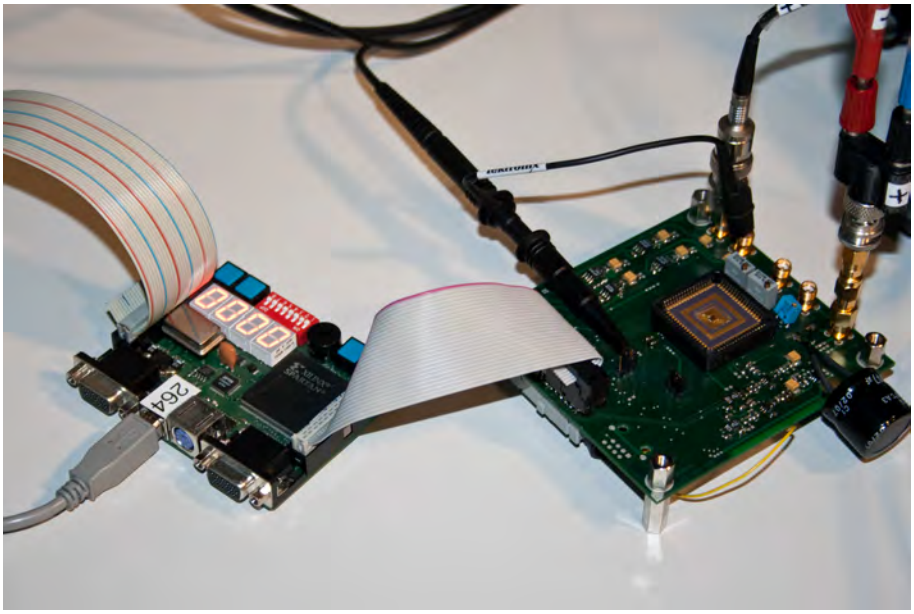


Figure 5.3: Test setup of the MuPix2 chip: the FPGA board (left) and the PCB where the chip sits in (right).

5.2 Measurements

The following measurements were done with an infrared laser diode[1] with a wavelength of 850 nm and a ^{90}Sr source.

[1] For test purposes: The light of this diode is invisible but it can be seen through a camera of a mobile phone.

5.2.1 Pulse Shapes

The pulse shapes for different settings can be compared in order to study the influence of these parameters on the performance of the chip. Since the signal of a pixel is compared to a threshold before this signal is output (ToT signal) and digitised, the pulse shape cannot be measured directly. However, the pulse shape can be reconstructed by scanning the pulse with increasing thresholds as shown in figure 5.5. The chip is lit with a LED that gets its signal from a pulse generator. Both the signal of the pulse generator and the ToT signal from a pixel are connected to an oscilloscope and the time difference between the rising edge of the LED signal and the rising edge of the ToT signal (latency) as well as the width of the ToT signal is determined. This ToT signal is shown in figure 5.4. Hence, for every threshold two measuring points are obtained. With increasing threshold the latency becomes longer and the ToT becomes shorter.

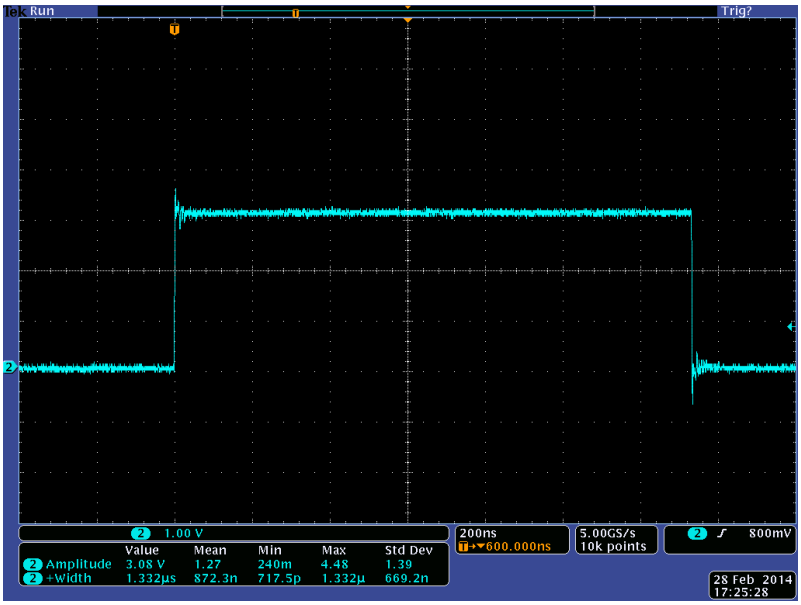


Figure 5.4: ToT signal of a pixel of the MuPix2 chip measured via a probe on an oscilloscope.

The pulse of an edge pixel is much higher than the pulse shape of a centre pixel (see figure 5.6). The pixels at the corner and at the edge of the chip collect more charge than a pixel at the centre of the chip, because at the edges there are less “rival” pixels and thus the charge can be collected from a larger volume (see figure 5.7). But this is only true if the chip is lit by an intense light source like a LED. If the chip is hit by particles like electrons with a low rate this effect is the other way round (see section 8.3).

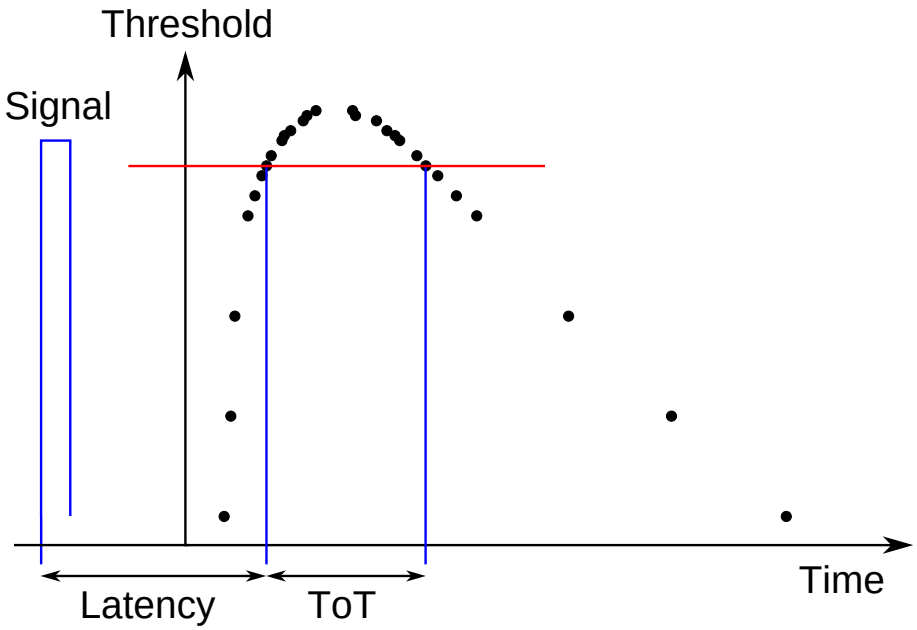


Figure 5.5: Pulse shape measurement.

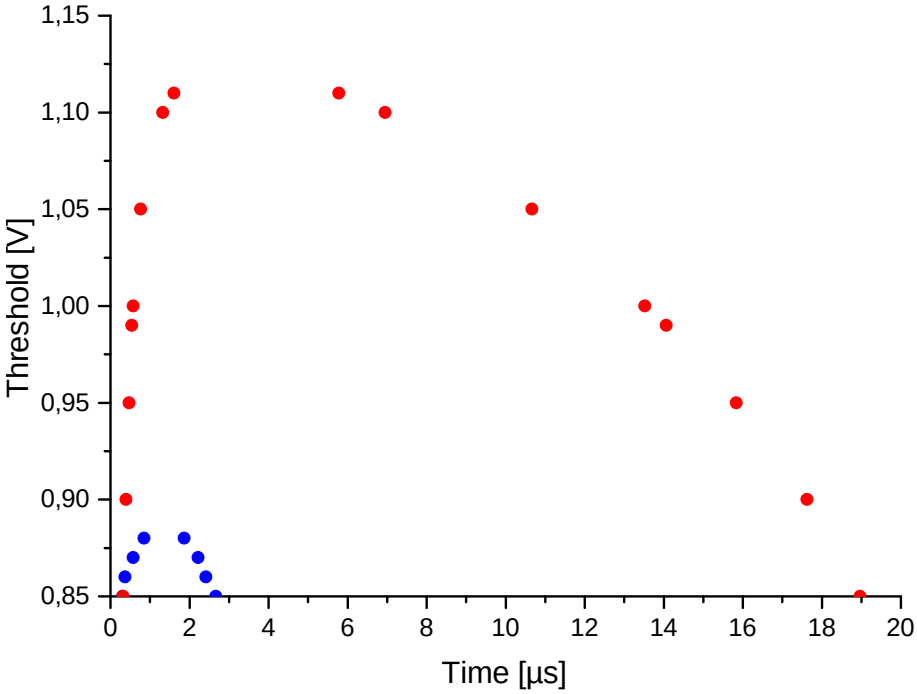


Figure 5.6: Pulse shapes of the MuPix2 chip for a centre pixel (blue) and a corner pixel (red).

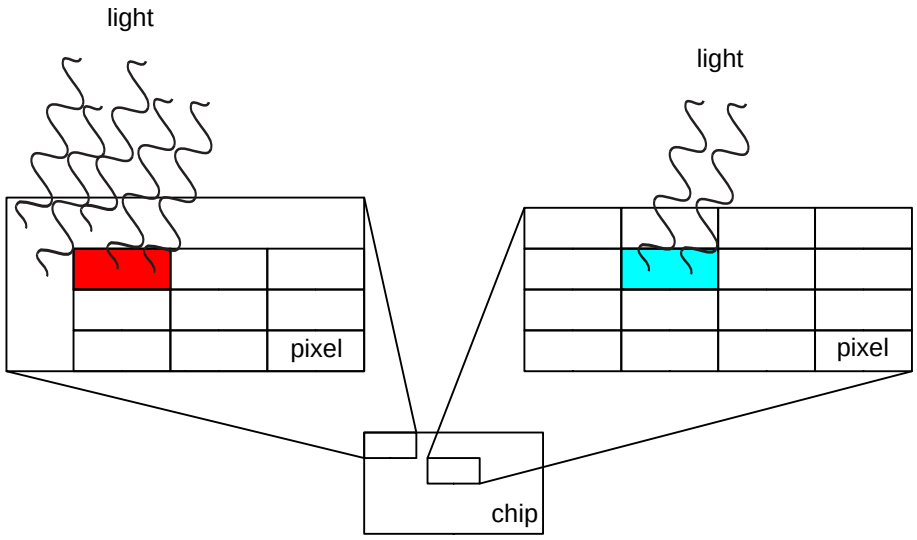


Figure 5.7: The ToT of a corner pixel is longer and the latency is shorter than for a centre pixel if irradiated with light due to a larger amount of charge collection.

5.2.2 Temperature Dependence

The pulse shapes at different temperatures can be compared as shown in figure 5.8. The pulse at a temperature of 60 °C is much smaller than the pulse at 30 °C. The ToT at the lowest measured threshold of 0.85 V decreased from 5.4 µs to 2.3 µs and the latency increased from 180 ns to 310 ns. This temperature effect has been corrected for the subsequent prototypes. A temperature of 60 °C was chosen because this value is expected as maximum temperature for the Mu3e experiment [Zim12].

5.2.3 ^{90}Sr Source

Comparison of pulse shapes of different Mupix2 chips can lead to the wrong conclusion that some chips are much more sensitive / efficient than others. Since the pulse shapes of only a few pixels were measured, variations could also be due to pixel effects. Therefore, two different chips were irradiated with a ^{90}Sr source and the chips were read out in the hit-flag mode, i. e. the whole pixel matrix of the chips was read out. For different thresholds all hits of 1000 readout frames were counted, where one frame was 5 µs long. The two tested chips have almost the same efficiency. The result can be seen in figure 5.9. The differences are of the order of 10% but increase with lower thresholds.

The MuPix2 chip has far too long shaping times for the Mu3e experiment which can be seen in the long ToT of several µs which is also the dead-time. In addition this chip is

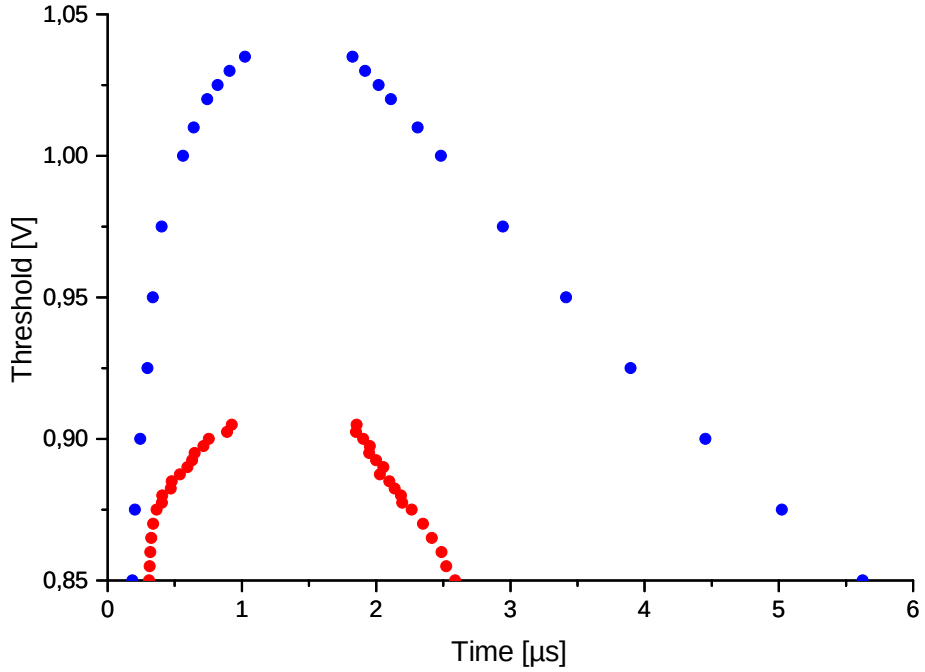


Figure 5.8: Pulse shapes of the MuPix2 chip at 30 °C (blue) and 60 °C (red) at a high voltage of -70 V.

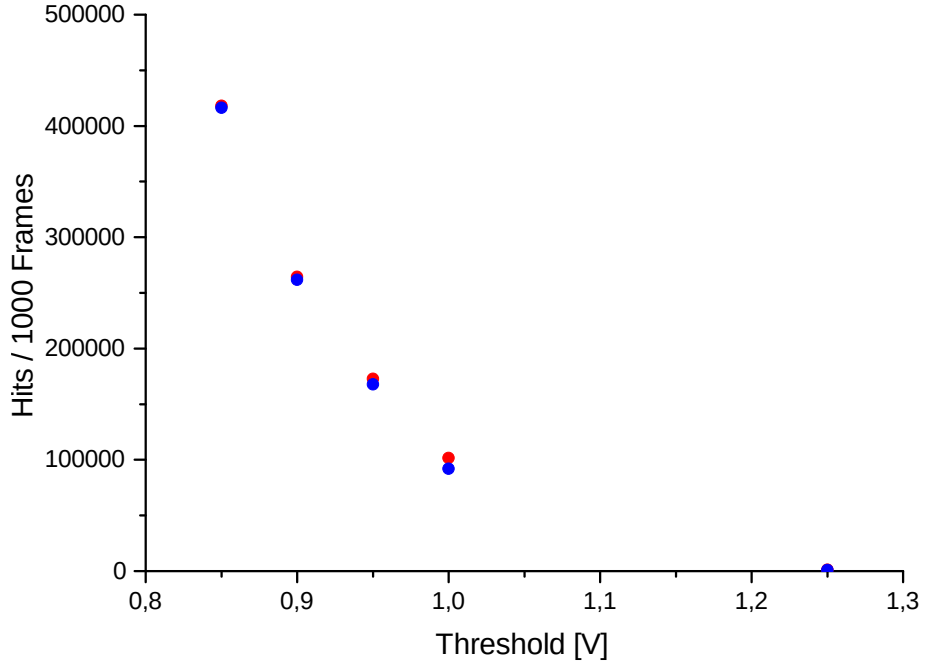


Figure 5.9: Hits of a ^{90}Sr source accumulated for 1000 frames (5 µs / frame) at different thresholds for two different MuPix2 chips.

very sensitive to temperature effects. However, the prototypes MuPix3 and MuPix4 that are discussed in the following chapters show better properties. The chip to chip variations of the MuPix2 chip seems to be very small which is important for the Mu3e experiment because the tracking detector will consist of 4860 chips [B$^+$12b].

6 MuPix3

The MuPix3 is the third MuPix prototype developed by Ivan Perić. It is supposed to have a better timing than the MuPix2, because the shaping times, and therefore the ToT, are too long for the Mu3e experiment. But due to an issue with the pixel enabling procedure, which should allow to enable arbitrary pixel patterns, this could not be tested. The MuPix3 chip has, compared to the MuPix2, a zero suppressed readout. In this thesis also a thinned MuPix3 chip was tested during two testbeams (see section 8.2 and section 8.3).

6.1 Setup

6.1.1 The Chip

The MuPix3 chip has a size of $(4 \times 5)\,\mathrm{mm}^2$, its pixel matrix consists of 32×40 pixels and each pixel has a size of $(92 \times 80)\,\mu\mathrm{m}^2$. Therefore the chip has an active area of $9.42\,\mathrm{mm}^2$. In figure 6.1 a size comparison between the MuPix2 and the MuPix3 chip is shown.

An arbitrary set of pixels can be enabled so that only these pixels can be read out both in the hit-flag mode and in the ToT mode. The ToT mode is different to the MuPix2 chip: Not only one single pixel can be analysed but an arbitrary set of pixels can be selected. Hence, not the output signal of one single pixel but the output of a logic OR of all enabled pixel signals is provided. However, enabling the pixels does not work properly, because by mistake in the design the RAM cells on the chip cannot store the information properly which pixel was selected. After switching on the setup pixels are enabled randomly. Pixels can be disabled without any problems but not enabled again, for enabling, a power cycle is required. Because of that issue, the MuPix3 prototype was not tested as intensely as the other prototypes.

The MuPix3 chip can also be read out in the hit-flag mode. For this prototype, only the pixels that registered a hit are read out in the hit-flag mode (zero suppressed readout). The pixels are organised in columns and rows. To optimise the space on the chip, every pixel column is divided into two readout columns as shown in figure 6.2. The pixel address scheme reflects the location of the corresponding readout cells.

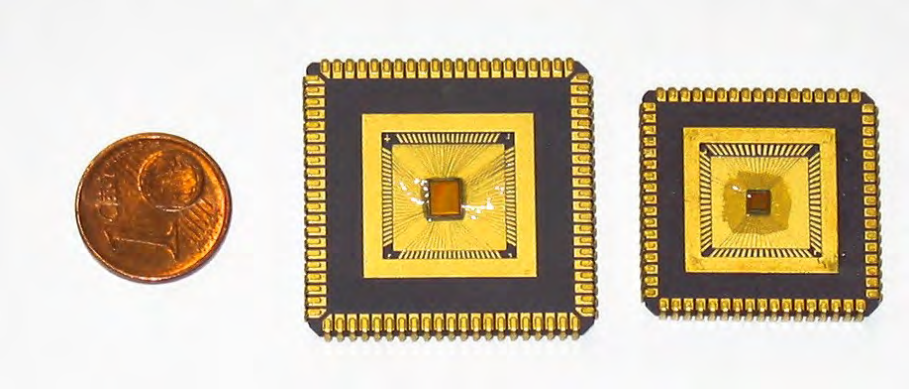


Figure 6.1: Picture of a MuPix3 (left) and a MuPix2 (right) chip.

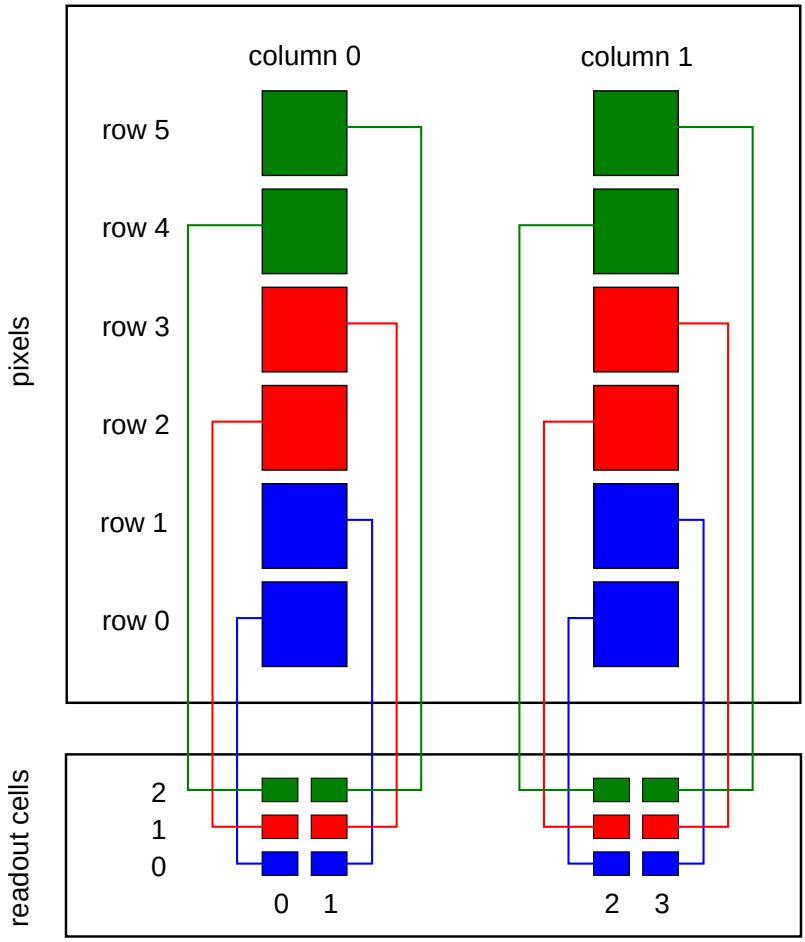


Figure 6.2: Schematic of the readout cells of the MuPix3 and MuPix4.

6.1.2 The Hardware

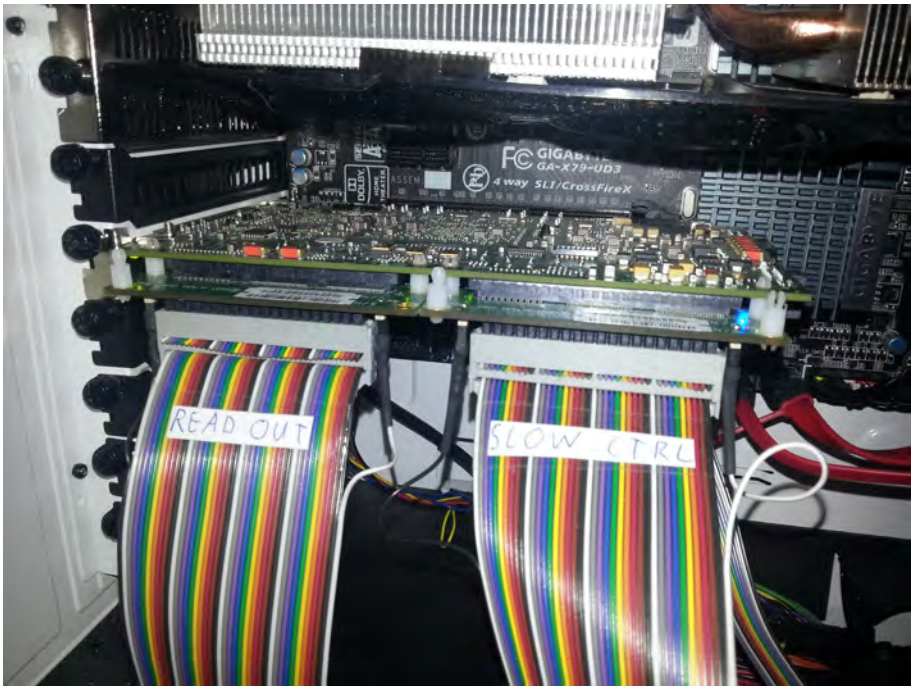
The setup consists of a MuPix PCB, designed by Dirk Wiedner, where the chip sits in a socket (see figure 6.3) and the Stratix IV GX FPGA Development Kit from Altera® (see [str14]) that is connected via two ribbon cables (slow control and readout) to the MuPix PCB. The schematic of this PCB can be seen in appendix B. The FPGA is mounted on a PCIe card sitting inside the readout PC. The ToT signal and the signals to set the PCB DACs for the threshold and the injection, for example, are on the slow control cable. The signals that are necessary for reading out the chip in the hit-flag mode are on the readout cable. The MuPix3 PCB has two injection DACs because for the MuPix3 there are two different injection signals. Injection 1 is connected to the first row, which is the lowest row, and to the second row and injection 2 is connected to the third and fourth row and so on, as can be seen in figure 7.1. The jumper J508 sitting between the readout cable and the chip socket has to be set at the position that is farther from the socket, otherwise no ToT signal can be seen. The ToT signal can be tapped at the LEMO® connector marked with “HB”. The same way the injection 1 and 2 signals can be tapped at the connector marked with “Injection1” and “Injection2”.

6.2 Measurements

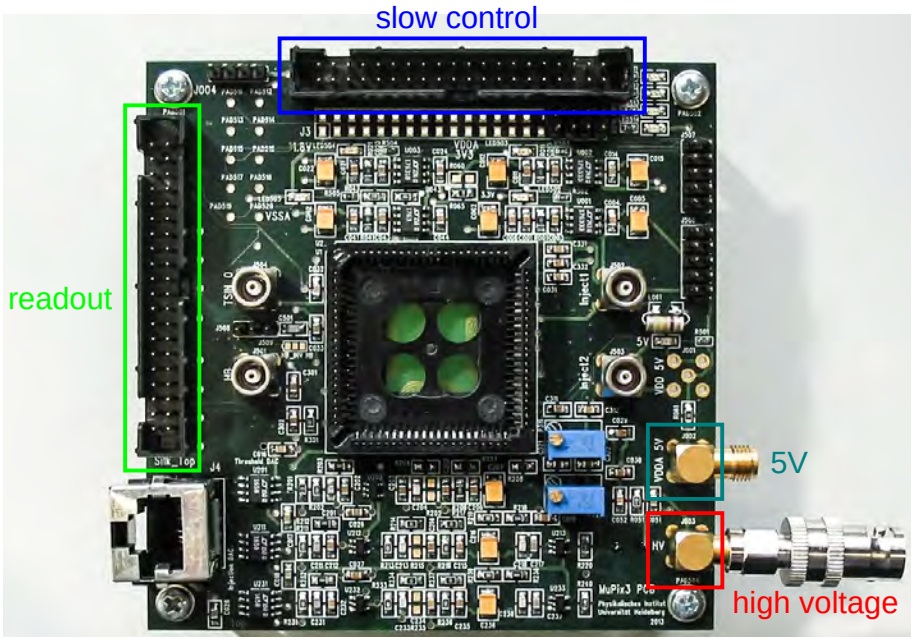
6.2.1 Pulse Shape

The pulse shape was measured with a threshold scan as described for the MuPix2 chip. Since no single pixel can be enabled separately, the pulse shape of all randomly enabled pixels is measured and that leads to big variations of the latency and the ToT (see figure 6.4). Therefore information which can be obtained from the pulse shapes of the MuPix3 chip is difficult to interpret.

There was no useful result obtained for the MuPix3 chip at the tests in the laboratory because of the pixel enabling issue.



(a) Picture of the FPGA board inside the readout PC



(b) Picture of the MuPix3 test PCB

Figure 6.3: Figure 6.3a shows the FPGA board sitting inside the readout PC. The left ribbon cable has to be connected to the “readout” connector and the right cable has to be connected to the “slow control” connector of the MuPix3 PCB as shown in figure 6.3b.

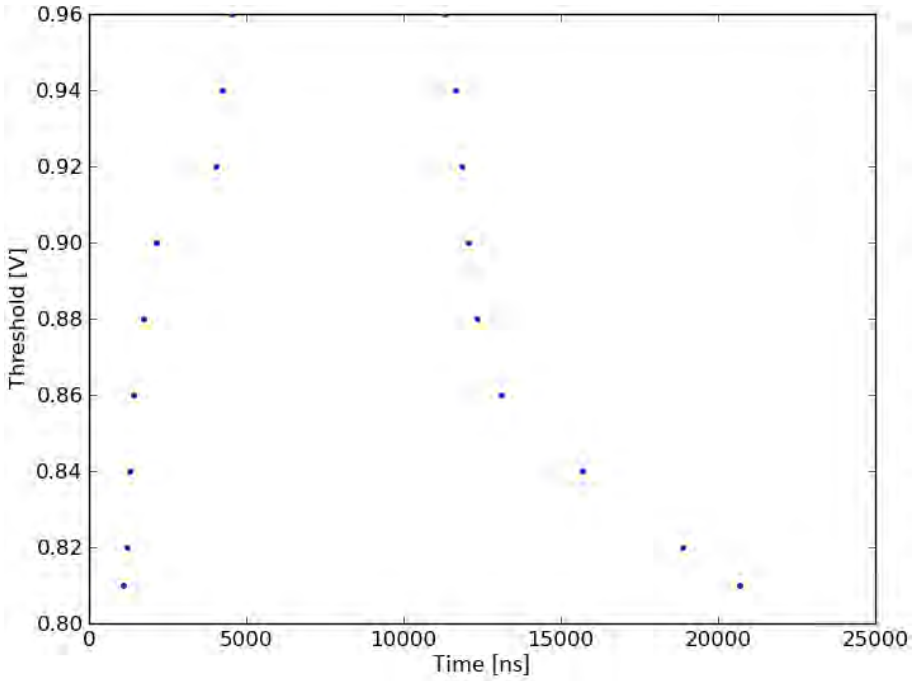


Figure 6.4: Pulse shape of all enabled pixels of the MuPix3 chip [Fö14].

7 MuPix4

7.1 Setup

7.1.1 The Chip

The MuPix4 chip has a size of $(4 \times 5)\,\mathrm{mm}^2$, its pixel matrix consists of 32×40 pixels and each pixel has a size of $(92 \times 80)\,\mu\mathrm{m}^2$. Therefore the chip has an active area of $9.42\,\mathrm{mm}^2$. See also table 5.1.

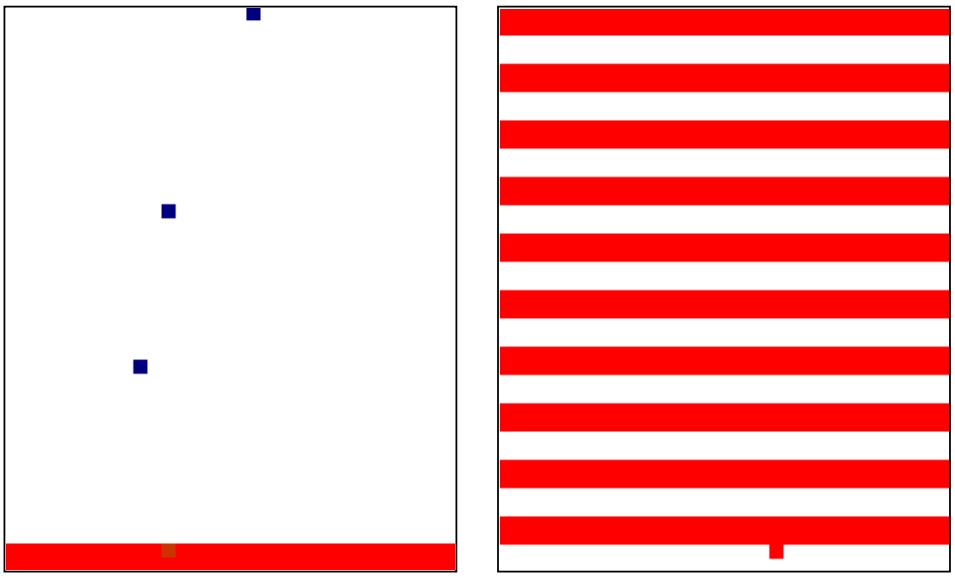
The MuPix4 prototype can be read out in the zero suppressed hit-flag mode and in the ToT mode, too. The readout cells are connected to the pixels the same way as in the MuPix3 chip (see figure 6.2).

The readout of this prototype is similar to that of the MuPix2 chip: Pixels cannot be disabled for the hit-flag mode, and the ToT signal of a selected single pixel can be analysed. However, the readout in the hit-flag mode is zero suppressed as with the MuPix3.

The chip has two input pads for two different injection signals like the MuPix3 chip. However, all rows to which the injection 1 is connected provide the wrong row address "zero", so that every hit is shown in the lowest two rows by design mistake (see figure 7.1).

7.1.2 Wire Bonding

The MuPix4 chip has pads to input and output the signals. There are pads to supply the chip with power and HV, furthermore there are pads that are connected to the ground potential. Furthermore, there are pads to set the internal currents and voltages and to enable a pixel for the ToT mode. The voltage for the baseline, the threshold and the injection pulses are input, too. If the readout sequence is started by applying the digital readout signals on the readout chip pads, the addresses of the hit pixels are applied at the twelve bit lines, six for the column and the row address each. The chip has no integrated counter so that an external clock has to feed the timestamps via eight bit lines into the chip. The chip then applies together with the pixel addresses the value of the timestamps when the hit occurred. The bonding diagram can be seen in appendix C.



(a) injection 1 (b) injection 2

Figure 7.1: Readout in the hit-flag mode of the two injections of the MuPix4 chip: 7.1a shows the readout of injection 1 and 7.1b shows the readout of injection 2.

MuPix2 and MuPix3 chips could be wire bonded without problems. But with the MuPix4 there was an issue in the beginning:

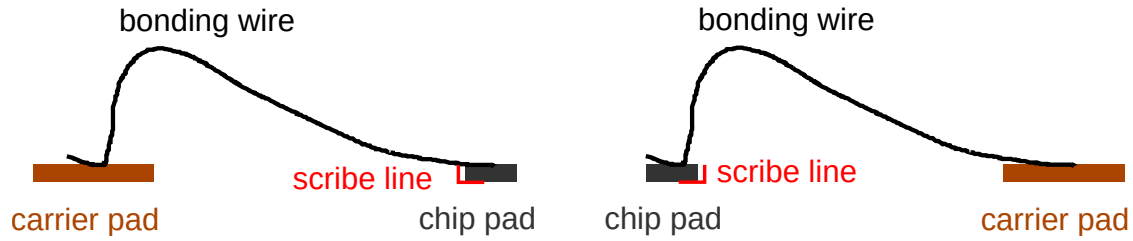
The first chips were wire bonded from the chip carrier to the chip, which caused short circuits between some pins and the substrate. The concerned bonding wires came too flat to the chip, so that they touched the scribe line (see figure 7.2a), which is connected to the substrate. In our case the substrate is at the potential of the HV. By pulling the bonding wires upwards, with a special needle, the short circuits could only be removed temporarily. However, the problem reappeared after some time. It seemed, that the HV bent the bonding wires back towards the scribe line.

The final solution was to bond from the chip to the chip carrier, because then the distance between the bonding wires and the scribe line was larger (see figure 7.2b).

7.1.3 The Hardware

The hardware is the same as for the MuPix3 chip. Both the pixel addresses in the hit-flag mode and the ToT signal of one pixel are sent to the FPGA board. The tune DACs (TDACs) can only be set if the jumper J508 is at the position that is closer to the chip socket.

In the beginning a large digital crosstalk was discovered of the readout signals on the



(a) bonding from carrier to chip

(b) bonding from chip to carrier

Figure 7.2: Drawing of the MuPix4 bonding problem: Figure 7.2a shows the bonding procedure that caused the short circuits between random signals and the substrate by touching the scribe line and figure 7.2b shows the solution of this problem.

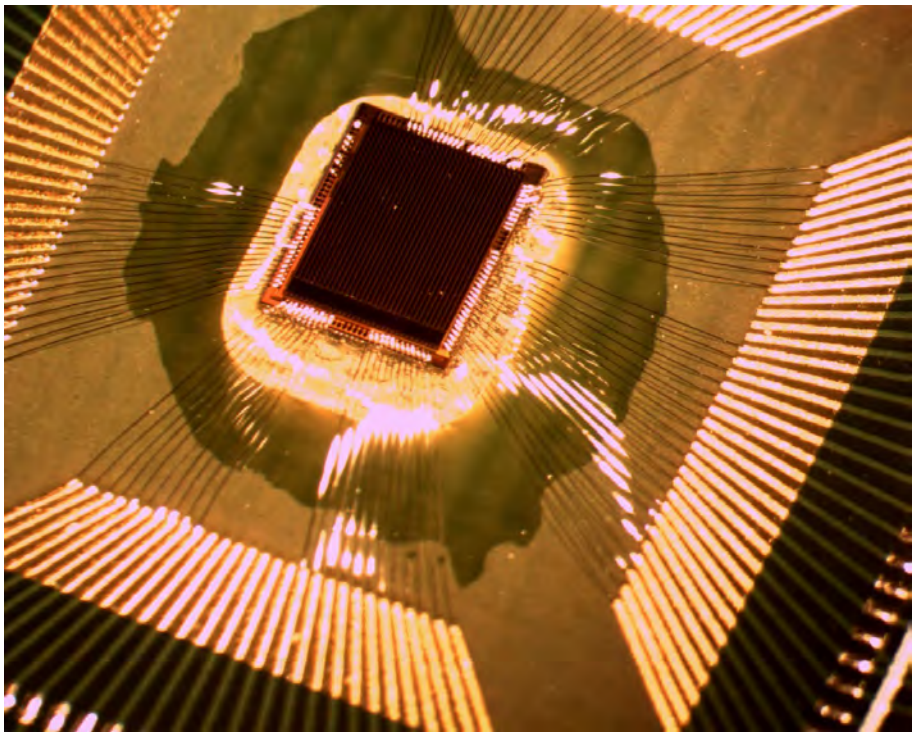


Figure 7.3: MuPix4 chip glued and directly wire bonded on a thinned PCB.

ToT signal, so that the readout in the hit-flag mode produced more and more hits at thresholds below 1.3 V. Under this condition no signals of a ^{90}Sr or ^{55}Fe source or of the injection pulses could be seen, only the signal of a laser diode could be detected. After a first step of debugging, where high-frequency parts of some signals were filtered by soldering capacitors directly at the pins of the chip socket between signals and ground, this crosstalk was only present at thresholds below 0.87 V. Some of these concerned signals were for example threshold, injections and baseline. The next step was to connect more power and ground pins of the MuPix4 chip via wire bonds to the chip carrier and hence to the PCB. That reduced the crosstalk below a threshold of 0.85 V. Connecting the analogue and digital ground to each other reduced the crosstalk further below a threshold of 0.82 V. In the first step (filtering the signals) the two grounds were also connected, so that it can be assumed that the connection of the analogue and digital ground leads to the largest improvement.

7.2 Measurements

7.2.1 Pulse Shapes

The pulse shapes are not directly measured by using an oscilloscope because the used FPGA firmware written by Niklaus Berger has the option to make histograms of the ToT signal automatically, i. e. it counts how often each ToT was sampled with a binning of 20 ns which is the period of a 50 MHz cycle. This FPGA driven measurements have the advantages that the data can be better analysed and it is possible to do also large scans without doing every step by hand. Because the FPGA cannot show how the ToT signal looks like, the ToT signal taken with the oscilloscope is shown in figure 7.4. In addition the FPGA can trigger a pulse generator to which the LED is connected to obtain the latency. This information is stored in a text file and the pulse shape is obtained by means of a python programme. The ToT is about 1000 ns long at low thresholds which is much shorter than the ToT of the MuPix2 chip which was of the order of several µs [Per12b].

The pulse shapes for different temperatures (see figure 7.5) show that the temperature effect is very small for the MuPix4.

7.2.2 Signal-to-Noise Ratio

A large signal-to-noise ratio ensures that at a well chosen threshold the signal efficiency is high while the noise is very low.

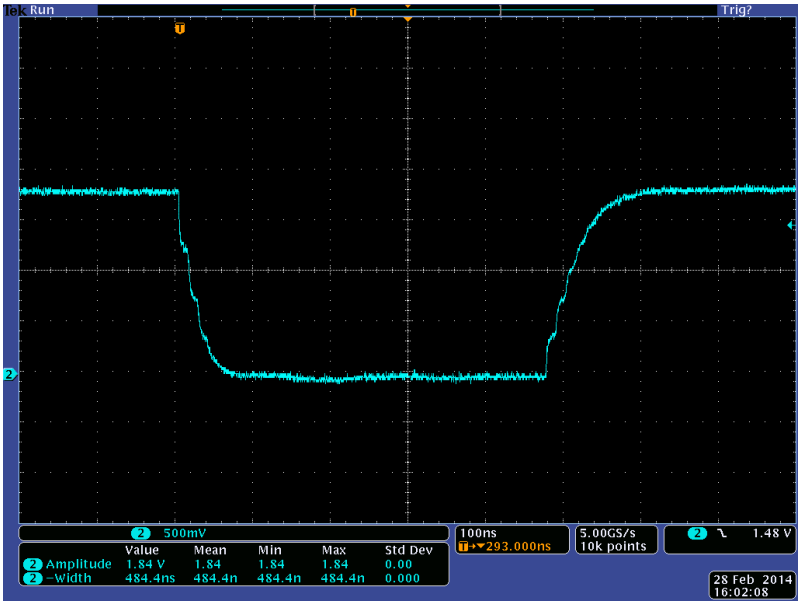


Figure 7.4: ToT signal of a centre pixel of the MuPix4 chip.

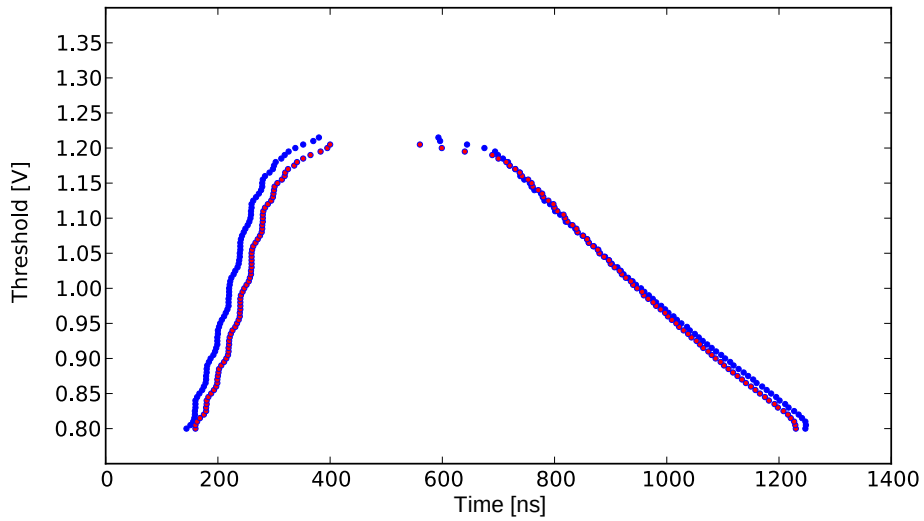


Figure 7.5: Pulse shapes of the MuPix4 chip at 30 °C (blue) and 60 °C (red).

The signal-to-noise ratio (SNR) was measured in two ways:

Time over Threshold Mode

The ToT mode was used to measure the noise of the baseline. The threshold was set above the baseline and then decreased below the baseline in steps. If there was no noise at all, the ToT signal would be always high[1] when the threshold is above the baseline and it would be always low[1] when the threshold is below the baseline. But noise leads to fluctuations (baseline, signal input, threshold) so that even if the threshold is slightly above the baseline there are noise hits seen. The FPGA generates a ToT histogram for each threshold for a fixed time. While the threshold decreases, the ToT signal becomes longer and longer until it is always low. Then the FPGA cannot detect the ToT signal anymore because the rising edge is missing. Then the ratio of the total ToT of a histogram to the generation time for this histogram is plotted against the threshold.

From the obtained S-curve the noise can be determined by fitting an error function to it. The following function was used:

$$f(x) = A \cdot erf\left(\frac{1}{\sqrt{2}\cdot\sigma}\cdot(x - x_c)\right) + c \tag{7.1}$$

The width σ of this error function is a measure of the noise and the mean value x_c is the value of the baseline (see figure 7.6). c is the vertical displacement of the function. For thresholds below 780 mV the ratio of the total ToT to the measuring time decreases again. This is due to the fact, that the FPGA cannot detect the ToT anymore, because it is always low and the rising edge is missing. The value of the baseline at a temperature of 24 °C and at a HV of -70 V is 778 mV and the noise around the baseline is 2 mV. At a temperature of 70 °C the baseline is slightly higher (780 mV) but the noise stays the same. Since the error function fit in figure 7.6 differs from the measured curve, the noise could be larger and thus the SNR could be smaller.

Not only the noise but also the signal must be measured in order to calculate the SNR. Hence, the S-curve was measured again with an injection signal calibrated to the signal of a ^{55}Fe source. For every threshold 100 injection pulses are generated and the hits that were registered by a single pixel were counted by counting the entries of the ToT histogram of the FPGA. The ratio of registered hits to generated injections is plotted against the threshold (see figure 7.7). There are some points at thresholds below 800 mV

[1] High means that there is no signal and low means that there is a signal because the signal of the ToT is inverted for the MiPix4 (see figure 7.4).

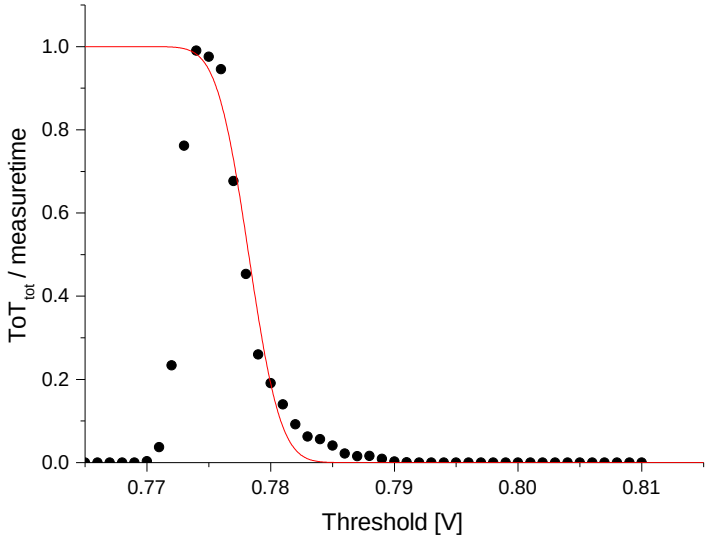


Figure 7.6: S-curve of the baseline with error function fit at a temperature of 24 °C and at a high voltage of -70 V.

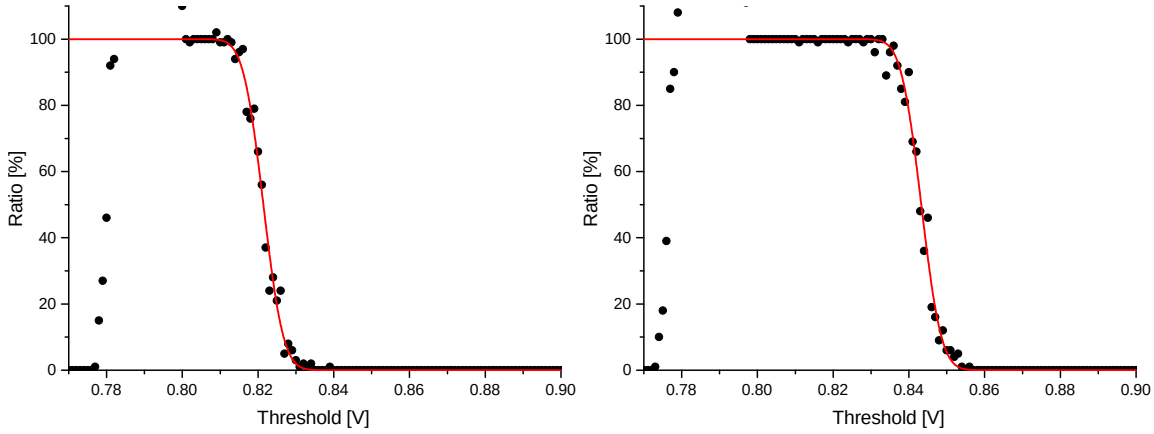
with a ratio of more than 100% because of noise. The mean value x_c of the error function fit is 827 mV at -1 V and 852 mV at -70 V. The width σ of the error function fit is 6 mV at -1 V and 5 mV at -70 V. The width σ of this error function fit is not only due to the noise of the chip but also due to the noise and fluctuations of the injection signal. Hence, for calculating the SNR of this signal not the width of figure 7.7 but the width of figure 7.6 is used for the value of the intrinsic noise. The SNR is calculated by dividing the difference of the mean value x_c and the baseline by the noise σ:

$$\text{SNR} = \frac{\text{signal} - \text{baseline}}{\text{noise}} \tag{7.2}$$

The values of the SNR for two different temperatures and HV is shown in table 7.1. As expected, the SNR is best for a high voltage of -70 V and at room temperature and it is worst for a very low high voltage of -1 V and at 70 °C. Even at high temperatures of 70 °C a good signal-to-noise ratio of SNR = 31.5 (at HV = -70 V) can be obtained. Since the detector will operate at temperatures of about 40 °C, a SNR between 31.5 and 37.0 is expected. The MuPix2 chip has a similar SNR between 21.5 and 35.7 (both values for room temperature, see [Per12b]).

Temperature / HV	-1 V	-70 V
24 °C	24.5	37.0
70 °C	21.0	31.5

Table 7.1: Signal-to-noise ratios for the MuPix4 chip at 24 °C and 70 °C and high voltages of -1 V and -70 V.



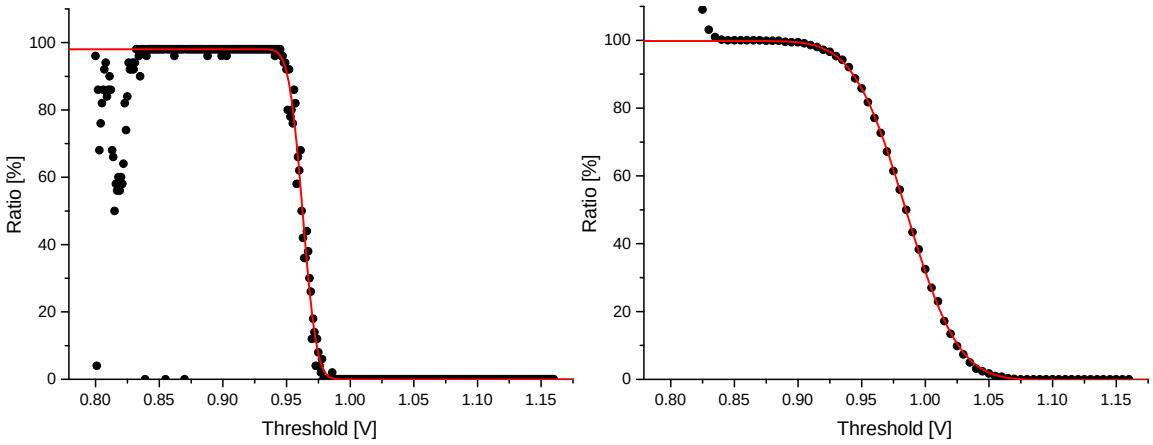
(a) HV: -1 V

(b) HV: -70 V

Figure 7.7: S-curves of the injection for the MuPix4 chip in the ToT mode at (a) -1 V and (b) -70 V at 70 °C.

Hit-Flag Mode

With the hit-flag mode, both the S-curve of one single pixel and the S-curve of the whole pixel matrix can be measured. Again, like in the ToT mode, 100 injection pulses are generated and the registered hits are counted. For the whole matrix 640 hits are expected per injection pulse because every injection reaches half of the chip ($= \frac{32\times40}{2}$). Figure 7.8a shows the S-curve of one single pixel and figure 7.8b shows the S-curve of the whole pixel matrix with the highest possible injection pulse of 1.8 V. The mean values x_c of the fitted error functions are 963 mV for one pixel and 985 mV for the whole matrix, the widths σ are 9 mV for one pixel and 32 mV for the whole matrix. The width for the whole pixel matrix is larger because of pixel to pixel variations. Every single pixel can be tuned in threshold, to obtain a more uniform response. No SNR could be obtained because the readout created hits at thresholds below 820 mV because of the digital crosstalk; the baseline is at 778 mV.



(a) one single pixel (b) whole pixel matrix

Figure 7.8: S-curves of the injection for the MuPix4 chip in the hit-flag mode for (a) one single pixel and (b) for the whole pixel matrix.

The MuPix4 chip has much shorter shaping times and thus a shorter ToT (about 1 µs) as the MuPix2 chip (several µs). That means that the dead-time is also short. Furthermore, the temperature effect is very small compared to the MuPix2 chip. The SNR of the MuPix4 chip is even at high temperatures of 70 °C above 30.

8 Testbeam Campaigns

In the context of this master thesis five testbeam measurements were executed: four at the Deutsches Elektronen-Synchrotron (DESY) in Hamburg (Germany) and one at the Paul Scherrer Institute (PSI) in Villigen (Switzerland).

8.1 March 2013 at DESY

The electrons or positrons in the DESY II synchrotron generate a beam of bremsstrahlung photons at a carbon fibre inside the synchrotron. These photons are then converted into electron / positron pairs at a metal plate. A dipole magnet is then used to separate the electrons and the positrons horizontally. The electron beam is extracted through a collimator to the testbeam area (see figure 8.1). The magnet current can be changed to control the energy of the electrons. The energy of the electrons can be varied between 1 GeV and 6 GeV, the maximum beam rate is obtained at approximately 3 GeV [B$^+$07]. All testbeam measurements at DESY were operated at the testbeam line T22. During this testbeam the MuPix2 chip was tested.

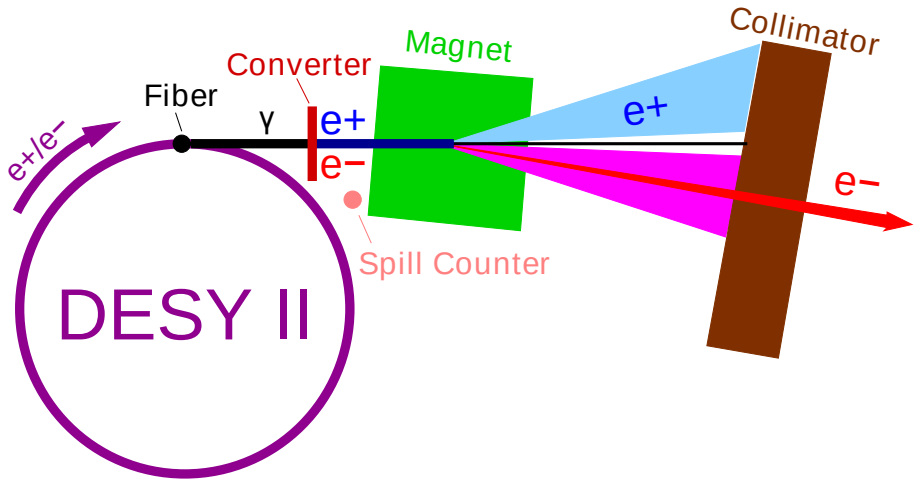


Figure 8.1: Schematic layout of a testbeam at DESY [DES14].

For the measurements the EUDET telescope [Rub12] was used. The main part of this telescope are six MIMOSA26 chips. The integration time of these chips is 115 µs. The

MIMOSA26 chips are read out in a rolling shutter mode. When a trigger signal is sent, the current frame is finished and one further frame is read out. This creates an integration time of the telescope of $(2 \cdot 115)$ µs. The telescope with the MuPix2 chip in the device under test (DUT) position can be seen in figure 8.2. In order to be able to mount the MuPix PCBs to the rotation stage of the telescope an adapter was made (see appendix E).

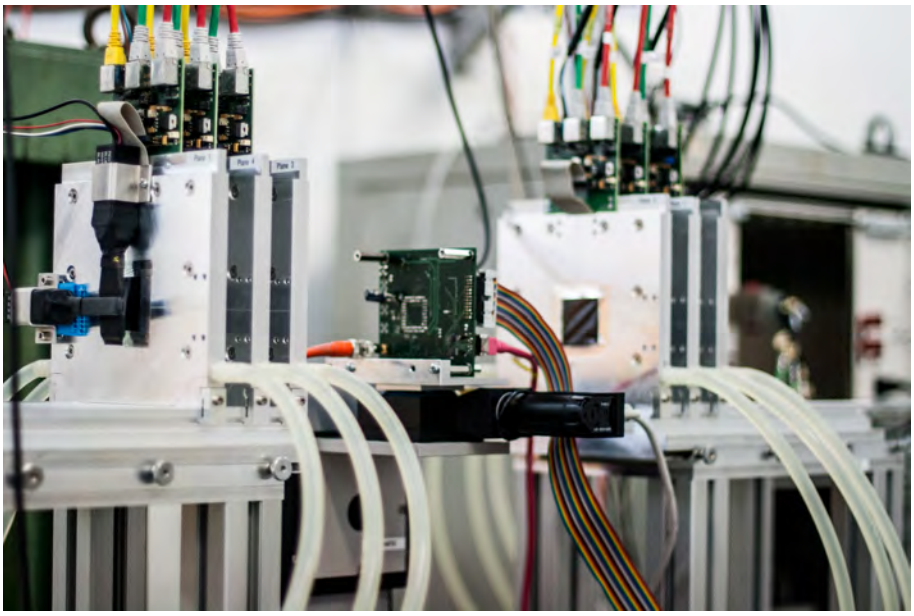


Figure 8.2: Picture of the EUDET telescope ACONITE at DESY with the MuPix2 PCB mounted on the rotation stage.

8.1.1 MuPix2

The MuPix2 chip was operated in the device under test (DUT) position such that its efficiency could be determined from reconstructing the tracks. Therefore the MuPix2 chip was operated only in the hit-flag mode. The MuPix2 took data for only 1 µs after the trigger signal, much shorter than the integration time of the EUDET telescope, so that only a few hits of tracks were stored, which were also registered by the telescope. Furthermore, it is not known at which time during the rolling shutter readout of the MIMOSA26 chips, the trigger signal was sent. Because of this timing problem, no efficiency could be determined.

8.2 June 2013 at DESY

During this testbeam a thick ($\approx 600\,\mu m$) and a thinned ($\approx 90\,\mu m$) MuPix3 chip were tested in the DUT position. The integration time of the MuPix3 chip was the whole time between two trigger signals to ensure that all hits of tracks were stored, which were also registered by the telescope. However, no efficiency was determined because of the pixel enabling issue. The chip was not only operated in the hit-flag mode but also in the ToT mode to measure pulse lengths.

8.2.1 Thick MuPix3 Chip

From the ToT histograms the mean of the ToT distribution of all enabled pixels was obtained by fitting a Gaussian function to the data. Since it is not known which pixels were enabled, only estimations can be made.

The ToT seems to decrease slightly with increasing high voltage (see figure 8.3), but it is expected to be the other way round, because more and more charge should be collected by the pixel electrodes with rising high voltage (see [Per12b]). This unexpected but not pronounced behaviour could be explained by the fact, that after every power cycle of the MuPix3 chip another set of random pixels is enabled. Figure 8.4 shows an almost linear decrease of the ToT with increasing threshold as expected.

8.2.2 Thinned MuPix3 Chip

During this testbeam also a thinned MuPix3 chip was tested. A ToT histogram for a threshold of 0.83 V and a high voltage of -60 V can be seen in figure 8.5a. The "peak 1" at low ToT could be due to a set of a few pixels that are less efficient because this peak only occurs at low thresholds below or equal to 0.83 V (see figure 8.6). The ToT is almost constant at high voltages between -60,V and -90 V at a threshold of 0.83 V (see figure 8.5b). The ToT is slightly longer for the thinned than for the thick chip. This could be explained by the fact that the electric field is inversely proportional to the distance d between the n-well and the p-substrate of the pixels ($E = u/d$). Because at strong electric fields the electrons generated by an ionising particle can ionise further atoms in the depletion layer. But it could also be a pixel or chip variation. For the thinned chip the ToT also decreases linearly with increasing threshold (see figure 8.6). Unfortunately the chips cannot be tested before and after thinning because they have to be glued and wire bonded to the chip carrier for testing and this procedure can only be done once per chip.

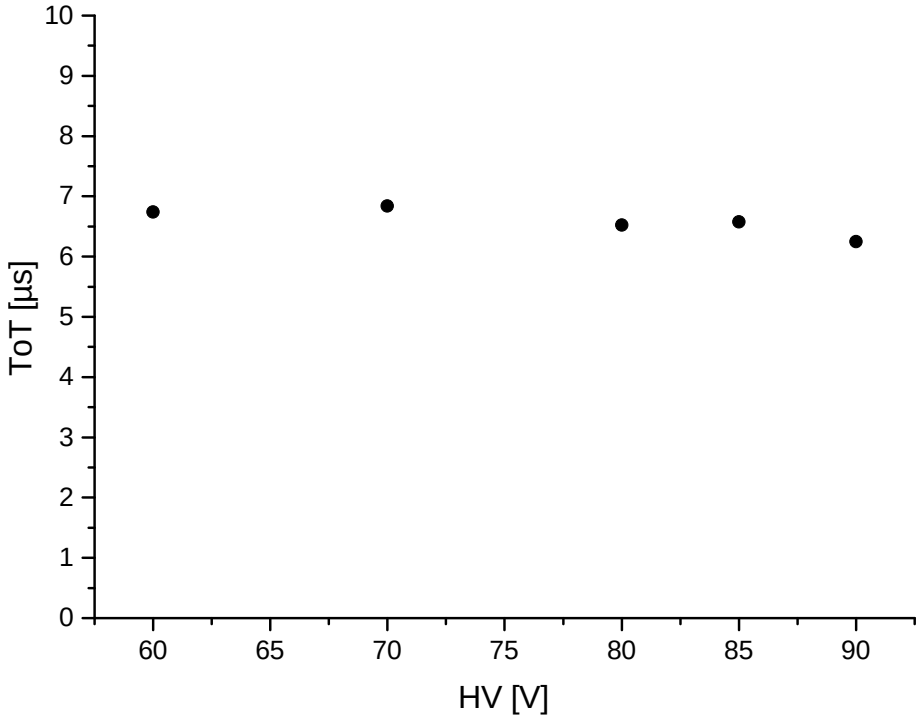


Figure 8.3: HV dependence of the ToT of the thick MuPix3 chip at a threshold of 0.83 V and at a beam energy of 3 GeV.

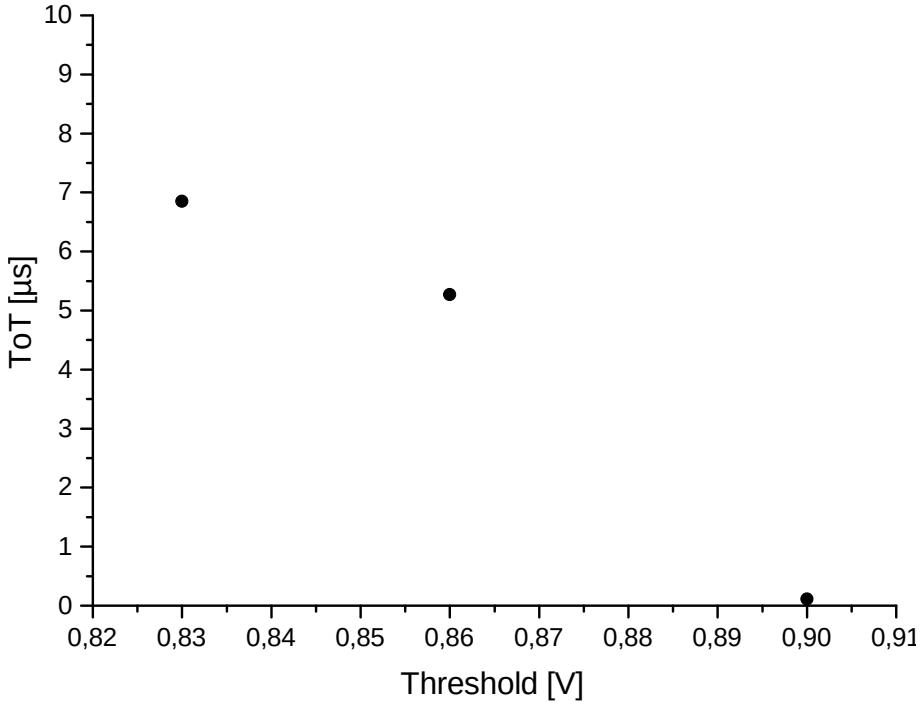
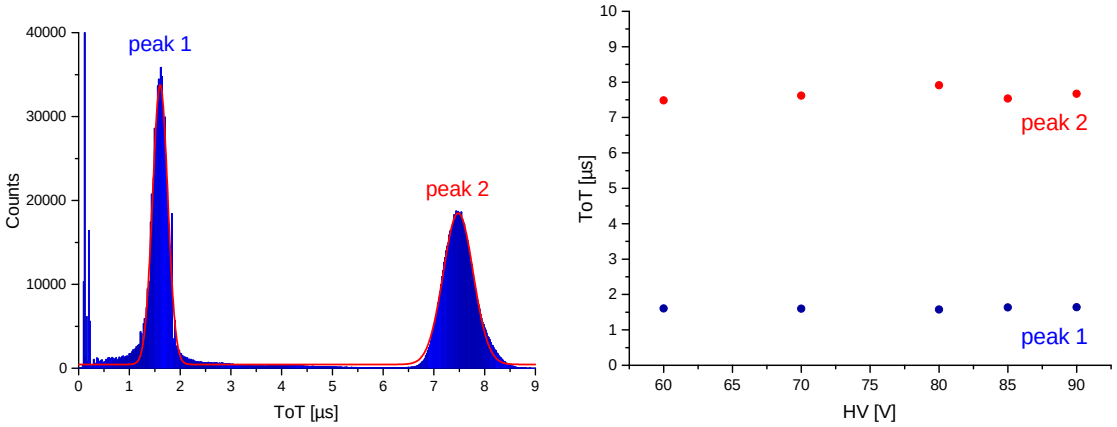


Figure 8.4: Threshold dependence of the ToT of the thick MuPix3 chip at a high voltage of -70 V and at a beam energy of 3 GeV.



(a) ToT histogram (b) HV dependence of ToT

Figure 8.5: Figure 8.5a shows the ToT histogram of the thinned MuPix3 chip at a threshold of 0.83 V, at a high voltage of -60 V and at a beam energy of 3 GeV. Figure 8.5b shows the HV dependence of the ToT of the thinned MuPix3 chip at a threshold of 0.83 V and at a beam energy of 3 GeV.

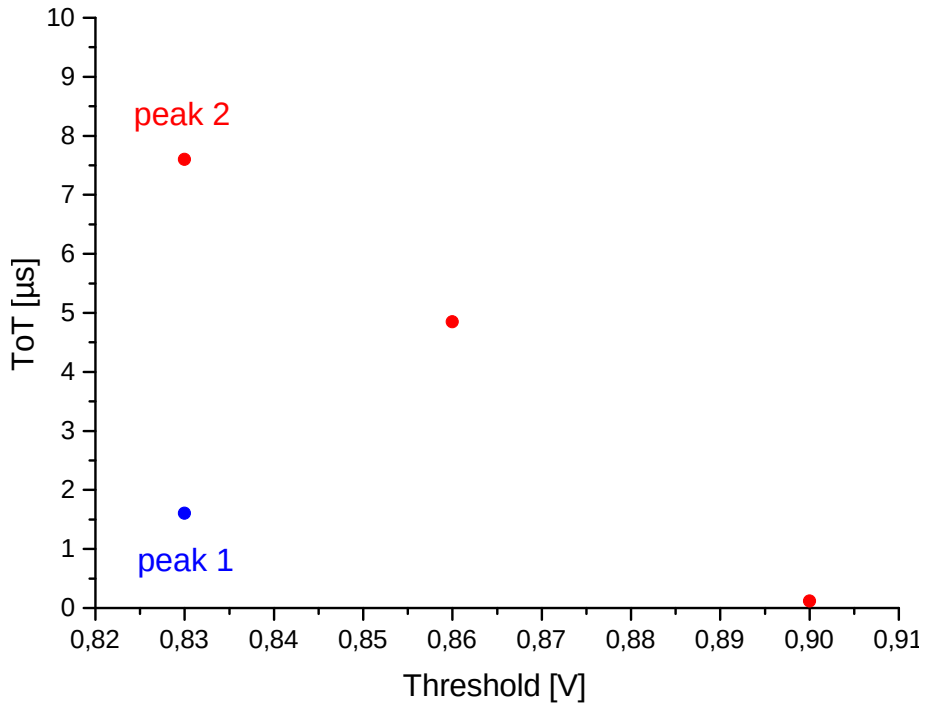


Figure 8.6: Threshold dependence of the ToT of the thinned MuPix3 chip at a high voltage of -70 V and at a beam energy of 3 GeV.

8.3 September 2013 at PSI

The third testbeam campaign was carried out at the piM1 beamline at PSI. The piM1 beamline provides pions with a momentum range between 100 MeV/c and 500 MeV/c [piM14], in this testbeam campaign an energy of 193.2 MeV was used. The pions decay most likely into muons which furthermore decay into electrons so that the chip could also be tested with electrons. All chips were operated in the ToT mode because no telescope was available and therefore efficiency measurements were impossible. During this testbeam also the latency could be measured because upstream and downstream of the MuPix chips timing scintillating tiles were placed (see figure 8.8). The latency is defined as the time between the detection of a particle in the tiles and the detection of the same particle in the MuPix chip. The ToT signal and the time of the two tile signals were measured and stored. Measurements were done with a thick ($\approx 600\,\mu m$) and a thinned ($\approx 80\,\mu m$) MuPix2 and a thick ($\approx 600\,\mu m$) and a thinned ($\approx 90\,\mu m$) MuPix3 chip. The following measurements are limited to electrons. The signal size distribution of the front scintillating tile can be seen in figure 8.7. The measurements of the electrons were obtained by cutting on the electron signal.

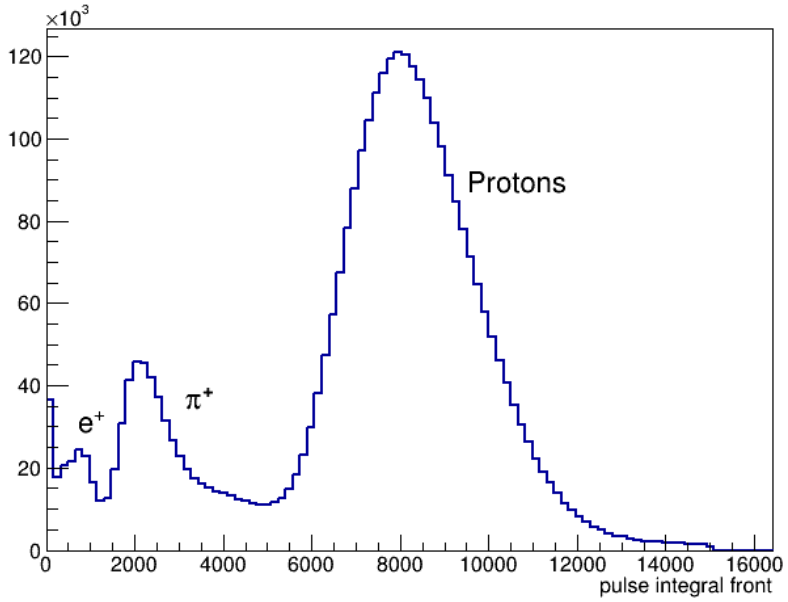


Figure 8.7: Beam composition obtained from the front scintillating tile.

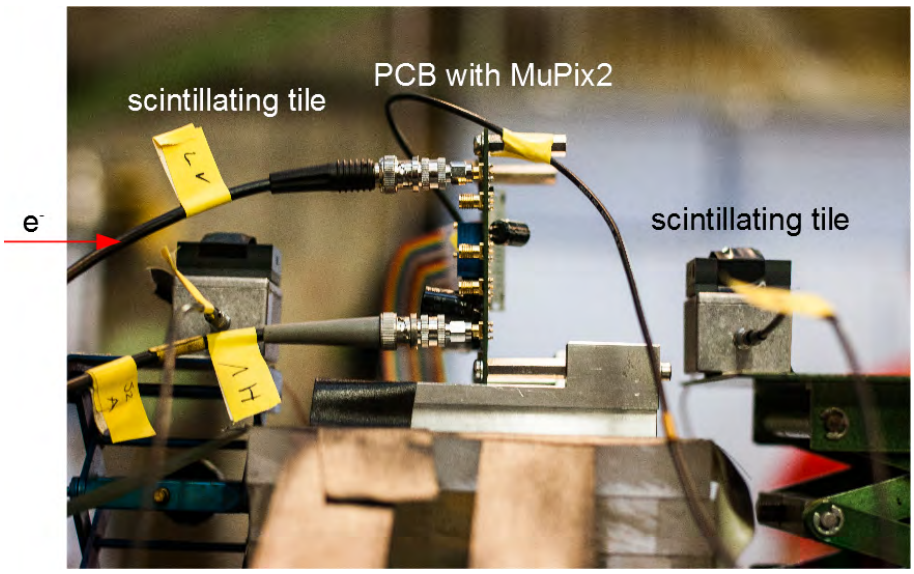


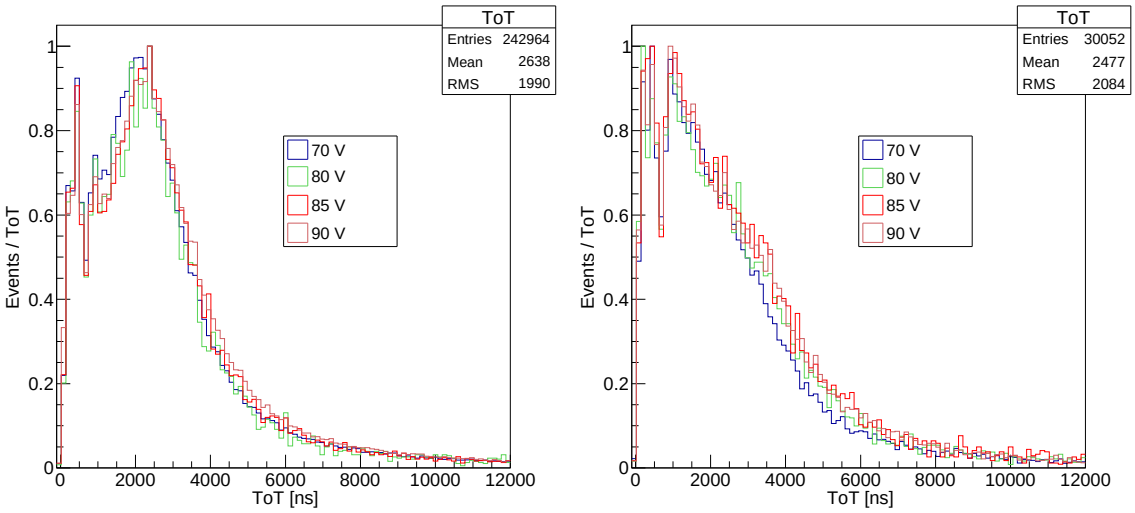
Figure 8.8: Setup at the PSI testbeam: PCB with the MuPix2 chip and up and downstream scintillating tiles.

8.3.1 MuPix2

In order to measure the ToT signal in the counting hut, an additional LEMO® cable had to be soldered to the PCB. This cable was then connected to an approximately 15 m long BNC cable. All measurements were done at a fixed threshold of 840 mV. The ToT increases slightly with increasing high voltage for both the thick and the thinned chip (see figures 8.9 and 8.10). However, the thinned chip seems to not work properly[1] at a high voltage of -90 V. It is observed that pixels at the edge have a shorter ToT than pixels at the centre of the chip. That can be explained by the fact that electrons ionise atoms also at the edge of the chip outside the pixel matrix. This charge has a longer drift path and therefore less charge reaches the electrode (see figure 8.11). The ToT of the thinned chip is longer than the ToT of the thick chip (see figure 8.12) which is the case for all measured pixels, therefore it is most likely no pixel variation effect. This could maybe be explained by a higher electric field of the thinned chip between the p-substrate and the n-well assuming that the size of the depletion layer depends on the thickness of the substrate. The latency of the thick and the thinned chip is almost the same and shows no HV dependence (see figure 8.13), but it can be seen that the latency at -90 V for the thinned chip is slightly higher, which is consistent with the short ToT in figure 8.10. The latency of a corner pixel is on average longer than of a centre pixel (see figure 8.14) because the charge that is

[1] Since the chip could not be tested before thinning, that could also be attributed to a bad chip.

created outside the pixel matrix needs more time to reach the electrode (see figure 8.11).



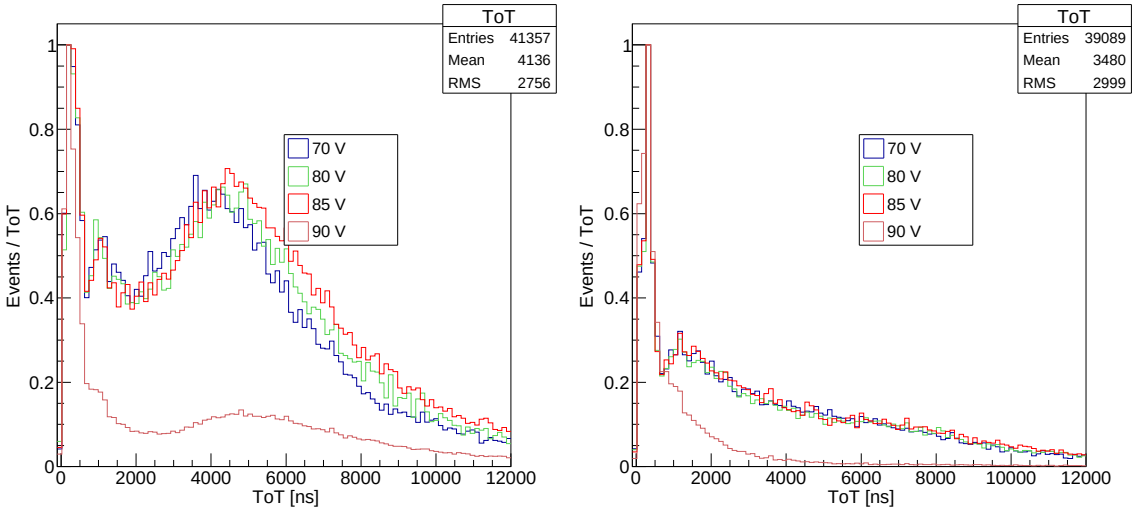
(a) centre (b) edge

Figure 8.9: ToT histograms of the thick MuPix2 chip for different HV and different pixels normalised to the maximum: 8.9a shows the histograms for centre pixels and 8.9b shows the histograms for edge pixels [Hut14].

8.3.2 MuPix3

The ToT signal was tapped at the "HB" LEMO® connector of the PCB. The measurements were done at a threshold of 830 mV and, if not denoted differently, without disabling pixels.

Figure 8.15 shows a slight decrease of the ToT for both the thick and thinned chip with increasing high voltage which is not expected. The charge collection should be faster for higher high voltages. The latency decreases with increasing high voltage from 160 ns to 140 ns (see figure 8.16) as expected but the latency is longer (180 ns) for the thin chip. The pixel dependence of the ToT is undefined. As seen in figure 8.17 the ToT distribution is the smallest if no pixels are disabled. This implies that only a very small number of pixels are enabled after switching on the MuPix3 chip. In addition, after every power cycle another set of pixels is enabled. The thinned chip has almost no pixel dependence of the latency but has a higher latency than the thick chip (see figure 8.18). The latency of the thick chip is the longest if only the edge pixels are enabled and it is the shortest if all pixels are enabled which is consistent with the MuPix2 chip. If the edge pixels are



(a) centre (b) edge

Figure 8.10: ToT histograms of the thinned MuPix2 chip for different HV and different pixels normalised to the maximum: 8.10a shows the histograms for centre pixels and 8.10b shows the histograms for edge pixels [Hut14].

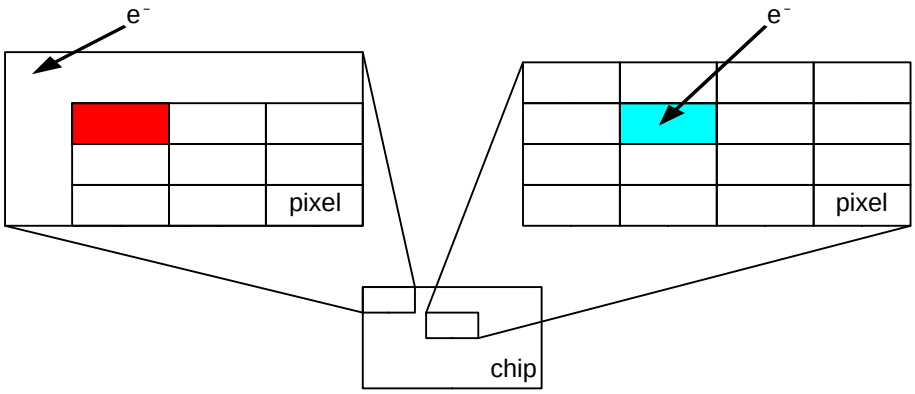


Figure 8.11: The ToT of a corner pixel is shorter and the latency is longer than for a centre pixel if hit by a single particle, which in one case is outside abd in the other case inside the pixel cell.

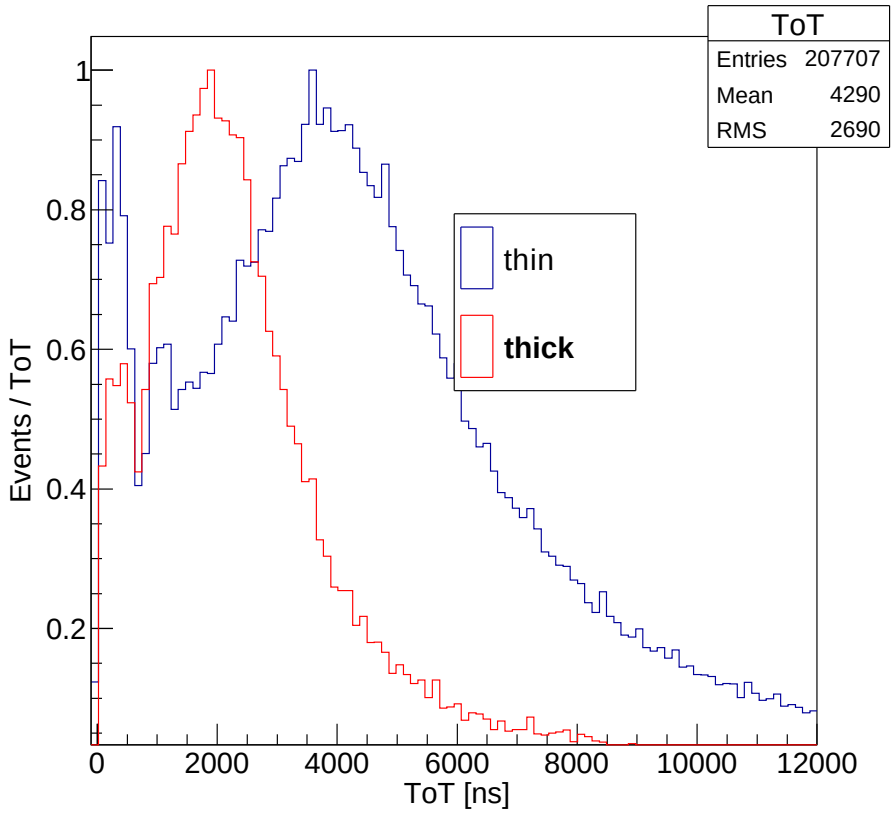
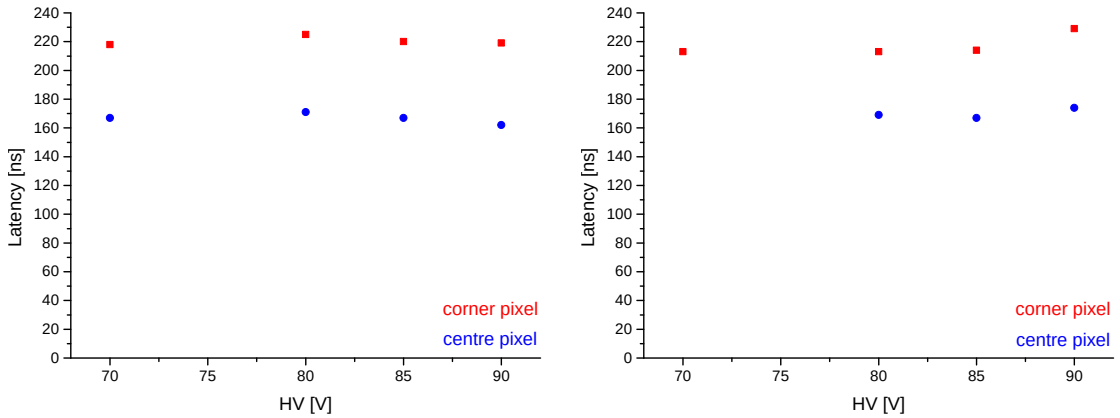


Figure 8.12: ToT histograms for the thick and the thinned MuPix2 chip at a HV of -85 V normalised to the maximum [Hut14].



(a) thick (b) thinned

Figure 8.13: HV dependence of the latency for a centre and a corner pixel of the MuPix2 chip: 8.13a shows the dependence for the thick chip and 8.13b shows the dependence for the thinned chip.

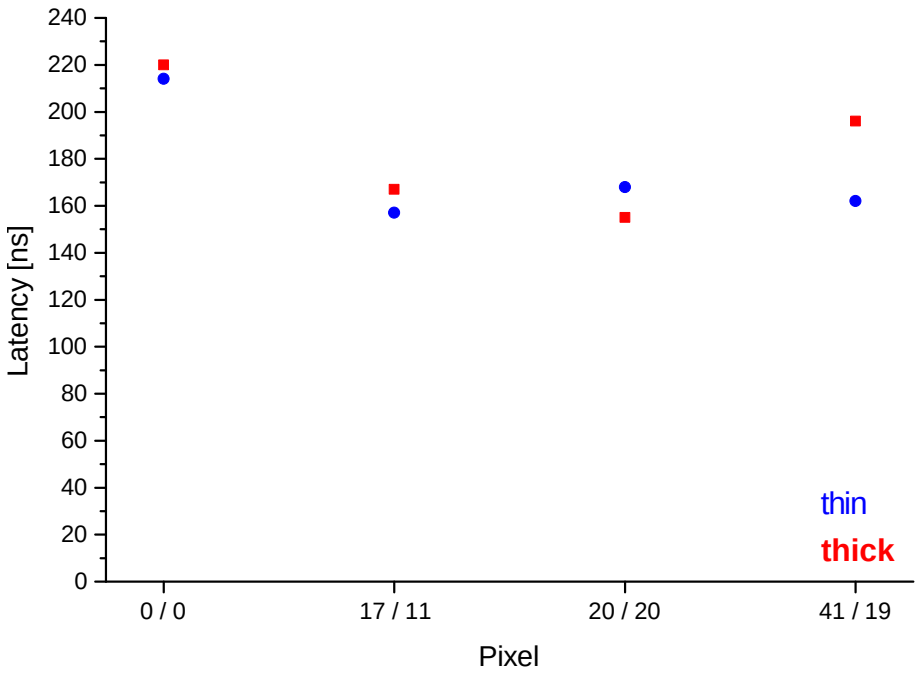
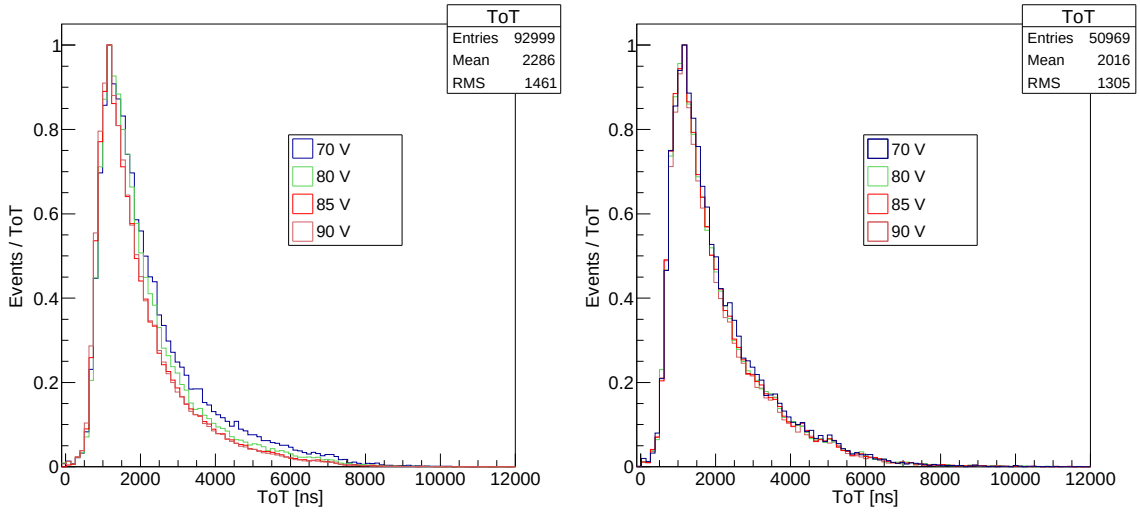


Figure 8.14: Latency for the thick and the thinned MuPix2 chip for different pixels. The numbers on the x-axis represent the pixel addresses (column / row).

disabled, the latency should become shorter, because the contribution of the edge pixels with a longer latency is missing. However, this is not the case.

8.3.3 MuPix4

On the last day, right before packing, the MuPix4 chip was placed in the beam. But there was no time to switch the beam on due to trouble in the accelerator. However, while testing the connection of the ToT signal from the beam area to the hut with a ^{90}Sr source, the MuPix4 chip detected real particles the first time.



(a) thick (b) thinned

Figure 8.15: ToT histograms of the MuPix3 chip for different HV normalised to the maximum: 8.15a shows the histograms for the thick chip and 8.15b shows the histograms for the thinned chip [Hut14].

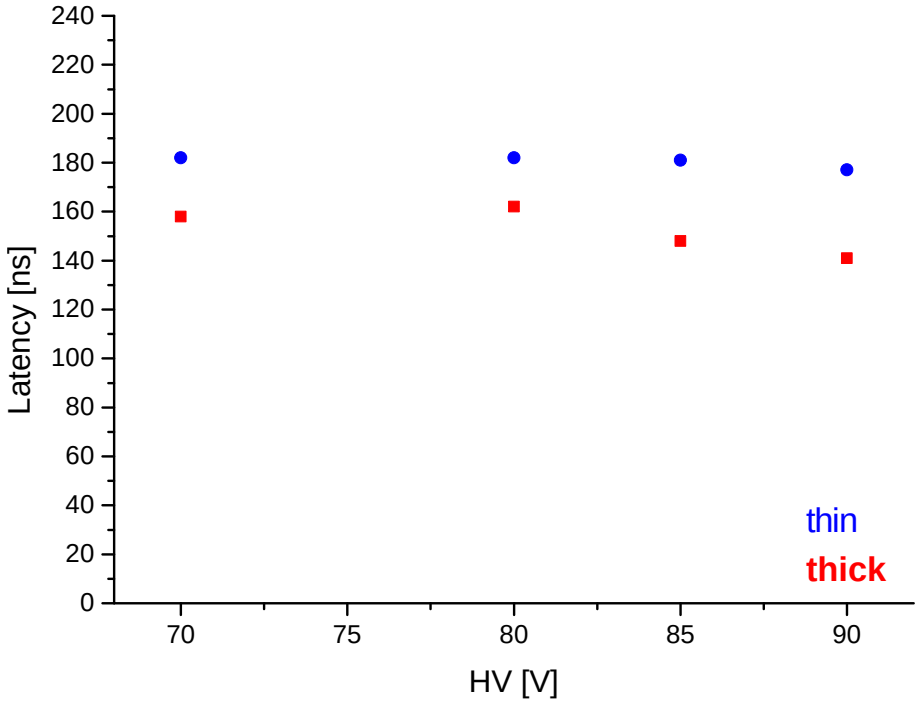


Figure 8.16: HV dependence of the latency of the thick and the thinned MuPix3 chip.

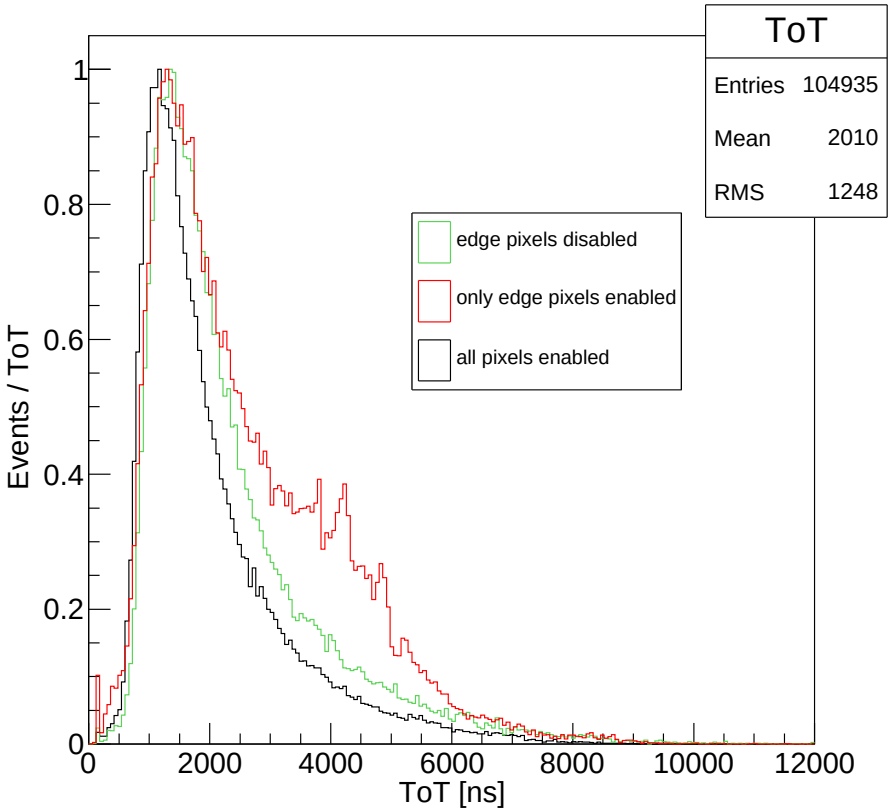


Figure 8.17: ToT histograms of the thick MuPix3 chip for different pixels at a HV of -85 V normalised to the maximum [Hut14].

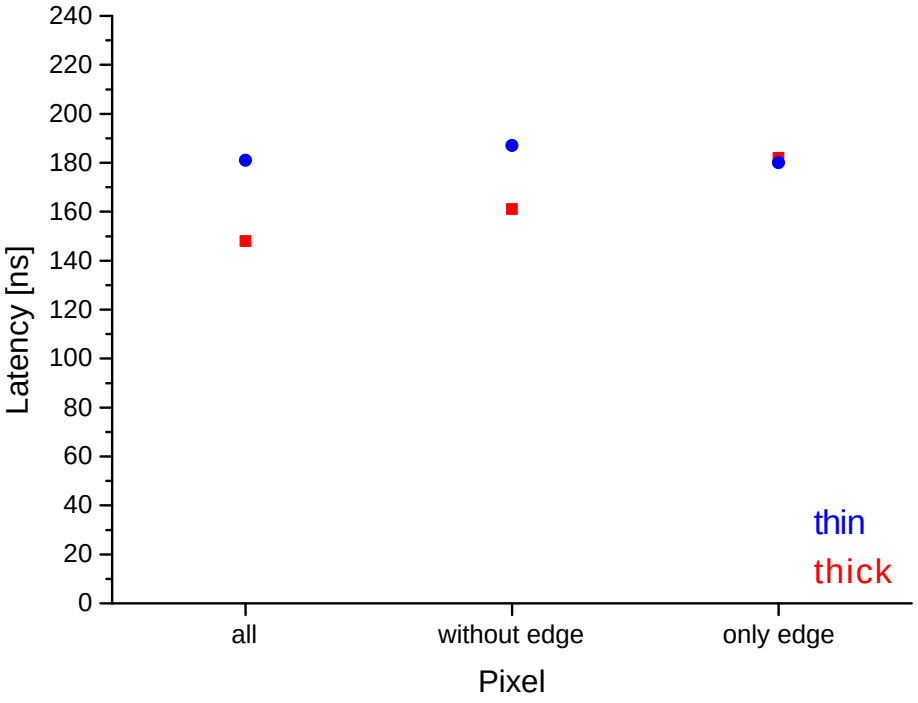


Figure 8.18: Pixel dependence of the latency of the thick and the thinned Mupix3 chip at a HV of -85 V.

8.4 October 2013 at DESY

The energy of the electron beam was 3 GeV because at this energy the electron rate was close to maximum. During this testbeam the MuPix4 setup of Ivan Perić was used, because the digital crosstalk was too large with our setup at that time (see section 7.1.3).

8.4.1 MuPix4

The integration time for the MuPix4 chip readout was set to twice the integration time of the MIMOSA26 chips both before and after the trigger signal. For the timing measurements the integration time had to be shorter.

Timing Measurements

The timing resolution was obtained by making a histogram of the differences between the timestamps of the chip and the trigger signal from the trigger logic unit (TLU). The timing resolution is about 17 ns which is the fastest ever achieved result for MAPS (see the parameter "p2" in figure 8.19, note that this value is in units of 10 ns).

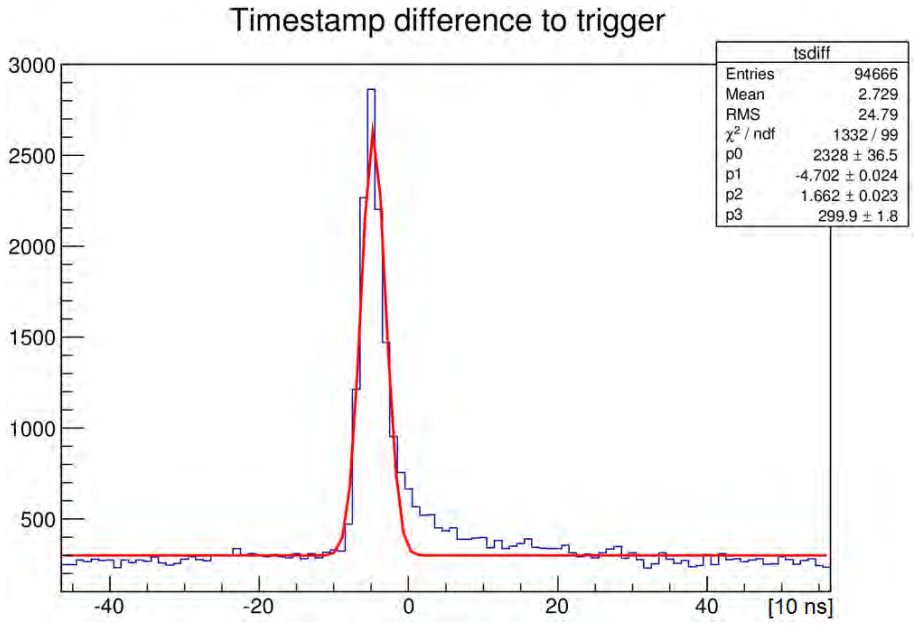


Figure 8.19: Histogram of the difference between the MuPix4 timestamp and the trigger signal (plot made by Niklaus Berger).

Efficiency Measurements

The determination of the efficiency of the MuPix4 chip yielded a value of 99% (see figure 8.20). An improvement is expected, if the measurement is done by tuning the threshold of every pixel individually.

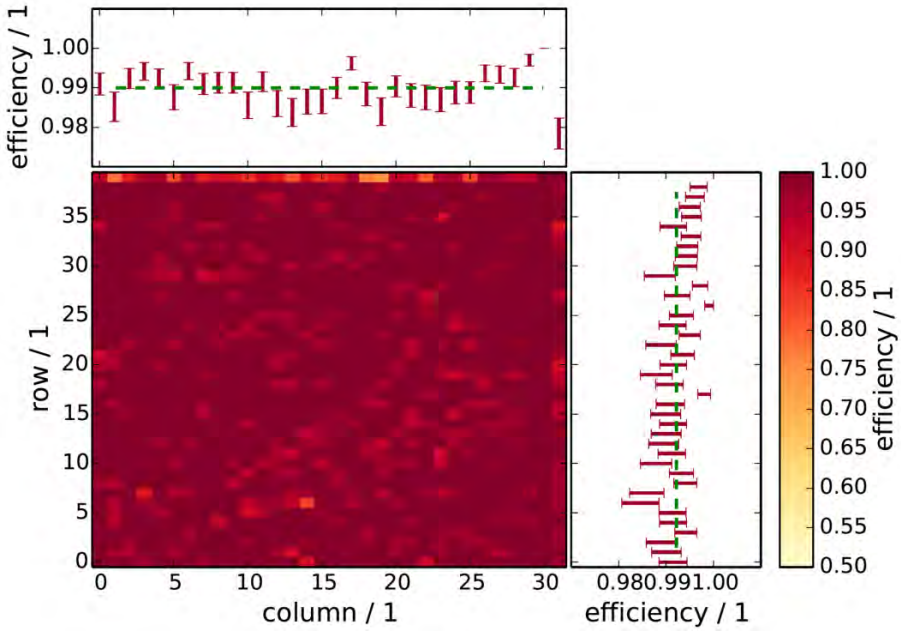


Figure 8.20: Plot of the efficiency of the MuPix4 chip [Kie15].

8.5 February 2014 at DESY

8.5.1 MuPix4

During this testbeam first the MuPix4 setup of Ivan Perić was used and then our setup was used in the device under test position. The integration time for the MuPix4 chip with our setup was between the last trigger signal and 200 µs after the current trigger signal. The efficiency measurements have only be analysed for the setup of Ivan Perić.

Efficiency Measurements

With the data taken during this testbeam the efficiency of the MuPix4 chip could be determined for different thresholds and rotation angles relative to the beam direction (see figure 8.21). Efficiencies of more than 96% could be achieved and the best efficiency was almost 100% at a threshold of 823 mV and a rotation angle of 45°.

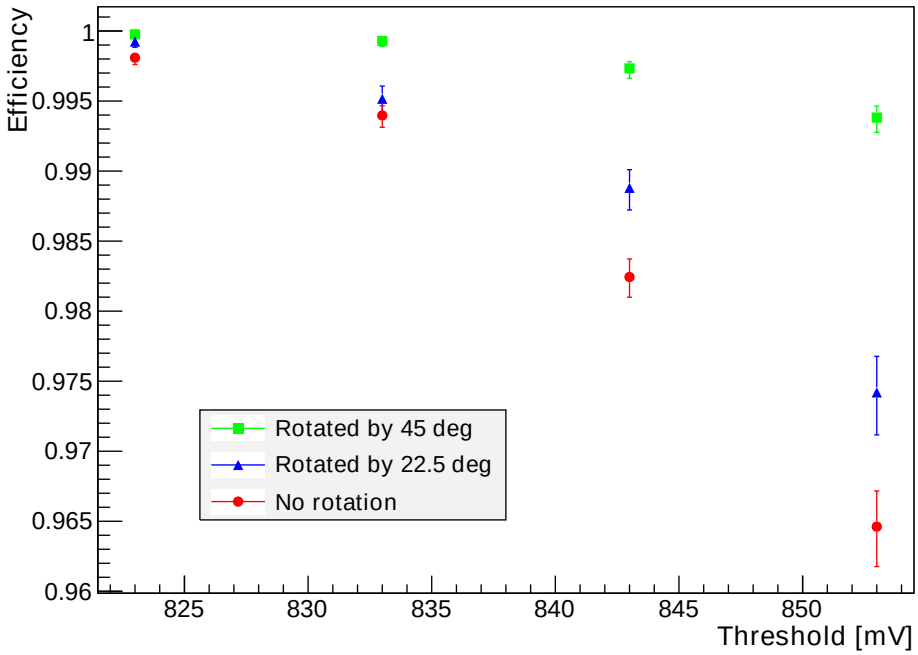


Figure 8.21: Efficiency of the MuPix4 for different rotation angles and thresholds at a HV of -70 V [KvB14].

MuPix4 Telescope

A first telescope consisting of four MuPix4 chips that are placed one after another has been tested [Hut14]. Correlations between the rows and columns of different chips could be seen and an offline track fitting is in process.

The testbeam measurements show that the thinned MuPix2 and MuPix3 prototypes work almost as well as the thick ones but show some unexpected behaviours. It is not yet understood why the ToT of the thinned chips is longer than the ToT of the thick chips. Therefore, more chips has to be thinned and tested.
The MuPix4 chip has a very good efficiency of almost 100% and an extremely good timing resolution of 17 ns.

Part III

Discussion

9 Discussion and Outlook

The proposed Mu3e experiment searches for the lepton flavour violating, and thus in the Standard model forbidden, decay $\mu^+ \rightarrow e^+e^-e^+$ with a target sensitivity of $< 10^{-16}$ which is four orders of magnitude better than previous experiments [B$^+$12b]. In the extended Standard model which includes neutrino mixing this decay is suppressed with a branching ratio of BR $< 10^{-54}$. Hence the observation of this decay would be a clear hint for new physics beyond the Standard Model.

The Mu3e experiment uses HV-MAPS for the tracking detector because these sensors have important advantages. The HV-MAPS have a fast charge collection time and can be thinned down to 50 µm. Consequently the material of the detector can be minimised and therefore, the momentum resolution can be improved by reducing multiple scattering of the positrons and electrons.

In this thesis three HV-MAPS prototypes (MuPix2, MuPix3, MuPix4) have been tested. In addition thinned MuPix2 and MuPix3 chips have been tested.

The pulse shape of the MuPix2 chip has been measured for temperatures of 30 °C and 60 °C. The latency increases from 180 ns to 310 ns and the ToT decreased from 5400 ns at 30 °C to 2300 ns at 60 °C. The ToT measured at the PSI testbeam was about 2000 ns for the thick MuPix2 chip and for the thinned chip a two times higher value of about 4000 ns was measured. This could be explained by the fact that the distance between the p-substrate and the n-well electrode is smaller at the thinned chip and therefore the electric field is stronger. At a high voltage of 90 V the thinned chip seems not to work properly anymore. But since the chip could not be tested before thinning this measurement has to be repeated with more thinned chips. Otherwise, the thinned chip shows good functionality if the high voltage is below 90 V.

No timing information of a single pixel could be obtained by measuring the pulse shape of the MuPix3 chip, because the measured ToT signal is always an OR of all enabled pixels. The common ToT signal was measured to have large fluctuations. The ToT measured at the second DESY testbeam with 3 GeV electrons was about 7000 ns at low thresh-

olds and decreased almost linearly with increasing thresholds. At the same time with increasing HV the ToT decreased slightly. The latency obtained at the PSI testbeam with electrons is for the thick chip between 140 ns and 160 ns whereas the thinned chip has a longer latency of about 180 ns. The ToT was about 2000 ns long. In principle the thinned chip shows the same behaviour as the thick chip. For these measurements only a few pixels were enabled.

The MuPix4 chip has to be wire bonded from the chip to the chip carrier to avoid short circuits between the scribe line, which is at the potential of the high voltage, and the signal lines. The timing of the MuPix4 chip has been improved compared to the MuPix2: The ToT is much shorter but the pulse hight is comparable. The MuPix4 chip is also less effected by high temperatures, which can be seen in the SNR: The SNR for the expected operation conditions for the Mu3e experiment is larger than 31.5 for 70 °C at HV = -70 V because temperatures of about 40 °C are expected. New MuPix4 PCBs have been designed where the digital crosstalk of the readout in the hit-flag mode is almost completely eliminated. In the future MuPix4 chips have to be thinned and tested.

The efficiency of the MuPix4 chip calculated from the data of the testbeams is almost 100%. Furthermore an excellent timing resolution of 17 ns was determined.

The first telescope consisting of four MuPix4 chips has been successfully tested and correlations between the columns and rows of different chips could be seen [Hut14].

The first MuPix6[1] prototype has been wire bonded and is now being tested. The issue of the wrong pixel addresses for every second double row, which the MuPix4 has, has been corrected.

The high efficiency and very good spatial and timing resolution of the MuPix4 prototype fulfil already now the specifications of the Mu3e pixel detector. In the coming year larger prototypes with fully integrated digital readout will be designed and tested.

[1] The MuPix6 is the fifth HV-MAPS prototype for the Mu3e experiment.

Part IV

Appendix

A Layouts of the MuPix Prototypes

In this chapter the layouts of the MuPix prototypes are shown. The lower part of the chip is the digital part where the readout cells are located. This part is also visible to the naked eye. That helps to glue the chip in the right direction on the chip carrier or on the PCB. This part is very large in the MuPix2 chip but has been reduced in the following prototypes. The pixels as well as the bonding pads can be seen. Using a microscope, the IBM® label in the upper left corner and the text “MUPIXEL” in the upper right corner can be seen.

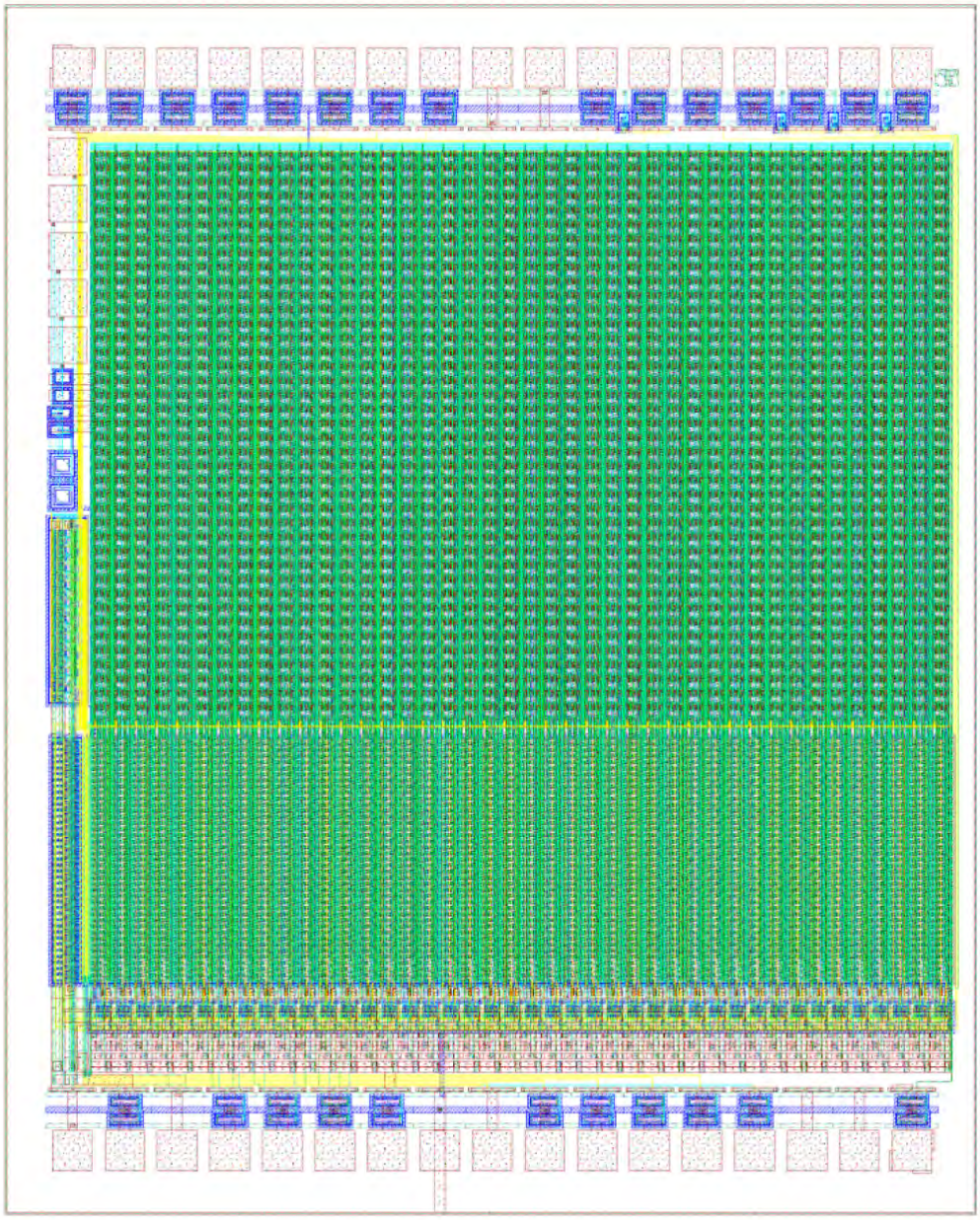


Figure A.1: Layout of the MuPix2 chip.

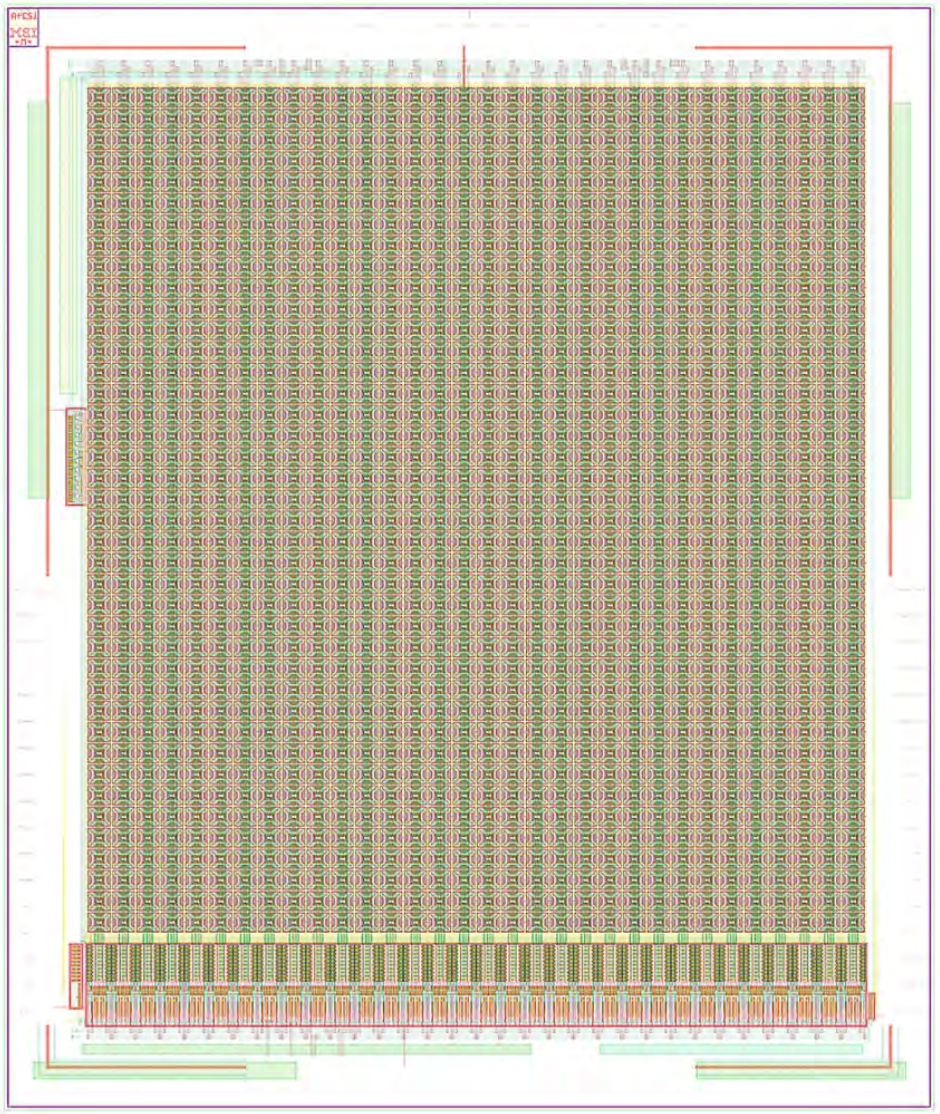


Figure A.2: Layout of the MuPix3 chip.

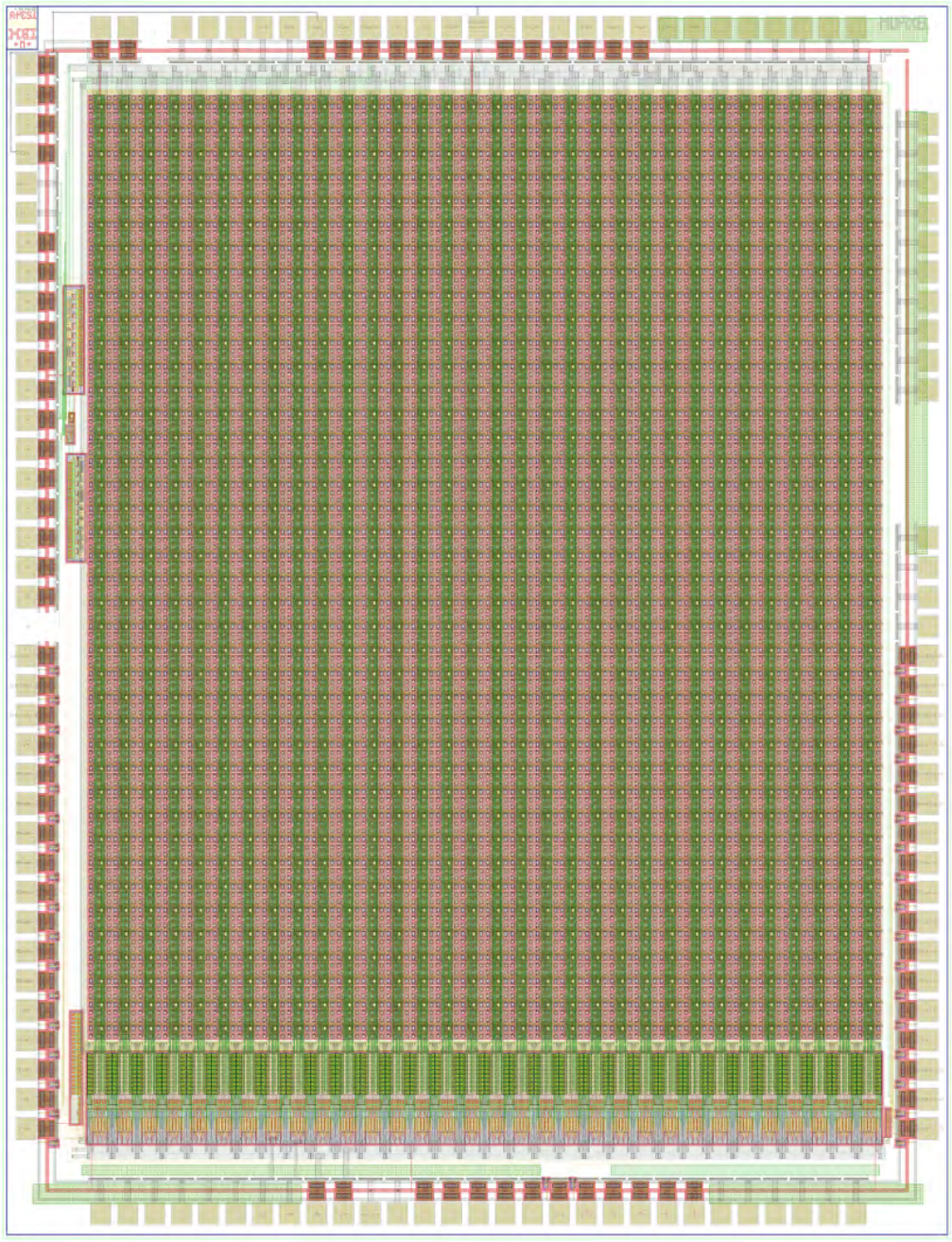


Figure A.3: Layout of the MuPix4 chip.

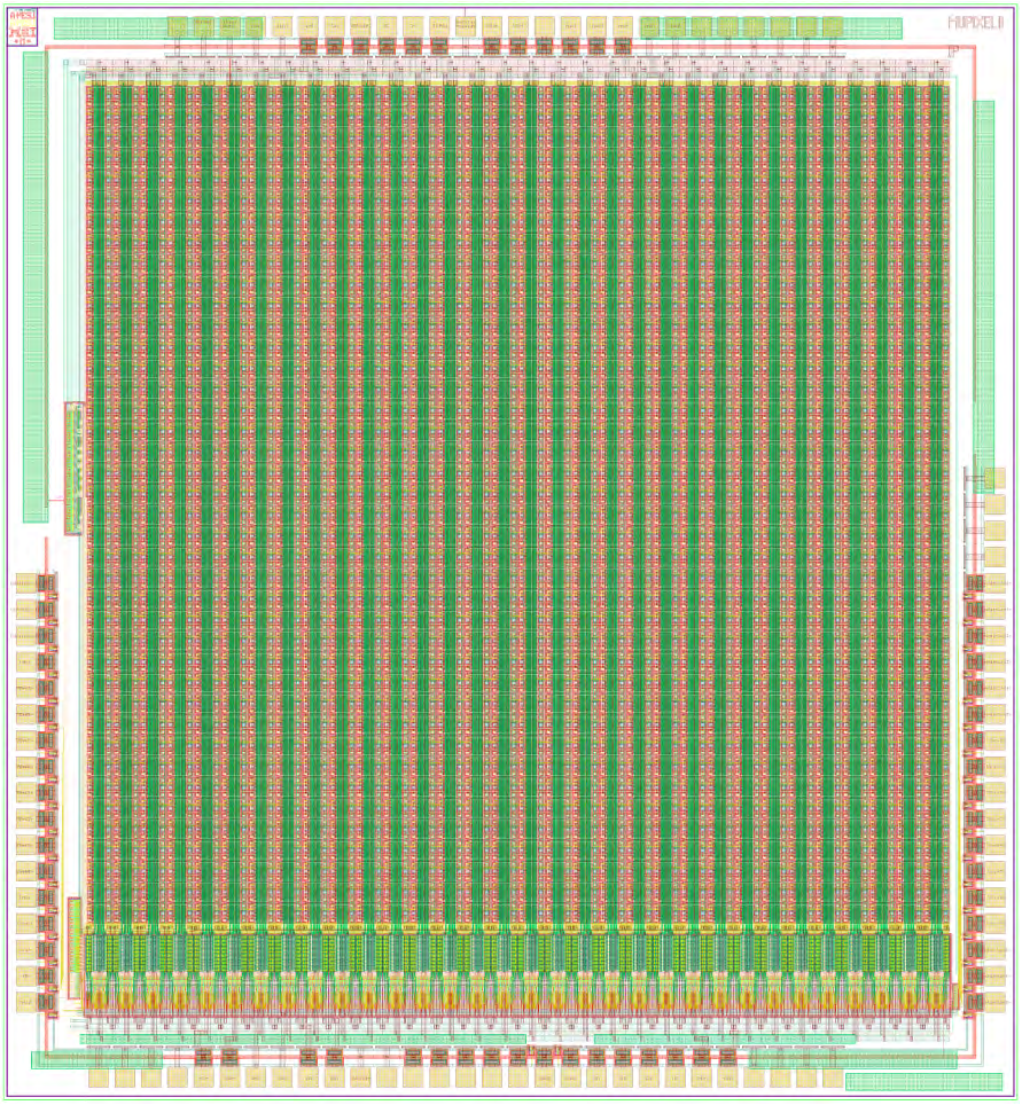
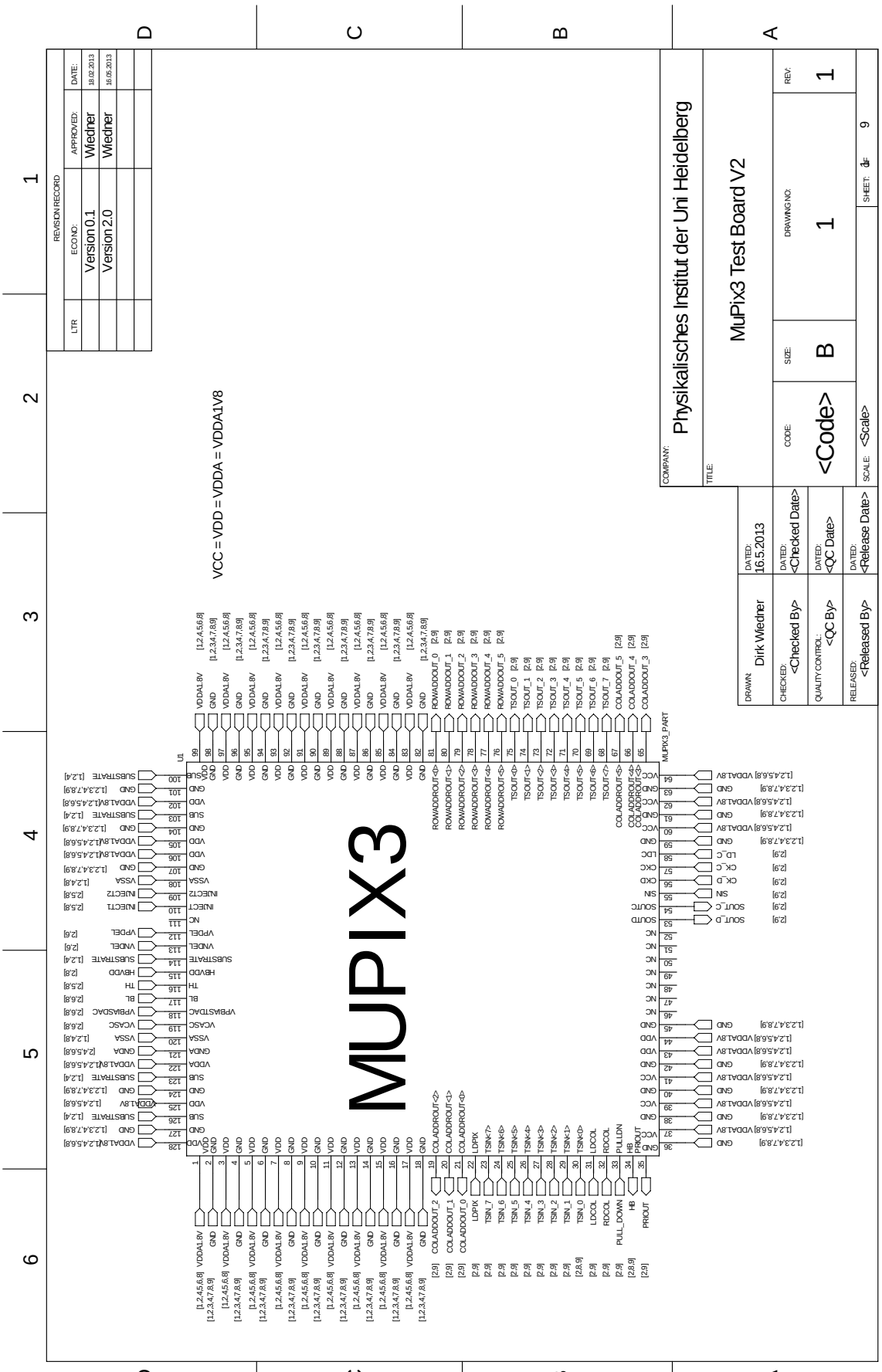


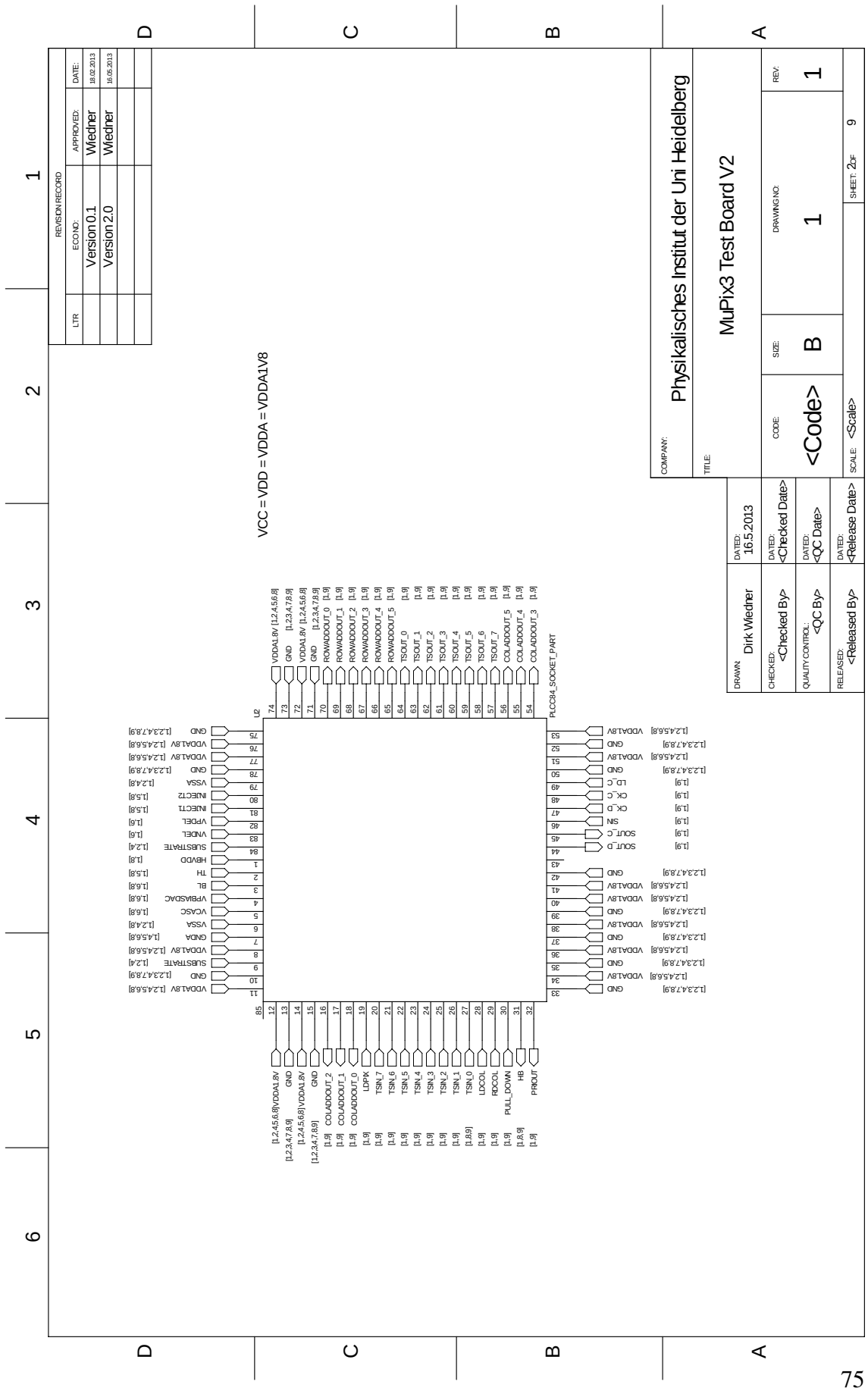
Figure A.4: Layout of the MuPix6 chip.

B Schematics of the MuPix3 and MuPix4 PCBs

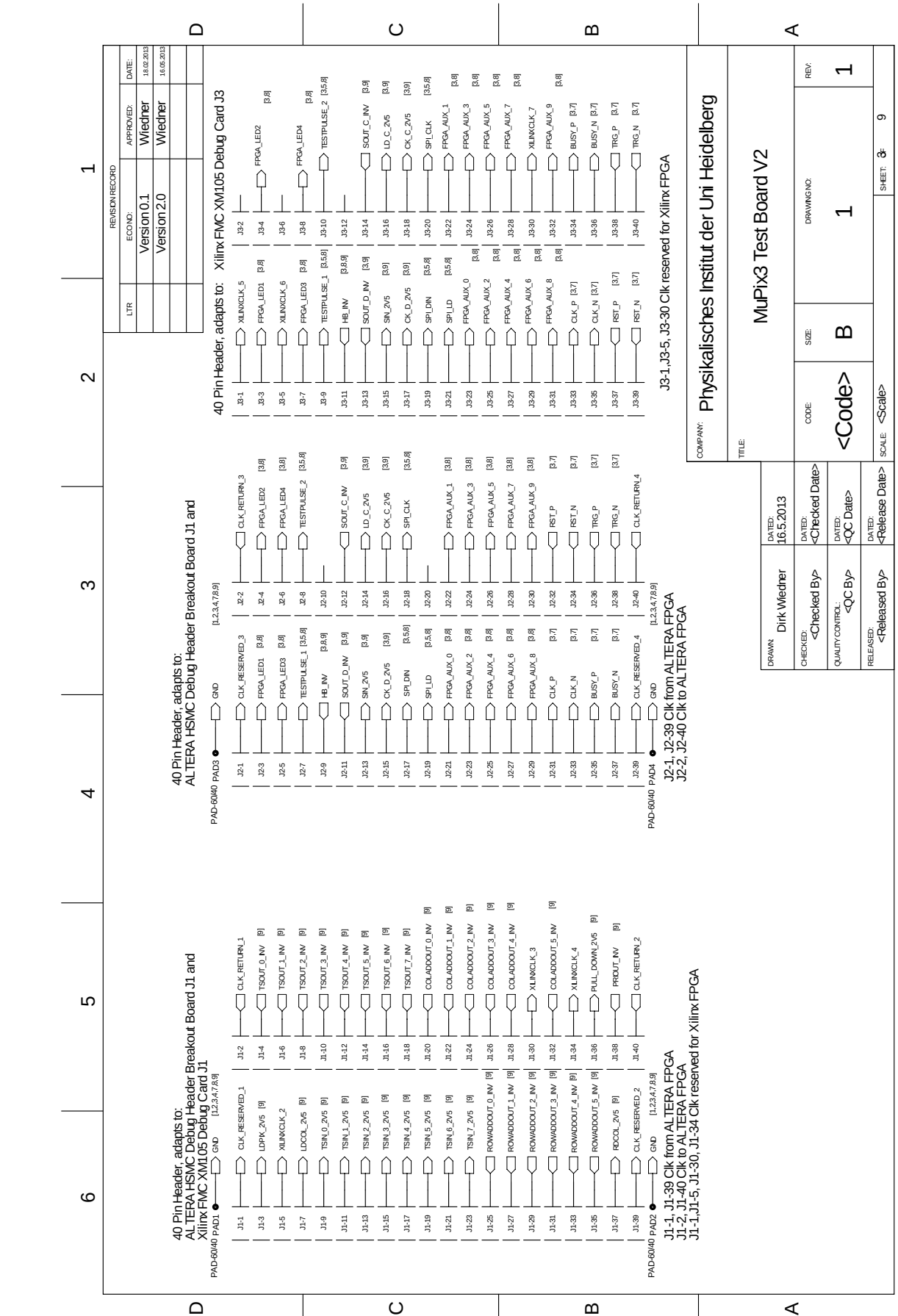
The schematics of the MuPix3 PCB and MuPix4 PCB, designed by Dirk Wiedner, are shown in this chapter. The MuPix3 and MuPix4 chip can both be used with the MuPix3 and the MuPix4 PCB. However, the MuPix4 PCB was only used during the DESY test-beam in February 2014. The MuPix4 PCB is designed to eliminate the digital crosstalk when the Mupix4 chip is used. The first page of the schematics (see figure B.1a and figure B.2a) shows the chip and its connections. The second page shows the connections of the chip socket (see figure B.1b and figure B.2b). The third page shows the pins of the readout and slow control connectors (see figure B.1c and figure B.2c). On the left side the pins of the readout connector are shown, in the middle the pins of the slow control connector corresponding to the Stratix IV GX FPGA Development Kit from Altera® are shown and on the right side the pins of the slow control connector corresponding to a Xilinx® FPGA board, which we do not use, are shown.



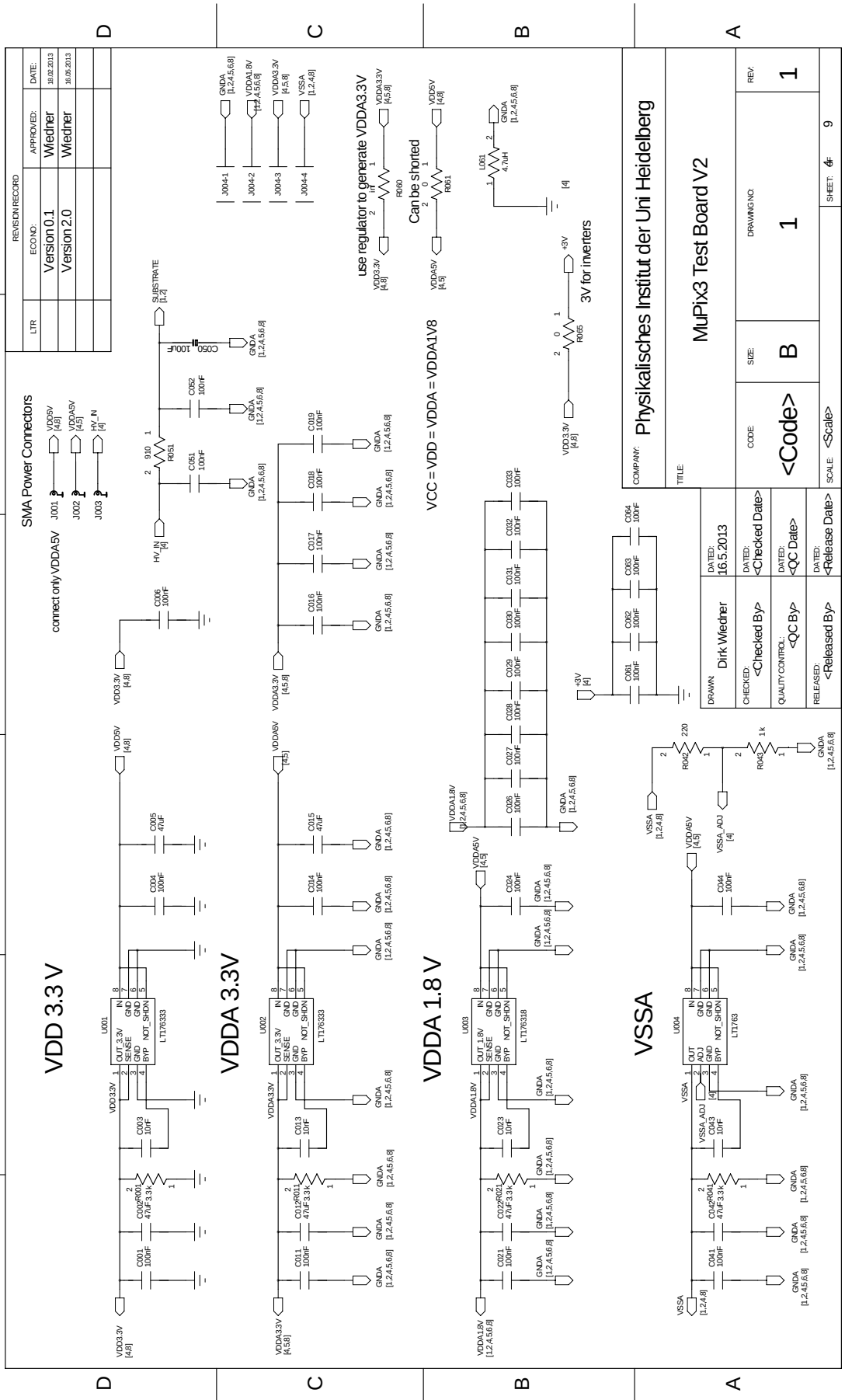
(a) Schematic of the MuPix3 PCB (page 1/9): The connections of the chip are shown.



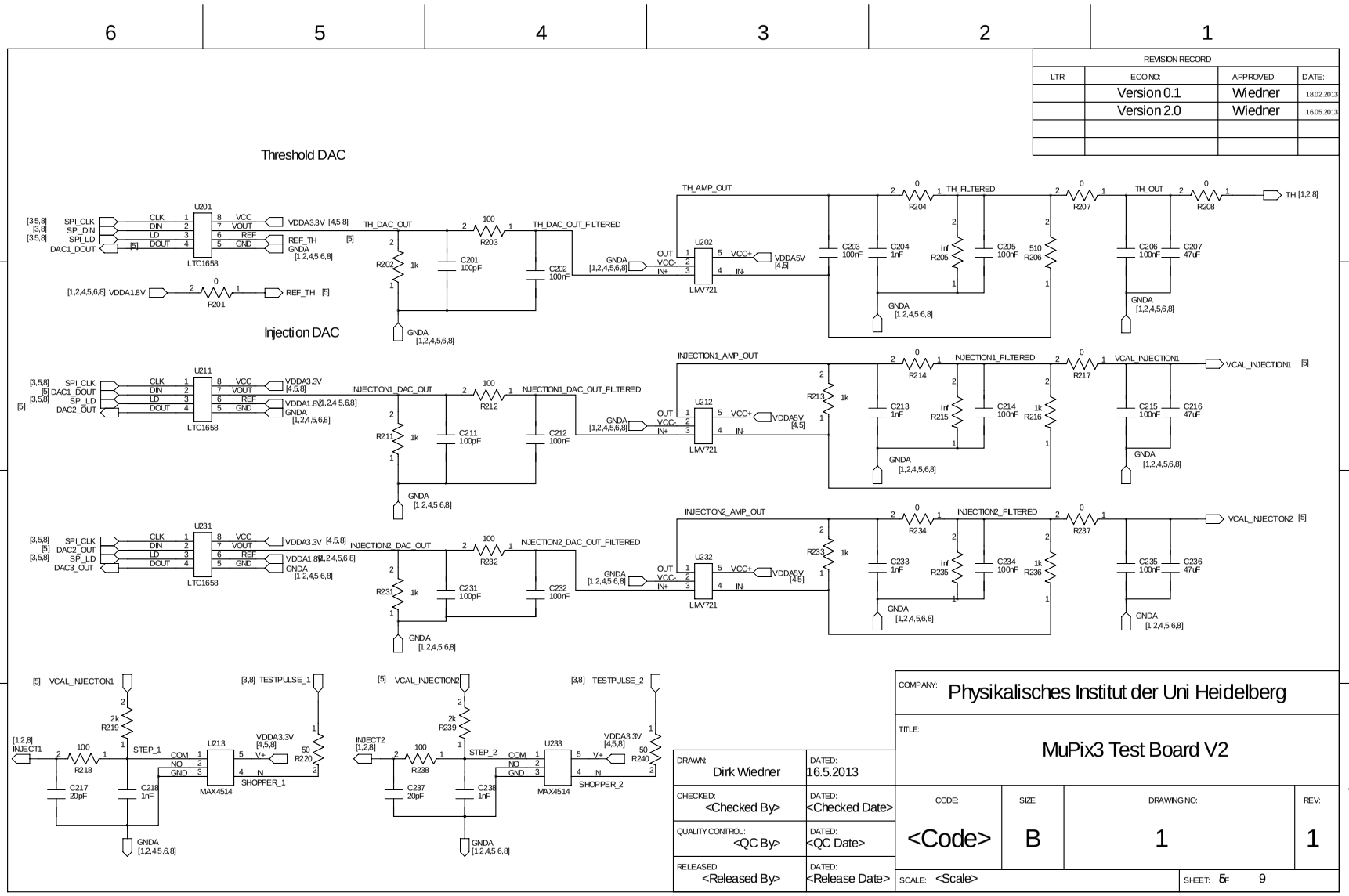
(b) Schematic of the MuPix3 PCB (page 2/9): The connections of the chip socket are shown.



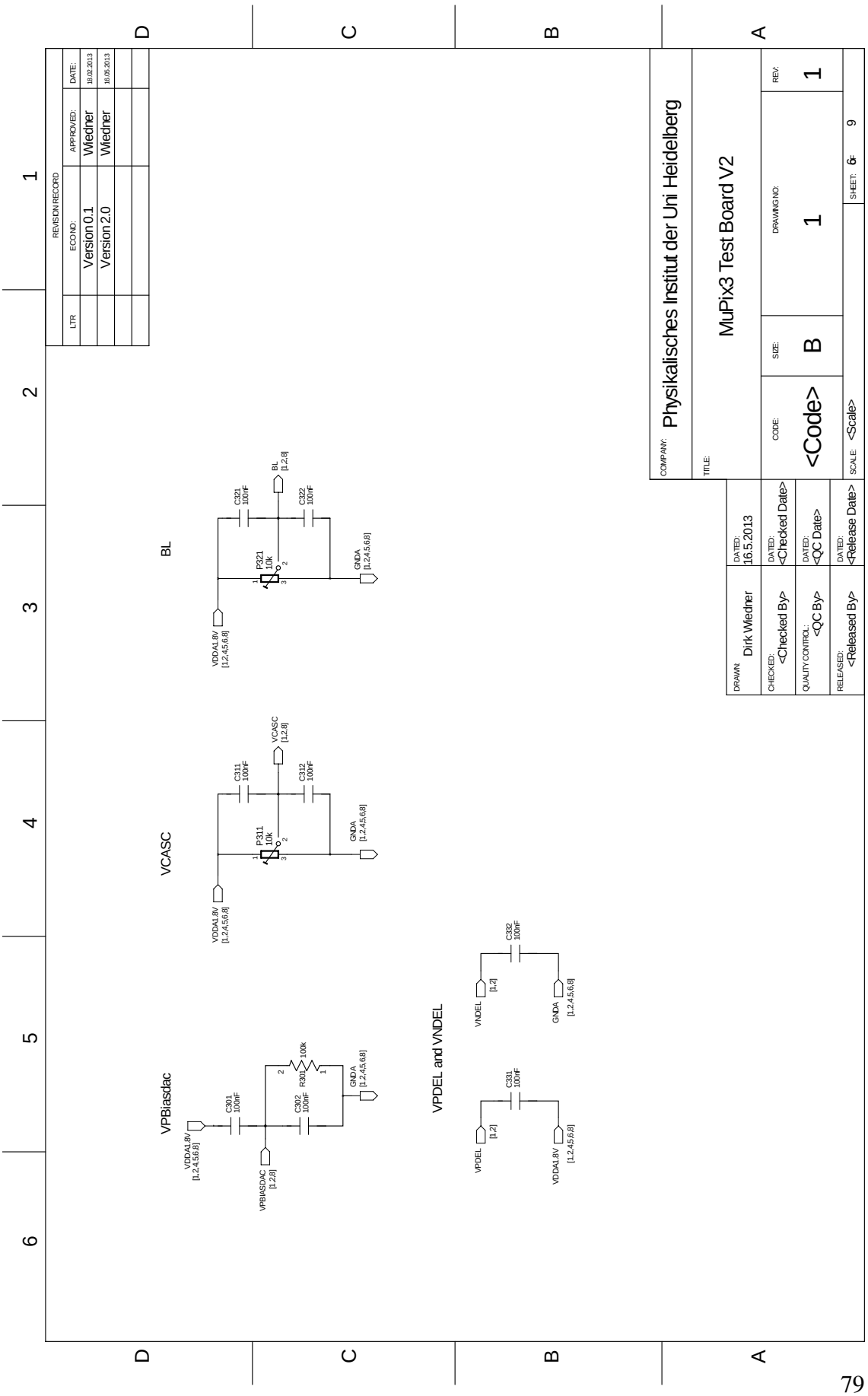
(c) Schematic of the MuPix3 PCB (page 3/9): The pins of the slow control and readout cables are shown.



(d) Schematic of the MuPix3 PCB (page 4/9).



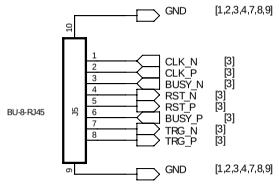
(e) Schematic of the MuPix3 PCB (page 5/9).



(f) Schematic of the MuPix3 PCB (page 6/9).

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
	Version 0.1	Wiedner	18.02.2013
	Version 2.0	Wiedner	16.05.2013

RJ45 connector to Eudet Trigger Logic Unit



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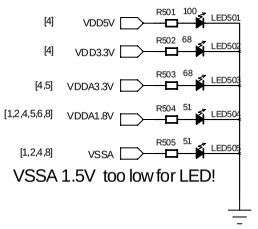
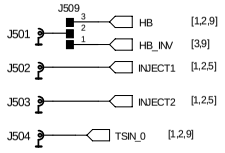
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 7 OF 9	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
	Version 0.1	Wiedner	18.02.2013
	Version 2.0	Wiedner	16.05.2013

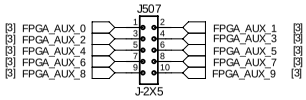
Power LEDs



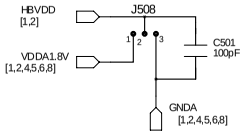
LEMO Testpoints



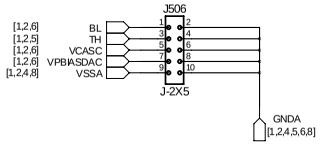
Paralell FPGA auxilliary bus

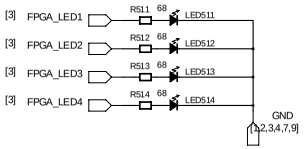


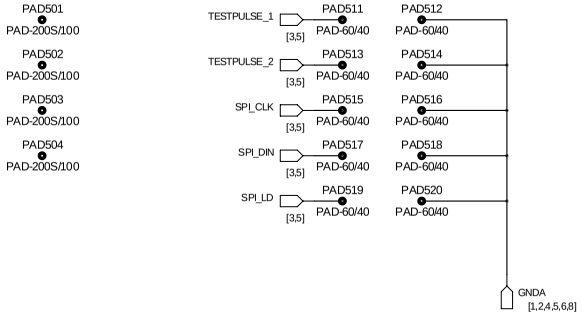
HBVDD



analoge testpoints







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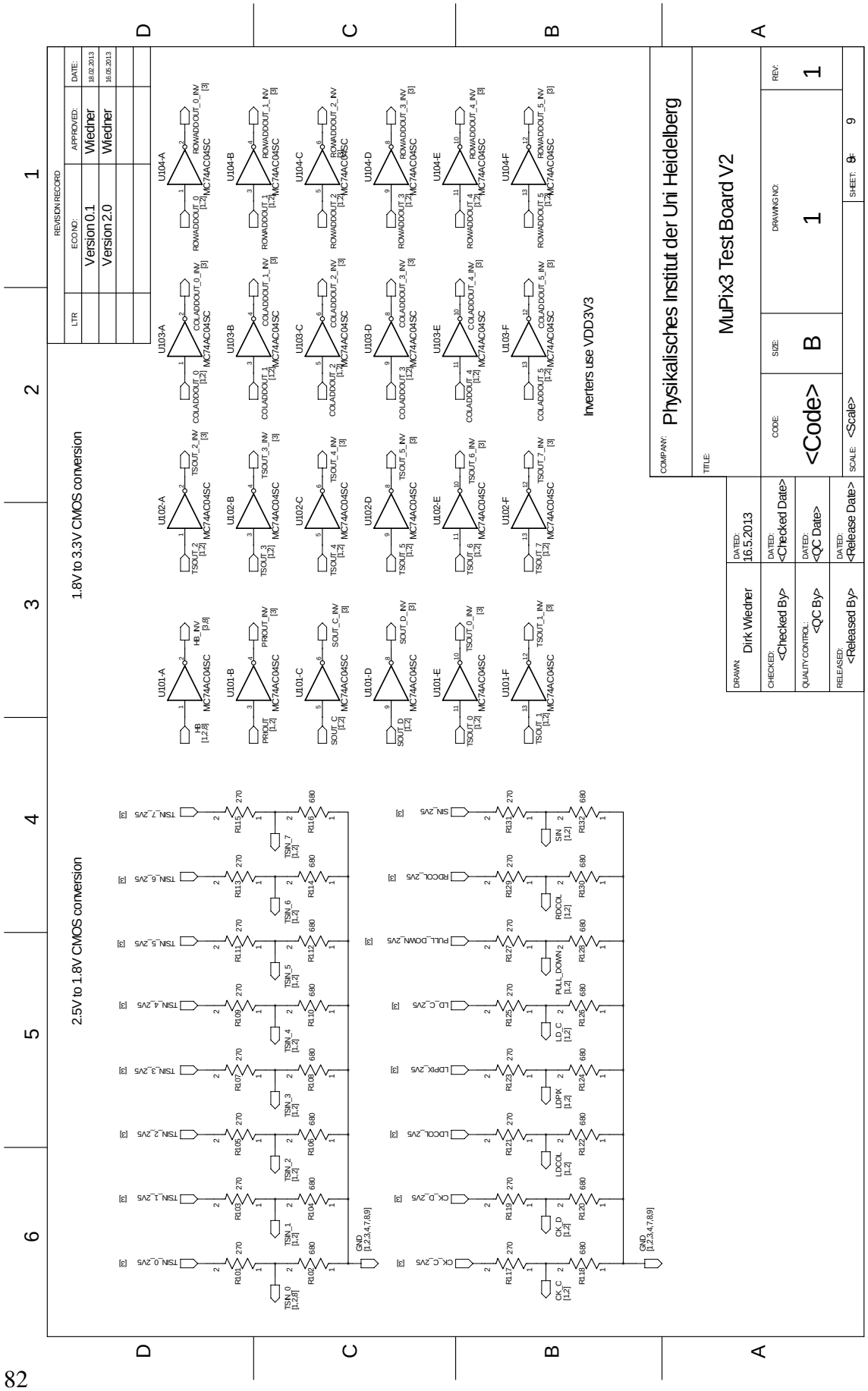
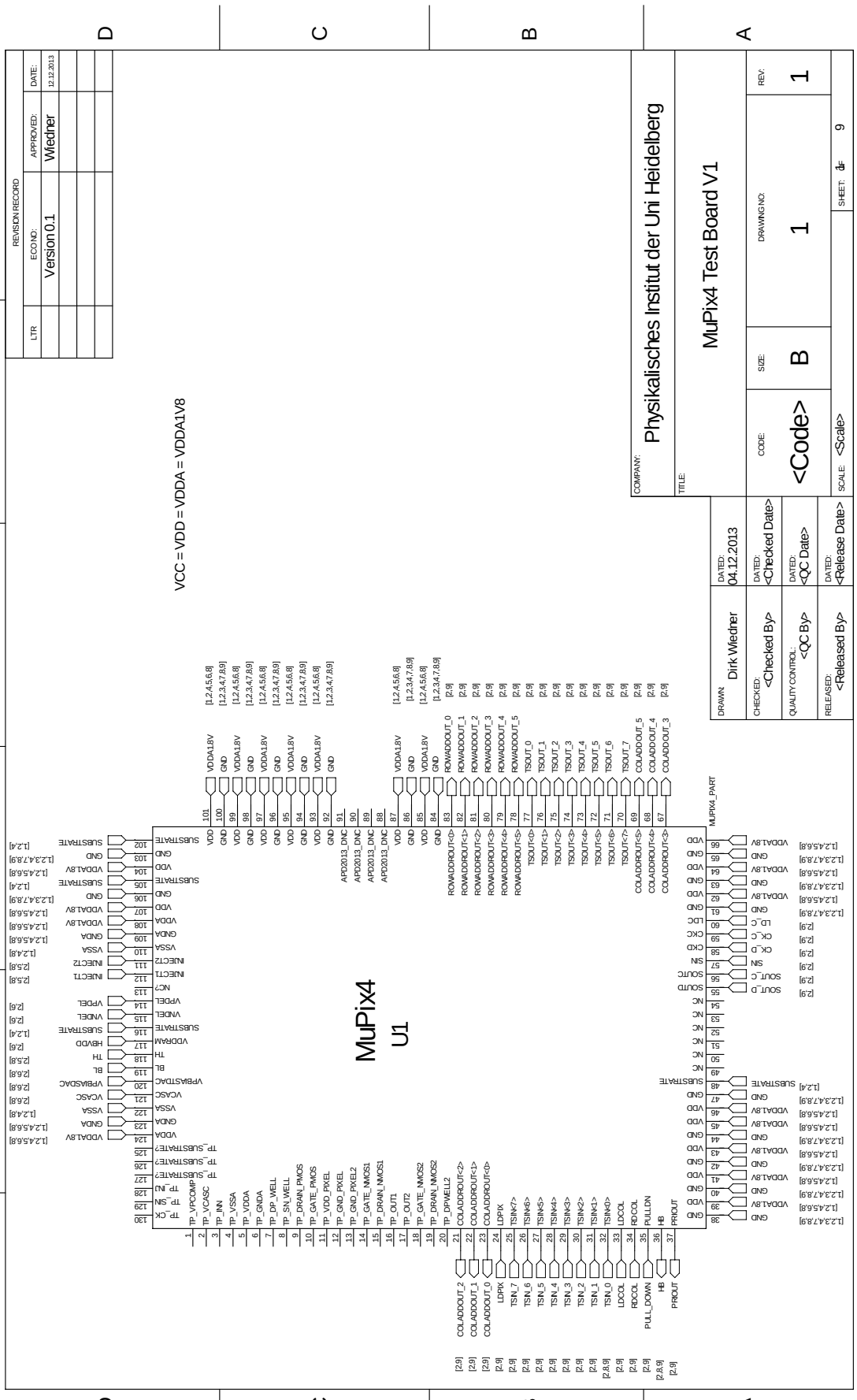
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 8 of 9	

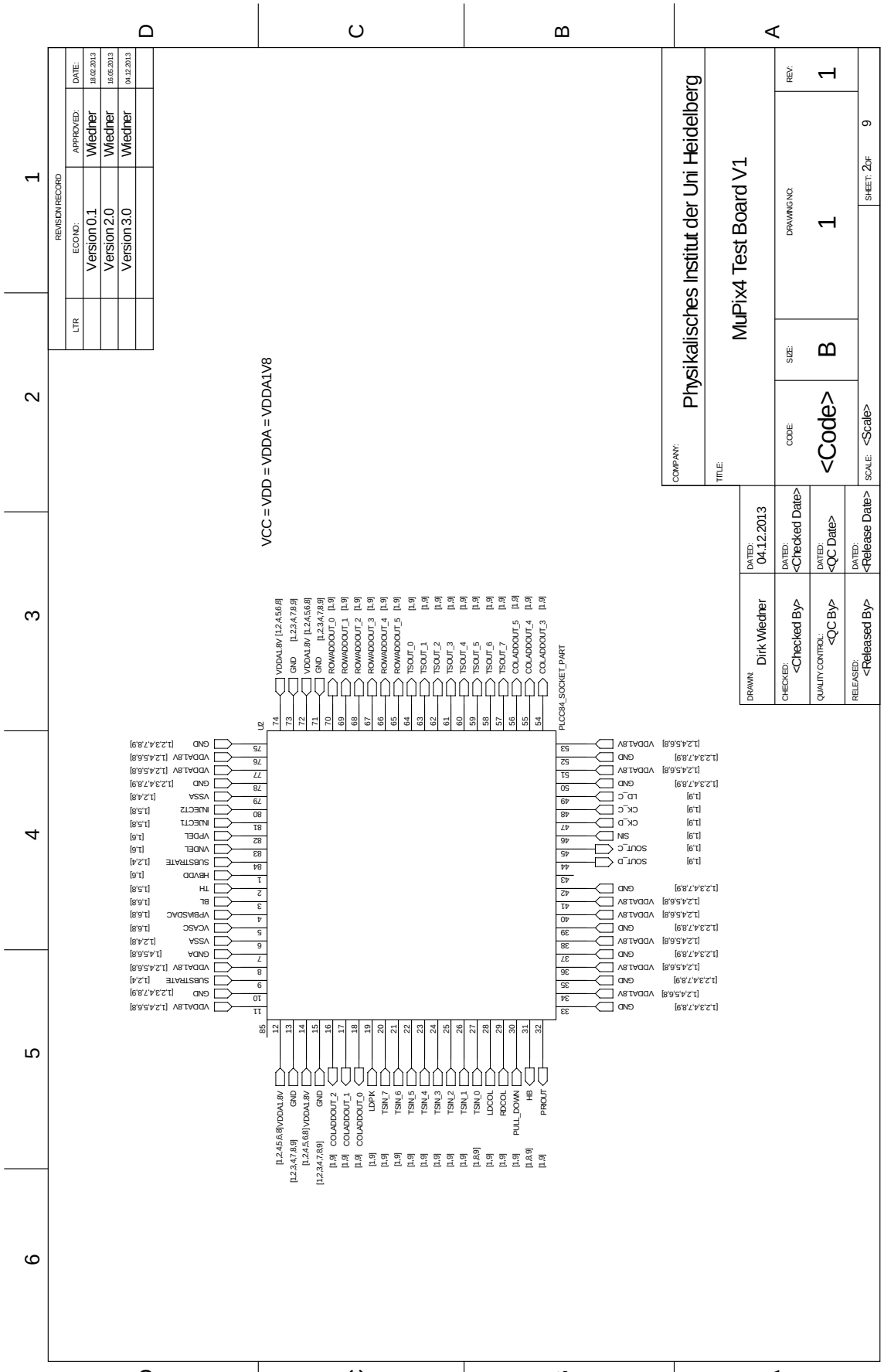


(i) Schematic of the MuPix3 PCB (page 9/9).

Figure B.1: Schematic of the MuPix3 PCB.



(a) Schematic of the MuPix4 PCB (page 1/9): The connections of the chip are shown.



(b) Schematic of the MuPix4 PCB (page 2/9): The connections of the chip socket are shown.

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
	Version 0.1	Wiedner	18.02.2013
	Version 2.0	Wiedner	16.05.2013
	Version 3.0	Wiedner	04.12.2013

40 Pin Header, adapts to:
ALTERA HSMC Debug Header Breakout Board J1 and
Xilinx FMC XM105 Debug Card J1

PAD-60/40	PAD1	GND	[1,2,3,4,7,8,9]
J1-1	CLK_RESERVED_1	J1-2	CLK_RETURN_1
J1-3	LDPK_2V5 [9]	J1-4	TSOUT_0_INV [9]
J1-5	XILINXCLK_2	J1-6	TSOUT_1_INV [9]
J1-7	LDCOL_2V5 [9]	J1-8	TSOUT_2_INV [9]
J1-9	TSIN_0_2V5 [9]	J1-10	TSOUT_3_INV [9]
J1-11	TSIN_1_2V5 [9]	J1-12	TSOUT_4_INV [9]
J1-13	TSIN_2_2V5 [9]	J1-14	TSOUT_5_INV [9]
J1-15	TSIN_3_2V5 [9]	J1-16	TSOUT_6_INV [9]
J1-17	TSIN_4_2V5 [9]	J1-18	TSOUT_7_INV [9]
J1-19	TSIN_5_2V5 [9]	J1-20	COLADDOUT_0_INV [9]
J1-21	TSIN_6_2V5 [9]	J1-22	COLADDOUT_1_INV [9]
J1-23	TSIN_7_2V5 [9]	J1-24	COLADDOUT_2_INV [9]
J1-25	ROWADDOUT_0_INV [9]	J1-26	COLADDOUT_3_INV [9]
J1-27	ROWADDOUT_1_INV [9]	J1-28	COLADDOUT_4_INV [9]
J1-29	ROWADDOUT_2_INV [9]	J1-30	XILINXCLK_3
J1-31	ROWADDOUT_3_INV [9]	J1-32	COLADDOUT_5_INV [9]
J1-33	ROWADDOUT_4_INV [9]	J1-34	XILINXCLK_4
J1-35	ROWADDOUT_5_INV [9]	J1-36	PULL_DOWN_2V5 [9]
J1-37	RDCOL_2V5 [9]	J1-38	PRDUT_INV [9]
J1-39	CLK_RESERVED_2	J1-40	CLK_RETURN_2
PAD-60/40	PAD2	GND	[1,2,3,4,7,8,9]

J1-1, J1-39 Clk from ALTERA FPGA
J1-2, J1-40 Clk to ALTERA FPGA
J1-1,J1-5, J1-30, J1-34 Clk reserved for Xilinx FPGA

40 Pin Header, adapts to:
ALTERA HSMC Debug Header Breakout Board J1 and

PAD-60/40	PAD3	GND	[1,2,3,4,7,8,9]
J2-1	CLK_RESERVED_3	J2-2	CLK_RETURN_3
J2-3	FPGA_LED1 [3,8]	J2-4	FPGA_LED2 [3,8]
J2-5	FPGA_LED3 [3,8]	J2-6	FPGA_LED4 [3,8]
J2-7	TESTPULSE_1 [3,5,8]	J2-8	TESTPULSE_2 [3,5,8]
J2-9	HB_INV [3,8,9]	J2-10	
J2-11	SOUT_D_INV [3,9]	J2-12	SOUT_C_INV [3,9]
J2-13	SIN_2V5 [3,9]	J2-14	LD_C_2V5 [3,9]
J2-15	CK_D_2V5 [3,9]	J2-16	CK_C_2V5 [3,9]
J2-17	SPI_DIN [3,5,8]	J2-18	SPI_CLK [3,5,8]
J2-19	SPI_LD [3,5,8]	J2-20	
J2-21	FPGA_AUX_0 [3,8]	J2-22	FPGA_AUX_1 [3,8]
J2-23	FPGA_AUX_2 [3,8]	J2-24	FPGA_AUX_3 [3,8]
J2-25	FPGA_AUX_4 [3,8]	J2-26	FPGA_AUX_5 [3,8]
J2-27	FPGA_AUX_6 [3,8]	J2-28	FPGA_AUX_7 [3,8]
J2-29	FPGA_AUX_8 [3,8]	J2-30	FPGA_AUX_9 [3,8]
J2-31	CLK_P [3,7]	J2-32	RST_P [3,7]
J2-33	CLK_N [3,7]	J2-34	RST_N [3,7]
J2-35	BUSY_P [3,7]	J2-36	TRG_P [3,7]
J2-37	BUSY_N [3,7]	J2-38	TRG_N [3,7]
J2-39	CLK_RESERVED_4	J2-40	CLK_RETURN_4
PAD-60/40	PAD4	GND	[1,2,3,4,7,8,9]

J2-1, J2-39 Clk from ALTERA FPGA
J2-2, J2-40 Clk to ALTERA FPGA

40 Pin Header, adapts to: Xilinx FMC XM105 Debug Card J3

J3-1	XILINXCLK_5	J3-2	
J3-3	FPGA_LED1 [3,8]	J3-4	FPGA_LED2 [3,8]
J3-5	XILINXCLK_6	J3-6	
J3-7	FPGA_LED3 [3,8]	J3-8	FPGA_LED4 [3,8]
J3-9	TESTPULSE_1 [3,5,8]	J3-10	TESTPULSE_2 [3,5,8]
J3-11	HB_INV [3,8,9]	J3-12	
J3-13	SOUT_D_INV [3,9]	J3-14	SOUT_C_INV [3,9]
J3-15	SIN_2V5 [3,9]	J3-16	LD_C_2V5 [3,9]
J3-17	CK_D_2V5 [3,9]	J3-18	CK_C_2V5 [3,9]
J3-19	SPI_DIN [3,5,8]	J3-20	SPI_CLK [3,5,8]
J3-21	SPI_LD [3,5,8]	J3-22	FPGA_AUX_1 [3,8]
J3-23	FPGA_AUX_0 [3,8]	J3-24	FPGA_AUX_3 [3,8]
J3-25	FPGA_AUX_2 [3,8]	J3-26	FPGA_AUX_5 [3,8]
J3-27	FPGA_AUX_4 [3,8]	J3-28	FPGA_AUX_7 [3,8]
J3-29	FPGA_AUX_6 [3,8]	J3-30	XILINXCLK_7
J3-31	FPGA_AUX_8 [3,8]	J3-32	FPGA_AUX_9 [3,8]
J3-33	CLK_P [3,7]	J3-34	BUSY_P [3,7]
J3-35	CLK_N [3,7]	J3-36	BUSY_N [3,7]
J3-37	RST_P [3,7]	J3-38	TRG_P [3,7]
J3-39	RST_N [3,7]	J3-40	TRG_N [3,7]

J3-1,J3-5, J3-30 Clk reserved for Xilinx FPGA

DRAWN: Dirk Wiedner	DATED: 04.12.2013
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

COMPANY: Physikalisches Institut der Uni Heidelberg

TITLE: MuPix4 Test Board V1

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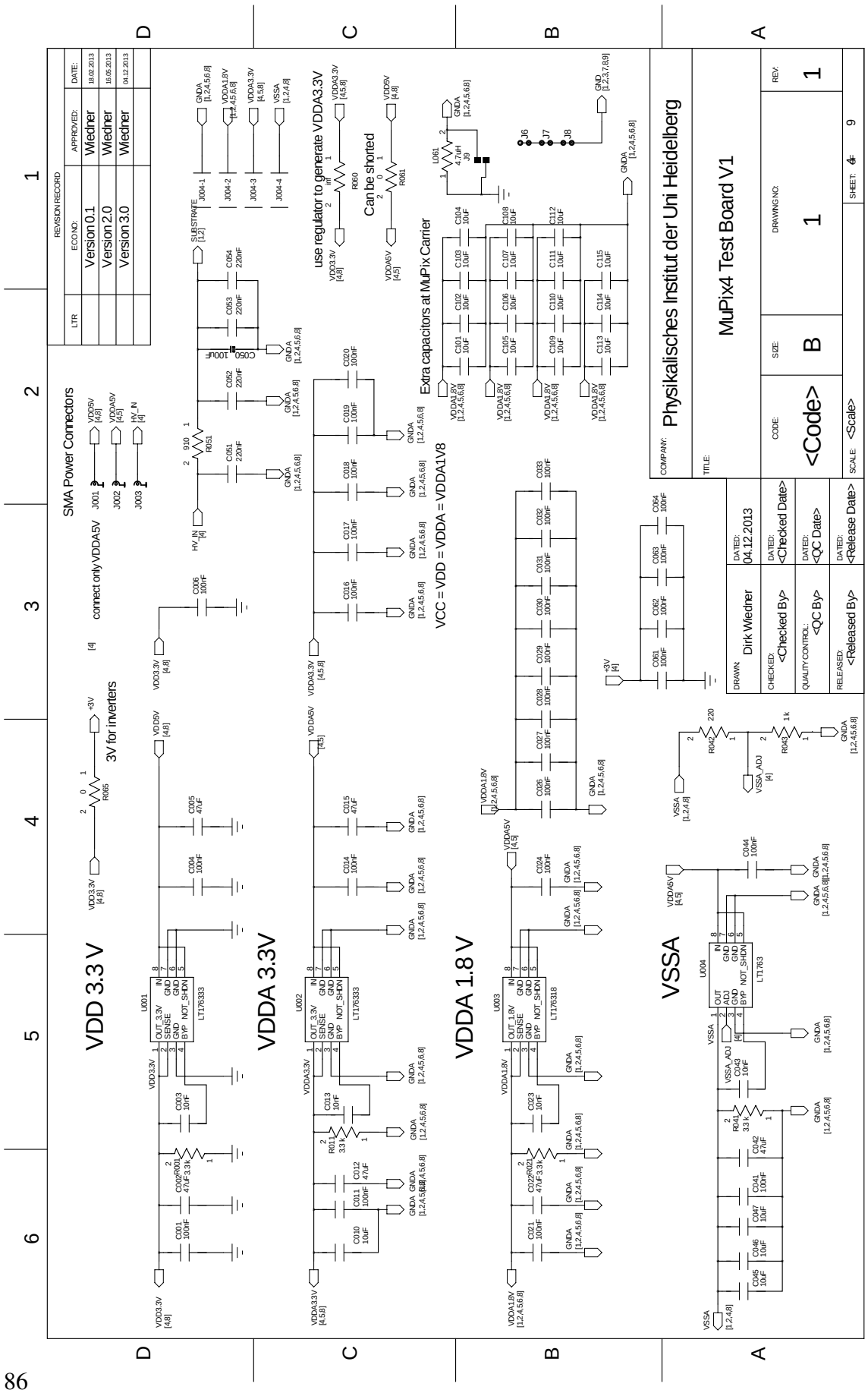
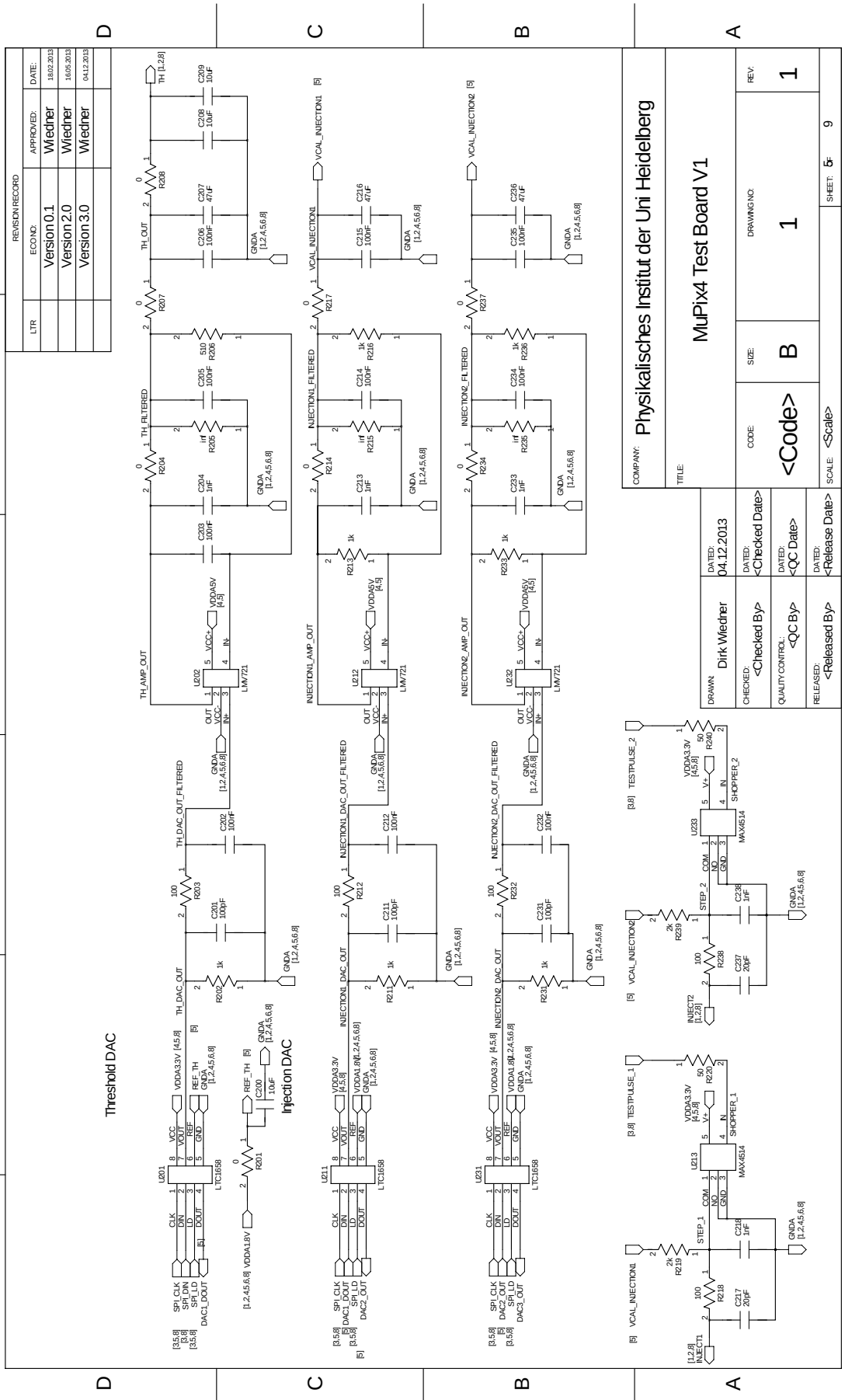


(d) Schematic of the MuPix4 PCB (page 4/9).



(e) Schematic of the MuPix4 PCB (page 5/9).

REVISION RECORD			
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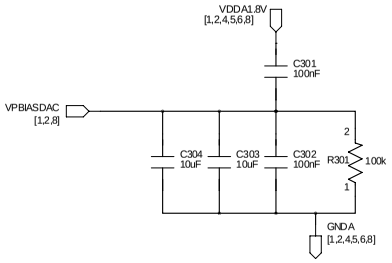
	Version 2.0	Wiedner	16.05.2013
	Version 3.0	Wiedner	04.12.2013

VPBiasdac



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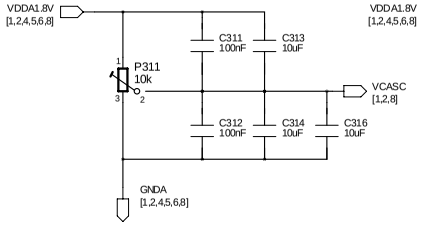

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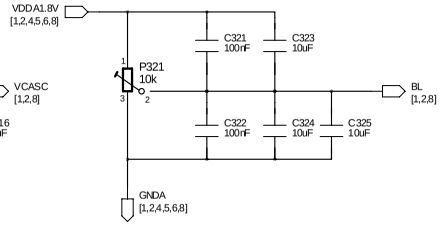
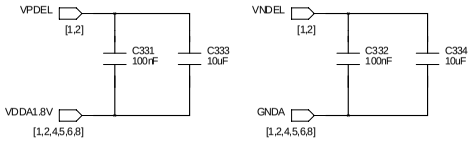


VPDEL and VNDEL



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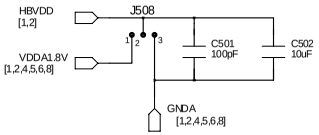

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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 6 OF 9	

(f) Schematic of the MuPix4 PCB (page 6/9).

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
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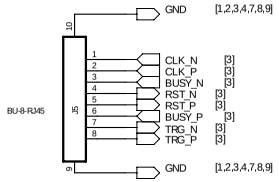
	Version 2.0	Wiedner	16.05.2013
	Version 3.0	Wiedner	04.12.2013

RJ45 connector to Eudet Trigger Logic Unit



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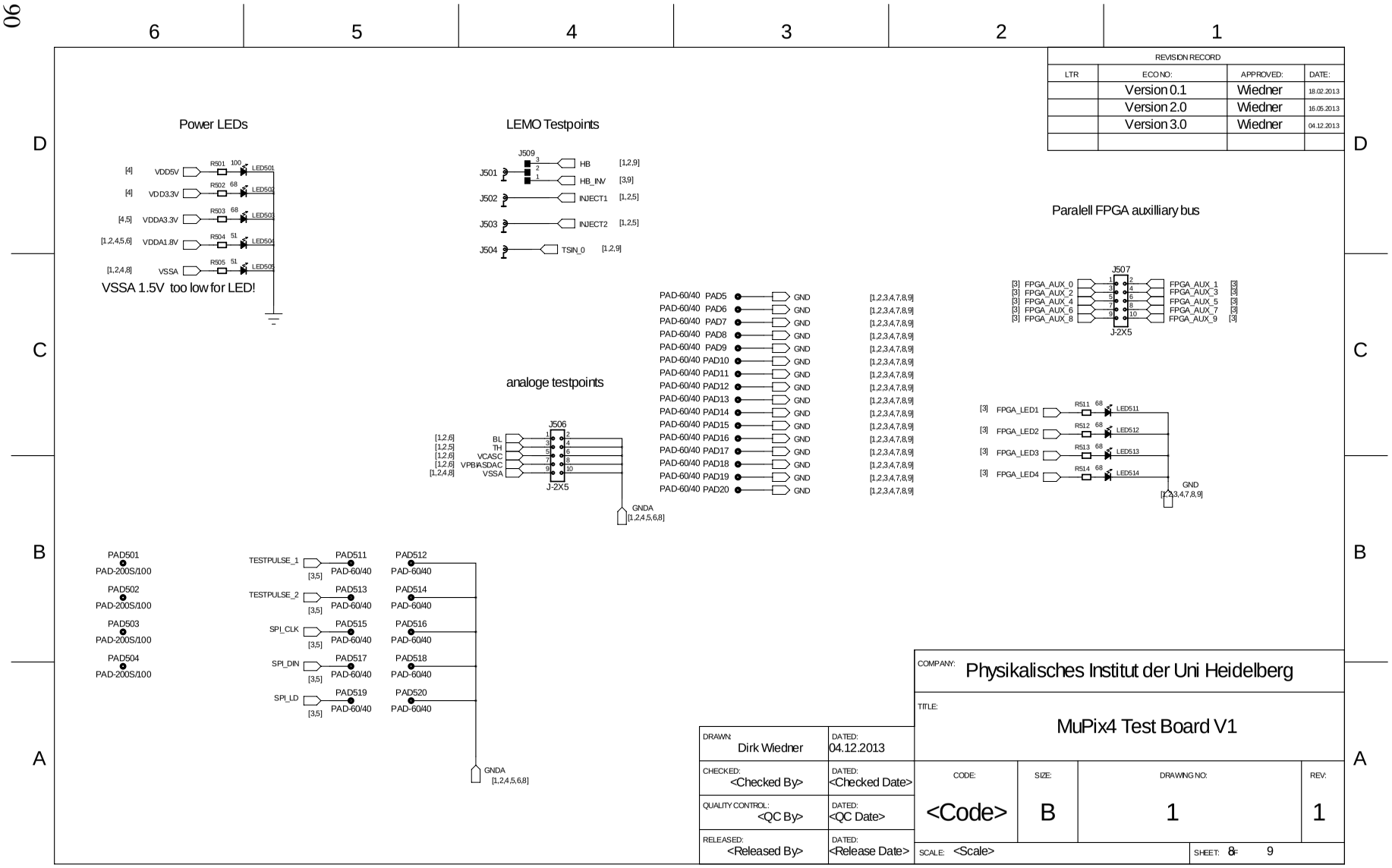
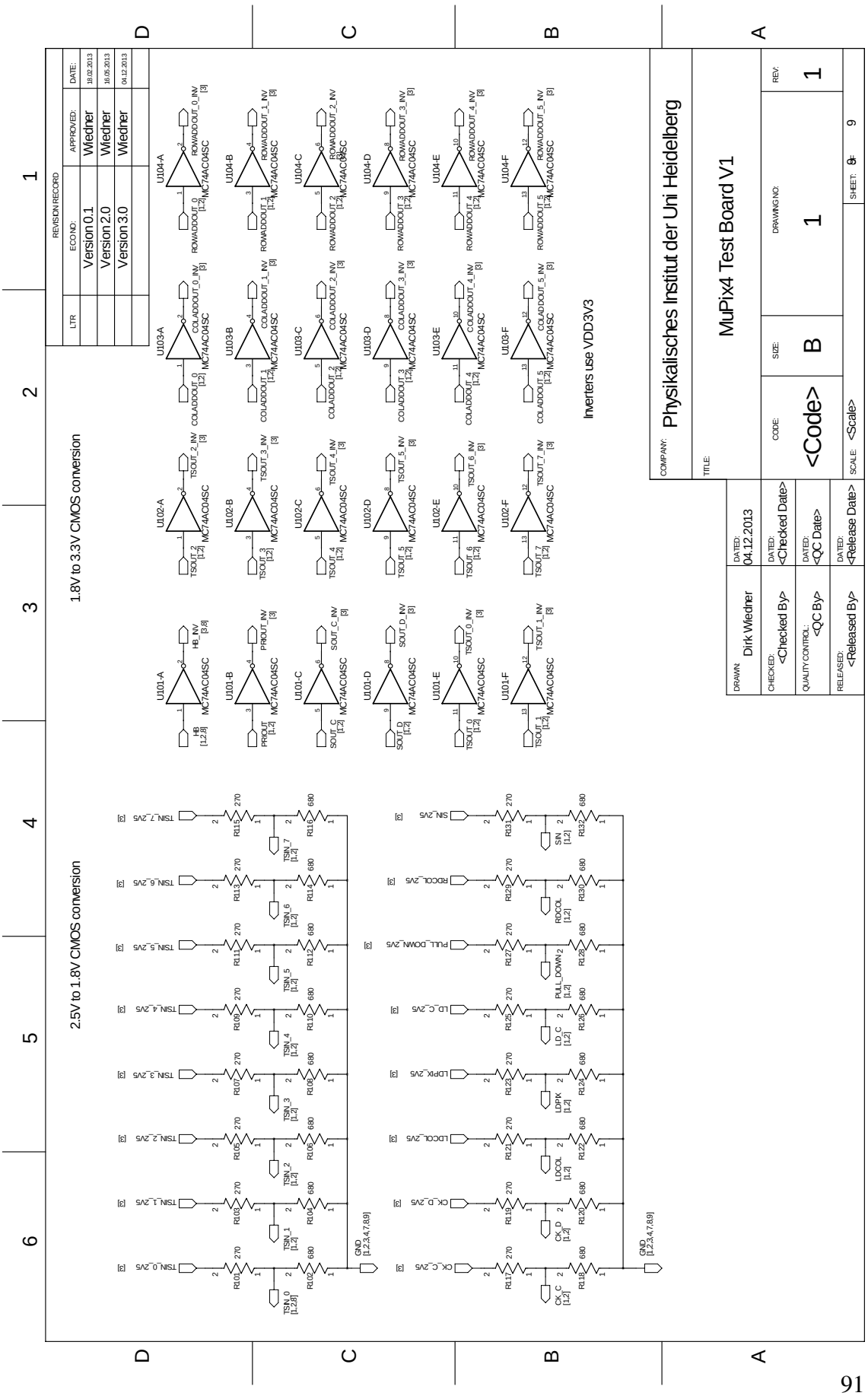
(g) Schematic of the MuPix4 PCB (page 7/9).



(h) Schematic of the MuPix4 PCB (page 8/9).



(i) Schematic of the MuPix4 PCB (page 9/9).

Figure B.2: Schematic of the MuPix4 PCB.

C Bonding Diagrams for the MuPix4 Chip

Figure C.1 shows the bonding diagram to wire bond the MuPix4 chip to a carrier and figure C.2 shows the diagram to wire bond it directly on a MuPix4 PCB. The dashed lines symbolise the additional wires for power and ground to reduce the digital crosstalk. Since the carrier has less bonding pads than the chip, some power and ground pads of the chip have to be wire bonded to the same carrier pad. The bonding diagrams for both the MuPix3 and MuPix4 chip can also be obtained from the schematics of the MuPix3 and MuPix4 PCBs (see appendix B).

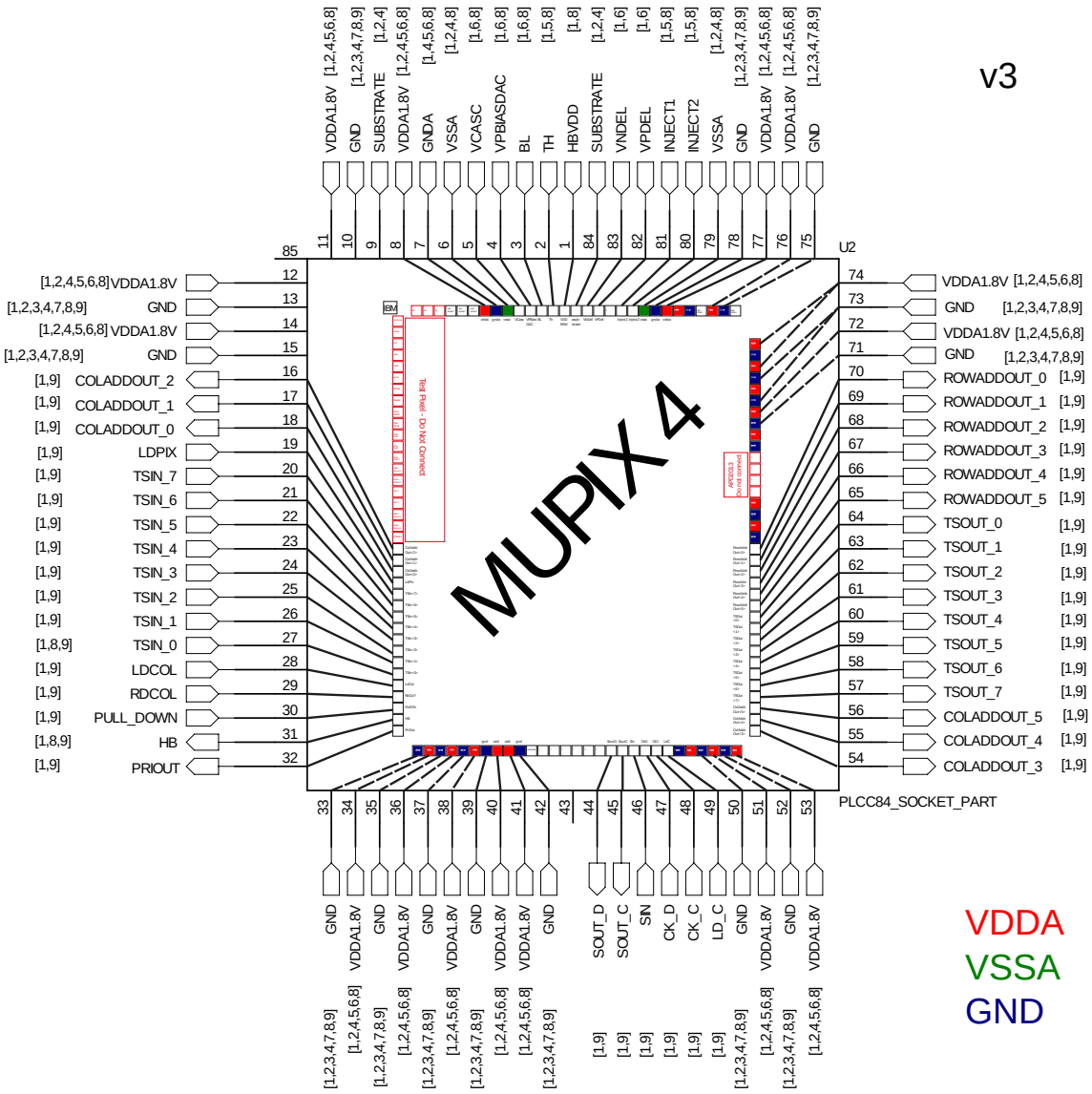


Figure C.1: Bonding diagram for the MuPix4 chip (bonding on a carrier), extra power and ground wires are dashed.

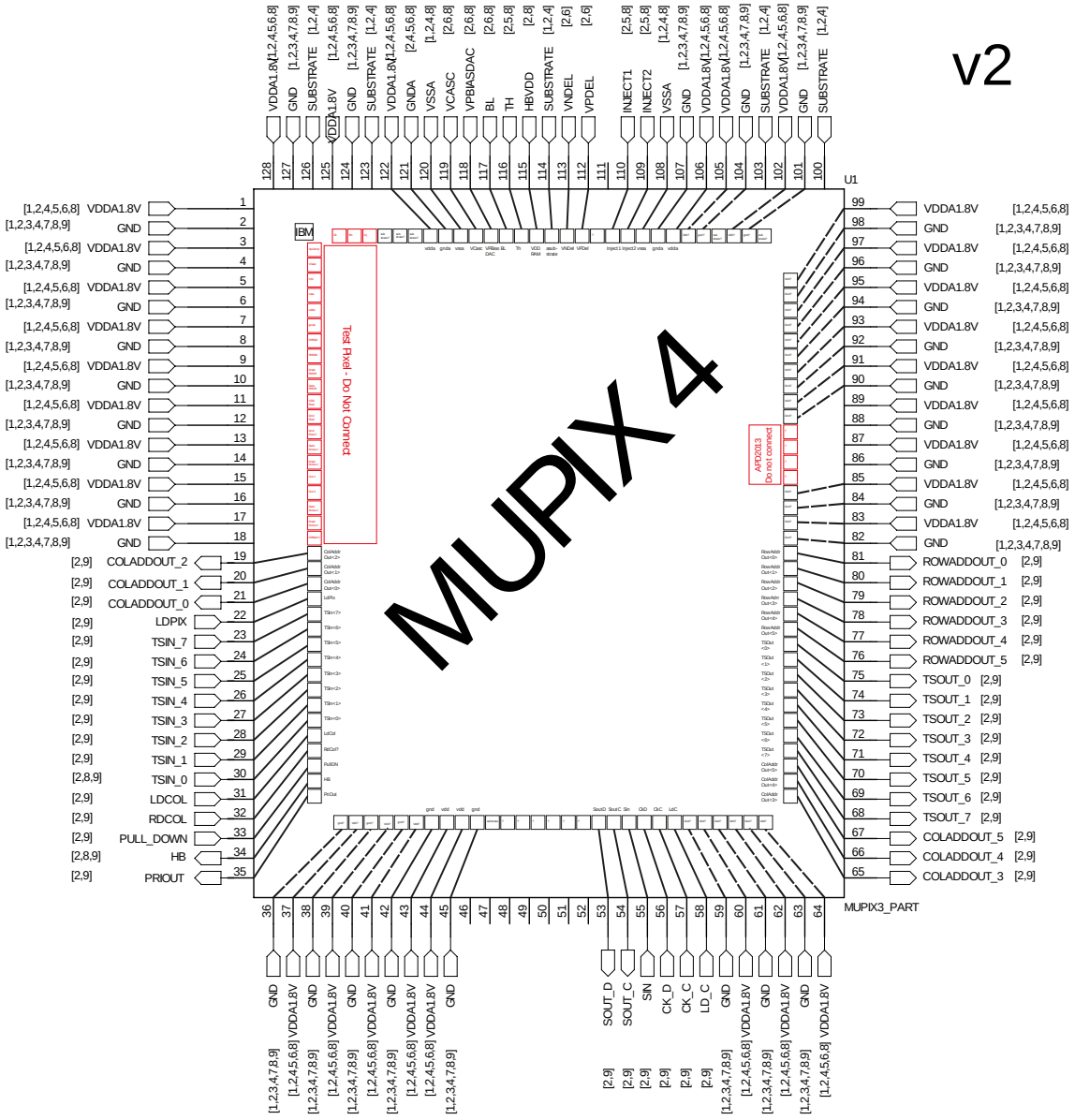


Figure C.2: Bonding diagram for the MuPix4 chip (bonding directly on a PCB), extra power and ground wires are dashed.

D Graphical User Interface of the Configuration and Data Readout Software

The configuration and the data readout of the MuPix3 and MuPix4 chip is controlled by a programm written in C++. A screenshot of the graphical user interface can be seen in figure D.1. It is divided into several boxes:

Board DACs The value of the threshold and of the two injections can be set.

Chip DACs The values of the internal chip voltages can be set.

Pixel Configuration Only the button "Write Pixel Values" is used for the MuPix4 chip. This sets the pixel which should be read out in the ToT mode. The pixel has to selected by clicking in the hit map before.

Pixel Navigation With the buttons "up", "down", "left" and "right" the pixel that should be read out in the ToT mode is changed.

Injections The length of the two injection signals can be set and the signals can be injected to the chip by clicking the buttons.

Pulse Shape By clicking the button an automatic pulse shape measurement is done.

Readout The readout of the hit-flag mode can be started by clicking the "Start Readout" button.

S curve Automatic S-curve measurements, where the threshold is changed in small steps, can be started here by clicking the "Measure S-curve" button. It can be chosen

which injection should be used by clicking the two check boxes “Injection1” and / or “Injection2”. The numbers that are inserted into the “HV” or “Temp” text box will be in the name of the saved file.
If “all” is selected, a S-curve measurement in the hit-flag mode will start, in which the number of hits which registered a hit are counted.
If “single” is selected, a measurement in the hit-flag mode will start, in which 100 injection signals are generated and for every pixel the registered hits are counted.
If “one single” is selected, the same measurement will be done but only for one previous selected pixel. If “noise (ToT)” is selected, a S-curve measurement in the ToT mode for a previous selected pixel will start, in which no injection signals are generated and the S-curve of the baseline is measured.
If “one single (ToT)” is selected, a measurement in the ToT mode for a previously selected pixel will start, in which 100 injection signals are generated and for the selected pixel the registered hits are counted.
If “one single (ToT, Inj)” is selected, a S-curve measurement in the ToT mode will start similar to the previous one, but the threshold will be kept constant and the hight of the injection signals will change in small steps. This option does not work yet.

Drawmode It can be chosen if no readout event should be drawn or every, every 10^{th} or every 1000^{th} event.

Eudaq Settings required while measuring with the EUDET telescope at DESY can be set here.

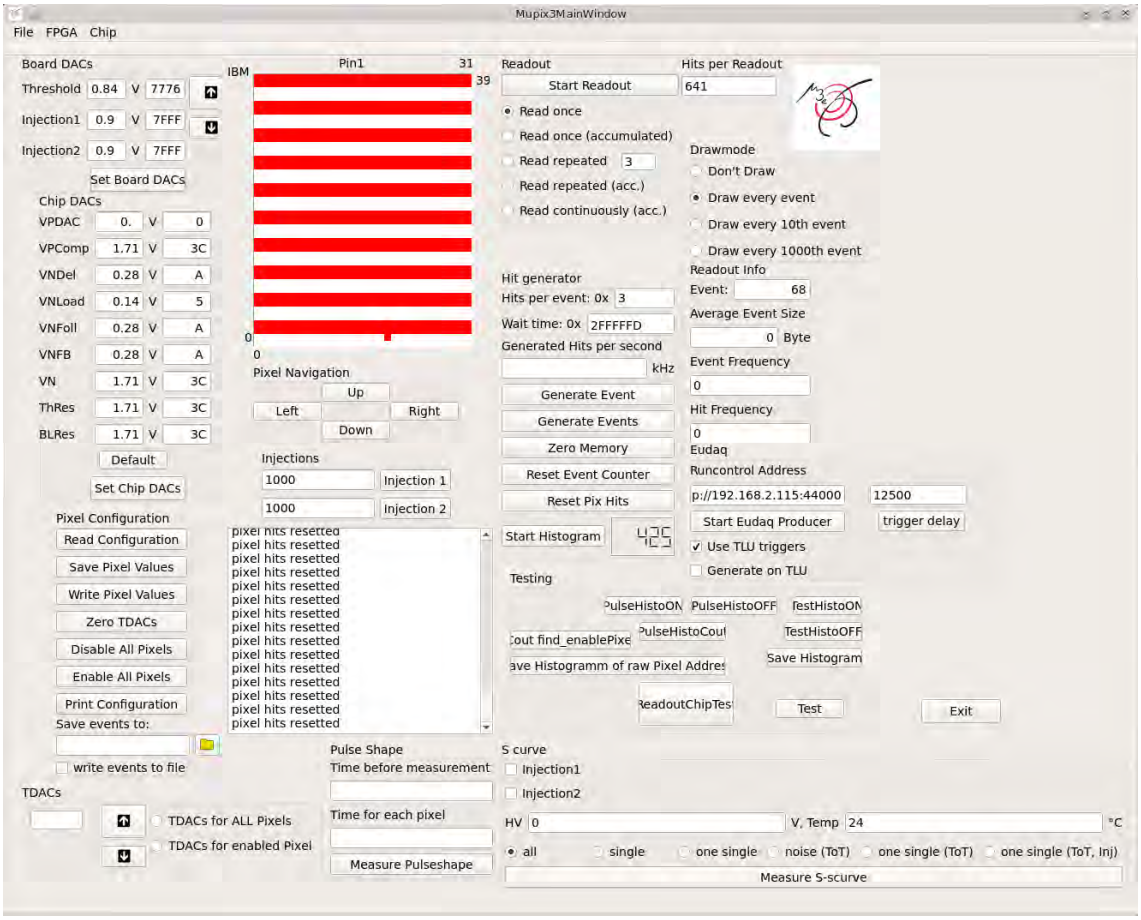


Figure D.1: Screenshot of the graphical user interface of the configuration and readout software of the MuPix4.

E Mechanical Adapter for the Rotation Stage at the Telescope at DESY

A mechanical adapter for the rotation stage at the DESY telescope at the testbeam area T22 to mount the MuPix2 PCB was made (see figure E.2). The small board is needed so that the big board can rotate without getting stuck at the rotation stage (figure E.1). Hence, the big one is mounted on top of the small one as seen in figure 8.2. The big board has holes for immersed screws so that the MuPix PCBs do not touch the screws. The adapter is designed such that the chip is on top of the rotation axis of the rotation stage. There are holes for M5 and M4 screws in the upright part of the big board. The M5 holes are for the MuPix2 PCB and the M4 holes are for the MuPix3 and MuPix4 PCBs.

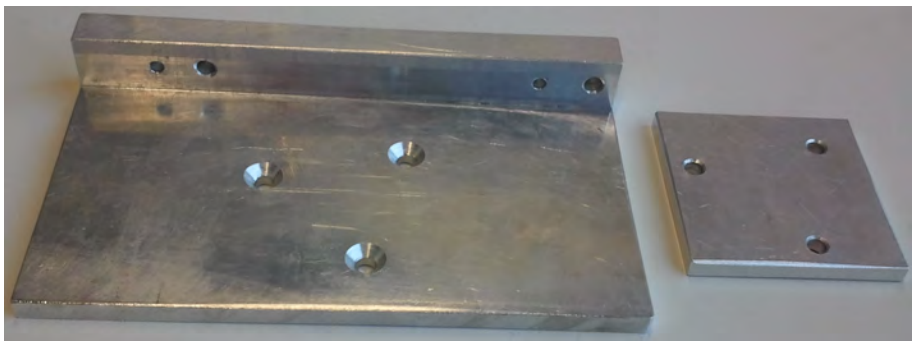
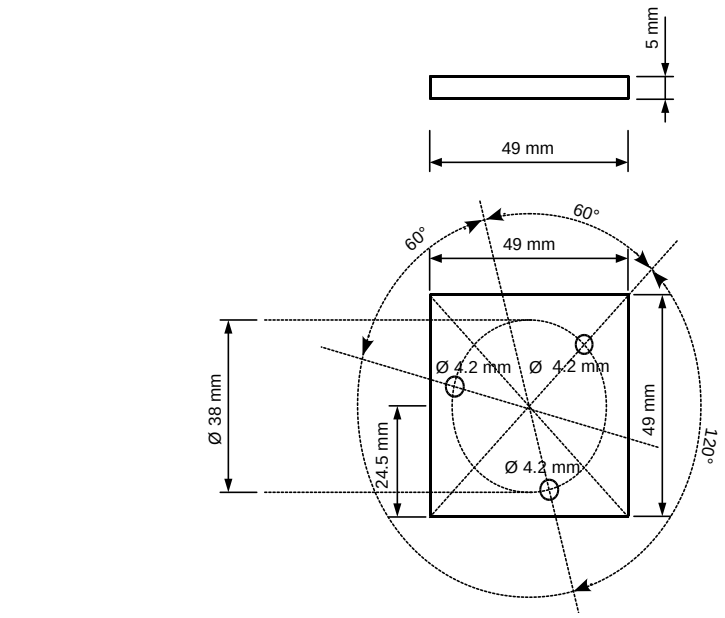
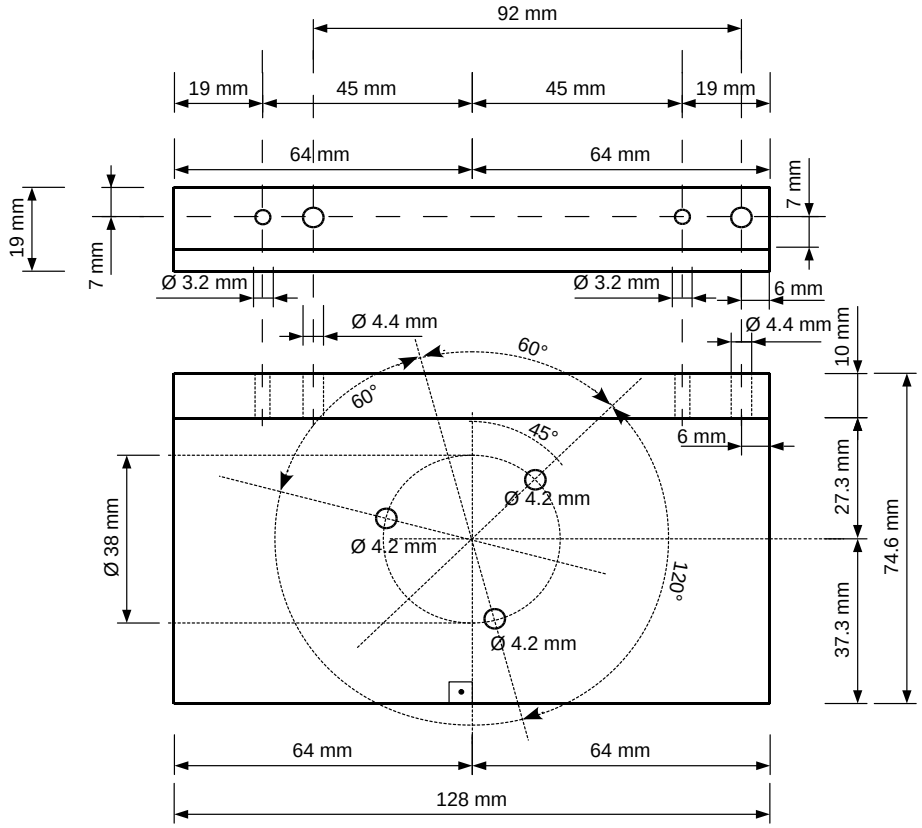


Figure E.1: Picture of the mechanical adapter to mount the MuPix PCBs on the rotation stage at the testbeam area T22 at DESY.



(a) lower part of the adapter



(b) upper part of the adapter

Figure E.2: Drawing of the mechanical adapter for the MuPix2, MuPix3 and MuPix4 PCBs for the telescope stage at DESY.

F Lists

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G Bibliography

[A+01] Q. R. Ahmad et al. Measurement of the charged current interactions produced by B-8 solar neutrinos at the Sudbury Neutrino Observatory. *Phys. Rev. Lett.*, 87:071301, 2001.

[A+13] J. Adam et al. New Constraint on the Existence of the $\mu^+ \to e^+\gamma$ Decay. *Phys. Rev. Lett.*, 110:201801, 2013.

[Aug12] Heiko Christian Augustin. Charakterisierung von HV-MAPS. Bachelor's Thesis, University of Heidelberg, 2012.

[B+88] U. Bellgardt et al. Search for the Decay $\mu^+ \to e^+e^+e^-$. *Nucl. Phys.*, B299:1, 1988.

[B+07] Ties Behnke et al. Test Beams at DESY. `http://www.eudet.org/e26/e28/e182/e283/eudet-memo-2007-11.pdf`, June 2007. EUDET-Memo-2007-11.

[B+12a] J. Beringer et al. (Particle Data Group). Review of Particle Physics. *Phys. Rev.*, D86:010001, 2012.

[B+12b] A. Blondel et al. Research Proposal for an Experiment to Search for the Decay $\mu \to eee$. December 2012.

[BCC+13] A.M. Baldini, F. Cei, C. Cerri, S. Dussoni, L. Galli, et al. MEG Upgrade Proposal. *ArXiv e-prints*, January 2013.

[CN05] We-Fu Chang and John N. Ng. Lepton flavor violation in extra dimension models. *Phys. Rev.*, D71:053003, 2005.

[DES14] `http://testbeam.desy.de/e130573/e130913/testbeamlayout.pdf`, March 2014.

[dG09] A. de Gouvêa. (Charged) Lepton Flavor Violation. *Nucl. Phys B. (Proc. Suppl.)*, 188:303–308, 2009.

[DK09] Rashid M. Djilkibaev and Rostislav V. Konoplich. Rare Muon Decay $\mu^+ \to e^+e^-e^+\nu_e\overline{\nu}_\mu$. *Phys. Rev.*, D79:073004, 2009.

[E+03] K. Eguchi et al. First results from KamLAND: Evidence for reactor anti-neutrino disappearance. *Phys. Rev. Lett.*, 90:021802, 2003.

[F+98] Y. Fukada et al. Evidence for oscillation of atmospheric neutrinos. *Phys. Rev. Lett.*, 81:1562–1567, 1998.

[Fö14] Fabian Förster. Chip Readout and Direct Memory Access for the Mu3e Experiment. Master's thesis, University of Heidelberg, 2014. thesis in work.

[Gri11] David J. Griffiths. *Introduction to Elementary Particles*. Wiley-VCH, second, rev. edition, 2011.

[Hig12] Higgs booklet: First observations of a new particle in the search for the Standard Model Higgs boson at the LHC, 2012.

[Hut14] Lennart Huth. MuPix – Low Momentum Particle Telescope. Master's thesis, University of Heidelberg, 2014. thesis in work.

[Kie15] Moritz Simon Maria Kiehn. Titel tba. PhD thesis, University of Heidelberg, 2015. thesis in work.

[KvB14] Moritz Kiehn and Dorothea vom Bruch. MuPix4 Testbeam February 2014, Overview and First Results with Ivan's Setup. Mu3e Collaboration Meeting, internal presentation, March 2014.

[Per07] Ivan Perić. A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology. *Nucl. Instrum. Meth.*, A582:876–885, 2007.

[Per12a] Ivan Perić. MuPixel small pixel detector description. 2012.

[Per12b] Ann-Kathrin Perrevoort. Characterisation of High Voltage Monolithic Active Pixel Sensors for the Mu3e Experiment. Master's thesis, University of Heidelberg, 2012.

[piM14] piM1 beam line. `http://aea.web.psi.ch/beam2lines/beam_pim1.html`, March 2014.

[PKF11] I. Perić, C. Kreidl, and P. Fischer. Particle pixel detectors in high-voltage CMOS technology - New achievements. *Nucl. Instr. Meth.*, A 650:158, 2011.

[PSI14] The proton accelerator at the Paul Scherrer Institute: forty years of top-flight research. http://www.psi.ch/media/the-proton-accelerator-forty-years-of-top-flight-research, March 2014.

[PT10] I. Perić and C. Takacs. Large monolithic particle pixel-detector in high-voltage cmos technology. *Nucl. Instrum. Meth.*, A624:504, 2010.

[Rub12] Igor Rubinskiy. High Resolution EUDET telescope (status and development plans). talk, May 2012. 20^{th} RD50 Workshop on Radiation hard semiconductor devices for very high luminosity colliders, Bari, Italy.

[sta14] http://upload.wikimedia.org/wikipedia/commons/0/00/Standard_Model_of_Elementary_Particles.svg, March 2014.

[str14] http://www.buyaltera.com/scripts/partsearch.dll?Detail&name=544-2594-ND, March 2014.

[uxi14] http://www.uxibo.de/uxipedia/index.php/Main_Page, March 2014.

[Zim12] M. Zimmermann. Cooling with Gaseous Helium for the Mu3e Experiment. Bachelor's thesis, University of Heidelberg, 2012.

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Erklärung

Ich versichere, dass ich diese Arbeit selbstständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, den 19.03.2014 . . . . . .