The LHCb Outer Tracker Front End Electronics

A.Berkien, H.Deppe, A.Pellegrino, T.Sluijk, U.Stange, U.Trunk, U.Uwer,
D.Wiedner, A.Zwart

Abstract

This note provides an overview of the front-end electronics used to readout the drift-times of the LHCb Outer Tracker straw tube chambers. The main functional components of the readout are the ASDBLR ASIC for amplification and signal digitization, the OTIS ASIC for the time measurement and for the L0 buffering, and the GOL ASIC to serialize the digital data for the optical data transmission. The L1 buffer board used to receive the data which is sent via the optical link is a common LHCb development and is not described here. This note supersedes an earlier document [1].

1 The LHCb Outer Tracker

The LHCb Outer Tracker (OT) [2] is a straw tube drift-chamber detector and consists of 3 stations with a surface of $6 \times 5 \mathrm{m}^2$. A station has four stereo-layers. Each stereo-layer consists of 2×9 chamber modules with a width of 34 cm and a length of 5 m. The modules are electrically subdivided in an upper and lower section.

Figure 1 shows a schematic xy-view of an OT chamber. To keep the material in the center of the detector acceptance small, mechanical supports as well as read-out and service electronics must be placed at the outer edges of the detector layers.

The detector modules comprise 256 single 2.5 m long straw tubes with a diameter of 5 mm. The tubes are glued to 2 supporting panels from which the gas-tight detector modules are built. The straws of the upper and lower panel section are not connected and form separate readout channels. In this way the high particle rate, expected for the module center, is distributed on upper and lower channels. The module width corresponds to 64 straws (34 cm). In total the OT has about 54000 channels.

1.1 Straw tubes

The used drift-tubes have a diameter of $5\,\mathrm{mm}$, an anode wire of $25\,\mu\mathrm{m}$. As couinting gas we envisage to use Ar/CF4/CO2 or Ar/CO2. Table 1 summarizes the working point and the maximum drift-time for the two counting gases.

Signals for different counting gases		
	$Ar/CO_2/CF_4$	Ar/CO_2
Operating Voltage	1540 V	1500 V
Max. Drift-time	37 ns	44 ns
Signal rise time	< 4 ns	
Charge deposition by MIP	220 fC	

Table 1: Operating voltage and signal properties for two counting gas options (gas gain ~ 40000).

The straw (cathode) is a laminate of 3 different materials. Kapton XC-160 (25% of volume carbon doped Kapton) with a surface condcutivity of $200\,\Omega/\square$ (equivalent to a resistivity of $60\,\mathrm{k\Omega/m}$) is used as inner cathode material. To improve the signal transmission of the fast signal part, and to reduce cross-talk between neighboring straws a $12.5\,\mu\mathrm{m}$ thick (skin depth at 40 MHz is $\sim 13\,\mu\mathrm{m}$) aluminium foil is used as outside layer. It was necessary to introduce an additional
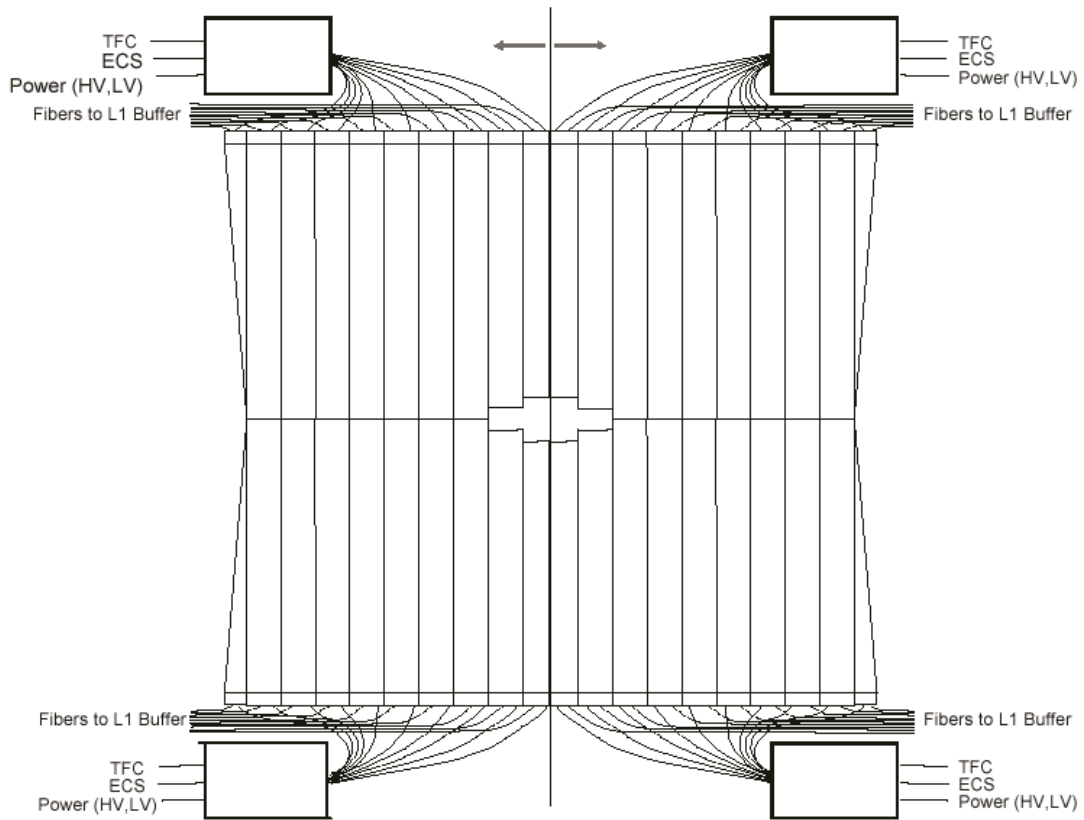
Figure 1: Outer Tracker chambers: readout and service electronics is placed at the outer edges of the detector.

layer of non-conductive Kapton in between to ensure gas tightness of the straws. The aluminum foil is pre-laminated to the non-conductive Kapton foil. Straws are wound using this pre-laminate together with the Kapton XC foil. The non-conductive foil isolates the aluminium shield from the inside cathode foil. The connection of both foils to the chamber reference ground is addressed below. The electrical properties for the drift-tubes have been extensively studied [3]. Important properties are summarized in Table 2.

1.2 Elements of the readout electronics

The drift-time of ionization clusters prodcued by through-going particles is measured for every drift-tube. Reference for the time measurement is the beam crossing (BX) signal. Hit times are digitized for every bunch crossing (25 ns)

2

Straw electrical properties	
Characteristic Impedance	316 Ω
Capacitance	10 pF/m
Signal propagation	3.8 ns/m
Analog Cross talk	$\leq 0.5\%$

Table 2: Electrical properties of the drift-tubes (Kapton XC + aluminium straws) [3]: The quoted value for the impedance is not considering the frequency dependence of the ohmic resistance of the 25 μm anode wire (skin-effect). The cross-talk number is given for the next neighbor.

and stored in a digital pipeline to wait for the Level-0 (L0) decision. On a positive L0 decision, the digitized data is transmitted via optical links to the Level-1 (L1) buffer boards, which are the front-end of the common readout-system.
A schematics of the front-end electronics is shown in Fig. 2. The elements of the Outer Tracker specific readout-electronics are:

- **Feedthrough board:** This passive printed-circuit board (PCB) is part of the module. It provides the electrical connections to the straws. Moreover it defines the reference ground for electronics and straws.

- **High-voltage board:** The board distributes the high-voltage to the straw channels. It contains capacitors for the signal decoupling from the chamber HV. It is plugged directly to the feed-through board.

- **ASDBLR board:** The board carries two ASDBLR chips. The ASDBLR ASIC is an 8-channel amplifier-shaper-discriminator with ion-tail cancellation and basline restoration designed for the ATLAS TRT [4].

- **OTIS board:** Two ASDBLR boards are plugged to a common board for the time measurement. The board carries the OTIS, an 32-channel TDC-chip which especially designed for LHCb Outer Tracker [9]. On a L0 accept the OTIS provides the digital event data on a 8-bit differential output.

- **GOL/Aux board:** 4 OTIS boards are connected to a GOL/Aux board. The GoL/Aux board [12] provides power, fast-control signals (BX clock, resets, L0 trigger) and slow-Control signals (I^2C) to OTIS and ASD boards. Moreover it reads the OTIS data. The GOL serializer chip is used to mulitplex the 32-bit OTIS information (4 × 8-bit) for a 1.6 Gbit/s optical link. The data is received by an optical receiver card, used as mezzanine card on the L1 buffer board (TELL1).
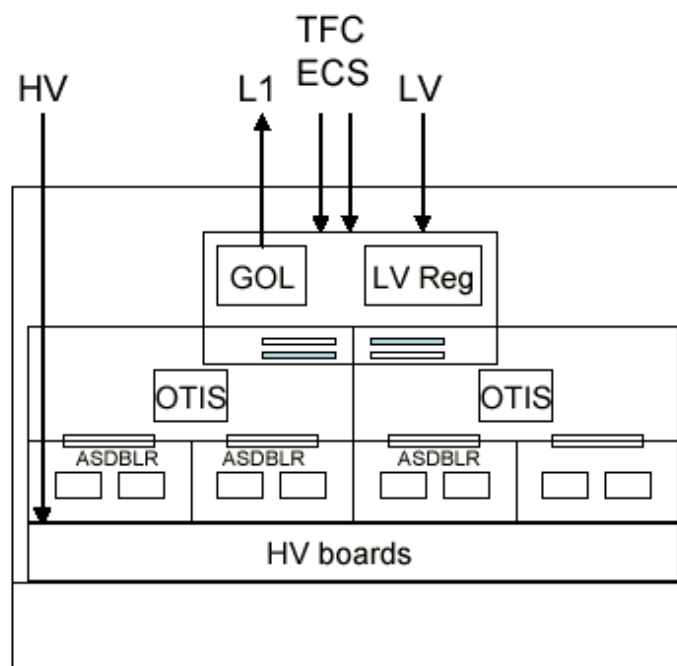
OTIS

Figure 2: Schematics of the Outer Tracker front-end electroncis

The above front-end boards all house inside the front-end electronics box which is schematically shown in Fig. 3. The electrronics boxes are mounted on the upper and lower end of a module. High-voltage and low-voltage cables, fast and slow-control cables as well as the optical fibers are connected to each electronics box individually. A front-end box ("module end") is the smallest independent readout unit of the Outer Tracker. Its output is an optical fiber providing the signals of the 128 channels of the module half (upper/lower) to the L1 buffer board.

In additon to the individual electronics boxes, there are distribution and service boxes and patch panels for low and high-voltage and for the optical signals at the vertical frames. The service boxes contain the necessary elecronics to reveive and decode the fast control (TTCRx chip) and slow control signals (SPECS slace). LVDS drivers allow the electrical dsirtibution of the control signals.

1.3 Requirements for the front-end electronics

Although the expected maximum occupancy of the Outer Tracker channels is only about 7% (MC study) the readout electroncis is designed to cope with occupancies larger than 10%. Taking signal propagation delays on the wire (max. 9.5 ns) and possible channel-to-channel time jitters into account the electronics must be able to record drift-times above 50 ns (at least for $Ar/CO_2/CF_4$). To exploit the full spatial resolution of the straw tubes a drift-time resolution of 1 ns is required.

The electronics is mounted at the outside edge. The expected radiation dose for

Figure 3: Schematical view of a front-end electroncis box.

an operation of LHCb of 10 years is about 10krad[1]

In addtion to the physics requirements Table 3 also gives the specifications by the trigger and DAQ system. L1 requirements do not affect the Outer Tracker specific electronics discussed in this note.

2   Front-End Electronics Components

2.1   Module Shielding, Grounding and Feedthough boards

Module shielding: In addition to the alu shielding of the single straws it was decided to enclose the straws of a module by an additional Faraday shielding: The straw supporting panels, as well as the module side-walls carry a $12.5\,\mu$m thick alu foil (skin depth at 40 MHz $\sim 13\mu$m). When gluing the box together the side-wall shielding is connected electrically to the panel shields. The top and

---

[1]This value is more than a factor 10 smaller than at the time of the OTIS chip specification. At that time the design of the tracker still assumed chambers inside the dipole magnet where the radiation level is much higher.

Outer Tracker Requirements	
max. drift-time in $ArCF_4CO_2$ ($ArCO_2$)	37 ns (44 ns)
max. occupancy	10%
double hit sequence	$<$ 20 ns
radiation dose (10 years)	$<$ 10 krad
temp. range	15 ... 70° C
TDC resolution	$<$ 1 ns

DAQ/L0 requirements	
max. L0 rate	1.1 MHz
L0 Latency / Pipeline	4.0 μs / 160 events
BX Counter	12 bit
max. readout time	900 ns
size of Derandomizer	≥ 16

Table 3: Outer Tracker and L0 trigger requirements for the front-end electronics.

bottom sides of the module are electrically closed by the feed-though boards.

Straw and Module Ground: As described in section 1.1 the outer alu foil of the straws and the innner conductive Kapton-XC foil are insulated. Moreover, when gluing the straws to the conductive panel surface a connection between the straw aluminium shield and the panel surface is not guranteed such that, in the worst case, Kapton XC, straw outer layer and panel surface are insulated from each other. The HV operation of the straws, the fast signal transmission along the straw as well as the principles of grounding demand a common ground point to which Kapton XC (HV ground), straw outer layer (signal ground) and the panel alu surface (shield) are connected. This point is represented by the ground layers of the feed-through board. Fig 4 shows the end of module with the feed-through boards and the ground connections.

Feed-through board [5]: The feed-through board provides the electrical connection between the signal wires (anodes) inside the gas-tight module and the front-end electronics at the out-side. The board also carries the pads to which the anode wires are soldered. As the wire position is guaranteed by the end-pieces the absolut pad postion is less important and do not have to be particularly precise. The printed-circuit board (PCB) consists of 3 layers:

- The upper layer with the solder pads for the anode wires inside the gas-volume and a ground surface.
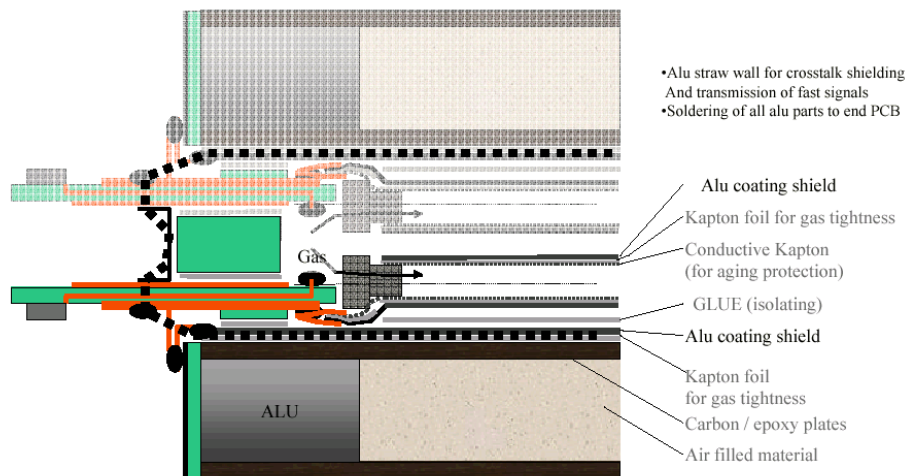
6

Figure 4: Module end with the feed-through defining the module ground.

- The middle layer with the signal traces.

- the bottom layer with the signal connector, contact springs for the ground connection to the HV boards, a ground strip which is soldered to the module ground, and pads to conncect to the straw cathode foil.

Fig. 5 shows a feed-through board with mounted components (conncetors, grounding springs). The gound connections to the feed-though boards are realized in the following ways: Every straw has a thin tongue (12mm length) at its end, used to conncect the outside aluminum layer to the inner Kapton XC (either by ultra sonic soldering or by a rivet). A small copper strip attached to the tongue is soldered to the ground pads of the feed-through board. The connection to the aluminium shielding foil of the panels is ensured by an additional solder strip.
The feed-through board defines the "module ground" and is used as reference for the subsequent electronics. The ground connection to the HV board is ensured by large surface spring contatcs.

2.2   HV Board

While the feed-through board an is integral part of the drift-chamber module, the HV board is not: two 32-channel HV boards are plugged to one feed-through board. For the HV signal connection SMD Samtec conncetors [2] are used. The

---

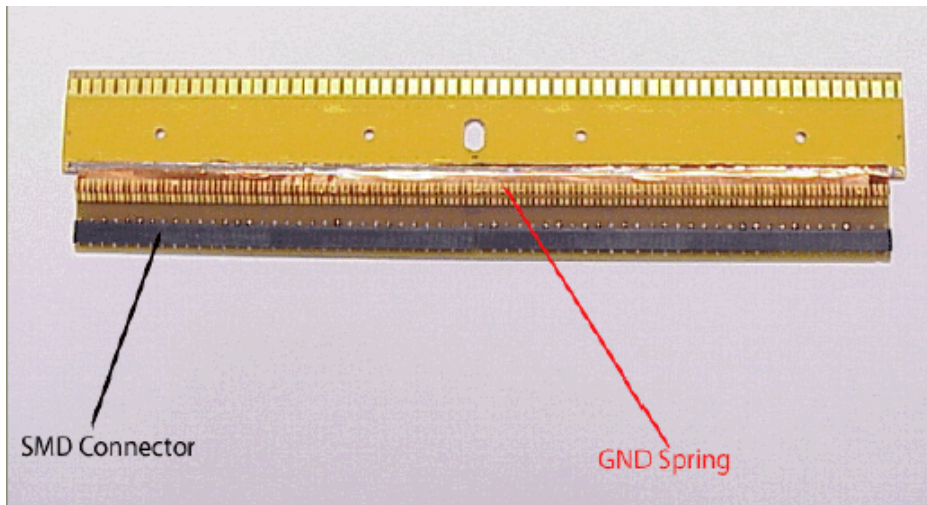[2]2/10 inches, every second contact is removed

Figure 5: Feed-through board.

spring-contacts of the feed-through boards ensure excellent connection to the module reference ground.

The HV board supplies the 32 channels it is connected to with a common HV. Pre-resistors of 1 MΩ are used in front of every channel to decouple the anode from each other and to avoid large currents in case of shorts in the drift-tubes. SMD ceramic capacitors[3] (330pF, 4kV max.), $4.6 \times 2 \times 1.5 \text{mm}^3$ are used to decouple the chamber signals from the HV. The electronics scheme of 16 out of 32 channels is shown in Fig. 6.

The the high channels density, the compact size of the HV capacitors (less than 4 mm between the two contacts of the capacitors) and the relatively large operating voltage (1500 V) demands additional insulation of the capacitors to avoid discharges across the capacitor surface. This is in particular necessary as the HV boards will be operated in air (early prototypes of the HV boards have shown leakage currents of up to 100 nA/channel during test beams at CERN).

The baseline design therefore forsees an embedding of the capacitors in the multi-layer PCB as shown in Fig. 7. The casting process should avoid stress on the ceramic capacitors. As it is difficult to reach the area underneath the capacitor pick-and-place paste must be used to position the capacitors and to avoid discharges in this area.

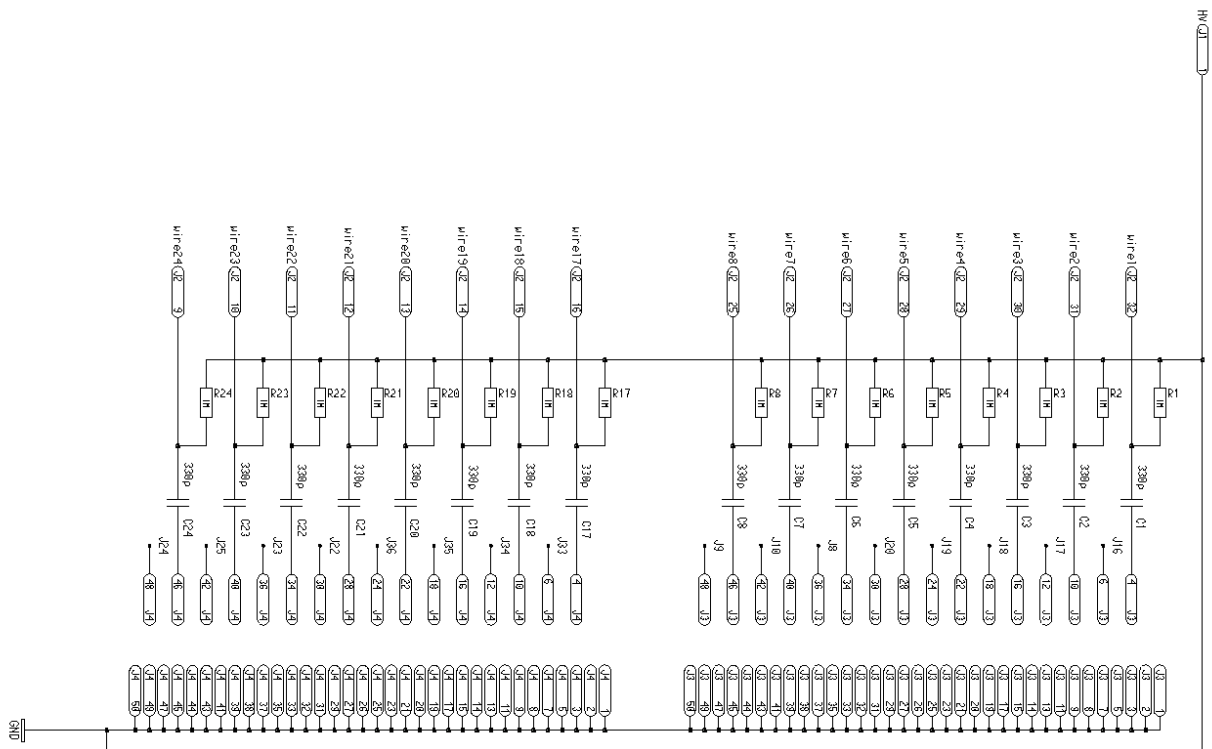[3]JOHANSON 302R29W331KV4E

8

Figure 6: HV board schematics for 16 out of the 32 channels per board.

2.3 ASDBLR Board

ASDBLR ASIC

The ASDBLR ASIC is an eight-channel amplifier-shaper-discriminator with baseline restoration designed for the read-out of the ATLAS Transition Radiation Tracker (TRT) [4]. The ASDBLR ASIC is a differential amplifier, each channel having an active negative-current input (InA), where the anode straw connects, and a "dummy" positive-current input (InB), for Common-Mode rejection. The ASDBLR is radiation-hard (7 MRad) and has high hit-rate (20 MHz with stable threshold, 100:1 dynamic range) capabilities. It consists of eight identical channels on 340 μm pitch, implemented in radiation tolerant 0.8 μm BiCMOS Technology (DMILL).

The current inputs are amplified, passed to a fast (25 ns) shaping stage to perform the slow-ions tail cancellation, then through a non-linear differentiation circuit called BaseLine-Restorer (BLR) to break the path from the shaper to the comparator and prevent that DC offsets or low-frequency noise can reach the comparator stage, and finally passed through two ("low" and "high") comparators. The digital comparator outputs are summed as current steps to form a differential ternary output with sharp turn-on (1 ns risetime). For the application
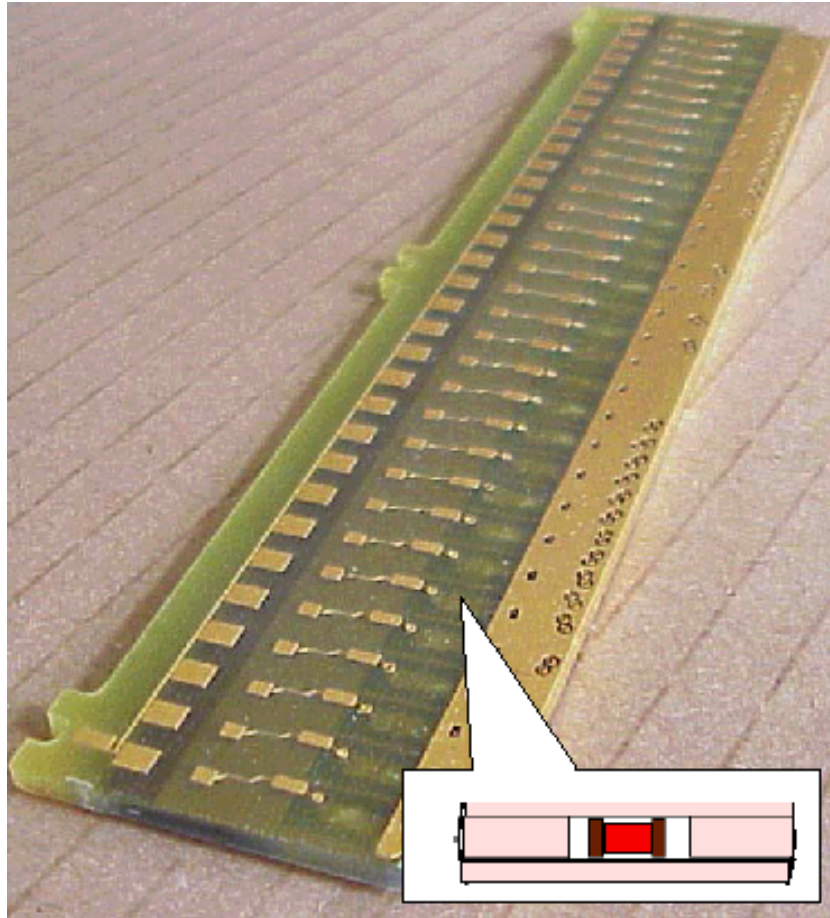
9

Figure 7: HV board: capacitors are embedded into the PCB as shown.

in Outer Tracker only the "low" (tracking) threshold comparator is used.
It operates on $\pm 3\,$V supplies with a typical power requirement of about $40\,$mW
per channel (the exact value depending on the programmed value of the Ternary
and Monitor outputs). A detailed description of the chip design, construction
and performance can be found in Ref. [4]. Studies of the operational properties
of the ASDBLR chip for the readout of Outer Tracker straw tubes can be found
in Refs. [3, 6].

ASDBLR board

The essential function of the ASDBLR Board [7] is to host two ASDBLR preamplifier-
discriminator ASICs. the design principles of the ASDBLR Board are largely based
on the results of the ASDBLR studies done for the Outer Tracker. The choice of

10

placing two ASDBLRs per board is a trade-off between two extreme scenarios: having eight ASDBLR's and two OTIS's on a single FE board, and having one single ASIC per board.

The amplifier input sees the contribution of several parasitic capacitances. Keeping all traces and especially the sensitive input lines as short as possible reduces the capacitive and inductive cross talk. Additionally, to reduce the channel-to-channel cross-talk, each signal pin on the connector is surrounded by ground pins on either side. Moreover, the ground planes of the HV and ASDBLR Boards are directly coupled over the full board widths via special contact springs. The amplifier input noise can be characterized as follows [4]: $\mathrm{ENC} \simeq 2100\,e + 145\,e/\mathrm{pF} \times C_{\mathrm{in}}\,[\mathrm{pF}]$ [8]. The total contribution of the FE Electronics has been measured to be about 20 pF (7 pF from the traces of the Feed-Through Board, 7 pF from those of the HV Board, and 6 pF from the ASDBLR Board traces and extra protection circuitry). Therefore the total input noise contributed by the electronics is about $5000\,e \simeq 0.8\,\mathrm{fC}$, consistsent with our measurement [8], which must be compared to an effective signal size of 20 fC (taking the shaping time into account).

The main contribution to the power consumption on the ASDBLR board is expected to come from the ASDBLR ASIC. This has been estimated to be $\delta P_+ \simeq \delta P_- \simeq 80\,\mathrm{mA} \times 3\,\mathrm{V} = 240\,\mathrm{mW}$, which gives a total of 960 mW per ASDBLR board. The ASDBLR Board has been provided with a heat-spreading layer in the PCB, to which heat-conducting mounting posts are coupled. These cooling posts are then intended to be coupled to the internal cooling chassis of the front-end electronics box. Tests with prototypes of the ASDBLR boards (see below) showed that the ASDBLR chip internal temperature was less than $25\,^{\circ}\mathrm{C}$ above the cooling-surface temperature ($\sim 20\,^{\circ}\mathrm{C}$).

2.4 OTIS and OTIS Board

OTIS TDC Chip

The OTIS chip [9] is developed for the readout of the LHCb Outer Tracker straw tubes. The chips operates synchronous to the 40 MHz LHC clock. Main components of the chip are:

- the TDC core, consisting of a DLL, hit register and hit decoder

- the L0 pipeline buffer together with the derandomizing buffer to cover the L0 latency and to cope with fluctuations of the trigger rate

- the control logic for the trigger and memory management and to prepare the output data

11

- the I2C interface for setup and slow control

In addition the chip comprises 4 DACs to provide the threshold voltages for the ASD discriminator chips. The block diagram of the OTIS chip is shown in Figure 8. The chip serves 32 input channels (LVDS) and provides 8 bit wide data output (differential CMOS).

TDC core: For the time measurement a DLL, consisting of a chain of 32 double staged delay elements, is used. The BX clock propagates through the chain. A phase detector compares the delayed clock with the original one. Depending on the observed phase shift a charge pump adjusts the voltage controlled delay elements until the phase difference vanishes. In this state the DLL is locked and the DLL clock can be used as reference for the time measurements. To decrease the uncertainty of the digitization the number of DLL tabs are doubled by using both stages of each of the 32 delay elements. The output of the DLL stages are used to clock 64 hit registers and to latch the the discriminated hit signal. A decoder converts the status of the 64 registers into a 6 bit "fine time".

Pipeline and derandomizing buffer: Pipeline and derandomizing buffer are built as arrays of dual ported SRAM cells. The memory dimensions are 164 events x 240 bits and 48 events x 240 bits respectively. The depths of both buffers are thus larger than required by the L0 specifications.

Control Algorithm: The control algorithm provides trigger and memory management as well as the control of the data output stream. The hardware description language *Verilog* was used to code the algorithm.

Readout modes: On a positive L0 trigger the control algorithm can search detector hits in up 3 bunch crossings. In the multi BX modes not all possible hits can be transmitted within the required 900 ns readout time. Therefore, there are 2 different readout modes to cope with this situation:

1. every channel, wether hit or not, appears in the readout. Only the first hit is transmitted.

2. times are transmitted only for channels with hits. A 32-bit hit mask for every bunch crossing indicates the channels with hits. If the maximum numer of possible hits is reached the event is truncated.

Test modes: On a power-up reset a memory test es executed. The chip allows further to write known hit/time patterns into the pre-pipeline register.

Slow control: The slow-control interface to the chip is implemented using I^2C. The interface allows to read and write the control registers, to load the pre-pipeline register with test-data (play back mode), to read an accepted event from the derandmoizing buffer (important for laboratory usage of the chip), and to set 4 DACs used to provide the thresholds to 4 ASDBLR chips (see below).
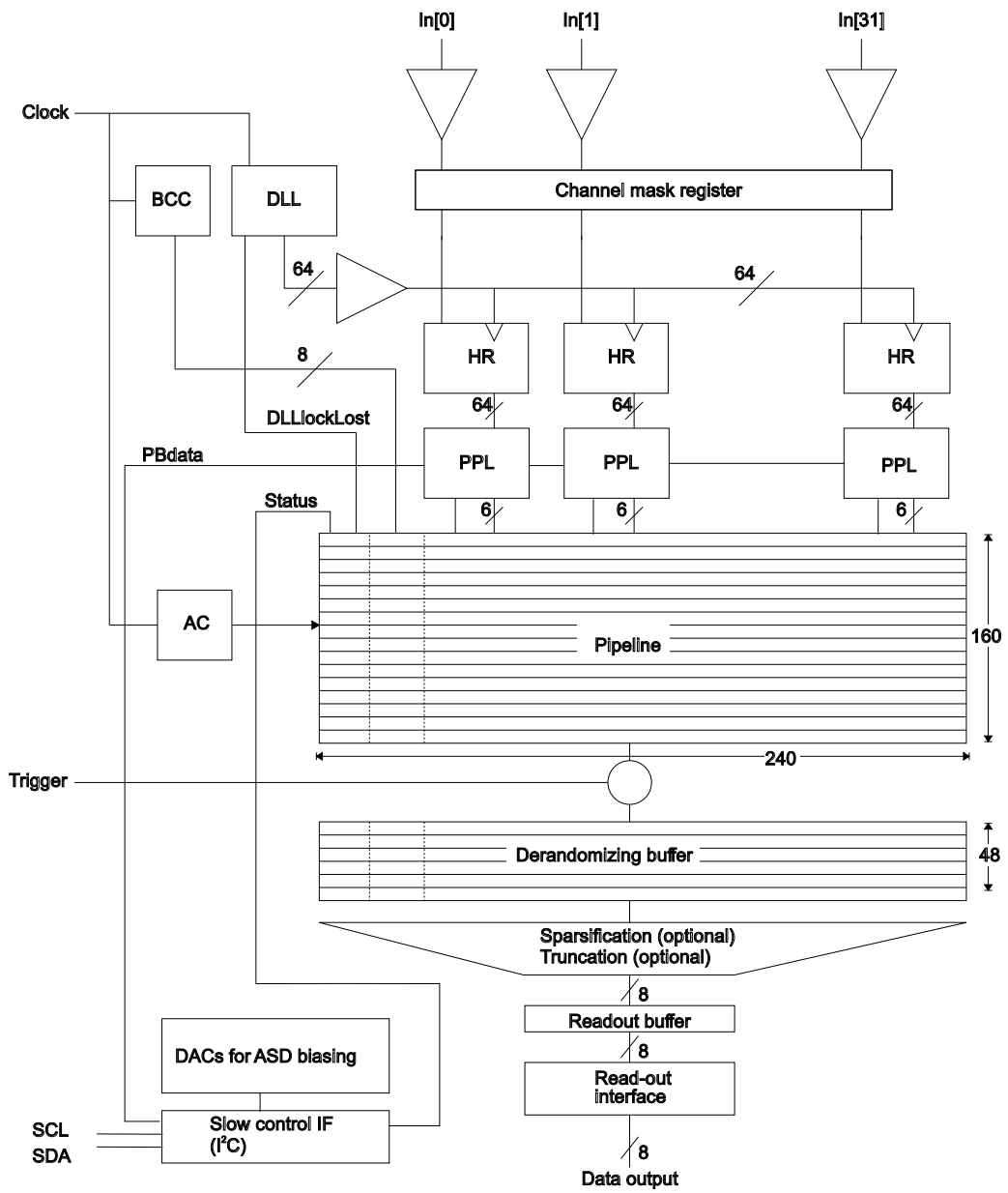
Figure 8: Block diagram of the OTIS TDC chip.

OTIS Board

The OTIS board [10] is situated inside the front-end electronics box. It is designed to service the bare-unpacked OTIS chips[4]. The board gets the hit data from the ASDBLR boards and provides the OTIS TDC data to the GOL/Aux board. The OTIS board provides the mechanical and electrical connection between the ASDBLR boards and the GOL/Aux board. Therefore it passes signals and low voltages from the GOL/Aux board to the ASDBLR board.
A simplified electrical schematics and the meachanical layout is shown in Fig.9. To service both straw layers (2×64 channels) the shown OTIS and ASDBLR boards are doubled and connected recto-verso to the back-side of the GOL/Aux board. Due to the symmetry only two different versions of the OTIS board, a "left" and a "right" board, are required.

ASDBLR-to-OTIS interface

For the hit inputs of the OTIS chip LVDS pads are used. The ASDBLR chip on the other hand provides differential outputs based on open-collector drivers with a maximum current for the "low threshold" of 0.8 mA. To interface the ASDBLR signals to the OTIS a termination scheme using two 3.9 kΩ pull-up resistors and a 120 kΩ resistor as line termination is proposed [11]. The termination resistor leads to a maximum signal swing 48 mV at the LVDS pads sufficiently large to switch the inputs. A detailed definition of the ASDBLR-to-OTIS interface can be found in Ref. [11].

2.5 GOL/Aux Board

The GOL/Auxiliary board [12] is connected to 4 OTIS boards. It serializes the TDC Data and outputs the data to an optical link. The board supplies the OTIS boards with low voltage, fast control and slow control signals and has outputs for voltage/temperature sensing. A layout of the GOL/Aux board is shown in Fig. 10
For data serialization the GOL/Aux board uses the GOL chip [13]. The chip is a CERN EP development in rad-hard 0.25 μm technology. It serializes the 32 Data bits coming from the four OTIS boards on one module end. The Data is encoded with 8/10 bit Giga-bit ethernet encoding [14], resulting in 1.6 Gbit/s output rate. The serial data is driven into a VCSEL diode coupled to 50/125 μm optical fiber.

---

[4]Currently the preferred solution is to not pack the OTIS chips but to use a chip-on-board design.
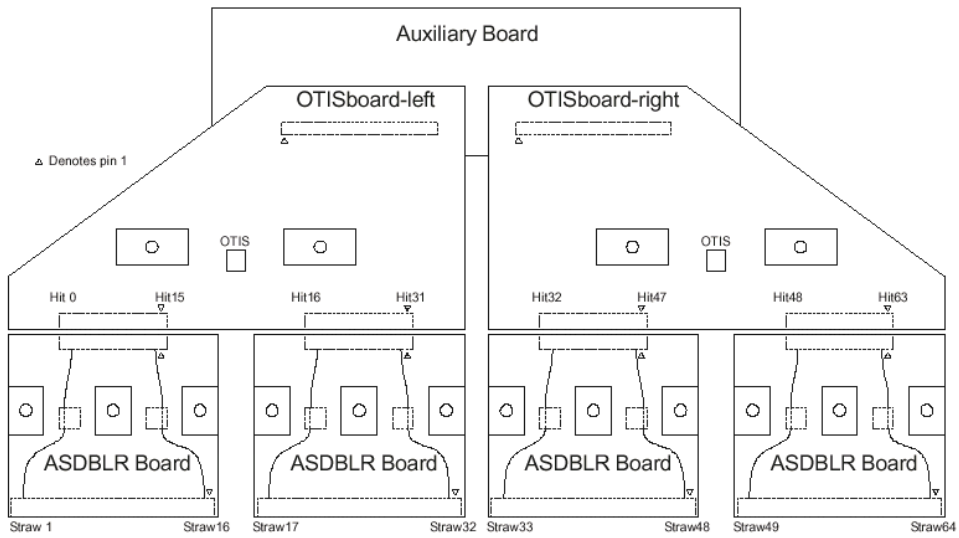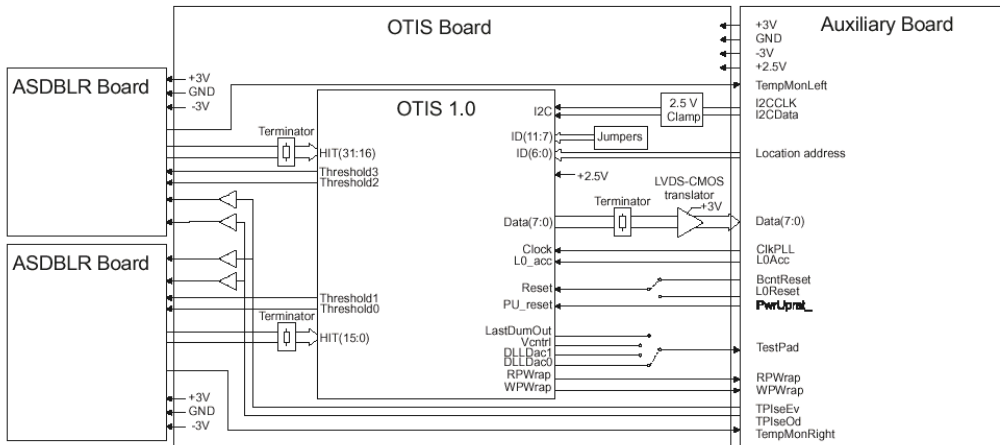
Figure 9: Simplified electrical schematics (top) and mechanical layout of the OTIS board.
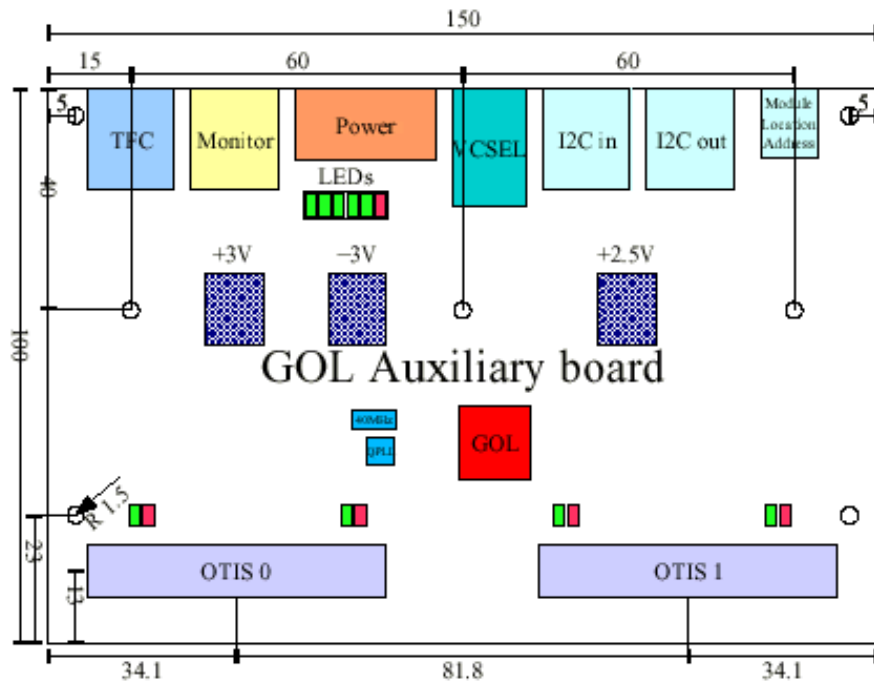
Figure 10: Layout of the GOL/Aux board.

The GOL serializer requires for the clock signal a jitter of less than 100 ps (peak-peak). The QPLL chip (CERN EP) is used to stabilize the clock signal received from the the service box (TTCrx chip) . The QPLL uses a specially cut voltage controlled quartz oscillator ($4\times$ LHC frequency) . The filterd clock is also supplied to the OTIS boards.

All fast control signals such as clock, L0 Trigger Accept, L0 Reset, Bunch Count Reset, Event Count Reset, and test-pulse signals for odd and even preamplifier channels are distributed as LVDS signals. Slow control signals are distributed over I^2C bus to the OTIS TDC and GOL serializer chips.

The fast-control signals as well as the slow-control signals are distributed electrically from the distribution/services boxes to the GOL/Aux boards. For the fast-control signals the connection is a point-to-point connection where an equal cable lenghth ensures an approximate synchronous timing of the signals. The slow-control signals are distributed via an I^2 bus. A single bus-line connects all GOL/Aux boards of one stereo-layer (9 modules, daisy-chained). An electrical decoupling of the 9 GOL/Aux boards from the bus-line is foreseen.

Radiation hard power regulators developed at CERN supply the low voltage.

16

Positive types L4913 deliver +3 V for the ASDBLR and +2.5 V for GOL, OTIS and QPLL. One negative type L7913 are used for the -3 V of the ASDBLR. The power is derived from incoming ±6 V. The power regulators are a majort heat source and are therefor mounted directly on the cooling structure.

2.6   Optical Link

For the transmission of the serialized detector data from the GOL/Aux board to the L1 buffer board an optical link is used.
The serialized GOL output (1.6 Gbit/s, 8/10 bit Giga bit ethernet standard [14]) drives a commercial VCSEL diode, which was tested to be radiation tolerant by the LHCb Inner Tracker group. For optical transmission VCSEL diode is connected to an optical fiber. The fiber consists of 3 sections.
A SMA connectorized multi-mode fiber with 50/125 μm size runs to the optical patch-panel on the detector frame. At the patch panel the 9 fibers of one quarter layer are fed into a 12 fiber optical ribbon cable, also 50/125 μm. The ribbon spans the 70-80 m distance to the trailer where another patch panel is located, close to the Trigger ELectronics and L1 boards (TELL1) [15]. A short optical ribbon connects the patch panel to the optical receiver cards on the TELL1, allowing an easy exchange of fiber destinations without exposing the long ribbon cable to mechanical stress.
Two optical receiver cards (O-RxCards) can be mounted on one TELL1 board. Each O-RxCard citeORx carries one commercial 12 fiber optical receiver [17] and twelve de-serializer chips [18], allowing a maximum of 24 optical inputs for each TELL1 board. The de-serialized data is synchronized and processed on the TELL1 board with the help of FPGAs. Details on the link synchronization can be found in Ref. [19].
As the optical link is common for the LHCb Inner Tracker, VETO, Outer Tracker and possibly further subsystems, many components as the fibers, VCSEL diodes and the O-RxCards are the same for these sub-detectors.
Apart from the optical data link described here, the Timing and Fast Control (TFC) system [20] and the slow control will utilize optical data transmission. These systems use different optical components, demanding radiation tolerance on the receiving side.

2.7   Front-end electronics box

Assembly and Maintenance

The front-end boards (4 HV boards, 8 ASDBLR boards, 4 OTIS boards and 1 GOL/Aux board) are mounted in an electronics box [21]. The box construction

17

provides a support frame to carry the boards. The support frame serves at the same time a heat-conductor and is in thermal contact with all major heat sources. The complet construction is enclosed with metal (ground) cover sheets. The front and the side view of an assembled box is shown in Fig. 11. The only board which stick out of the construction is the GLO/Aux board, which also carries all the connectors.
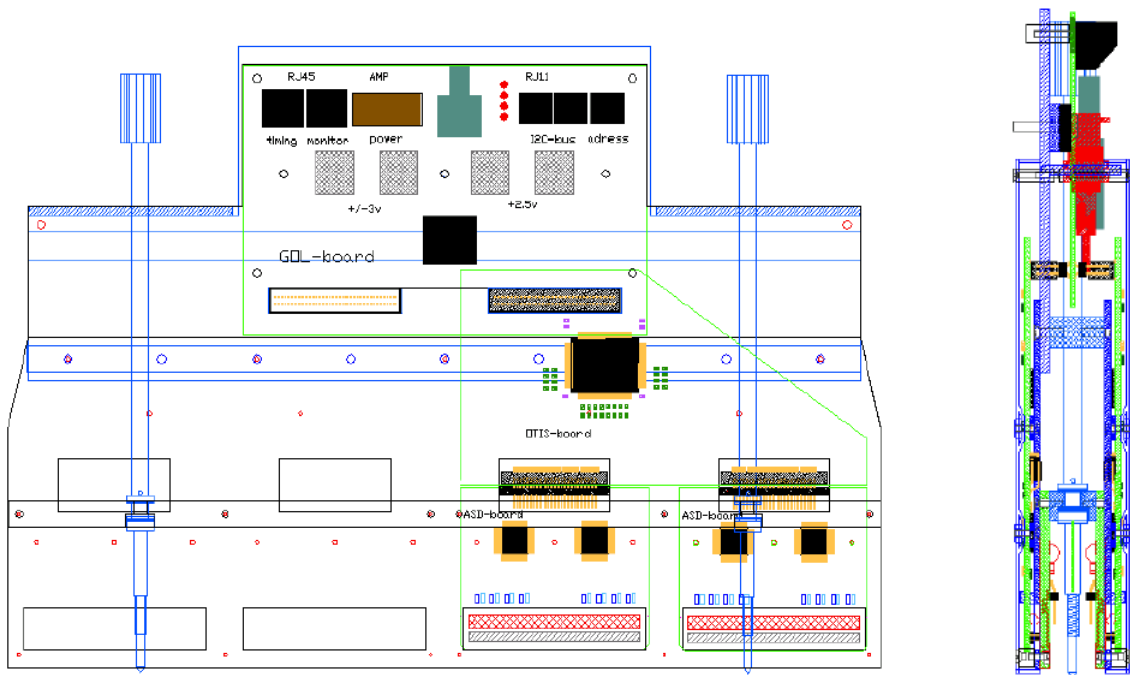

Figure 11: Assembly of the front-end electronics boards: front and side view.

The assembled electronics box is an independent unit and is plugged to the feed-through boards of the module. As the mounting of the box including the precise positioning of the connectors 128 pins between feed-through and HV boards is difficult, a mechanical guidances is foreseen. Screws will allow safe connection and disconnection of the box.

As the boxes are independent units they can be tested before installation. If readout and service cables are properly foreseeen the installation of the boxes on the final detectos can therefore take place independetly of the frame assembly.

If service of electronics boards inside the box becomes necessary, the whole box must be dismounted and opened.

In case of broken or hot wires we can disconnect one of the 4 HV connections remotely in the counting room. During chamber maintenance one can disconnect

the malfunctioning wires inidividually from the HV supply on the HV board.

Cooling

The front-end electronics and in particular the low-voltage regulators will dissipate about 25 W per front-end box [22, 23]. Multiplied with the total number of readout boxes (432) the power consumption results in a total heat production of about 10 kW for the total detector. It is not possible to release the heat into the experimental hall. Moreover the boxes are densly packed on the frames. Water cooling was therefore considered at an early stage of the design.
The active electronics boards are designed that the heat sources are in thermal contact (directly or using heat-spreading PCB layers of 100 μm thickness) with the cooling chassis of the front-end electronics box. The main cooling plate of the electronics box will be mounted against a water-cooled frame.
A cooling test with a thermally insulated front-end box has been done: Only the main cooling plate of the electronics box was cooled with air at room temperature ($\sim 20\,^{\circ}$C). Fig. 12 summarizes the temperatures measured at thermal equilibrium for the different parts of the front-end electronics. The equilibrium temperature of the cooling plate was $35\,^{\circ}$C. The highest temperature in the box was measured with $52\,^{\circ}$C on the OTIS chip. For the amplifier chips values of about $42\,^{\circ}$C have been measured. The temperatures of all deivices are only between 8 and 17 degrees higher than the one of the cooling plate demonstrating the effectiveness of the cooling design. Moreover the absolute temeperature of the all boards will decrease when the cooling plate is thermally connected to the water cooled system.

3   Control and Services

Each of the three Outer Tracker stations consist of four double-layers of straw tubes arranged in a XUVX sequence. Pairs of these planes (XU and VX) are mounted onto frames that can be slided in two halves from and to the beam-pipe, like curtains. Each Detector "curtain" carries nine front-end electronics boxes per side (9 on the top and 9 on the bottom of the curtain); this results in a total of 36 Front End boxes per detector curtain. The Front End boxes have connections to the power supplies (High Voltage and Low Voltage), the Experiment Control System (ECS), and the Timing and Fast Control (TFC). In addition, optical fibers carry the data from each Front End box from the detector to the counting room. The Distribution and Control Box will provide the interface to all these services. Since each detector curtain is a unit with independent movements, Distribution and Control Boxes are foreseen on each
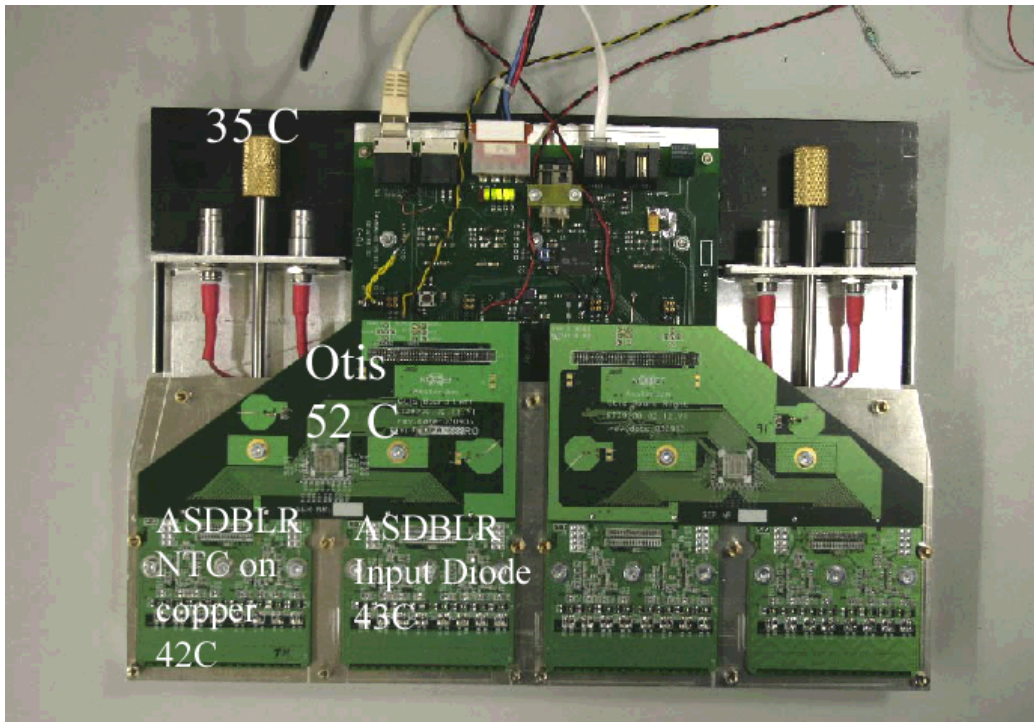
Figure 12: Cooling tests of the front-end electronics. The indicated temperatures have been measured when the box was encloded with thermal insulation and only the cooling plate was cooled.

detector curtain, as shown in Fig. 13. A detailed description of the Distribution and Control Boxes can be found in Ref. [24].

Each Distribution Box consists of:

- **High Voltage Distribution Box:** From the point of view of the HV distribution, the 128 straw-tube channels in each front-end box are sub-divided in 4 groups of 32 straws, with separate HV connections to the Counting Room; in this way, a minimal detector area of 32 straws can be disconnected when a faulty wire shortens the HV power supply. In this scheme, each detector curtain has 144 HV connections to the counting room, realized with shielded 56-conductors HV cables with Radiall 52 pins rectangular HV connectors, carrying 48 HV channels and interlock signals to switch-off the HV when the connector is not connected.

- **Low Voltage Distribution Box:** A Front End box typically draws a current of 2.6 A from the positive power supply and 0.9 A from the negative power supply. For one detector curtain, this adds up to a current of 93.6

20

A for the +6V supply and 32 A for the -6V supply. The Low Voltage Distribution Box will provide the interface to the LV supply for 36 Front End Boxes, the Master Control Box, and the Slave Control Boxes, via patch panels.

- **Optical Fibers Distribution Box:** The digitized data is sent via 12-fold optical cables to the optical receiver cards of the L1 buffer boards. In our scheme one optical ribbon cables serves the 9 front-end boxes of a stero-layer. Four ribbon cables are routed to a Fiber Distribution Box that is mounted on the detector curtain. The distribution from the Fiber Distribution Box to the front-end boxes are done by single fibers with SMA connectors. For each ribbon cable, only nine individual fibers are connected to the Front-End boxes, leaving a total of twelve spare fibers per Fiber Distribution Box.

The **Control Box** distributes the TFC and ECS signals to and from the Front End boxes; it is subdivided in three parts: one **Master Control Box** and two **Slave Control Boxes**. The two Slave Control Boxes are one at the top of the Detector curtain and one at the bottom of the Detector Curtain, respectively. The advantage of this approach is that the TFC cables are kept to a minimum length and only one TTCrx and SPECS slave chips per Detector Curtain are needed. Both the connection from the Slave Control Box to the Master Control Box as well as the connection from the Slave Control Box to the Front End boxes are made with 14 equal-length twisted pair shielded cables and 30 pin shielded Metral connectors in a star configuration. The length of each cable is approximately 5 meter, giving rise to time skews below 1%. The difference in the length of the pairs within the cable is about 0.7% resulting in a time difference between the Front End Boxes of about 850 ps.

Another important part of the Control Box is the test-pulse system which is currently being designed[25]. The system will allow to send synchronized test pulses to the front-end electronics. The test-pulses are capacitively coupled to the ASDBLR inputs.
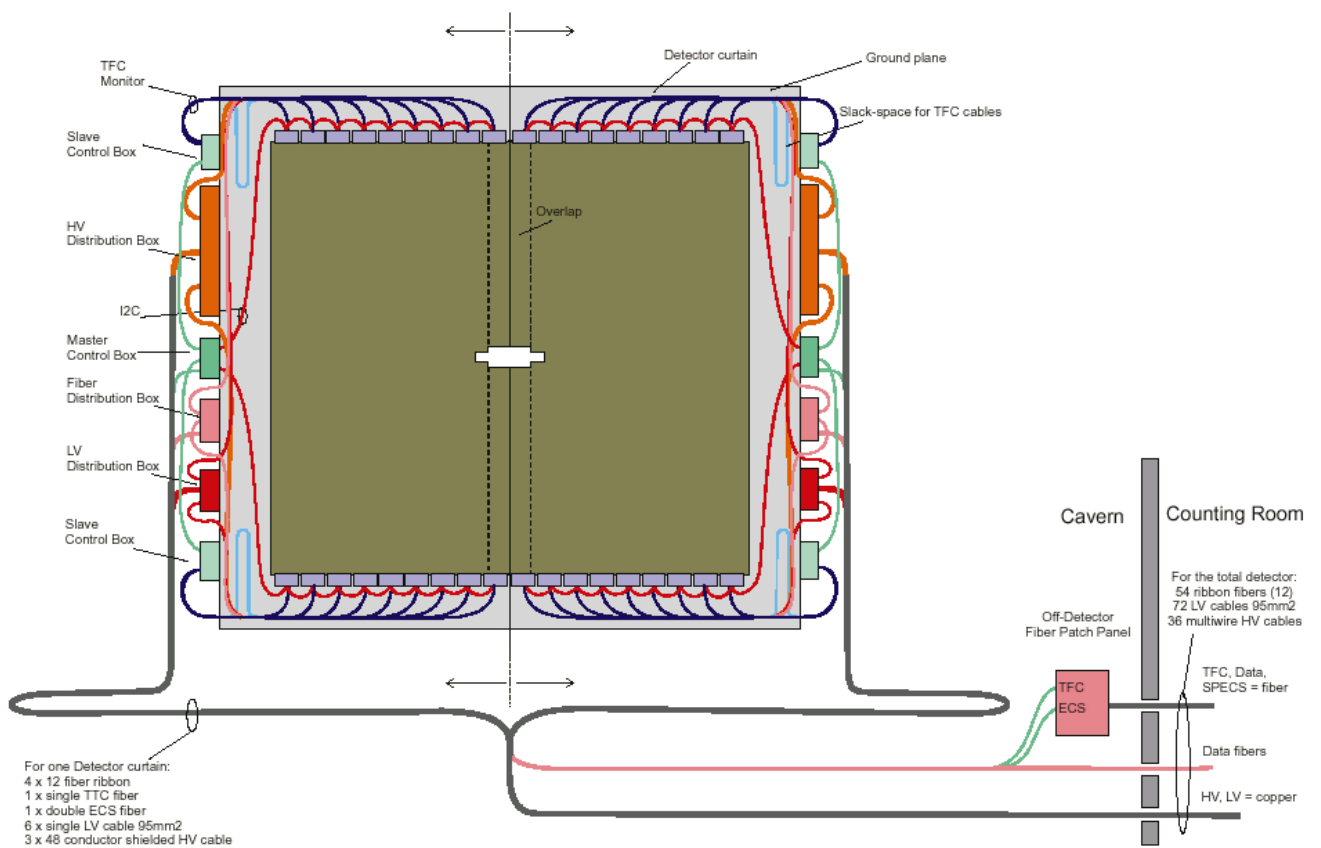
TFC Monitor

Slave Control Box

HV Distribution Box

I2C

Master Control Box

Fiber Distribution Box

LV Distribution Box

Slave Control Box

Detector curtain

Ground plane

Slack-space for TFC cables

Overlap

Cavern   Counting Room

For the total detector:
54 ribbon fibers (12)
72 LV cables 95mm2
36 multiwire HV cables

Off-Detector
Fiber Patch Panel

TFC
ECS

TFC, Data,
SPECS = fiber

Data fibers

HV, LV = copper

For one Detector curtain:
4 x 12 fiber ribbon
1 x single TTC fiber
1 x double ECS fiber
6 x single LV cable 95mm2
3 x 48 conductor shielded HV cable

Figure 13: Schematic view of services: Low-voltage, high-voltage, read-out fibers,fast-control, slow-control.

4 Detector Grounding

For a single module the reference ground of electronics and HV is the ground of the electronics box which is defined by the feed-through board. As all modules are mechanically and electrically connected to the curtain frame made out of aluminium, it is this frame which will work as the chamber ground reference point. Except a single connection to the "safety ground" of the experimental hall, the frame will be kept floating:

- Gas and water pipes must be insulated from the frame.

- Connected low voltage power supplies are kept floating in the counting rooms.

- For the HV distribution, supplies with floating outputs are used. The ground shield of the HV lines are tied to the safety ground using a special "ground fault circuitry" in the counting room.

- Slow-Control and Fast-Control systems will be electrically decoupled.

A detailed description of the foreseen grounding scheme can be found in Ref. [26].

References

[1] M. Feuerstack-Raible et al., The LHCb Outer Tracker readout electronics, LHCb note LHCb-2001-013.

[2] LHCb Collaboration, LHCb Outer Tracker – Technical Design Report, CERN, Sep. 2001, LHCC/2001-024.

[3] V. Gromov and T. Sluijk, Electrical Properties of various types of straw tubes considered for the LHCb Outer Tracker, LHCb Technical Note LHCb-2001-001.

[4] R. Bevensee et al., IEEE (1996) Trans. on Nucl. Sci., Vol. 43, 1725;
N. Dressnandt et al., 'Implementation of the ASDBLR Straw Tube Readout ASIC in DMILL Technology", IEEE (2000) Trans. on Nucl. Sci., Vol. 48, 1239;
M. Newcomer and A. Romaniouk, ASDBLR chip operational properties studies at CERN. ATLAS Internal Note INDET-NO-122, 1996.
http://www.hep.upenn.edu/atlas/asdblr/
http://www.quark.lu.se/ãtlas/electronics/trt/chip_asdblr.html
http://www.hep.upenn.edu/atlas/asdblr/presentations/prr/
DMILL_Fabs.pdf

[5] S. Bachmann et al., Definition of Feed-trough and Splitting Boards, LHCb Technical Note LHCb-2003-052;

[6] V. Gromov et al., Study of Operational Properties of the ASDBLR Chip for the LHCb Outer Tracker,LHCb Technical Note LHCb-2000-054.

[7] A.Berkien et al., An ASDBLR board Prototype for the LHCb Outer Tracker, to appear as LHCb note;
http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/ ASDBLR.ps

[8] A.Berkien et al., Noise performance of the ADSBLR board for the LHCb Outer Tracker, in preparation.

[9] H.Deppe et al., The OTIS Reference Manual – Version 1.1,
http://wwwasic.kip.uni-heidelberg.de/lhcbot/secure/Specifications/ OTIS11-UserManual.pdf.
H.Deppe et al., "Status Report for the Chip Review on June 5, 2003",
http://physi.uni-heidelberg.de/ uwer/lhcb/Otis/Overview.pdf

[10] A. Zwart et al., OTIS Board Version 1.0, to appear as LHCb Technical Note;
http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/ OtisBoard.pdf.

[11] T. Sluijk and U. Uwer, OTIS-to-ASDBLR interface, to appear as LHCb Technical Note;
http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/ otis2asd-specs.ps.

[12] D.Wiedner et al., Specification for a Prototype of the Auxiliary Board for the Outer Tracker, LHCb Internal Note LHCb-2003-129.

[13] P. Moreira et al., GOL Reference Manual, Gigabit Optical Link Transmitter manual http://proj-gol.web.cern.ch/proj-gol/manuals.htm

[14] IEEE Std 802.3, 1998 Edition.

[15] G. Haefeli et al., TELL1 Specification for a common read out board for LHCb, LHCb Note LHCb-2003-007.

[16] D.Wiedner et al., Prototype for an Optical 12 input Receiver Card for the LHCb TELL1 Board, LHCb Internal Note LHCb-2003-137.

[17] SNAP12 12 channel pluggable optical module MSA, Specifications, Appendix to the SNAP12 Multi-Source Agreement

[18] TLK 2501 – 1.6 to 2.5 GHz deserializer, Texas Instruments; Revision July 2003; `http://Jocus.ti.com/lit/ds/symlink/tlk2501.pdf`.

[19] H.Deppe et al., Synchronization of the LHCb Outer Tracker Optical Links, to appear as LHCB note,
`http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/`
`sync.ps`.

[20] Jorgen Christiansen et al., TTCrx Reference Manual, A Timing, Trigger and Control Receiver ASIC for LHC Detectors

[21] A.Berkien et al., The Front Ende Electronics Box for the LHCb Outer Tracker, LHCb note in preparation.

[22] T.Sluijk et al., Power Consumption of the Outer Tracker Front-End Electronics, Outer Tracker internal note.
`http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/`
`power-consumption.ps`.

[23] A.Berkien et al., Cooling Test of the FE electroncis box, in preparation.

[24] T.Sluijk and A.Zwart, Distribution-Boxes and Control-Boxes for the Outer Tracker, to appear as LHCb note,
`http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/`
`Distribution_Box.pdf`.

[25] U. Uwer and A. Zwart, Test Pulse System for the LHCb Outer Tracker Detector,
`http://physi.uni-heidelberg.de/ uwer/lhcb/Electronics/Review/`
`Test_Pulse.pdf`.

[26] T.Sluijk et al. Grounding and Shielding of the CERN LHCb Outer Tracker Detector, to appear as LHCb Technical Note;
`http://www.nikhef.nl/ toms/grounding/`
`Grounding-and-Shielding-of-the-Outer-Tracker-Detector.pdf`.