NATIONAL INSTITUTE FOR NUCLEAR AND HIGH ENERGY PHYSICS

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OTIS Board
Version 1.0

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The OTIS Board is a part of the Outer-Tracker Front-End Electronics. It carries the OTIS TDC that gets the 32-bit Hit information from two ASDBLR boards. The 8-bit TDC output data is fed to the AUX/GOL Board.

Preliminary Version

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14-8-2003 Preliminary Version

4-9-2003 Preliminary Version

elco 100uF 10V changed in ceramic capacitor 10uF 10V

coil resistance added

1. Functional Description

The OTIS Board is situated inside the Front-End Electronics of the Outer Tracker Modules and is mainly designed to service the bare –unpacked- OTIS 1.0 [1] chip: it gets the Hit data from the ASDBLR Boards [2] and sends the OTIS TDC data to the AUX/GOL Board [3].

In addition, it implements the following functionalities:

- the OTIS can provide four threshold levels to four ASDBLR chips
- receives the low-voltage biases from the regulators placed on the AUX/GOL boards and transfers (some of) them to the ASDBLR board
- receives the test pulse signal(s) and transfers them to the ASDBLR one for each board
- receives temperature monitor signal(s) from the ASDBLR boards and transfers them to the AUX/GOL board.

The main functionalities of the OTIS board are illustrated in the diagram in Figure 1.

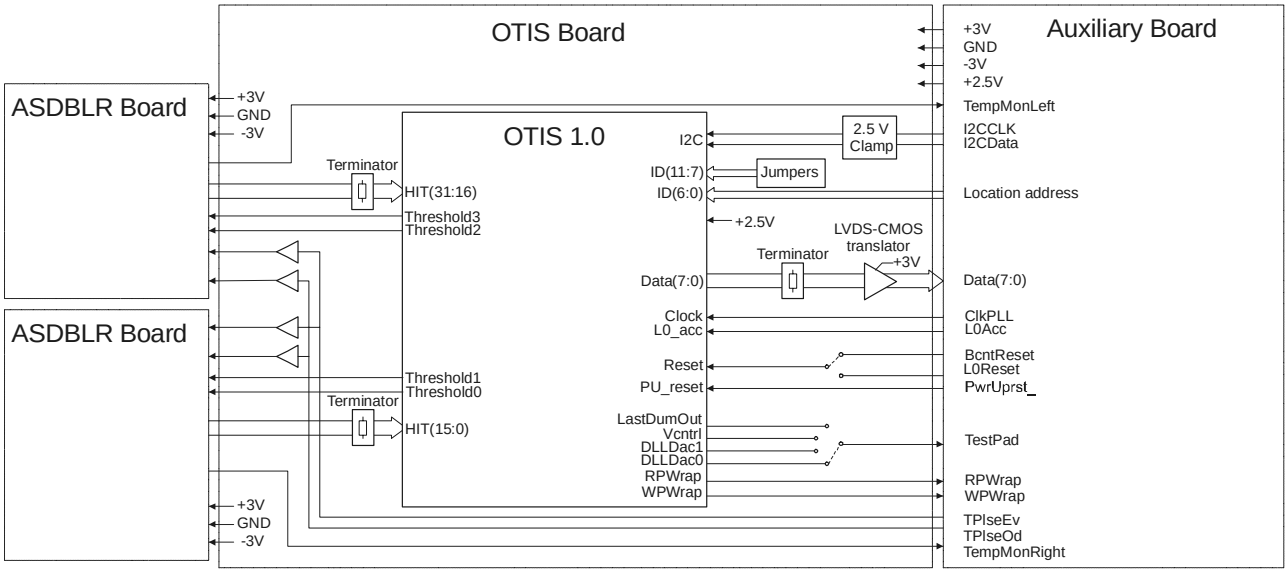

Figure 1: Functional scheme of the OTIS Board

The OTIS output data are LVDS signals, but the AUX/GOL Board expects CMOS data signals; therefore, an LVDS to CMOS converter is placed on the OTIS Board. Later versions of the OTIS will have differential CMOS outputs and can be connected directly to the GOL.

The OTIS has six test signals for debugging purposes: WPWrap and RPWrap are fed directly to the AUX/GOL Board, the remaining four (LastDumOut, Vcntrl, DLLDac0, DLLDac1) can be selectively -by jumper- transferred to a TestPad signal of the AUX/GOL Board.

From the AUX/GOL board, the OTIS board receives the signals of the Timing and Fast Control (TFC): clock, L0 Accept, BCN- and L0-reset. The OTIS is reset by a Power-Up reset or by a fast reset, generated either by the Bunch count reset or by the L0 reset -selectable by a jumper.

From the AUX/GOL board, the OTIS board receives also the signals of the Electronics Control System (ECS). The control of the OTIS is done with the use of I2C [4]; the I2C signals are

clamped to 2.5 Volt to protect the OTIS inputs. The Location Address supplies the I2C Address; the five high identifier bits ID(11:7) can be set by jumpers.

The power consumption of the board is 135 mW @ +3 Volt for the LVDS receivers and 220 mW @ +2.5 Volt for the OTIS. Special care is taken to separate the analog and digital supply voltages for the OTIS.

2. Layout of the OTIS Board

Due to the geometry of the Front-End Electronics (the connector to the AUX/GOL Board is placed asymmetrically on the OTIS Board), two types of boards are needed: OTIS board “left” and OTIS board “right”. This is shown schematically in Figure 2, which also shows the straw numbering in relation to the hit numbers: Straw(64:1) goes to Hit(63:0).

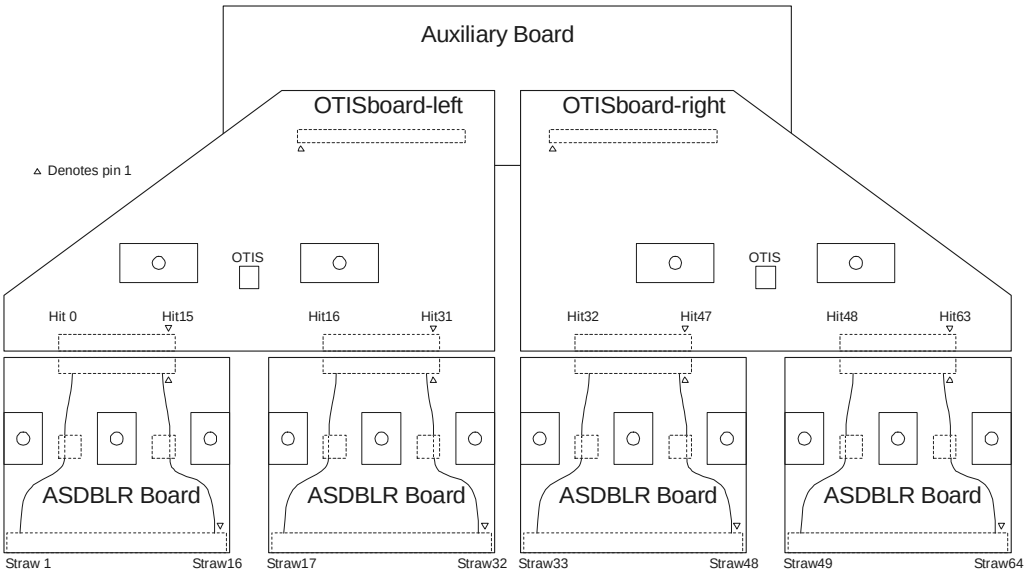

Figure 2: OTIS Boards and ASDBLR Boards as mounted on detector

The two boards are functionally identical, but the places of some components differ. Figure 3 shows the OTIS board as viewed from the side where components are placed; the layout of the board is done from this side. The board has four layers: the two outer layers are signal routing layers of 30 micron conductor thickness, the two inner layers are power layers of 100 micron copper.

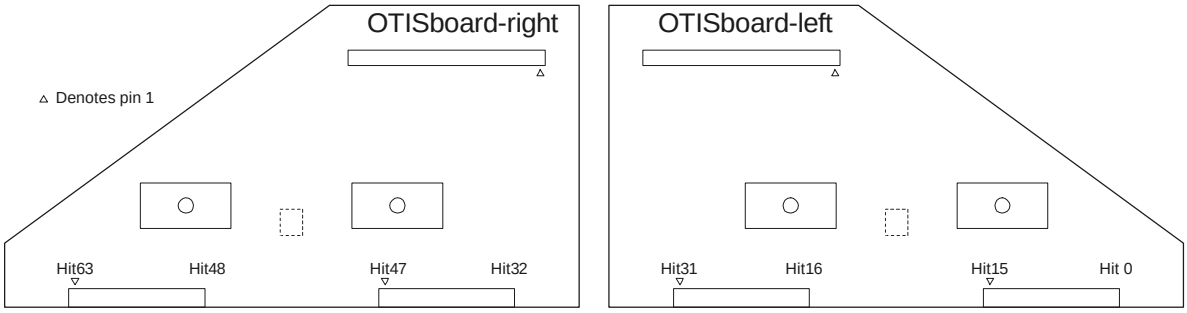

Figure 3: OTIS Boards viewed on the component side

Via the thick inner layers, the heat generated by the OTIS will be conducted over the whole board and to the surface next to the mounting holes. The OTIS board will be mounted on a cooling base; given a dissipation of 0.7W , a λ_{copper} of 300 W/mK and a λ_{epoxyr} of 0.2 W/mK the estimated temperature drop from OTIS to cooling base is about 25 degrees.

The Board ID (ID(11:7)) can be set by smd resistors on the pads next to the OTIS but on the component side (see figure 4). Each bit needs one resistor that can be placed left or right. If the resistor is placed on the left side, the corresponding ID bit will be '0', placed on the right side it will be a '1'.

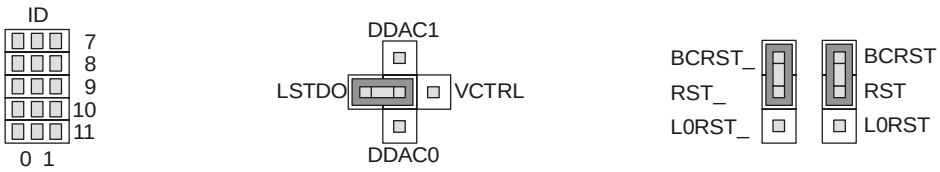

Figure 4: Board ID and jumper settings

The Reset and Test jumpers are also shown in Figure 4. The Reset(RST) is an LVDS signal and needs two jumpers connecting to the same signal (default Bunch Count Reset (BCRST)). The Test jumper connects one of the outer pins (test signals) to the center pin (testpad).

Because the pin numbering of the ASDBLR connector is not straightforward, the front view and footprint is given in figure 5.

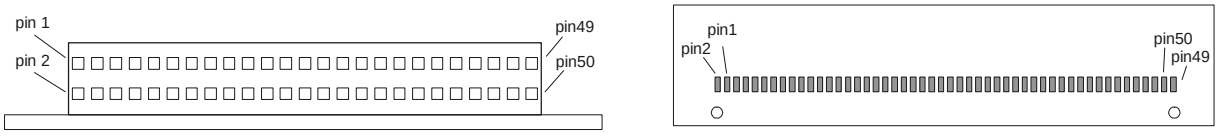

Figure 5: Front view and Footprint of the ASDBLR connector

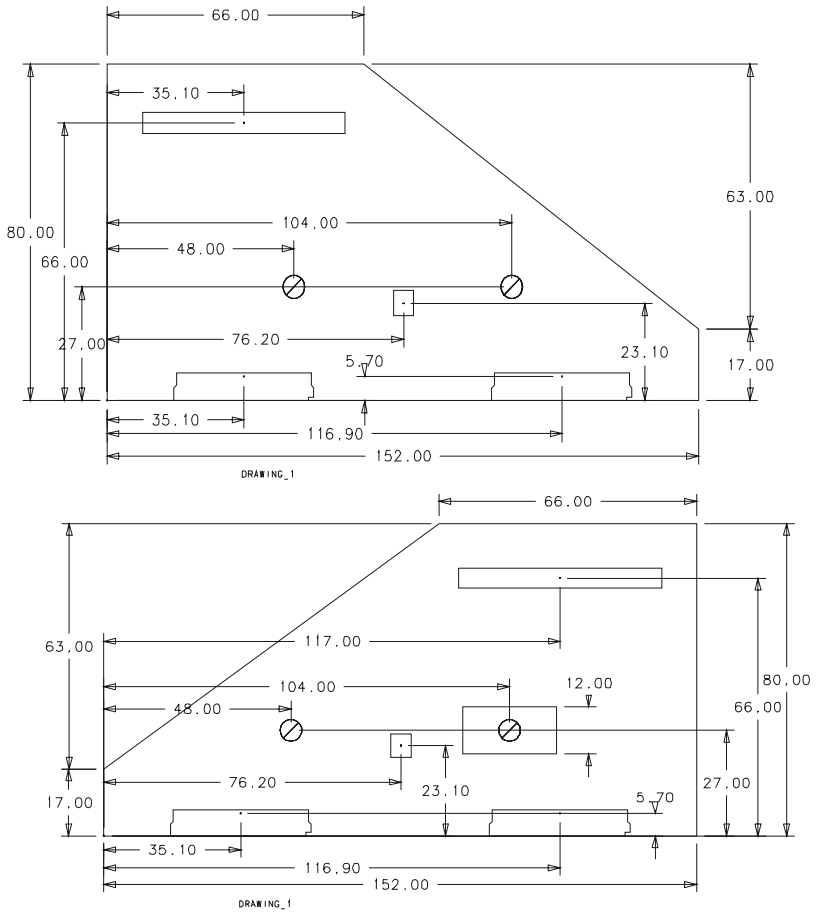

Figure 6: Dimensions of the OTIS boards

3. Components

A list of the components used is given in Table 1. The two 500nH coils to filter the OTIS VDD and VDDA are integrated in the PCB. The resistance of the coils is about 0.2 Ohm.

description	part number	geometry	count
buffer capacitor	10uF 10V Y5V	so1206	4
decoupling capacitor	100nF X7R	so0603	18
resistor	2K2	so0603	4
resistor	33 ohm	so0603	10
resistor	120 ohm	so0402	40
reference diodes	LM385BYZ2.5	sot23	2
LVDS receivers	DS90LV048ATMTC	mtc16	3
TDC	OTIS 1.0	chip 5.1x6 mm	1
connector 50s	SFMH_125_02_L_D_LC	34.67x6.22x3.43	2
connector 80s	SMS_140_01_G_D	50.8x5.59x8.51	1

Table 1: Parts List of the OTIS Board

4. Connector Pin Out

Pin nr	Signal	Pin nr	Signal
1	+3V	2	+3V
3	GND	4	GND
5	-3V	6	-3V
7	GND	8	GND
9	+2.5V	10	+2.5V
11	OtisN_Adr0	12	OtisN_Adr1
13	OtisN_Adr2	14	LocAdr3
15	LocAdr4	16	LocAdr5
17	Loc_Adr6	18	GND
19	TestPad	20	NC
21	I2cData	22	I2cClk
23	GND	24	GND
25	L0Acc_p	26	L0Reset_p
27	L0Acc_n	28	L0Reset_n
29	GND	30	GND
31	TstPlsEv_p	32	TstPlsOd_p
33	TstPlsEv_n	34	TstPlsOd_n
35	GND	36	GND
37	BCntRes_p	38	Clk_p
39	BCntRes_n	40	Clk_n
41	GND	42	GND
43	NC	44	Data0
45	NC	46	Data1
47	NC	48	Data2
49	NC	50	Data3
51	NC	52	Data4
53	NC	54	Data5
55	NC	56	Data6
57	NC	58	Data7
59	GND	60	GND
61	PuRst_	62	GND
63	WpWrap	64	RpWrap
65	TempMonL	66	TempMonR
67	NC	68	NC
69	GND	70	GND
71	+2.5V	72	+2.5V
73	GND	74	GND
75	-3V	76	-3V
77	GND	78	GND
79	+3V	80	+3V

Table 2: AUX/GOL Board Connector Pin Out

Pin nr	Signal	Pin nr	Signal
1	+3V	2	+3V
3	GND	4	GND
5	-3V	6	-3V
7	GND	8	GND
9	Hit31_n	10	Hit31_p
11	Hit30_n	12	Hit30_p
13	Hit29_n	14	Hit29_p
15	Hit28_n	16	Hit28_p
17	Hit27_n	18	Hit27_p
19	Hit26_n	20	Hit26_p
21	Hit25_n	22	Hit25_p
23	Hit24_n	24	Hit24_p
25	Hit23_n	26	Hit23_p
27	Hit22_n	28	Hit22_p
29	Hit21_n	30	Hit21_p
31	Hit20_n	32	Hit20_p
33	Hit19_n	34	Hit19_p
35	Hit18_n	36	Hit18_p
37	Hit17_n	38	Hit17_p
39	Hit16_n	40	Hit16_p
41	GND	42	GND
43	TestPlseEvL	44	TestPlsOdL
45	VThresh3	46	Vthresh2
47	TempmonL	48	GND
49	GND	50	GND

Table 3: ASDBLR Board Left Connector Pin Out

Pin nr	Signal	Pin nr	Signal
1	+3V	2	+3V
3	GND	4	GND
5	-3V	6	-3V
7	GND	8	GND
9	Hit15_n	10	Hit15_p
11	Hit14_n	12	Hit14_p
13	Hit13_n	14	Hit13_p
15	Hit12_n	16	Hit12_p
17	Hit11_n	18	Hit11_p
19	Hit10_n	20	Hit10_p
21	Hit9_n	22	Hit9_p
23	Hit8_n	24	Hit8_p
25	Hit7_n	26	Hit7_p
27	Hit6_n	28	Hit6_p
29	Hit5_n	30	Hit5_p
31	Hit4_n	32	Hit4_p
33	Hit3_n	34	Hit3_p
35	Hit2_n	36	Hit2_p
37	Hit1_n	38	Hit1_p
39	Hit0_n	40	Hit0_p
41	GND	42	GND
43	TestPlseEvR	44	TestPlsOdR
45	Vthresh1	46	Vthresh0
47	TempmonR	48	GND
49	GND	50	GND

Table 4: ASDBLR Board Right Connector Pin Out

5. References

[1] The OTIS Reference Manual Version 1.0
Harald Deppe, Uwe Stange, Ulrich Trunk, Ulrich Uwer
Physikalisches Institut Universität Heidelberg

[2] Auxiliary Board for the Outer Tracker
Ad Berkien, Tom Sluijk, Ulrich Uwer, Dirk Wiedner, Albert Zwart
Physikalisches Institut Universität Heidelberg – NIKHEF Amsterdam

[3] ASDBLR Board
t.b.a

[4] How to connect the I2C-Bus from Service-box to Front-End Modules
Albert Zwart
NIKHEF Amsterdam

6. Apendix

Schematics
Bill Of Materials
Artworks OTIS board-left
Artworks OTIS board-right