The OTIS Reference Manual

Harald Deppe, Uwe Stange,*
Ulrich Trunk,† Ulrich Uwer

Physikalisches Institut Universität Heidelberg

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Abstract

This document describes the port definitions, electrical specifications, modes of operation and programming sequences of the OTIS TDC. The chip is developed for the Outer Tracker of the LHCb experiment. OTIS1.0 is the first full-scale prototype of this 32 channel TDC and has been submitted in April 2002 in a standard 0.25μm CMOS process. Within the clock driven architecture of the chip a DLL provides the reference for the drift time measurement. The drift time data of every channel is stored in the pipeline memory until a trigger decission arrives. A control unit provides memory and trigger management and handles data transmission to the subsequent DAQ stage. The current chip version is OTIS1.2.

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*stange@kip.uni-heidelberg.de
†trunk@kip.uni-heidelberg.de

1 Document and Chip Version History

Document Version	Date	Author	Description
0.5	17.06.2002	U.S.	document created
0.7	21.06.2002	U.S.	typos, electrical specs
1.0	24.09.2002	U.S.	1st public version
1.1	06.02.2004	U.T.	include OTIS1.1
1.2	09.08.2004	U.S.	include OTIS1.2
Check http://wwwasic.kip.uni-heidelberg.de/lhcbot/ for the latest version			

Chip Version	Submission Date	Changes relating to previous version
OtisDLL1.0	19.10.2000	DLL prototype
OtisMEM1.0	21.03.2001	DLL & Memory prototype (pipeline)
BeetleSR1.0[1]	18.05.2001	Memory prototype (derandomizing buffer)
OTIS1.0	15.05.2002	First full-scale prototype
OTIS1.1	10.11.2003	TDC fix & various other improvements
OTIS1.2	24.05.2004	Integration of MultiHit mode

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[1] We greatly appreciate that we were allowed to join this chip submission of the Beetle-Group.

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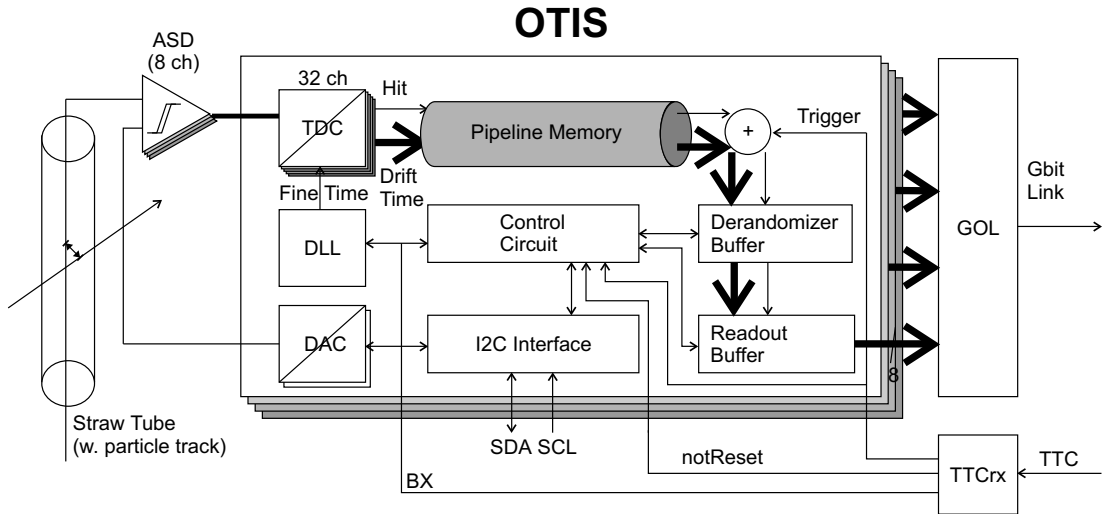
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Figure 1: OTIS block diagram

2 Conventions within this Document

- This document deals with versions 1.0 to 1.2 of the OTIS chip.

- Registers are 8 bit wide.

- The numbering of registers and indexing into single registers starts counting from zero. For example `TestReg[7:0] = 8'b00000001` stands for a register called `TestReg` which is loaded with the hexadecimal value `0x01`. The rightmost bit within this register (i.e. bit number 0) is the least significant bit (LSB). In this example the LSB carries the value 1, all other bits including the most significant bit (MSB) are 0.

All exeptions from these conventions are noted.

3 Chip Architecture

The OTIS chip for the outer tracker of the LHCb experiment is developed at the University of Heidelberg. A first full-scale prototype of the chip has been submitted in April 2002. OTIS is a 32 channel TDC (Time to Digital Converter) manufactured in a standard 0.25μm CMOS process.

In the LHCb experiment the signals from the straw tubes of the Outer Tracker are digitised with discriminator chips of the ASD family [1]. The OTIS TDC measures the arrival time of the ASD signals with respect to the LHC clock. In the detector it is forseen to combine the output data of 4 OTIS chips as input to the GOL serialiser chip [2]. The GOL chip then transmits data optically to the off detector electronics at 1.2 Gbit/s net data rate. Figure 1 depicts how the OTIS chip is integrated into the Outer Tracker front end electronics. The data processing of the OTIS TDC is clock driven: the chip operates synchronous to the 40MHz LHC clock. Main components of the OTIS chip are the TDC core, consisting of DLL, hit register and decoder and the pipeline plus derandomizing buffer. The last two are dual ported SRAM memories to cover the L0 trigger latency [3] and to cope with trigger rate fluctuations. A control algorithm provides memory management and trigger handling. In addition the chip integrates several Digital to Analog Converters (DACs) which provide the threshold voltages of the discriminator chips. A standard I^{2}C interface [4] is used for setup and slow control. The DLL (Delay Locked Loop) is a regulated chain of 32 delay elements consisting of two stages each. Since the output of every stage is used, the theoretical bin size is 390ps. Furthermore, 64 bins require 6 bit drift time encoding

Name	Explanation	Min.	Typ.	Max.	Unit
vdd, vdd_*[2]	Positiv digital supply	2.2	2.5	2.7	V
vdda	Positiv analog supply	2.2	2.5	2.7	V
gnd	Detector ground	-0.2	0	0.2	V

Table 1: DC characteristics of the OTIS chip

per channel. The drift time data plus hit mask and status information is stored in the 240 bit wide pipeline memory. The capacity of the memory is 164 words to allow a maximum latency of 160 clock cycles. If a trigger occurs the corresponding data words are transferred to the derandomizing buffer which is able to store data for up to 16 consecutive triggers. The control unit's task is to read out the data of each triggered event within 900ns via an 8 bit wide bus running at 40MHz.

OTIS1.1 has been submitted for manufacturing in November 2003. It features a modified TDC to overcome the problem of missing codes for chip version OTIS1.0. Other changes visible to the user include changed read out header bits and a modified register map. Additionally the LVDS data output pads have been changed to differential CMOS outputs. Further modifications include buffers for the ASD threshold outputs and a new implementation of the control algorithm as well as the possibility of slow data output via I^{2}C interface.

The control algorithm of OTIS1.2 (submitted in May 2004) finally provides the MultiHit operation mode. Other changes with respect to its predecessor chip will result in a smaller DNL figure and smaller offset voltage spread for the ASD threshold voltages. Compared to OTIS1.1, the chip size changed. This implicates changes in pad positions, however the arrangement of the pads did not change.

4 Electrical Specifications

4.1 DC Characteristics

The OTIS chip needs two positiv operating voltages: analog and digital supplies of nominal +2.5V with respect to Ground (gnd, 0V) each. The operational range of vdda and vdd is predetermined by the manufacturing process. Minimum, maximum and nominal values for the supply voltages are listed in table 1.

All supply voltages should be thoroughly blocked against gnd (e.g. a 100nF ceramic capacity in parallel with a 68μF tantal capacity between vdd/vdda and gnd). The blocking capacitors should be placed as close as possible to the chip.

After powering the chip, the OTIS chip performs a power up reset (c.f. chapter 6.1). In this state the power consumption is 185mA (or 463mW). Power consumption rises to 220mA (or 550mW) when operating the chip at the nominal LHC bunch crossing frequency of 40MHz. It is not yet verified if power consumption rises while the chip transmits data to the following DAQ stage. But if so, it is expected that the power consumption will stay well below 1W which is an estimation for the upper bound of the power consumption per chip [5].

4.2 AC Characteristics

The OTIS chip has 3 different types of I/O pads. The signal levels for these pads are given in table 2.

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[2]any power supply net having a name starting with vdd_

	logic 0			logic 1			Unit
I^{2}C (OTIS1.0)							
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
I^{2}C (OTIS1.1 & OTIS1.2)							
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	7.0	2.5	V
output	—	—	0.0	—	—	2.5	V
CMOS							
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.4	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
LVDS (100Ω termination)							
	offset voltage			differential voltage			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	0.0	2.5	1.2	0.1	2.5	0.2	V
output	—	—	1.02	—	—	1.38	V

Table 2: Specification of signal levels

5 Slow Control

5.1 I^{2}C Interface

The slow control interface of all OTIS chips is a standard mode I^{2}C slave device capable to transfer data at a transfer rate of 100kbit/s. The chip address, necessary to access a single device on the I^{2}C bus, is assigned by means of the address pads ID<0> (LSB) to ID<6> (MSB) for OTIS1.0. At chip versions OTIS1.1 & OTIS1.2 these pads are ID<12> (LSB) to ID<18> (MSB). The ID pads (see tables 7, 8 and 9) contain internal pull down resistors. Note that the OTIS I^{2}C interface does not respond to reserved I^{2}C addresses. Reserved addresses are 7'b0000XXX and 7'b1111XXX. In other words, valid addresses range from 8 to 119.

The internal registers can be accessed via the pointer register. This register contains the address of the following register to be written to or read from. The pointer is internally incremented by 1 after each transferred data frame. Thus registers with adjacent addresses are accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Figure 2 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit first. In write mode the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data byte(s). After the transmission of one data frame, the pointer addresses the next register because of its auto-incrementing function. The transfer of the pointer register is mandatory in write mode. For read mode there are two possibilities:

- Preset pointer: Data output immediately starts after initialization and transmission of the chip address. The pointer has been set in a previous transfer.

- New pointer: After initialization and transfer of the chip address, a new pointer byte gets programmed. Then, after re-initialization and transmission of the chip address, data output starts.

DRAFT DRAFT DRAFT DRAFT DRAFT DRAFT DRAF

Write mode:

S	Slave address	R/W: 0	A	Pointer Byte	A	D7	D6	D5	D4	D3	D2	D1	D0	A	(...)	P

Read mode:

Preset pointer

S	Slave address	R/W: 1	A	D7	D6	D5	D4	D3	D2	D1	D0	(...)	A	P

Pointer set followed by immediate read−out

S	Slave address	R/W: 0	A	Pointer Byte	A	Sr	Slave Address	R/W: 1	A	D7	D6	D5	D4	D3	D2	D1	D0	A	(...)	P

Figure 2: I^{2}C-bus write and read sequences for accessing registers on the OTIS chip
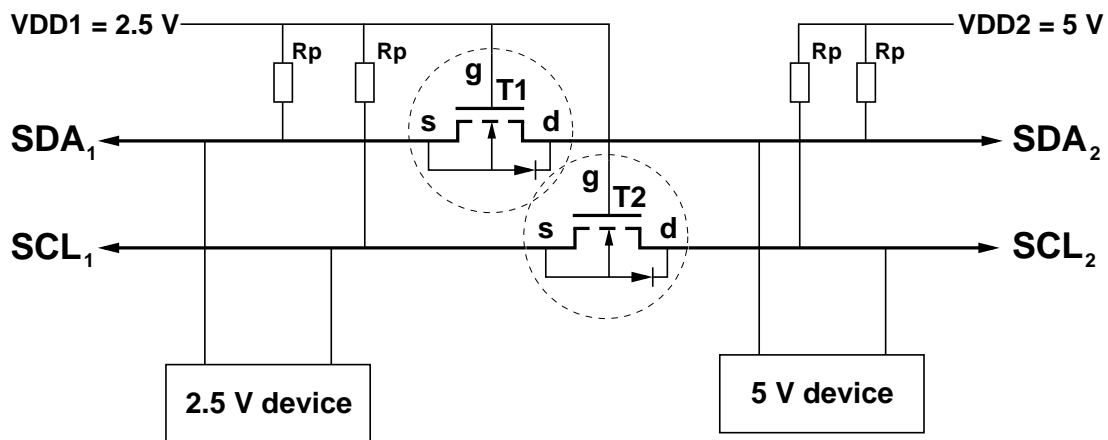
Figure 3: Bidirectional level shifter circuit (BSN20 from Philips Semiconductors)

Commercially available I^{2}C devices usually operate at $+3.3$V or $+5$V. To interconnect these devices with the OTIS I^{2}C interface, a bidirectional level shifter is required. A simple solution is the use of a discrete MOS-FET for each bus line [6]. Figure 3 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

The chips `OTIS1.1` and `OTIS1.2` both feature a 5V compliant I^{2}C interface. Thus the level shifter circuit depicted in figure 3 can be omitted as the chips directly interface with commercial 5V or 3.5V I^{2}C controllers. The ASIC laboratory Heidelberg uses the ELV I^{2}C-PC-Interface [7] to connect the I^{2}C bus to a personal computer. A graphical user interface that uses the ELV box to allow writing to and reading from all OTIS registers is available for download (requires LabVIEW) [8].

5.2 Configuration Registers

5.2.1 Configuration Registers of `OTIS1.0`

`OTIS1.0` provides a set of 20 status and configuration registers. Table 3 summarizes name, address, type and bit content of each register. In principle there are only two types of registers: read only registers and registers that allow read and write access. But the registers of type read only divide into registers that hold static and dynamic content. Those status registers that provide read only access to dynamic content can be resetted to `0x00` by an external I^{2}C write access. The data byte of this write access is discarded. Those resettable registers are called read only since their dynamic content only depends on the status of the chip and internal counters.

Address	Name	Type	Bit Assignment/Description	
0	PosID	read only	7 - 5	0
			4 - 0	Position ID
1	I2CID	read only	7	0
			6 - 0	I2CID[6:0]
2	StatusReg	read only	7 - 4	0
			3	SEU[3]
			2	Buffer overflow
			1	DLL lock lost[3]
			0	Memory selftest failed
3	RecievedT	read only	7 - 0	Number of recieved trigger
4	RejectedT	read only	7 - 0	Number of rejected trigger
5	ReadMode	read/write	7 - 4	X
			3	Truncation[3]
			2	SuppressZero / notSingleHit[3]
			1 - 0	Number of Events per trigger
6	DebugMode	read/write	7 - 6	X
			5 - 3	signal select
			2	Pads on/off
			1	Playback/SFT
			0	Debug mode on/off
7	Latency	read/write	7 - 0	Latency register
8 - 11	ChannelMask	read/write	7 - 0	Channel mask register
12, 13	DLLDAC	read/write	7 - 0	DLL DAC register
14 - 17	ASDDAC	read/write	7 - 0	ASD DAC register
18, 19	PBData	read/write	7 - 0	Playback data

Table 3: OTIS1.0 status and configuration registers

DebugMode[5:3]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Read out sequence	Start of sequence	End of sequence
3'b100	Derandomizing buffer fill level	Buffer empty	Buffer full

Table 4: Status information (OTIS1.0)

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[3]not implemented on OTIS1.0.

- `POSID, I2CID:` These two registers provide 12 bits of TDC identification number. `POSID` and `I2CID` are read only and their content is determined through the TDC ID pads 1, 138 - 141, and 2 - 8 respectively (see figure 13 and table 7). The `I2CID` register holds redundant data as the I^{2}C ID is known prior to any I^{2}C read access.

- `StatusReg:` The `StatusReg` register provides information about failed memory self test (bit number 0 set) and buffer overflow (bit number 2 set) in case of a full derandomizing buffer. Detection of SEU or lost DLL lock is not implemented in `OTIS`1.0. Status information can be resetted through I^{2}C write access to this register.

- `RecievedT, RejectedT:` The OTIS chip counts the number of recieved and rejected L0-trigger signals since last L0-reset. 8 LSBs of these counters are available through `RecievedT` and `RejectedT` registers. The counter registers can be resetted through I^{2}C write access.

- `ReadMode:` As `OTIS`1.0 only features the `SingleHit` operation mode, bits number 3 to 7 of the `ReadMode` register are ignored. Bit number 2 selects the operation mode and again setting this bit to 0 is the only reasonable choice. The bits number 0 and 1 combined togehter represent the number of data sets that will be searched for hits upon incoming trigger signals. Note that the search depth figure starts counting from zero. Changes in the `ReadMode` register only take effect after a L0 reset signal.

- `DebugMode:` Several internal status signals can be monitored at the two service pads `WPWrap` and `RPWrap`. The signals to observe can be selected with bits number 3 - 5 of the `DebugMode` register. Valid bit combinations are listed in table 4. `DebugMode[2]=1` switches off signal monitoring, i.e. monitoring is enabled by default. The bits `DebugMode[1:0]` are used to select and activate one out of two special operation modes: `DebugMode[1:0]=2'b11` selects memory selft test mode, `DebugMode[1:0]=2'b01` selects play back mode and `2'bX0` switches debug mode operation off.

- `Latency:` The content of the `Latency` register defines the latency, i.e. the distance between memory write and read pointer. `Latency[7:0]=0x00` sets the distance to 1 (maximum is `0xA3`). Changes in the `Latency` register only take effect after a L0 reset.

- `ChannelMask:` The 32 bits of the 4 `ChannelMask` registers individually switch on or off single channels of the OTIS chip. To switch off a channel, the corresponding bit must be set to 1, i.e. all channels are switched on by default.

- `DLLDAC, ASDDAC:` Interface to the (unbuffered) DLL- and ASD-DACs.

- `PBData:` Interface to 2 shift registers that are used as storage for play back data sets.

5.2.2 Configuration Registers of `OTIS`1.1 & `OTIS`1.2

`OTIS`1.1 & `OTIS`1.2 provide a set of 66 status and configuration registers. Table 5 summarizes name, address, type and bit content of each register. In principle there are only two types of registers: read only registers and registers that allow read and write access. But the registers of type read only divide into registers that hold static and dynamic content. Those status registers that provide read only access to their dynamic content can be resetted to `0x00` by an external write access via the I^{2}C interface. The data byte of this write access is discarded. Those resettable registers are called read only since their dynamic content only depends on the status of the chip or chip internal counters.

Address	Name	Type		Bit Assignment/Description
0	PosID0	read only	7 - 4	0
			3 - 0	TDCID[11:8]
1	PosID1	read only	7 - 0	TDCID[7:0]
2	I2CID	read only	7	0
			6 - 0	I2CID[6:0]
3	Revision	read only	7 - 6	0
			5 - 3	Chip Version (3'b001)
			2 - 0	Chip Revision (3'b001 resp. 3'b010)
4	StatusReg	read/write	7 - 4	0
			3	SEU
			2	Buffer overflow
			1	DLL lock lost
			0	Memory selftest failed
5	RecievedT	read/write	7 - 0	Number of recieved triggers
6	RejectedT	read/write	7 - 0	Number of rejected triggers
7	EventID	read only	7 - 0	EventID
8	SEUCntr	read/write	7 - 0	Number SEUs detected
9	ReadMode	read/write	7	0
			6	Previous drift time
			5	DataValid (1=on, 0=off)
			4	Comma (1=on, 0=off)
			3	Truncation[4]
			2	MultiHit[4] / SingleHit
			1 - 0	Number of Events per trigger
10	DebugMode	read/write	7 - 5	Service pad signal select (see table 6)
			4	Servic pads (1=on, 0=off)
			3 - 1	Debug modes:
				3'b001 ReadFIFO on
				3'b010 SFT autoBankSelect
				3'b011 SFT PadBankSelect
				3'b100 PB autoBankSelect w/o FIFO
				3'b101 PB autoBankSelect w FIFO
				3'b110 PB PadBankSelect w/o FIFO
				3'b111 PB PadBankSelect w FIFO
			0	Debug mode (1=on; 0=off, ignore bits 3-1)
11	DLLReg	read/write	7 - 1	0
			0	DLL reset (1=active, 0=off)
12	Latency	read/write	7 - 0	Latency register
13	Offset	read/write	7 - 4	BX counter wrap-around
			3 - 0	BX counter offset
14	Reserved0	read/write	7 - 0	Without any functionality
15 - 18	ChannelMask	read/write	7 - 0	Channel mask register
15	Reserved1	read/write	7 - 0	Without any functionality
20 - 23	DLLDAC	read/write	7 - 0	DLL DAC register
24 - 27	ASDDAC	read/write	7 - 0	ASD DAC register
28, 29	PBData	read/write	7 - 0	Playback data
30 - 65	ReadFIFO	read/write	7 - 0	Slow event data readout

Table 5: OTIS1.1/1.2 status and configuration registers

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[4]not implemented on OTIS1.1

- `POSID0`, `POSID1`: These two registers provide 12 bits of TDC identification number. `POSID` and `POSID1` are read only and their content is determined through the TDC ID pads 5 - 15 and 22 (see table 8 and 9).

- `I2CID`: This register provides 7 bits of I^{2}C ID number. `I2CID` is read only and its content is determined through the TDC ID pads 23 - 29 (see table 8 and 9). The `I2CID` register holds redundant data as the I^{2}C ID is known prior to any I^{2}C read access.

- `Revision`: Read only register representing chip version and revision number:
  OTIS1.1: `Revision[7:0]=8'b00001001` — OTIS1.2: `Revision[7:0]=8'b00001010`

- `StatusReg`: The `StatusReg` register provides information about failed memory self test (bit number 0), lost DLL lock (1), buffer overflow in case of a full derandomizing buffer (2) and detection of a SEU within the slow control (3). Status information can be resetted through I^{2}C write access to this register.

- `RecievedT`, `RejectedT`, `EventID`: The OTIS chip counts the number of accepted and rejected L0 trigger signals as well as the number of completed data output sequences. 8 LSBs of each counter are available through the `RecievedT`, `RejectedT` and `EventID` registers. The first two counter registers can be resetted through I^{2}C write access. `EventID` register gets resetted via the L0 EventID reset signal. If there is no pending read out (i.e. the derandomizing buffer is empty) and none of the counter registers has been individually resetted, then `RecievedT = EventID + RejectedT` (except for possible counter overflows).

- `SEUCntr`: Interface to a 8 bit counter that stores the number of detected SEUs. Resettable through I^{2}C write access.

- `ReadMode`: Sets the operation mode of the OTIS chip. As OTIS1.1 still lacks the `MultiHit` mode, the only reasonable choice for bit number 2 is `ReadMode[2]=0`. For chip version OTIS1.2 `ReadMode[2]=1` selects `MultiHit` operation mode. If operating in `MultiHit` mode, bit number 3 selects optional truncation of the data output stream to 900ns in order to keep all chips synchronised.Bit number 4 selects whether or not to precede every non-consecutive data output sequence with a comma byte (`0xFF`). If bit number 5 is set, then every data output sequence gets anounced through the `DataValid` pad. Bits number 0 and 1 combined togehter represent the number of data sets that will be searched for hits upon incoming trigger signals. Note that the this search depth figure starts counting from zero. Changes in the `ReadMode` register only take effect after a L0 reset signal.

- `DebugMode`: Several internal status signals can be monitored at the two service pads `WPWrap` and `RPWrap`. The signals to observe can be selected with bits number 5 - 7 of the `DebugMode` register. Valid bit combinations are listed in table 6. `DebugMode[4]=1` switches off signal monitoring, i.e. monitoring is enabled by default. The bits `DebugMode[3:1]` are used to select several special operation modes. These are memory self test and play back mode (as for OTIS1.0). But versions 1.1 and 1.2 of the OTIS chip additionally offer the possibility to steer data set selection from outside the chip. A third debug feature is the possibility to store a complete data output sequence in a set of FIFO registers. These registers are accessable via I^{2}C interface. Refer to tables 5 and 6 on how to select and activate the different debugging features.

- `DLLReg`: Setting `DLLReg[0]=1` executes a DLL reset.

- `Latency`: The content of the `Latency` register defines the latency, i.e. the distance between memory write and read pointer. `Latency[7:0]=0x00` sets the distance to 1 (maximum is `0xA3`). Changes in the `Latency` register only take effect after a L0 reset.

- `Offset`: The content of the `Offset` register provides the possibility to fine tune the behaviour of the bunch crossing counter. Bits 4 - 7 allow adjustment of the overflow mark

DebugMode[7:5]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Playback info	PB mode enabled	BankSelect
3'b100	Read out sequence	Start of sequence	End of sequence
3'b101	Derandomizing buffer fill level	Buffer empty	Buffer full
3'b110	ReadFIFO information	FIFO enabled	FIFO has data
3'b111	DLL lock info	VCtrl $\leq$ DLLDAC3	VCtrl $\geq$ DLLDAC0

Table 6: Status information (OTIS1.1/1.2)

(3556 - 3571) of the 12 bit wide bunch crossing counter: Offset[7:4]=4'b0111 selects the nominal value 3563. The bits number 0 - 3 allow adjustment of the first BX number after a BX reset: BX counter starts counting from zero after a L0 Reset. A BX reset sets the bunch crossing number to Latency + Offset[3:0]. Changes in the Offset register only take effect after a L0 reset.

- ChannelMask: The 32 bits of the 4 ChannelMask registers individually switch on or off single channels of the OTIS chip. To switch off a channel, the corresponding bit must be set to 1, i.e. all channels are switched on by default.

- DLLDAC, ASDDAC: Interface to the DLL- and ASD-DACs.

- PBData: Interface to 2 shift registers that are used as storage for play back data sets.

- ReadFIFO: Interface to the FIFO registers that are able to store one complete data output sequence.

6 Modes of Operation

6.1 Reset

OTIS1.0: If pad number 37 (see table 7) is coupled capacitively (10nF - 100nF) to gnd, the chip performs a power up reset. Within this power up reset all status and configuration registers are set to 0 and the I²C interface is set into the idle state, thus the chip is ready for programming. The duration of the power up reset varies with the capacity connected to the PwrUpReset pad.

The pads number 35 and 36 are used to execute a fast reset. This is needed to synchronise the OTIS chip to the LHC bunch crossing clock or to reset the DLL if lock was lost. OTIS1.0 initiates a fast reset if the LVDS pad recieves levels representing zero. There is no timing requirement between clock and reset which must be met as long as it is guaranteed that the clock is running while the chip gets resetted.

OTIS1.1 & OTIS1.2: The functionality of the PwrUpReset pad (number 130 in tables 8 and 9) was slightly modified: After the expiry of the RC-delay described above, an additional delay of 32 clock cycles was introduced to assure the locking of the DLL, which is only guaranteed if the clock is running when PwrUpReset or DLLReset are released. The latter (pad number 165 in tables 8 and 9)was introduced to independently reset the DLL. The L0Reset (pad numbers 135 & 136 in tables 8 and 9) terminates any ongoing readout, resets the fast control to the idle state, resets all memory and derandomiser buffer pointers to zero and discards all pending triggers. However, it does not reset any on-chip counters. Thus the EVReset and BXReset signals (pad numbers 166

to 169 in tables 8 and 9) were introduced to perform this task on the Event- and BX-counters respectively.

6.2 Normal Operation Mode

OTIS1.0: To select normal (or `SingleHit`) operation mode, the content of the `ReadMode` register must be set to `8'bXXXXXOxx`. The upper 5 bits have no functionality and the lower 2 bits determine the search depth (in BX) per trigger.

OTIS1.1: This chip version still lacks the `MultiHit` read mode. This is why the lower 4 bits of the `ReadMode` register show the same functionality as for chip version `OTIS1.0`. With bits number 4 and 5 `Comma` and `DataValid` can be switched on and off. If the `comma` bit is set to 1, every non-consecutive data output sequence is preceded with a `comma` byte (`0xFF`). The `DataValid` bit determines wheter or not every ongoing data output sequence gets anounced through the `DataValid` pad. Bit number 6 of the `ReadMode` register determines the drift time figures for unhit channels during data output. If set to 0, unhit channels show blanked out drift times: `8'b11000000`. If set to 1, unhit channels still carry the `No-Hit` information, but possibly show remainding drift times from previous hits: `8'b11xxxxxx`. This feature is intended to provide more detailed insights into on-chip data flows.

OTIS1.2: For chip version `OTIS1.2` only bit number 7 of the `ReadMode` register is not used. Now bit number 2 allows selection of `SingleHit` or `MultiHit` operation mode. For `MultiHit` mode this bit must be set to 1. While in `MultiHit` mode, the bit number 3 of the `ReadMode` register turns data stream truncation on or off. In contrast to the `SingleHit` mode, the `MultiHit` mode allows transmission of up to 3 drift times per channel and trigger. Figures 4 and 5 show how the output data is formatted in the two operation modes. To simplify matters, drift time data is byte-aligned for `MultiHit` mode too: the two most significat bits are zero. Figures 6 (`OTIS1.0`) and 7 (`OTIS1.1` & `OTIS1.2`) show how status information is organised in the header which preceeds every output data frame.

Since `OTIS1.1` a newly introduced header bit indicates the optional data stream truncation for `MultiHit` mode. The status bits `SFT`, `DLL lock lost` and `SEU` are ored to a single error bit. The `DLL lock lost` bit is set if the DLL's control voltage exceeds the voltage range given by the `DLLDAC` registers (20 upper limit, 23 lower limit). The two other `DLLDAC` registers are used to set the bias of the corresponding discriminators (21 upper limit, 22 lower limit), which controls their speed and sensitivity. Furthermore, 4 bits indicating the data frame's position in the readout stream (`EventID`) are added to the header data. Also the `buffer overflow` bit was changed to a sticky behaviour, such that it can be only cleard with a `LOReset` signal.

6.3 Debugging Features

The OTIS chips provide several debugging features. First of all test data can be written to the pipeline via the I^{2}C-interface. Additionally one can start a memory self test or one can select status information such as full or empty derandomizing buffer to be observable at the two service pads. To switch on `debug` mode, the bit number 0 of the `DebugMode` register must be set to 1.

- Playback mode
  Test (or play back) data can be written to the registers number 18 and 19 (resp. 28 and 29). If data is written to these registers via the I^{2}C interface, the pointer does not proceed to the next register address. In combination with the fact that the two `PBData` registers are organised as shift registers, it is possible to store two independent sets of drift time and hit information which are then alternately written to the pipeline.

- Memory self test
  If started, the memory self test performs integrity checks for memory in- and output. Run time information about the memory self test can be obtained from the two debug pads `WPWrap` and `RPWrap` (see tables 4 and 6). To exit from the memory self test, the user must clear bit number 0 of the `DebugMode` register.

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Output Data Format (`SingleHit` Mode)

Bit:	0..31	32..39	40..47	...	280..287
Data:	Header	Drift Time 0	Drift Time 1	...	Drift Time 31

Drift Time Encoding

Hit Position	Drift Time Encoding
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	11XXXXXX

Figure 4: `SingleHit` mode data format & drift time encoding

Output Data Format (`MultiHit` Mode, 1BX/Trigger)

Bit:	0..31	32..63	64..71	...	64+(8n)..71+(8n)
Data:	Header	1 Hitmask	Drift Time 0	...	Drift Time n

Output Data Format (`MultiHit` Mode, 2BX/Trigger)

Bit:	0..31	32..95	96..103	...	96+(8n)..103+(8n)
Data:	Header	2 Hitmasks	Drift Time 0	...	Drift Time n

Output Data Format (`MultiHit` Mode, 3BX/Trigger)

Bit:	0..31	32..127	128..135	...	128+(8n)..135+(8n)
Data:	Header	3 Hitmasks	Drift Time 0	...	Drift Time n

Figure 5: `MultiHit` mode data format

Header Data Format (OTIS1.0)

Byte	1		2		3		4
	MSB LSB	MSB	LSB	MSB	LSB	MSB	LSB
Bit No.	0..11	12,13	14..17	18..21	22,23	24..31	
Data	TDC ID	0	Status	RO	0	BX	

Selftest failed	Buffer overflow	DLL lock lost	Single Event Upset	Number of BX	Read Mode	Playback Busy
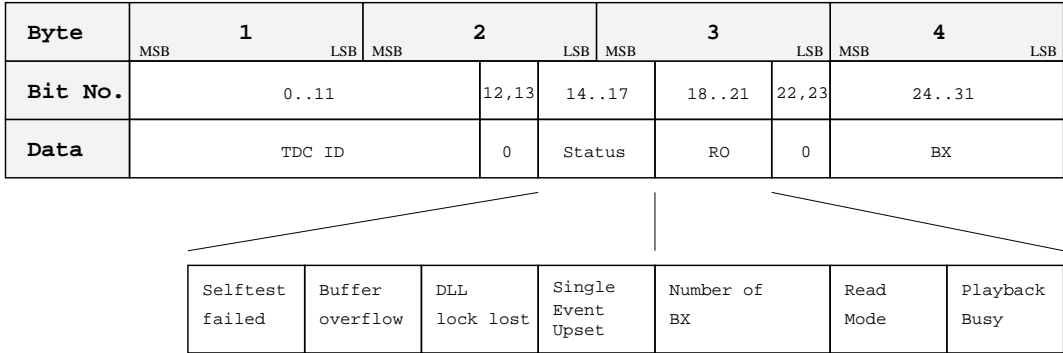
Figure 6: Header data format of OTIS1.0

Header Data Format (OTIS1.1/1.2)

Byte	1		2		3				4
	MSB LSB	MSB	LSB	MSB			LSB	MSB	LSB
Bit No.	0..11	12..16	17,18	19	20..23	24..31			
Data	TDC ID	RO	Err	0	Event-ID	BX			

Read Mode	Number of BX	Truncation	Playback	SFT, DLL, SEU	Buffer Overflow
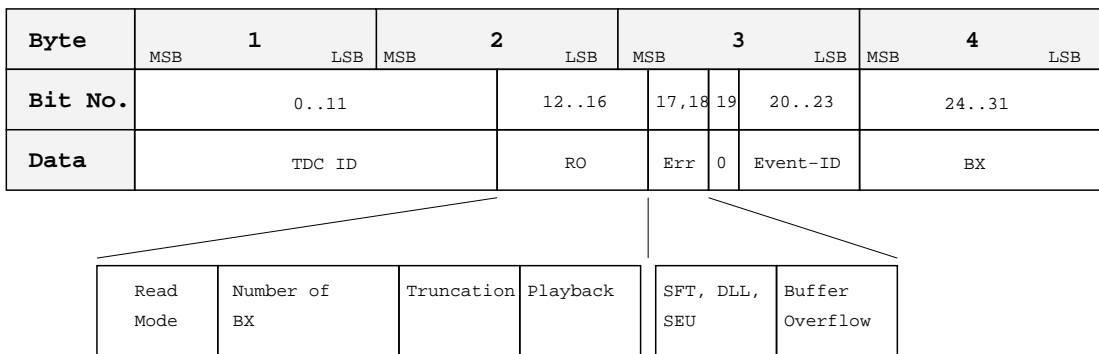
Figure 7: Header Data Format of OTIS1.1/1.2

Digital to Analog Converter

1.2kOhm load

DLL Lock Range

(Room Temperature)
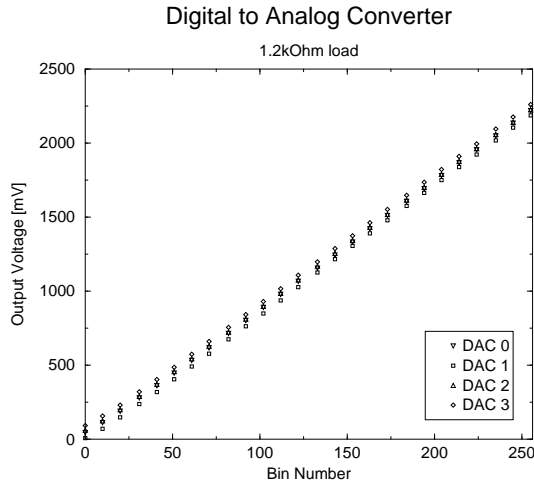
Figure 8: DAC Measurement
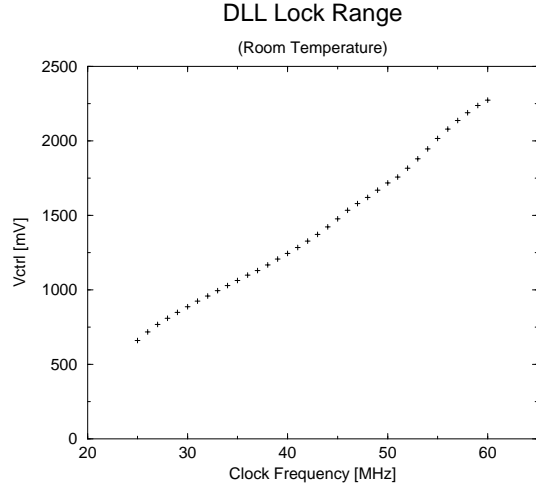
Figure 9: DLL Lock Range

To make status information visible at the pads `WPWrap` and `RPWrap`, the bit number 2 of the `DebugMode` register has to be set to 0. The different combinations of status signals can be set with bits number 3 to 5 of the `DebugMode` register. The possible combinations are listet in table 4.

`OTIS1.1` and `OTIS1.2` include basically the same debug features as `OTIS1.0`, which can be selected in the same way, except for changed register addresses and bit positions (c.f. tables 5 and 6). Additionally both chips offer the possibility to store one complete data output sequence in a set of registers organised as FIFO.

7 `OTIS1.1` Sample Measurements

Digital to Analog Converter
Figure 8 shows the behaviour of the 4 digital to analog converters which provide the threshold voltages for the ASD discriminator chips. The outputs of the DACs are now buffered and therefore able to drive currents up to 600μA. Figure 8 shows how the output voltages at an external load (1.2kOhm) vary with programming of the DAC registers. Extra design effort went into chip version `OTIS1.2` in order to decrease the spread in between all 4 channels (which is $\approx$80mV for `OTIS1.1`).

DLL Lock Range
Figure 9 combines data from 2 different measurements concerning the lock range of the DLL. The diagram shows the control voltage of the single delay elements against the LHC clock frequency. Data from 25MHz to 46MHz has been obtained with standard chip settings. The chip operated at a different supply voltage ($V_{dda} = 3.3$V instead of 2.5V) from 47MHz to 60Mhz. The resulting offset in V_{ctrl} has been taken into account for this summary. At room temperature and provided that reset is active befor clock is running, the DLL reaches its lock state for clock frequencies that range from 25MHz to 60MHz.

Data Output Sequence
A complete data output sequence for the `SingleHit` mode is shown in figure 10. The signals shown are `Trigger`, data output sequence start (`WP`) and stop (`RP`), `DataValid` and `Data 0` to `Data 7`. The trigger signal (see marker `G1`) starts data processing within the OTIS chip. Then, 3 clock cycles later (at marker `G2`) the actual data output sequence starts. In this special case, data output is preceded by a comma byte. After transmission of 4 header bytes, the triggered drift times follow. In this case none of the 32 drift time bytes contains valid drift time data:

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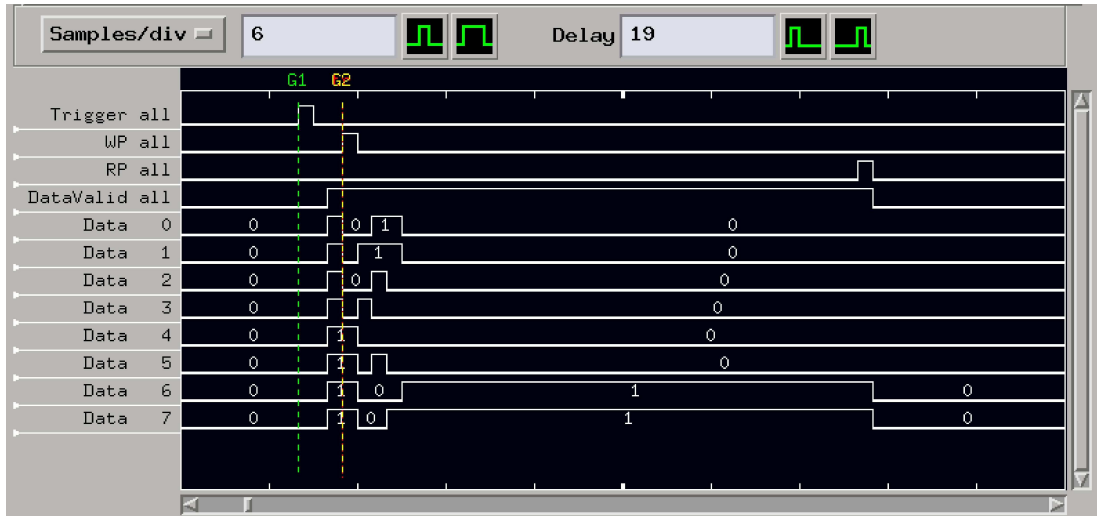
Figure 10: Data Output Sequence

the output is `0xC0` for all 32 channels. Note that in case of a comma byte, the `DataValid` signal is active for 37 clock cycles - the debug signals `ROStart` and `ROStop` only enclose 36 clock cycles.

Drift Time Measurement
Figure 10 shows the linear dependancy between input signal delay (x-axis) and drift times (y-axis) derived from the input signal. Drift time data contributing to this figure ranges from 0 to 63. Thus data only represents an overall drift time range of 25ns. In this diagram 0ns drift times belong to a input signal delay of 6ns and range to 24.9ns (resp. 30.9ns input delay). The drift time figures repeat below input signal delay of 6ns and above a delay of 30.9ns .

Differential Non-Linearity
To calculate a figure for the differential non-linearity, several million drift times derived from random input signals need to be stored and analysed. The DLL bin sizes can be calculated from the histogramm of all drift times. Now the difference in bin size of always two subsequent DLL bins can be calculated. But one needds to take into account that allways two bins of different size form one delay element of the DLL. A sample diagramm displaying bin size differences against the bin number is shown in figure 12. Now the sum of the biggest and (the absolut value of the) smallest bin size difference is called differential non-linearity. The data of diagram 12 results in a DNL of (1.25 ± 0.04)LSB or (489 ± 16)ps. The dominating contribution to the DNL originates from an unregulated dummy delay element at the beginning of the delay chain. As this dummy element is adjustable for the latest chip version too, the DNL figure is expected to be less than 1LSB for `OTIS1.2`.

8   List of known Problems and Bugs

- `OTIS1.0`
  - The data output pads (pads number 13 to 28) are implemented as LVDS pads though the serialiser chip GOL [2] requires single ended CMOS.
  - The memory self test shows a temperature dependency.
  - The measured drift times do not follow the detector signals arrival time linearily.

18
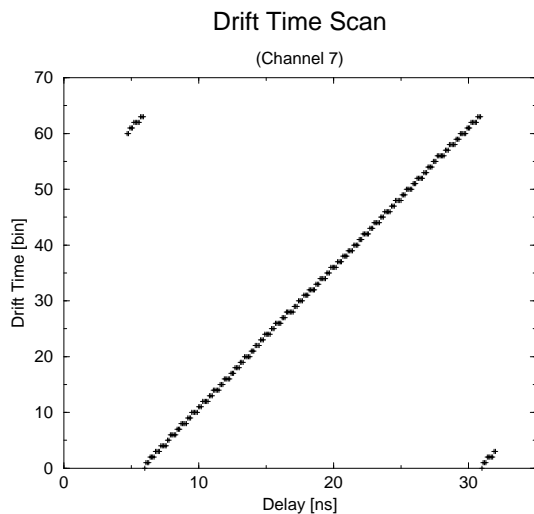
Figure 11: Drift Time Scan	Figure 12: DNL
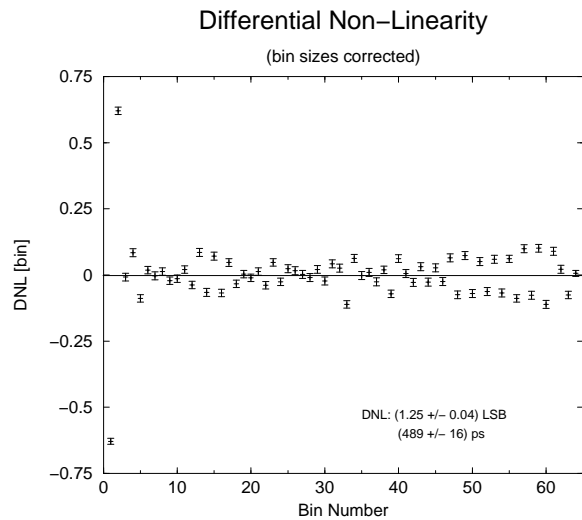
- `OTIS1.1`

    - The bunch crossing counter shows erratic behaviour due to underestimated driver strengths.
    - Big offset spread for ASD threshold voltages.
    - `MultiHit` mode still missing.
    - Missing inverter causes malfunction of DLL lock lost status information.

- `OTIS1.2`

    - N.N.

9 How to get the OTIS chip working

- Event-ID
  Problem: the EventID does not follow the number of processed triggers.
  Solution: ensure that the input pads of the EventID reset signal are not floating: an open LVDS input may reset the EventID counter.

- Output signal heights
  Problem: the data output signals (Data, DataValid) do not reach nominal values (2.5V)
  Solution: (`OTIS1.1` testboard V1 only) if you are using the SAMTEC connector to access data output signals, please remove the termination resistors (R5, R6, R7, R8 and R12)

- OTIS TDCID and I2CID
  Problem: changing the TDCID has side effects on the I2CID
  Solution: (`OTIS1.1` testboard V1 only) be aware that on the testboard some of the I2C IDs are shortet to TDC IDs:
  ID[18] shorted to ID[5]
  ID[17]   . . .   ID[4]
  ID[16]   . . .   ID[3]
  ID[15]   . . .   ID[2]
  ID[13]   . . .   ID[1]
  ID[12]   . . .   ID[0]

- Digital supply voltage
  Problem: Voltage drop at coil L1 is too big
  Solution: (`OTIS1.1` testboard V1 only) bypass (short) coil L1

- DLL Lock
  Problem: DLL lock lost bit is set quite often
  Solution: 1) There is a bug in the lock lost bit generation. Refer to Vctrl for DLL lock state. 2) There is no pull up resistor in the DLL reset pad. Therefor the pad must be tied manually to 2.5V in order to avoid unintended DLL resets (and lock lost bits).

- PowerUpReset
  Problem: A power cycle does not always trigger a PowerUpReset
  Solution: Ensure that the capacitance at the PowerUpReset pad is fully discharged. Otherwise there will be no PowerUpReset.

- `OTIS1.1` missing drift time codes
  Problem: There are missing drift time codes around bin number 32.
  Solution: Ensure that the trigger signal is synchronised to the rising edge of the LHC bunch crossing clock.

- `OTIS1.1` missing drift time codes
  Problem: When searching 3BX for hits, there are missing drift time codes near the end of the third BX.
  Solution: Ensure that the hit signal rate does not exceed 1/(3 x 25ns). In `SingleHit` mode only the first hit out of 3 possible hits will be repoerted.

A   OTIS1.0 Pad Layout and Description
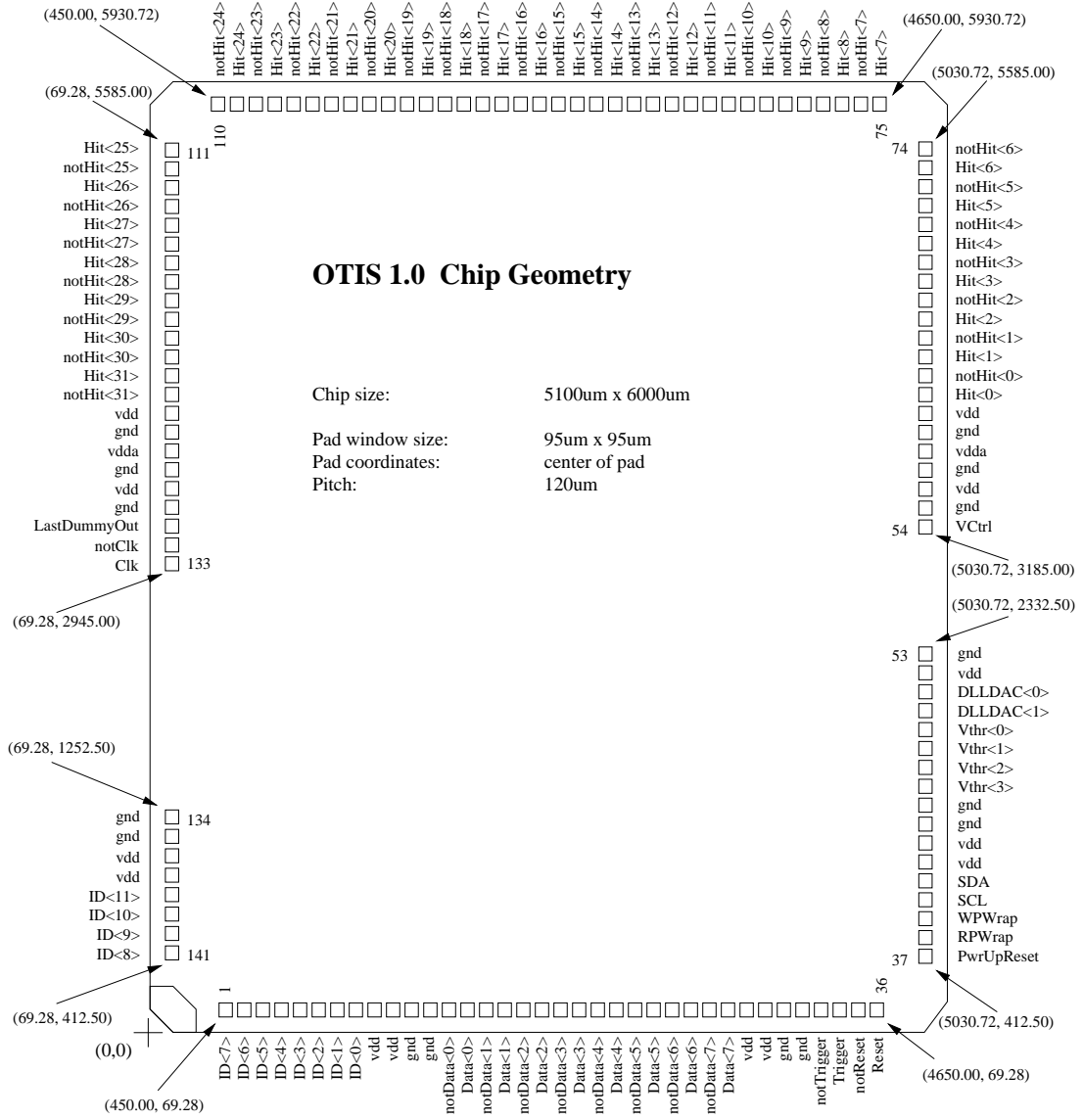
Figure 13: OTIS1.0 Pad Layout

Table 7: OTIS1.0 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	ID< 7 >	450.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 7)
2	ID< 6 >	570.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 6)
3	ID< 5 >	690.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 5)
4	ID< 4 >	810.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 4)
5	ID< 3 >	930.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 3)
6	ID< 2 >	1050.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 2)
7	ID< 1 >	1170.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 1)
8	ID< 0 >	1290.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 0)
9	vdd	1410.00	69.28	input	positiv digital supply
10	vdd	1530.00	69.28	input	positiv digital supply
11	gnd	1650.00	69.28	input	negativ digital supply
12	gnd	1770.00	69.28	input	negativ digital supply
13	notData< 0 >	1890.00	69.28	LVDS output (neg.)	data output (LSB)
14	Data< 0 >	2010.00	69.28	LVDS output (pos.)	
15	notData< 1 >	2130.00	69.28	LVDS output (neg.)	data output
16	Data< 1 >	2250.00	69.28	LVDS output (pos.)	
17	notData< 2 >	2370.00	69.28	LVDS output (neg.)	data output
18	Data< 2 >	2490.00	69.28	LVDS output (pos.)	
19	notData< 3 >	2610.00	69.28	LVDS output (neg.)	data output
20	Data< 3 >	2730.00	69.28	LVDS output (pos.)	
21	notData< 4 >	2850.00	69.28	LVDS output (neg.)	data output
22	Data< 4 >	2970.00	69.28	LVDS output (pos.)	
23	notData< 5 >	3090.00	69.28	LVDS output (neg.)	data output
24	Data< 5 >	3210.00	69.28	LVDS output (pos.)	
25	notData< 6 >	3330.00	69.28	LVDS output (neg.)	data output
26	Data< 6 >	3450.00	69.28	LVDS output (pos.)	
27	notData< 7 >	3570.00	69.28	LVDS output (neg.)	data output (MSB)
28	Data< 7 >	3690.00	69.28	LVDS output (pos.)	
29	vdd	3810.00	69.28	input	positiv digital supply
30	vdd	3930.00	69.28	input	positiv digital supply
31	gnd	4050.00	69.28	input	negativ digital supply
32	gnd	4170.00	69.28	input	negativ digital supply
33	notTrigger	4290.00	69.28	LVDS input (neg.)	L0 Trigger
34	Trigger	4410.00	69.28	LVDS input (pos.)	
35	notReset	4530.00	69.28	LVDS input (neg.)	Reset
36	Reset	4650.00	69.28	LVDS input (pos.)	
37	PwrUpReset	5030.72	412.50	input	Power Up Reset
38	RPWrap	5030.72	532.50	output	Read Pointer Wrap
39	WPWrap	5030.72	652.50	output	Write Pointer Wrap
40	SCL	5030.72	772.50	Input	I^2C Clock
41	SDA	5030.72	892.50	input/output	I^2C Data
42	vdd	5030.72	1012.50	input	positiv digital supply
43	vdd	5030.72	1132.50	input	positiv digital supply
44	gnd	5030.72	1252.50	input	negativ digital supply
45	gnd	5030.72	1372.50	input	negativ digital supply
46	Vthr< 3 >	5030.72	1492.50	output	Bias
47	Vthr< 2 >	5030.72	1612.50	output	Bias
48	Vthr< 1 >	5030.72	1732.50	output	Bias
49	Vthr< 0 >	5030.72	1852.50	output	Bias
50	DLLDAC< 1 >	5030.72	1972.50	output	Bias
51	DLLDAC< 0 >	5030.72	2092.50	output	Bias
52	vdd	5030.72	2212.50	input	positiv digital supply
53	gnd	5030.72	2332.50	input	negativ digital supply

Table 7: `OTIS1.0` Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
54	`VCtrl`	5030.72	3185.00	output	Control Voltage
55	`gnd`	5030.72	3305.00	input	negativ digital supply
56	`vdd`	5030.72	3425.00	input	positiv digital supply
57	`gnd`	5030.72	3545.00	input	negativ digital supply
58	`vdda`	5030.72	3665.00	input	positiv analog supply
59	`gnd`	5030.72	3785.00	input	negativ digital supply
60	`vdd`	5030.72	3905.00	input	positiv digital supply
61	`Hit< 0 >`	5030.72	4025.00	LVDS input (pos.)	Hit Signal
62	`notHit< 0 >`	5030.72	4145.00	LVDS input (neg.)	
63	`Hit< 1 >`	5030.72	4265.00	LVDS input (pos.)	Hit Signal
64	`notHit< 1 >`	5030.72	4385.00	LVDS input (neg.)	
65	`Hit< 2 >`	5030.72	4505.00	LVDS input (pos.)	Hit Signal
66	`notHit< 2 >`	5030.72	4625.00	LVDS input (neg.)	
67	`Hit< 3 >`	5030.72	4745.00	LVDS input (pos.)	Hit Signal
68	`notHit< 3 >`	5030.72	4865.00	LVDS input (neg.)	
69	`Hit< 4 >`	5030.72	4985.00	LVDS input (pos.)	Hit Signal
70	`notHit< 4 >`	5030.72	5105.00	LVDS input (neg.)	
71	`Hit< 5 >`	5030.72	5225.00	LVDS input (pos.)	Hit Signal
72	`notHit< 5 >`	5030.72	5345.00	LVDS input (neg.)	
73	`Hit< 6 >`	5030.72	5465.00	LVDS input (pos.)	Hit Signal
74	`notHit< 6 >`	5030.72	5585.00	LVDS input (neg.)	
75	`Hit< 7 >`	4650.00	5930.72	LVDS input (pos.)	Hit Signal
76	`notHit< 7 >`	4530.00	5930.72	LVDS input (neg.)	
77	`Hit< 8 >`	4410.00	5930.72	LVDS input (pos.)	Hit Signal
78	`notHit< 8 >`	4290.00	5930.72	LVDS input (neg.)	
79	`Hit< 9 >`	4170.00	5930.72	LVDS input (pos.)	Hit Signal
80	`notHit< 9 >`	4050.00	5930.72	LVDS input (neg.)	
81	`Hit< 10 >`	3930.00	5930.72	LVDS input (pos.)	Hit Signal
82	`notHit< 10 >`	3810.00	5930.72	LVDS input (neg.)	
83	`Hit< 11 >`	3690.00	5930.72	LVDS input (pos.)	Hit Signal
84	`notHit< 11 >`	3570.00	5930.72	LVDS input (neg.)	
85	`Hit< 12 >`	3450.00	5930.72	LVDS input (pos.)	Hit Signal
86	`notHit< 12 >`	3330.00	5930.72	LVDS input (neg.)	
87	`Hit< 13 >`	3210.00	5930.72	LVDS input (pos.)	Hit Signal
88	`notHit< 13 >`	3090.00	5930.72	LVDS input (neg.)	
89	`Hit< 14 >`	2970.00	5930.72	LVDS input (pos.)	Hit Signal
90	`notHit< 14 >`	2850.00	5930.72	LVDS input (neg.)	
91	`Hit< 15 >`	2730.00	5930.72	LVDS input (pos.)	Hit Signal
92	`notHit< 15 >`	2610.00	5930.72	LVDS input (neg.)	
93	`Hit< 16 >`	2490.00	5930.72	LVDS input (pos.)	Hit Signal
94	`notHit< 16 >`	2370.00	5930.72	LVDS input (neg.)	
95	`Hit< 17 >`	2250.00	5930.72	LVDS input (pos.)	Hit Signal
96	`notHit< 17 >`	2130.00	5930.72	LVDS input (neg.)	
97	`Hit< 18 >`	2010.00	5930.72	LVDS input (pos.)	Hit Signal
98	`notHit< 18 >`	1890.00	5930.72	LVDS input (neg.)	
99	`Hit< 19 >`	1770.00	5930.72	LVDS input (pos.)	Hit Signal
100	`notHit< 19 >`	1650.00	5930.72	LVDS input (neg.)	
101	`Hit< 20 >`	1530.00	5930.72	LVDS input (pos.)	Hit Signal
102	`notHit< 20 >`	1410.00	5930.72	LVDS input (neg.)	
103	`Hit< 21 >`	1290.00	5930.72	LVDS input (pos.)	Hit Signal
104	`notHit< 21 >`	1170.00	5930.72	LVDS input (neg.)	
105	`Hit< 22 >`	1050.00	5930.72	LVDS input (pos.)	Hit Signal
106	`notHit< 22 >`	930.00	5930.72	LVDS input (neg.)	

Table 7: `OTIS`1.0 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	`Hit< 23 >`	810.00	5930.72	LVDS input (pos.)	Hit Signal
108	`notHit< 23 >`	690.00	5930.72	LVDS input (neg.)	
109	`Hit< 24 >`	570.00	5930.72	LVDS input (pos.)	Hit Signal
110	`notHit< 24 >`	450.00	5930.72	LVDS input (neg.)	
111	`Hit< 25 >`	69.28	5585.00	LVDS input (pos.)	Hit Signal
112	`notHit< 25 >`	69.28	5465.00	LVDS input (neg.)	
113	`Hit< 26 >`	69.28	5345.00	LVDS input (pos.)	Hit Signal
114	`notHit< 26 >`	69.28	5225.00	LVDS input (neg.)	
115	`Hit< 27 >`	69.28	5105.00	LVDS input (pos.)	Hit Signal
116	`notHit< 27 >`	69.28	4985.00	LVDS input (neg.)	
117	`Hit< 28 >`	69.28	4865.00	LVDS input (pos.)	Hit Signal
118	`notHit< 28 >`	69.28	4745.00	LVDS input (neg.)	
119	`Hit< 29 >`	69.28	4625.00	LVDS input (pos.)	Hit Signal
120	`notHit< 29 >`	69.28	4505.00	LVDS input (neg.)	
121	`Hit< 30 >`	69.28	4385.00	LVDS input (pos.)	Hit Signal
122	`notHit< 30 >`	69.28	4265.00	LVDS input (neg.)	
123	`Hit< 31 >`	69.28	4145.00	LVDS input (pos.)	Hit Signal
124	`notHit< 31 >`	69.28	4025.00	LVDS input (neg.)	
125	`vdd`	69.28	3905.00	input	positiv digital supply
126	`gnd`	69.28	3785.00	input	negativ digital supply
127	`vdda`	69.28	3665.00	input	positiv analog supply
128	`gnd`	69.28	3545.00	input	negativ digital supply
129	`vdd`	69.28	3425.00	input	positiv digital supply
130	`gnd`	69.28	3305.00	input	negativ digital supply
131	`LastDummyOut`	69.28	3185.00	output	
132	`notClk`	69.28	3065.00	LVDS input (neg.)	LHC Clock
133	`Clk`	69.28	2945.00	LVDS input (pos.)	
134	`gnd`	69.28	1252.50	input	negativ digital supply
135	`gnd`	69.28	1132.50	input	negativ digital supply
136	`vdd`	69.28	1012.50	input	positiv digital supply
137	`vdd`	69.28	892.50	input	positiv digital supply
138	`ID< 11 >`	69.28	772.50	CMOS input (pull down)	TDC-ID (Bit No 11)
139	`ID< 10 >`	69.28	652.50	CMOS input (pull down)	TDC-ID (Bit No 10)
140	`ID< 9 >`	69.28	532.50	CMOS input (pull down)	TDC-ID (Bit No 9)
141	`ID< 8 >`	69.28	412.50	CMOS input (pull down)	TDC-ID (Bit No 8)

B   OTIS1.1 Pad Layout and Description
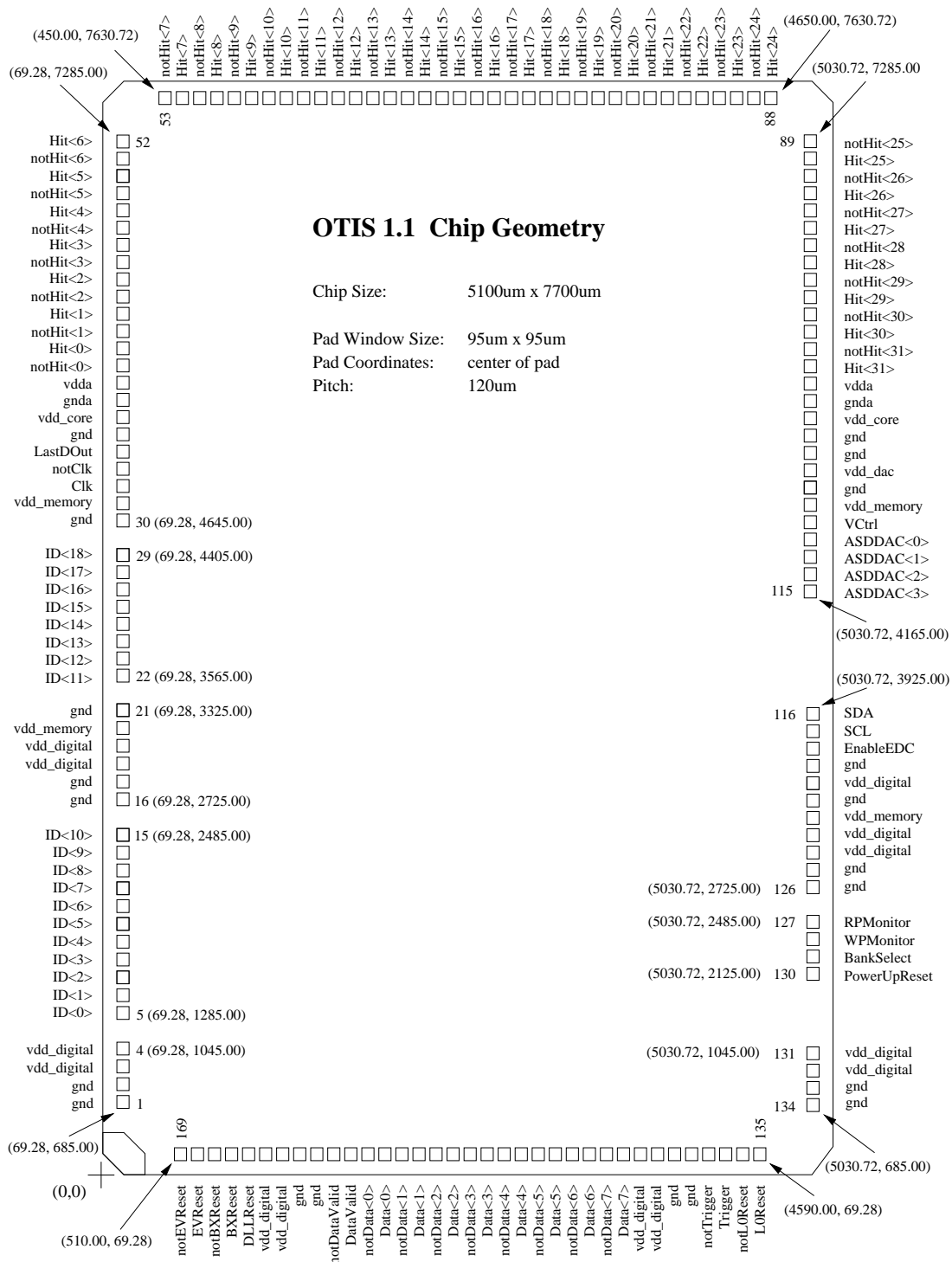
Figure 14: OTIS1.1 Pad Layout

Table 8: OTIS1.1 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	685.00	input	negative digital supply
2	gnd	69.28	805.00	input	negative digital supply
3	vdd_digital	69.28	925.00	input	positive digital supply
4	vdd_digital	69.28	1045.00	input	positive digital supply
5	ID< 0 >	69.28	1285.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1405.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1525.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1645.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1765.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1885.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	2005.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	2125.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	2245.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2365.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2485.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2725.00	input	negative digital supply
17	gnd	69.28	2845.00	input	negative digital supply
18	vdd_digital	69.28	2965.00	input	negative digital supply
19	vdd_digital	69.28	3085.00	input	positive digital supply
20	vdd_memory	69.28	3205.00	input	positive memory supply
21	gnd	69.28	3325.00	input	negative digital supply
22	ID< 11 >	69.28	3565.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3685.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3805.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3925.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	4045.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	4165.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	4285.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	4405.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	4645.00	input	negative digital supply
31	vdd_memory	69.28	4765.00	input	positive memory supply
32	Clk	69.28	4885.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	5005.00	LVDS input (neg.)	
34	LastDOut	69.28	5125.00		
35	gnd	69.28	5245.00	input	negative digital supply
36	vdd_core	69.28	5365.00	input	positive TDC supply
37	gnda	69.28	5485.00	input	negative DLL supply
38	vdda	69.28	5605.00	input	positive DLL supply
39	notHit< 0 >	69.28	5725.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5845.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5965.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	6085.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	6205.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	6325.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	6445.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	6565.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	6685.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6805.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6925.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	7045.00	LVDS input (pos.)	
51	notHit< 6 >	69.28	7165.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	7285.00	LVDS input (pos.)	

Table 8: OTIS1.1 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
53	notHit< 7 >	450.00	7630.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	7630.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	7630.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	7630.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	7630.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	7630.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	7630.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	7630.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	7630.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	7630.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	7630.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	7630.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	7630.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	7630.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	7630.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	7630.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	7630.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	7630.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	7630.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	7630.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	7630.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	7630.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	7630.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	7630.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	7630.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	7630.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	7630.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	7630.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	7630.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	7630.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	7630.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	7630.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	7630.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	7630.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	7630.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	7630.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	7285.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	7165.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	7045.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6925.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6805.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	6685.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	6565.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	6445.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	6325.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	6205.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	6085.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5965.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5845.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5725.00	LVDS input (pos.)	
103	vdda	5030.72	5605.00	input	positive DLL supply
104	gnda	5030.72	5485.00	input	negative DLL supply
105	vdd_core	5030.72	5365.00	input	positive TDC supply
106	gnd	5030.72	5245.00	input	negative digital supply

Table 8: `OTIS1.1` Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	gnd	5030.72	5125.00	input	negative digital supply
108	vdd_DAC	5030.72	5005.00	input	positive DAC supply
109	gnd	5030.72	4885.00	input	negative digital supply
110	vdd_memory	5030.72	4765.00	input	positive memory supply
111	VCtrl	5030.72	4645.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	4525.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	4405.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	4285.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	4165.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3925.00	input/output (5V open drain)	I^{2}C Data
117	SCL	5030.72	3805.00	CMOS input (5V)	I^{2}C Clock
118	EnableEDC	5030.72	3685.00	CMOS input (internal pull down)	enable I^{2}C EDC
119	gnd	5030.72	3565.00	input	negative digital supply
120	vdd_digital	5030.72	3445.00	input	positive digital supply
121	gnd	5030.72	3325.00	input	negative digital supply
122	vdd_memory	5030.72	3205.00	input	positive memory supply
123	vdd_digital	5030.72	3085.00	input	positive digital supply
124	vdd_digital	5030.72	2965.00	input	positive digital supply
125	gnd	5030.72	2845.00	input	negative digital supply
126	gnd	5030.72	2725.00	input	negative digital supply
127	RPMonitor	5030.72	2485.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	2365.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	2245.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	2125.00	input	Power Up Reset
131	vdd_digital	5030.72	1045.00	input	positive digital supply
132	vdd_digital	5030.72	925.00	input	positive digital supply
133	gnd	5030.72	805.00	input	negative digital supply
134	gnd	5030.72	685.00	input	negative digital supply
135	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notL0Reset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	negative digital supply
140	gnd	3990.00	69.28	input	negative digital supply
141	vdd_digital	3870.00	69.28	input	positive digital supply
142	vdd_digital	3750.00	69.28	input	positive digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	

Table 8: `OTIS`1.1 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
159	`DataValid`	1710.00	69.28	CMOS output (pos.)	Data Valid
160	`notDataValid`	1590.00	69.28	CMOS output (neg.)	
161	`gnd`	1470.00	69.28	input	negative digital supply
162	`gnd`	1350.00	69.28	input	negative digital supply
163	`vdd_digital`	1230.00	69.28	input	positive digital supply
164	`vdd_digital`	1110.00	69.28	input	positive digital supply
165	`DLLReset`	990.00	69.28	CMOS input	DLL Reset
166	`BXReset`	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	`notBXReset`	750.00	69.28	LVDS input (neg.)	
168	`EVReset`	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	`notEVReset`	510.00	69.28	LVDS input (neg.)	

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C   OTIS1.2 Pad Layout and Description
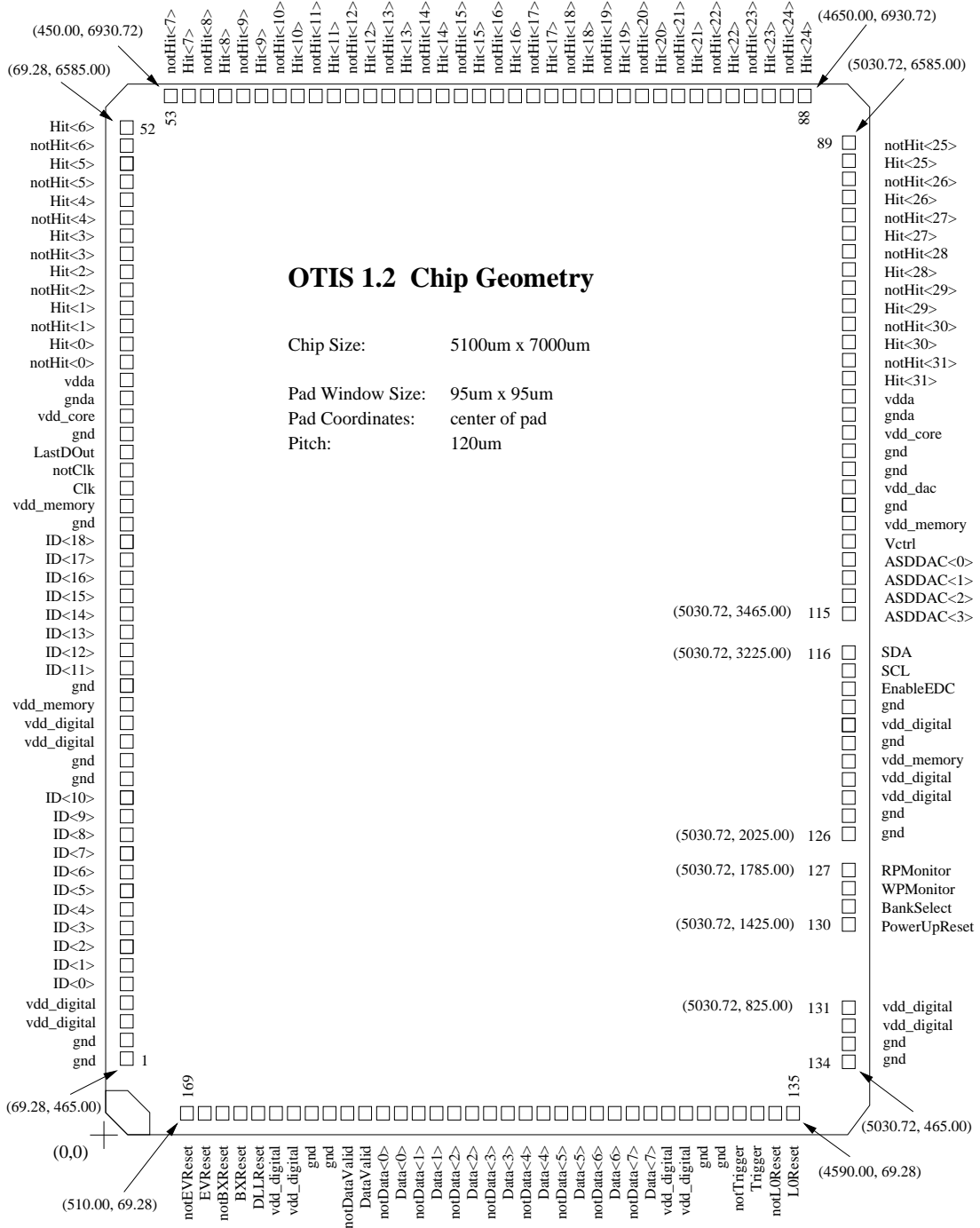
Figure 15: OTIS1.2 Pad Layout

Table 9: OTIS1.2 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	465.00	input	negative digital supply
2	gnd	69.28	485.00	input	negative digital supply
3	vdd_digital	69.28	705.00	input	positive digital supply
4	vdd_digital	69.28	825.00	input	positive digital supply
5	ID< 0 >	69.28	945.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1065.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1185.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1305.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1425.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1545.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	1665.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	1785.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	1905.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2025.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2145.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2265.00	input	negative digital supply
17	gnd	69.28	2385.00	input	negative digital supply
18	vdd_digital	69.28	2505.00	input	negative digital supply
19	vdd_digital	69.28	2625.00	input	positive digital supply
20	vdd_memory	69.28	2745.00	input	positive memory supply
21	gnd	69.28	2865.00	input	negative digital supply
22	ID< 11 >	69.28	2985.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3105.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3225.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3345.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	3465.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	3585.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	3705.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	3825.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	3945.00	input	negative digital supply
31	vdd_memory	69.28	4065.00	input	positive memory supply
32	Clk	69.28	4185.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	4305.00	LVDS input (neg.)	
34	LastDOut	69.28	4425.00		
35	gnd	69.28	4545.00	input	negative digital supply
36	vdd_core	69.28	4665.00	input	positive TDC supply
37	gnda	69.28	4785.00	input	negative DLL supply
38	vdda	69.28	4905.00	input	positive DLL supply
39	notHit< 0 >	69.28	5025.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5145.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5265.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	5385.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	5505.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	5625.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	5745.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	5865.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	5985.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6105.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6225.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	6345.00	LVDS input (pos.)	
51	notHit< 6 >	69.28	6465.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	6585.00	LVDS input (pos.)	

Table 9: `OTIS1.2` Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
53	notHit< 7 >	450.00	6930.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	6930.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	6930.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	6930.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	6930.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	6930.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	6930.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	6930.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	6930.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	6930.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	6930.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	6930.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	6930.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	6930.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	6930.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	6930.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	6930.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	6930.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	6930.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	6930.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	6930.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	6930.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	6930.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	6930.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	6930.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	6930.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	6930.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	6930.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	6930.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	6930.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	6930.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	6930.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	6930.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	6930.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	6930.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	6930.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	6585.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	6465.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	6345.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6225.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6105.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	5985.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	5865.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	5745.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	5625.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	5505.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	5385.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5265.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5145.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5025.00	LVDS input (pos.)	
103	vdda	5030.72	4905.00	input	positive DLL supply
104	gnda	5030.72	4785.00	input	negative DLL supply
105	vdd_core	5030.72	4665.00	input	positive TDC supply
106	gnd	5030.72	4545.00	input	negative digital supply

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Table 9: `OTIS1.2`Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	gnd	5030.72	4425.00	input	negative digital supply
108	vdd_DAC	5030.72	4305.00	input	positive DAC supply
109	gnd	5030.72	4185.00	input	negative digital supply
110	vdd_memory	5030.72	4065.00	input	positive memory supply
111	VCtrl	5030.72	3945.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	3825.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	3705.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	3585.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	3465.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3225.00	input/output (5V open drain)	I^{2}C Data
117	SCL	5030.72	3105.00	CMOS input (5V)	I^{2}C Clock
118	EnableEDC	5030.72	2985.00	CMOS input (pull down)	Enable I^{2}C EDC
119	gnd	5030.72	2865.00	input	negative digital supply
120	vdd_digital	5030.72	2745.00	input	positive digital supply
121	gnd	5030.72	2625.00	input	negative digital supply
122	vdd_memory	5030.72	2505.00	input	positive memory supply
123	vdd_digital	5030.72	2385.00	input	positive digital supply
124	vdd_digital	5030.72	2265.00	input	positive digital supply
125	gnd	5030.72	2145.00	input	negative digital supply
126	gnd	5030.72	2025.00	input	negative digital supply
127	RPMonitor	5030.72	1785.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	1665.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	1545.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	1425.00	input	Power Up Reset
131	vdd_digital	5030.72	825.00	input	positive digital supply
132	vdd_digital	5030.72	705.00	input	positive digital supply
133	gnd	5030.72	585.00	input	negative digital supply
134	gnd	5030.72	465.00	input	negative digital supply
135	LOReset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notLOReset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	negative digital supply
140	gnd	3990.00	69.28	input	negative digital supply
141	vdd_digital	3870.00	69.28	input	positive digital supply
142	vdd_digital	3750.00	69.28	input	positive digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	

Table 9: `OTIS1.2`Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
159	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
160	notDataValid	1590.00	69.28	CMOS output (neg.)	
161	gnd	1470.00	69.28	input	negative digital supply
162	gnd	1350.00	69.28	input	negative digital supply
163	vdd_digital	1230.00	69.28	input	positive digital supply
164	vdd_digital	1110.00	69.28	input	positive digital supply
165	DLLReset	990.00	69.28	CMOS input (pull up)	DLL Reset
166	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	notBXReset	750.00	69.28	LVDS input (neg.)	
168	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	notEVReset	510.00	69.28	LVDS input (neg.)	

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`http://lhcb-elec.web.cern.ch/lhcb-elec/html/key_parameters.htm`

[4]   Philips Semiconductors, The I^2C bus specification, available via
`http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf`

[5]   Minutes: Beetle-OTIS-Meeting, 24.01.2002, OTIS-User mailinglist:
`http://listserv.uni-heidelberg.de/cgi-bin/wa?A2=ind0201&L=otis-user&P=R336`

[6]   Bi-directional level shifter for I^2C-bus and other systems,
Application Note AN97055, Philips Semiconductors, 1998

[7]   `http://www.elv.de/Main.asp?Menue=Shop&Gruppe=SI-AZ&Artikel=499-86`

[8]   `http://www.kip.uni-heidelberg.de/~stange/`