Specifications IF13-1 Prototype of the Auxiliary Board for the Outer Tracker

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Abstract

The auxiliary board for the Outer Tracker supplies the low voltage (+2.5 V, -3.0 V, +3.0 V), fast and slow control signals to the OTIS TDC and ASDBLR preamplifier boards and transforms parallel electrical timing and status data from the OTIS into serial optical data (GOL). One auxiliary board will be used for every module end. It sits on the rim of the outer tracker modules and is connected to the service box on the frame and the OTIS boards being plugged into it.

LHCb Outer Tracker Internal Note

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1 Parts

A list of connectors and ICs used on the auxiliary board is shown in table 1, an overview is given in figure 3.

function	name/part number	size(WxHxD)[mm^3]
connector for TFC, slow control and monitoring	SCSI 50 pin	52.5x10.5x17.5
power connector	4-pin AMP Mate-N-Lok 5.08 mm pitch	25.5x8.8x13
laser VCSEL	Ulm Photonics Ulm850-05-TN-USMB0P	12.7x7.2x16.3 +mounting
control LEDs (2)	2 pc. signal construct ZAZW0422	5x10x20.5
Hex switch for module location address	KDR-16H	10x10x12.4
power regulator +2.5 V	1 * L4913 (SO-20)	12.95x2.65x10.55
power regulator +3.0 V	1 * L4913 (SO-20)	12.95x2.65x10.55
power regulator -3.0 V	1 * L7913 (SO-20)	12.95x2.65x10.55
serializer	GOL 1.0 144 L-fpBGA	13.0x1.63x13.0
de-jitter	QPLL2(LPCC-28)	5x1x5
quartz 160 MHz	CC1F-T1A	8.0x1.75x3.7
quartz 40 MHz	IQXO-71A	7.5 x 1.5 x 5
OTIS board connectors	SAMTEC ZML-140-54-S-D-530-SM	53.98x13.46x9.27
reset push button	Farnell 535-916	6.2x6.2x5

Table 1: Connectors and ICs needed for the auxiliary board

The GOL is a Gigabit Optical Link ASIC, specified in [1]. It receives 32 bits in parallel at 40 MHz from four OTIS [3] chips. The data is serialized and 8/10 bit encoded. The GOL 1.0 has a laser driver output sending data at 1.6 Gbit/s over a VCSEL diode. The VCSEL diode is a commercial product proved to be rad hard by the LHCb Silicon Tracker group [12] [13]. The QPLL [2] is necessary to reduce jitter to meet the requirements of the GOL. It comes along with a quartz oscillator. The rad hard power regulators L4913 for positive power and L7913 for negative power have an adjustable output voltage. Mind that the metal cooling surface on the package is internally connected to power and must be insulated when pressed against metal cooling

bars. The connector going off the module are a 50-pin SCSI connector for TFC, I^2C and Monitor signals from and to the distribution box.

The connector to the OTIS board [9] is a 80 pin SMD connector from SAMTEC.

1.1 Power regulators

Radiation hard power regulators developed at CERN are used for the LHCb Outer Tracker front-end electronics. The low voltage power regulators L4913 [4] for positive and L7913 [5] for negative voltage are adjustable types. The input voltage is +5.5 V or -5.5 V, while still referred to as +5 V and -5 V in the documentation. [1] The estimated power consumption is shown in table 2.

Component	Number /aux-card	Power / Comp	Heat / Box
ASD-BLR	16	420 mW	6.7 W
pull-up resistor network	128	15 mW	1.9 W
OTIS	4	550 mW	2.2 W
GOL	1	390 mW	0.4
Others			1 W
L4913ADJ L7913ADJ	2 1		12 W
Total			24 W

Table 2: Power consumption on the auxiliary card

Tables 3 and 4 shows the connectivity of the power regulators for the SO-20 package, note that the pin out for the negative power regulator is different from the positive one. For the prototype boards version IF13-0 the footprint for the negative power regulators are wrongly the same as for the positive types, mounting of the negative type L7913 will result in severe shorts. A scheme shown in [14] can be used to make a patch for the L7913 negative power regulator. As old versions (Q5 silicon) of the negative power regulator show oscillations ($\pm$ 1 V) the usage of Q6 silicon is recommended.

The resistive divider is R1 between Vout and ADJ and R2, R3 (parallel) between ADJ and ground. For R1 = 1 kOhm R2 and R3 must be

[1] As the voltage regulator needs almost 1.8 V at 2.5 A the input voltage has been changed from before 5 V to 5.5 V typical. The power consumption has risen accordingly.

R2 = 1 kOhm, R3 = 22 kOhm for Vout = +2.5 V and R2 = 1 kOhm and R3 = 2.2 kOhm for Vout = 3 V and Vout = -3 V, see figure 6, 1 μF capacitors to ground are recommended for the Vout pins, the additional 1 μF capacitor between sense and adjust pin is necessary to kill spikes, capacitors in connection with serial resistors are used to reduce oscillations. In order to compensate for voltage drops on the OTIS board HF blocking, it can be necessary to set the +2.5 V to +2.7 V. If the 100 kOhm resistors R190-192 are used the maximum output current will be reduced to 40 percent of the the 4.5 A default value, which is too low for regular operation, since only 66 percent of the maximum current can be used.

Pin Number in SO-20 slug up	Pin Name	Pin function	connectivity
1	Gnd	ground	Gnd
2	NC	not connected	not connected
3	NC	not connected	not connected
4	Vin	supply Voltage	+5 V
5	Vout1	out half power (right Vin)	+3 V, +2.5 V
6	Vout1	out half power (right Vin)	+3 V, +2.5 V
7	SH-cntrl	short circuit valve controlling	100k pull up
8	OCM	short circuit monitoring	LED 101
9	NC	not connected	not connected
10	Gnd	ground	Gnd
11	Gnd	ground	Gnd
12	INH	inhibit	Gnd
13	ADJ	ADJ	resistive divider +100 nF
14	SENSE/NC	sense output	Vout
15	Vout2	out half power (left Vin)	+3 V, +2.5 V
16	Vout2	out half power (left Vin)	+3 V, +2.5 V
17	Vin	supply Voltage	+5 V
18	NC	not connected	not connected
19	NC	not connected	not connected
20	Gnd	ground	Gnd

Table 3: Positive power regulator LHC4913 pin out

Pin Number in SO-20 slug up	Pin Name	Pin function	connectivity
1	V_{MINUS}	supply Voltage	-5 V
2	NC	not connected	not connected
3	NC	not connected	not connected
4	NC	not connected	not connected
5	SH-cntrl	short circuit valve controlling	100k pull up
6	OCM	short circuit monitoring	LED 102
7	V_{PLUS}	Voltage input for OCM, INH	2.5 V
8	NC	not connected	not connected
9	Gnd	ground	Gnd
10	V_{MINUS}	supply Voltage	-5 V
11	V_{MINUS}	supply Voltage	-5 V
12	INH	inhibit	Gnd
13	ADJ	ADJ	resistive divider +100 nF
14	NC	not connected	not connected
15	Vout	out power	-3 V
16	Vout	out power	-3 V
17	NC	not connected	not connected
18	NC	not connected	not connected
19	NC	not connected	not connected
20	V_{MINUS}	supply Voltage	-5 V

Table 4: Negative power regulator LHC7913 pin out.

1.2 GOL 1.0

The GOL 1.0 [1] is a radiation hard serializer with a 32 bit 40 MHz parallel input and a 1.6 Gbit/s serial laser driver output. Table 5 shows the connectivity of the GOL 1.0 on the auxiliary board. The GOL 1.0 is packaged to a 144 L-fpBGA. It is used in 32 bit 8B/10B Gigabit Ethernet mode.

The serial output is connected via a current divider to a VCSEL diode: from the GOL ld_cathode output to +2.5 V R136 = 100 Ohm , from GOL ld_cathode output to the VCSEL input R = 22 Ohm. For standard operation R136 is not needed.

The laser driver bias current is adjustable by jumpers. The settings for the laser diode bias current should then be 5.8 mA, corresponding to conf_id_0 = 0 (J107 open), conf_id_1 = 0 (J106 open), the equivalent register setting is config<6:0> = 0001100.

Until the best phase relation to the OTIS is found the conf_negedge pin is jumpered too, negative edge sampling is stated to be unsave. For the clock input the following possibilities are given:

- selectDiff = 1 (J101), differential clock from QPLL is used
- selectDiff = 0 (J101), solder jumper J102 to quartz, 40 MHz on-board quartz is used
- selectDiff = 0 (J101), solder jumper J102 to quartz and connector, 40 MHz on board quartz is used, clock can be used for monitoring (J111) and other boards
- selectDiff = 0 (J101), solder jumper to connector, external clock can be fed in (J111).

As the GOL chip should not have clock signals during power up, the selectDiff signal will be used in the experiment to choose the LVTTL clock input (with no input present) at power on from the service box and to switch to the valid differential clock signal after a delay.

JTAG boundary scan can be performed via a minimized JTAG-connector (S103). The ready signal is connected to LED1. Reset_b is an active low master reset connected to $\overline{PwrUpRst}$ (the OTIS and QPLL reset is active low too). The $\overline{PwrUpRst}$ comes from the timing and fast control (TFC) or is set with a push button (SW1). The I^2C bus is distributed over the service box (see 2.4). The power for the GOL 1.0 is +2.5 V, all inputs are 5 V tolerant. [2]

[2] A start up problem has been reported for the GOL 1.0: The GOL 1.0 does not start properly if the clock is present at power on.

1.3 QPLL2

The QPLL2 [2] is used as a jitter filter for the GOL 1.0 serializer and the OTIS TDC. Table 6 shows the connectivity of the QPLL2 on the auxiliary board. Either 120 MHz or 160 MHz mode is usable, since only the 40 MHz outputs will be used. We use the 160 MHz version (mode=1). The QPLL2 has LVDS as well as CMOS clock inputs. The LVDS inputs are connected to the clock coming from the service box, where another QPLL2 sits, getting the input signal from the TTCrx [7]. The QPLL2 comes in a LPCC-28 (5 mm x 5 mm, 0.5 mm pitch) package. The quartz is a CC1F-T1A from Micro Crystal Switzerland. Custom quartz oscillators with 160.31470 MHz produced for the LHC detectors will be employed. The quartz has an 8 * 3.7 * 1.75 mm^3 SMD package. The QPLL runs at +2.5 V. The migration from QPLL1 to QPLL2 should not introduce any difference in the board layout or handling, but gives a bigger locking range.

Pin Number 144 L-fpBGA	Pin Name	Pin function	connectivity	level	inout
G2	cav/tx_er	data type	J115-GND	CMOS	in
D10	clkLHC	40.08 MHz input clock	quartz	CMOS	in
D11	clkLHCn	diff 40.08 MHz clock n	ClkPll_n	LVDS	in
C12	clkLHCp	diff 40.08 MHz clock p	ClkPll_p	LVDS	in
C2	conf_glink	1:G-link, 0:8B/10B	Gnd	CMOS	in
G4	conf_i_ld<0>	laser driver bias current	J107	CMOS	in
H2	conf_i_ld<1>	laser driver bias current	J106	CMOS	in
B4	conf_i_pll	selects PLL bias current	+2.5 V (+15 μA)	CMOS	in
D2	conf_laser	1:laser driver, 0:line driver	+2.5 V	CMOS	in
D12	conf_negedge	1:falling clk, 0:rising clk	J105	CMOS	in
E2	conf_wmode16	1:16-bit, 0:32-bit	Gnd	CMOS	in
F1	dav/tx_en	data type	OTIS_GOL-DV	CMOS	in
L3-L5,M5,M6,	din<0-31>	input data	OtisN_D_p<0-7>	CMOS	in
L7,M8,M9,L9,				CMOS	in
K9,K10				CMOS	in
J10,J11,				CMOS	in
H11,G11,F12,				CMOS	in
K5,M4,K6,L6,				CMOS	in
M7,K7,L8,K8,				CMOS	in
M10,L10,K11,				CMOS	in
K12,J12,H12,				CMOS	in
G12,F11,				CMOS	in
E11	FF	ff1/ff0 G-link mode only	Gnd	CMOS	in
F10	flag<0>	flag bit<0> G-link only	Gnd	CMOS	in
E12	flag<1>	flag bit<1> G-link only	Gnd	CMOS	in
B5	i2c_addr<1>	I^2C device address	Gnd	CMOS	in
A5	i2c_addr<2>	I^2C device address	+2.5 V	CMOS	in
A4	i2c_addr<3>	I^2C device address	LocAdr3	CMOS	in
C4	i2c_addr<4>	I^2C device address	LocAdr4	CMOS	in
C3	i2c_addr<5>	I^2C device address	LocAdr5	CMOS	in
D3	i2c_addr<6>	I^2C device address	LocAdr6	CMOS	in
E1	JTAGTCK	JTAG clk (pull up)	JTAG_pin5	CMOS	in
H1	JTAGTDI	JTAG data in (pull up)	JTAG_pin1	CMOS	in
G3	JTAGTDO	JTAG data out	JTAG_pin3	CMOS	out
G1	JTAGTMS	JTAG mode sel. (pull up)	JTAG_pin6	CMOS	in
A8	ld_cathode	laser driver output	LD_Cathode	5.8 mA	out
J3	ready	transmitter ready	GOL_ready	CMOS	out
D1	reset_b	master reset	$\overline{PwrUpRst}$	CMOS	in
K3	SCL	I^2C clock	I2c_Clk	CMOS	in
K4	SDA	I^2C data	I2c_Data	CMOS	in
C11	selectDiff	Sel. clock source (pull-up)	J101	CMOS	in
A7	serial_line_n	diff bit stream output	J108	adj.	out
A6	serial_line_p	diff bit stream output	J109	adj.	out
J2	test_analog	test output	J110	?	out
F2	test_shift	en. test of internal logic	Gnd	CMOS	in
A1...	VDD	+2.5 V power	+2.5 V	+2.5 V	in
A3...	GND	ground	Gnd	Gnd	in

Table 5: GOL 1.0 pin out

Pin Number LPCC-28	Pin Name	Pin function	connectivity	level	inout
1	inLVDS-	diff clock input neg.	Clk_n (TFC)	LVDS	in
2	inLVDS+	diff clock input pos.	Clk_p (TFC)	LVDS	in
3	inCMOS	single ended clock	pull down	CMOS	in
4	externalControl	center freq. ext.	Gnd	CMOS	in
5	autoRestart, f0Select< 4 >	automatic PLL restart	+2.5 V	CMOS	in
6	reset, f0Select< 5 >	active low reset	$\overline{PwrUpRst}$	CMOS	in
7	f0Select< 3 >	frequency contr.	+2.5 V	CMOS	in
8	error	SEU error	QPLL_error LED 102	+2.5 V CMOS	out
9	locked	PLL status	QPLL_locked LED 102	+2.5 V CMOS	out
10	gnd	ground	Gnd	Gnd	in
11	vdd	+2.5 V power	+2.5 V	+2.5 V	in
12	lvds80MHz-	80 MHz clock output neg	J113	LVDS	out
13	lvds80MHz+	80 MHz clock output pos	J112	LVDS	out
14	f0Select< 2 >	frequency contr.	Gnd	CMOS	in
15	lvds160MHz-	160 MHz clock output neg	n.c.	LVDS	out
16	lvds160MHz+	160 MHz clock output pos	n.c.	LVDS	out
17	gnd	ground	Gnd	Gnd	in
18	vdd	+2.5 V power	+2.5 V	+2.5 V	in
19	lvds40MHz-	40 MHz clock output neg	ClkPLL_n J104	LVDS	out
20	lvds40MHz+	40 MHz clock output pos	clkPLL_p J103	LVDS	out
21	f0Select< 1 >	frequency contr.	Gnd	CMOS	in
22	vdd	+2.5 V power	+2.5 V	+2.5 V	in
23	cap	100 nF capacitor to Gnd	Gnd	Gnd	in
24	xtal1	Analog, Quartz crystal	to VCXO	?	inout
25	gnd	ground	Gnd	Gnd	in
26	xtal2	Analog, Quartz crystal	to VCXO	?	inout
27	mode	mode select 120 MHz(0) or 160 MHz(1)	J114	CMOS	in
28	f0Select< 0 >	frequency contr.	Gnd	CMOS	in

Table 6: QPLL pin out

1.4 Jumpers and push buttons

Table 7 shows all jumpers for the current design. Jumpers have been introduced for (phase) clock choice and to define the laser driving current. Three Hex switches for the module location address allow setting the module location during installation. The reset push button causes a power up reset for the GOL, the QPLL and the connected OTIS TDCs.

function	jumper	default
sel_diff	J101	+2.5 V
clkLHC quartz/extern	J102	off
clkpll test pins 40 MHz	J103, J104	n.c.
clkpll test pins 80 MHz	J112, J113	n.c.
conf_negedge	J105	Gnd
conf_i_id1	J106	Gnd
conf_i_id0	J107	Gnd
serial_line_p (optical transmitter)	J108	off
serial_line_n (optical transmitter	J109	off
test_analog (GOL)	J110	off
clkLHC extern	J111	off
QPLL_mode 120/160 MHz	J114	+2.5 V
GOL_Tx_Er	J115	GND!
$\overline{PwrUpRst}$(active low)	SW101	+2.5 V
Hex Switch for Module Location Address	SW201-SW203	0001
OTIS_GOL-DV	J200-203	J200

Table 7: Jumpers on the auxiliary board

1.5 Laser VCSEL

The VCSEL diode is a commercial Ulm850-05-TN-USMB0P from Ulm Photonics.

It has been irradiated to 300 KRads corresponding to $2{\cdot}10^{12}$p/cm^2 and $3.6{\cdot}10^{12}$n/cm^2 [12] and [13], the degradation in optical power stayed below (< 0.2 dB)

It is packaged in a USMB connectable plastic package. The Ulm VSCEL is designed to interface with 50/125 and 62.5/125 μm multi-mode fiber, using 850 nm wavelength. The voltage drop over the VCSEL is 2 V, the current modulation should be 5.8 mA (to be confirmed).

2 Signals

The signals distributed over this board comprehend timing and fast control, I^2C, low voltage monitoring, test pulse for the ASD and TDC data from the OTIS. Table 8 and 9 shows the distribution of the signals over the connector pins to the service box on the detector frame. The power pins are described here too. Table 10 shows the connectivity to the OTIS board. LEDs signal the basic functionality of the components.

signal	pin	signal	pin	in/out	level	comment
SDAmtos_p	1	SDAmtos_n	2	in	LVDS	I^2C master to slave
SDAstom_p	3	SDAstom_n	4	out	LVDS	I^2C slave to master
SCL_p	5	SCL_n	6	in	LVDS	I^2C clock
Spare	7	Spare	8	-	-	-
Pos_3V_Mon	9	Gnd	10	out	monitor	+3 V monitor
Neg_3V_Mon	11	Gnd	12	out	monitor	-3 V monitor
Pos_2V5_Mon	13	Gnd	14	out	monitor	+2.5 V monitor
Temp_Mon	15	Temp_Mon_return	16	out	monitor	Temperature monitor
GOL_ready	17	QPLL_locked	18	out	monitor	GOL status
Select_Diff_p	19	Select_Diff_n	20	in	LVDS	QPLL/QPLL status
Spare	21	Spare	22	-	-	Spare
Spare	23	Spare	24	-	-	Spare
TPOddLow_p	25	TPOddLow_n	26	in	LVDS	Testpulse Odd Low
TPOddHi_p	27	TPOddHi_n	28	in	LVDS	Testpulse Odd High
TPEvenLow_p	29	TPEvenLow_n	30	in	LVDS	Testpulse Even Low
TPEvenHigh_p	31	TPEvenHigh_n	32	in	LVDS	Testpulse Even High
Spare	33	Spare	34	-	-	Spare
Spare	35	Spare	36	-	-	Spare
Spare	37	Spare	38	-	-	Spare
$\overline{PwrUpRst\_p}$	39	$\overline{PwrUpRst\_n}$	40	in	LVDS	not Power Up Reset
$\overline{L0Reset\_p}$	41	$\overline{L0Reset\_n}$	42	in	LVDS	not L0 Reset
$\overline{EvCntReset\_p}$	43	$\overline{EvCntReset\_n}$	44	in	LVDS	not Event Counter Reset
$\overline{BCntReset\_p}$	45	$\overline{BCntReset\_n}$	46	in	LVDS	not Bunch Counter Reset
L0Accept_p	47	L0Accept_n	48	in	LVDS	L0 Trigger Accept
Clock_p	49	Clock_n	50	in	LVDS	Bx Clock

Table 8: Signal distribution on the connector to service box

Power	+5 V (+5.5 V)	1	in	power
	Gnd	2	in	Gnd
	Gnd	3	in	Gnd
	-5 V (-5.5 V)	4	in	power
Hex Switches for Module Location Address SW201	LocAdr3	1	in	+2.5 V/Gnd
	LocAdr4	4	in	+2.5 V/Gnd
	LocAdr5	3	in	+2.5 V/Gnd
	LocAdr6	6	in	+2.5 V/Gnd
SW202 quarter layer	LocAdr7	1	in	+2.5 V/Gnd
	LocAdr8	4	in	+2.5 V/Gnd
	LocAdr9	3	in	+2.5 V/Gnd
	LocAdr10	6	in	+2.5 V/Gnd
SW203 station	LocAdr11	1	in	+2.5 V/Gnd
	LocAdr12	4	in	+2.5 V/Gnd

Table 9: Power connector and Hex-switches

signal	in/out	level	pin	pin	level	in/out	signal
+3 V	out	power	1	2	power	out	+3 V
Gnd	out	Gnd	3	4	Gnd	out	Gnd
-3 V	out	power	5	6	power	out	-3 V
Gnd	out	Gnd	7	8	Gnd	out	Gnd
+2.5 V	out	power	9	10	power	out	+2.5 V
OtisN_Adr0	out	CMOS	11	12	CMOS	out	OtisN_Adr1
OtisN_Adr2	out	Gnd	13	14	CMOS	out	LocAdr3
LocAdr4	out	CMOS	15	16	CMOS	out	LocAdd5
LocAdr6	out	CMOS	17	18	CMOS	out	LocAdr7
LocAdr8	out	CMOS	19	20	CMOS	out	LocAdr9
I2c_Data	inout	CMOS	21	22	CMOS	inout	I2c_Clk
LocAdr10	out	CMOS	23	24	Gnd	out	Gnd
L0Acc_p	out	LVDS	25	26	LVDS	out	$\overline{L0Reset\_p}$
L0Acc_n	out	LVDS	27	28	LVDS	out	$\overline{L0Reset\_n}$
LocAdr11	out	CMOS	29	30	Gnd	out	Gnd
TPulseEvLo_p	out	LVDS	31	32	LVDS	out	TPulseOdLo_p
TPulseEvLo_n	out	LVDS	33	34	LVDS	out	TPulseOdLo_n
LocAdr12	out	CMOS	35	36	Gnd	out	Gnd
$\overline{BCntReset\_p}$	out	LVDS	37	38	LVDS	out	ClkPll_p
$\overline{BCntReset\_n}$	out	LVDS	39	40	LVDS	out	ClkPll_n
Gnd	out	Gnd	41	42	Gnd	out	Gnd
OtisND_n0	in	CMOSdiff	43	44	CMOSdiff	in	OtisND_p0
OtisND_n1	in	CMOSdiff	45	46	CMOSdiff	in	OtisND_p1
OtisND_n2	in	CMOSdiff	47	48	CMOSdiff	in	OtisND_p2
OtisND_n3	in	CMOSdiff	49	50	CMOSdiff	in	OtisND_p3
OtisND_n4	in	CMOSdiff	51	52	CMOSdiff	in	OtisND_p4
OtisND_n5	in	CMOSdiff	53	54	CMOSdiff	in	OtisND_p5
OtisND_n6	in	CMOSdiff	55	56	CMOSdiff	in	OtisND_p6
OtisND_n7	in	CMOSdiff	57	58	CMOSdiff	in	OtisND_p7
GOL-DV_n	in	CMOSdiff	59	60	CMOSdiff	in	GOL-DV_p
TPulseOdHi_p	in	LVDS	61	62	Gnd	in	Gnd
TPulseOdHi_n	in	LVDS	63	64	CMOS	in	$\overline{PwrUpRst}$
TpulseEvHi_p	in	LVDS	65	66	LVDS	in	$\overline{EventCntReset\_p}$
TpulseEvHi_n	in	LVDS	67	68	LVDS	in	$\overline{EventCntReset\_n}$
Gnd	out	Gnd	69	70	Gnd	out	Gnd
+2.5 V	out	power	71	72	power	out	+2.5 V
Gnd	out	Gnd	73	74	Gnd	out	Gnd
-3 V	out	power	75	76	power	out	-3 V
Gnd	out	Gnd	77	78	Gnd	out	Gnd
+3 V	out	power	79	80	power	out	+3 V

Table 10: Signal distribution on connectors to the OTIS board the four OTIS boards connected to one auxiliary board are numbered Y200-Y203, in the table N stands for this number.

2.1 OTIS data

The data coming from the OTIS TDCs consists of 8 bit per OTIS plus one Data Valid signal for the synchronization of the optical link. The OTIS data lines and the GOL-DV (tx_en) are differential CMOS signals with 50 Ohm impedance each. They are source terminated with 50 Ohm at the OTIS TDC or need a 100 Ohm termination between the differential pair close to the GOL chip, both schemes are supported by the hardware.

2.2 Timing and Fast Control

Some TFC signals must be decoded in the service box, such as $\overline{L0Reset}$ and the TestPulse. [3] The $\overline{BCntReset}$ and the $\overline{EvCntReset}$ are decoded by the TTCrx chip[7].

All TFC cables must have the same length of 5 m to minimize phase and timing problems. To avoid ground loops, all signals coming from the service box must be decoupled from service box ground. Clk_p and Clk_n are LVDS 40.08 MHz clock signals coming from the TTCrx.

A reset signal ($\overline{PwrUpRst}$) is directly issued by the ECS Specs [8]. The GOL, QPLL and OTIS resets will be connected to the $\overline{PwrUpRst}$ and a reset button (SW1). In order to perform a power up reset after the power is switched on, a capacitor is connected to the $\overline{PwrUpRst}$ signal, delaying the reset. To make up for a startup problem of the GOL 1.0, that occurs when the clock is present at power-on, the selectDiff signal is used by the ECS slave to select the active clock input after the chip is powered.

L0Acccept is the positive L0 trigger signal from the TTCrx [7]. The $\overline{L0Reset}$ is used by the OTIS to reset the L0 pipeline and the de-randomizing buffer pointers, to adapt programmed parameters. It is decoded from the TFC channel B broadcast. The bunch crossing ID reset $\overline{BCntReset}$ is used to restart the OTIS [3] bunch crossing counters, it is directly issued by the TTCrx. $\overline{EvCntReset}$ is the reset signal for the event counter on the OTIS, counting the L0 accepted signals. The OTIS must have a $\overline{L0Reset}$ to start operation.

2.3 Monitoring and LEDs

The temperature and the low voltage are monitored with the help of a rad hard ADC on the service box. Functionality of the power regulators, the GOL and the QPLL2 are indicated by LEDs and signaled to the service box.

[3] The FPGA used for the SPECS implementation can decode the TFC signals for all LHCb sub-detectors

Test Pulses can be send to check the functionality of the ASDs, four pairs of test pulses are foreseen:

- odd channels low pulse
- even channels low pulse
- odd channels high pulse
- even channels high pulse

Mind that the Gnd on the connector must not be connected to the service box ground, but only to the ADC inputs to avoid ground loops. The temperature sensor is a SMD NTC 100k in a 0805 sized package. All three voltages +2.5 V, +3 V and -3 V are sensed. The first (LED101) four LED signals are -3 V overcurrent monitor (OCM), +3 V (OCM), -5 V, +2.5 V (OCM). The second (LED102) four LEDs show +5 V, GOL_ready, $\overline{PLL\_error}$ (SEU), PLL_lock (table 11).

The LEDs are Signal Construct ZAZW 0422 types with 4 positions each. Mind that the diode voltage drop is 2.2 V for the green ones. It has been verified that even the green diodes are clearly visible connected to 2.5 V over a 100 Ohm resistor.

LED	pins	color	signal
101	1-2	green	-3 V OCM
	3-4	green	+3 V OCM
	5-6	green	-5.0 V
	7-8	green	+2.5 V
102	1-2	green	+5 V
	3-4	green	GOL_ready
	5-6	green	$\overline{PLL\_error}$
	7-8	green	PLL_lock

Table 11: LED assignment

2.4 I^2C

The I^2C serial bus supplies slow control signals to the OTIS TDC and GOL 1.0 (and optional further components in the service box). The bus is distributed over LVDS in a starlike scheme. One Hex Switch for the Module Location Address sits on the front of the board allowing to set the module location address for a built in module with a screwdriver (and some luck). Two more hex switches set station, layer and quarter position, so to define a unique module address in the Outer Tracker [6].

The three LSBs are hardwired on the auxiliary board to define the address for the GOL and the four OTIS chips (see table 12).

The I^2C address space available on one bus (7 bit address) is enough for the components on 9 detector module halves (4 OTIS + 1 GOL each), plus possible I^2C nodes on the service box. The OTIS uses only one I^2C address each while the GOL uses two consecutive I^2C addresses (for pointer and data). As the I^2C protocol reserves address 0 to 7 and 120 to 127 for system calls, they mustn't be used as device address. Table 12 shows how to split up the addresses for each I^2C chain (one each service box). The Two LSBs (0,1) are used to choose one out of four OTIS chips on a axillary board. Bit 2 (the third) is used to choose between GOL (1) or OTIS (0). The MSBs 3-6 are used to select one of the auxiliary boards, starting from 0001 going to 1001, 0000 and 1111 are reserved for the system, the remaining address space 1010-1110 can be used on the service box. The OTIS chip as well as the GOL chip have internal pull downs on all I^2C address inputs, so the address lines must be left open for low and pulled to +2.5 V for high. This implies that the Hex switch for the location address has to use real logic.

Decoupling of the I^2C signals from the service box is done by using LVDS signals. In accordance with the scheme proposed by the developers of the I^2C master, SPECS Slave [8], the bidirectional I^2C data lines SDA and the clock line SCL are translated into unidirectional differential signals, see figure 1. Using this scheme it is important to ensure that only the active low signals are driven by the LVDS transceivers, figure 2.

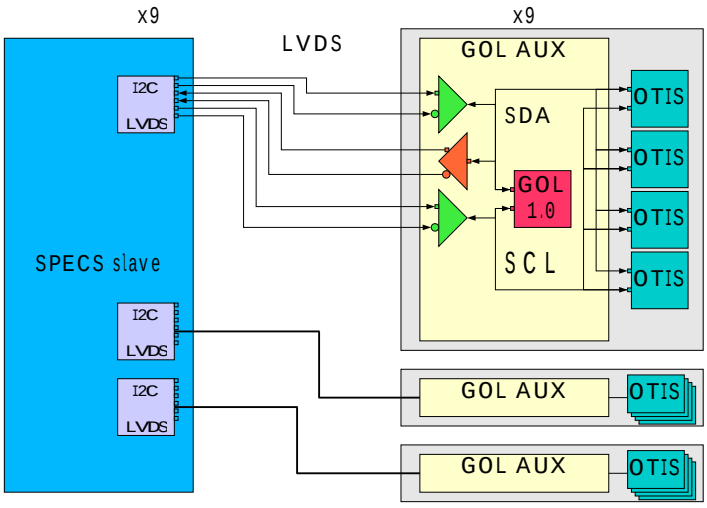


Figure 1: I^{2}C bus decoupling scheme using LVDS

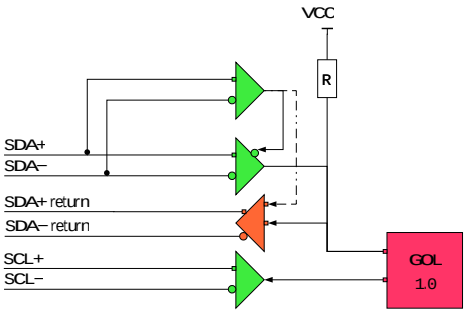


Figure 2: Disabling the inactive I^{2}C signals.

Address bit	device	possible values
0-2	OTIS0	000
	OTIS1	001
	OTIS2	010
	OTIS3	011
	GOL pointer	100
	GOL data	101
3-6	aux-board 0-8	0001-1001
	reserved	0000 and 1111
	service box	1010-1110

Table 12: I^2C addresses

3 Physical implementation

The physical implementation is given by the global OT module design. Here the dimensions stated on 12th Dec 2002 figure 3:

- Outer dimensions 150 mm x 100 mm x 1.6 mm
- center of 80 pin OTIS board connector from corner 13 mm, 34.1 mm
- 7 drills of 3.2 mm diameter for board mounting, four drills at the corners:
  - for the OTIS board side 23 mm from long side, 5 mm from the short side
  - for the service board side 5 mm from long side, 5 mm from the short side

  three drills between the power regulators: 40 mm from service box side, 15 mm / 75 mm / 135 mm from the short side.

The size of the bigger parts is shown in table 1, their position is subject to the layout. As the power regulators have to be screwed to the cooling, they have a fixed position on the back of the board. With exception of two 80 pin OTIS board connectors and resistors R144-R146 all other parts are mounted on the upper side of the board. A soldering gauge for the 80 pin OTIS board connectors has been machined, the dimensions can be taken from figure 19. The Auxiliary board describe here will be produced in fall 2004 (number IF13-1), see figures 4 and 5. The previous version IF13-0 is described in [14].

Figure 3: GOL-auxiliary board IF13-1 prototype, mechanical specifications.

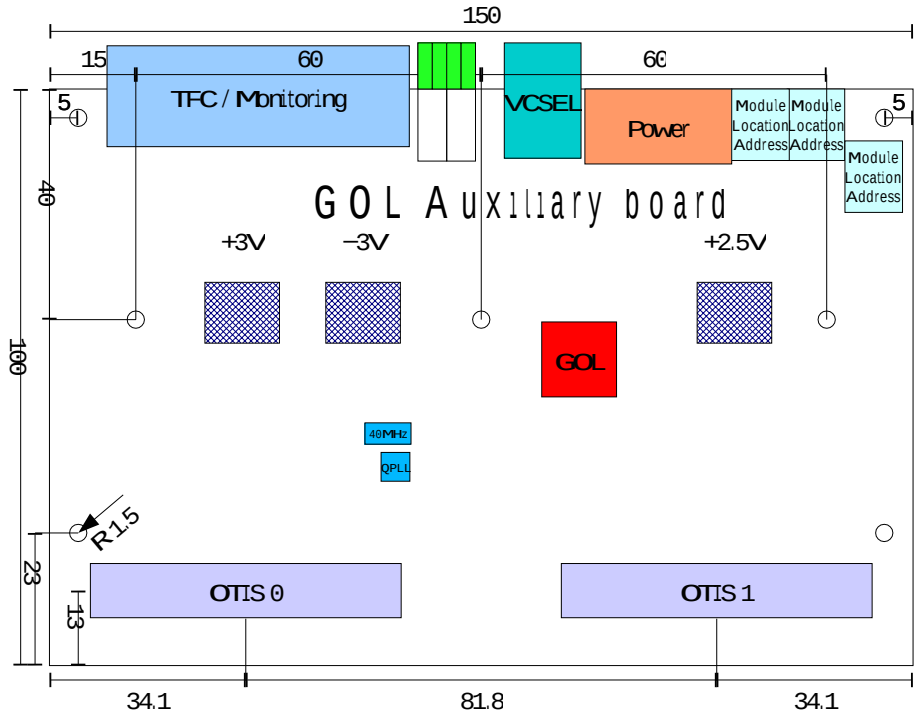
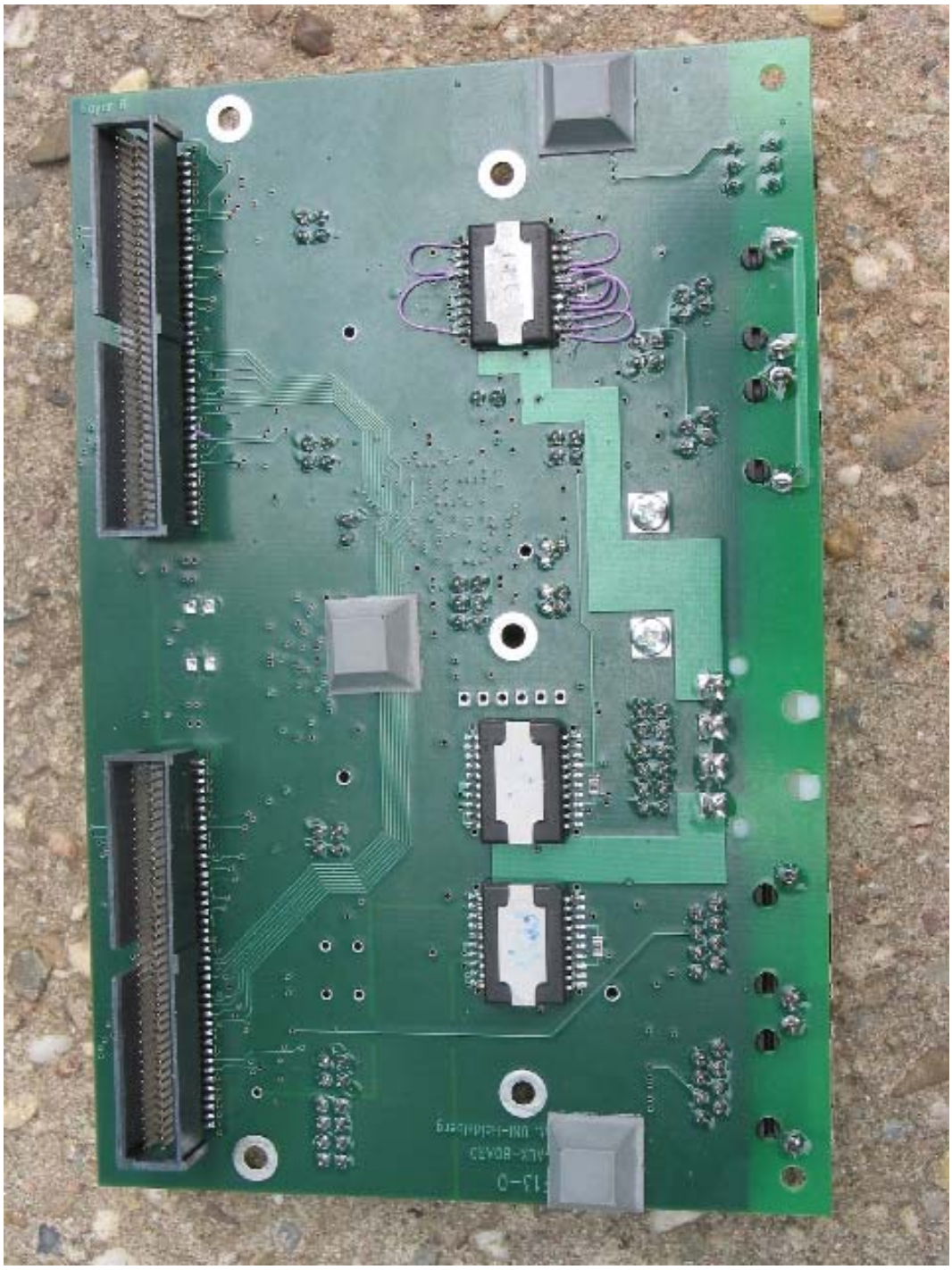


Figure 4: GOL-auxiliary board IF13-0 prototype, part side.

Figure 5: GOL-auxiliary board IF13-0 prototype, bottom side. Mind the changed pin out for the negative power regulator L7913



A Schematics

Figure 6 shows the schematics for the connectivity of the GOL 1.0, the QPLL, the power regulators, the power pins and the monitor signals.

Figure 7 shows the connectors for the OTIS boards, the TFC signals and the switches for the local address.

See figure 8 for the I^2C decoupling and the connectivity of the I^2C bus.

Figure 6: GOL-auxiliary board schematics (1/3)

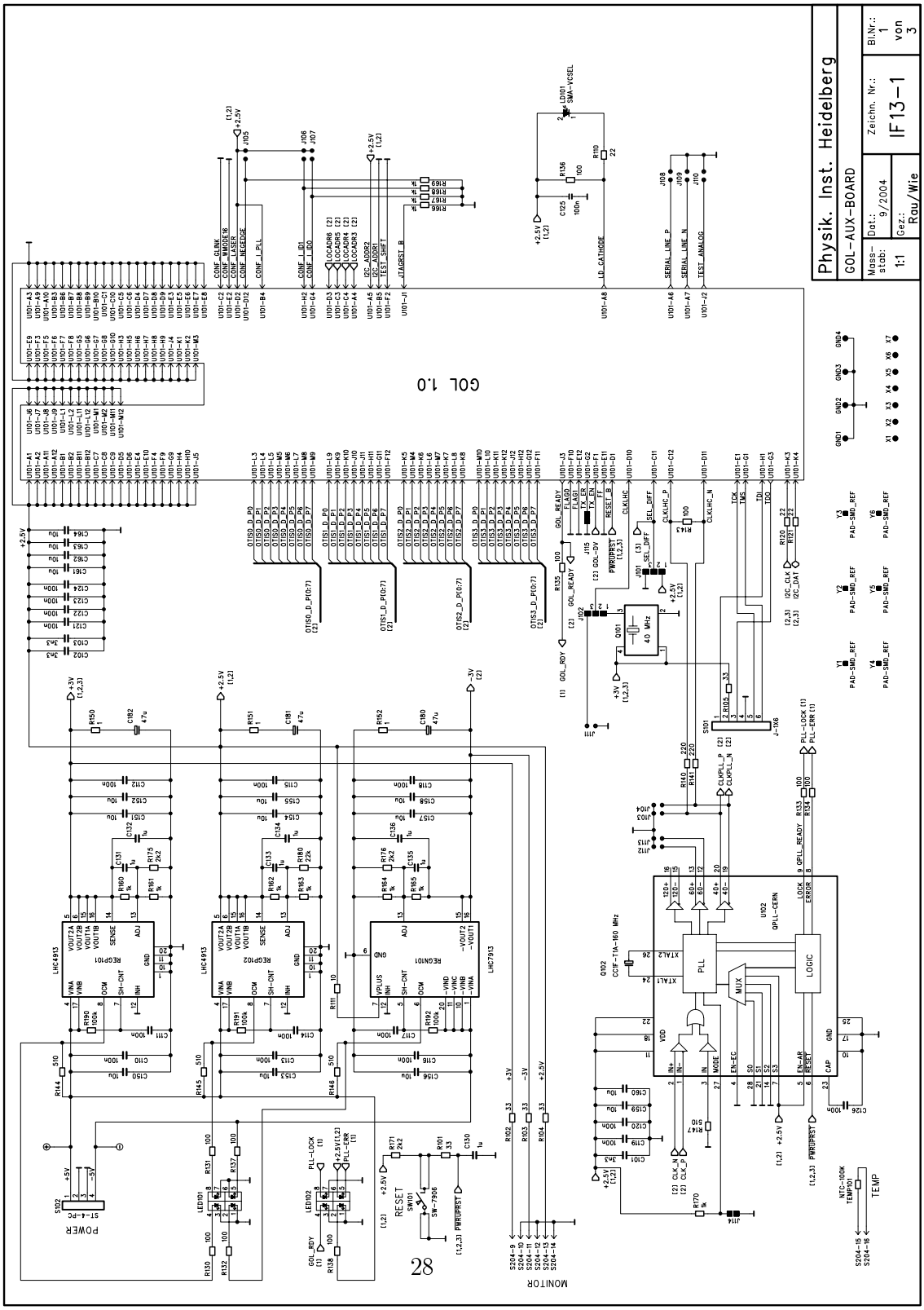


Figure 7: GOL-auxiliary board schematics (2/3)

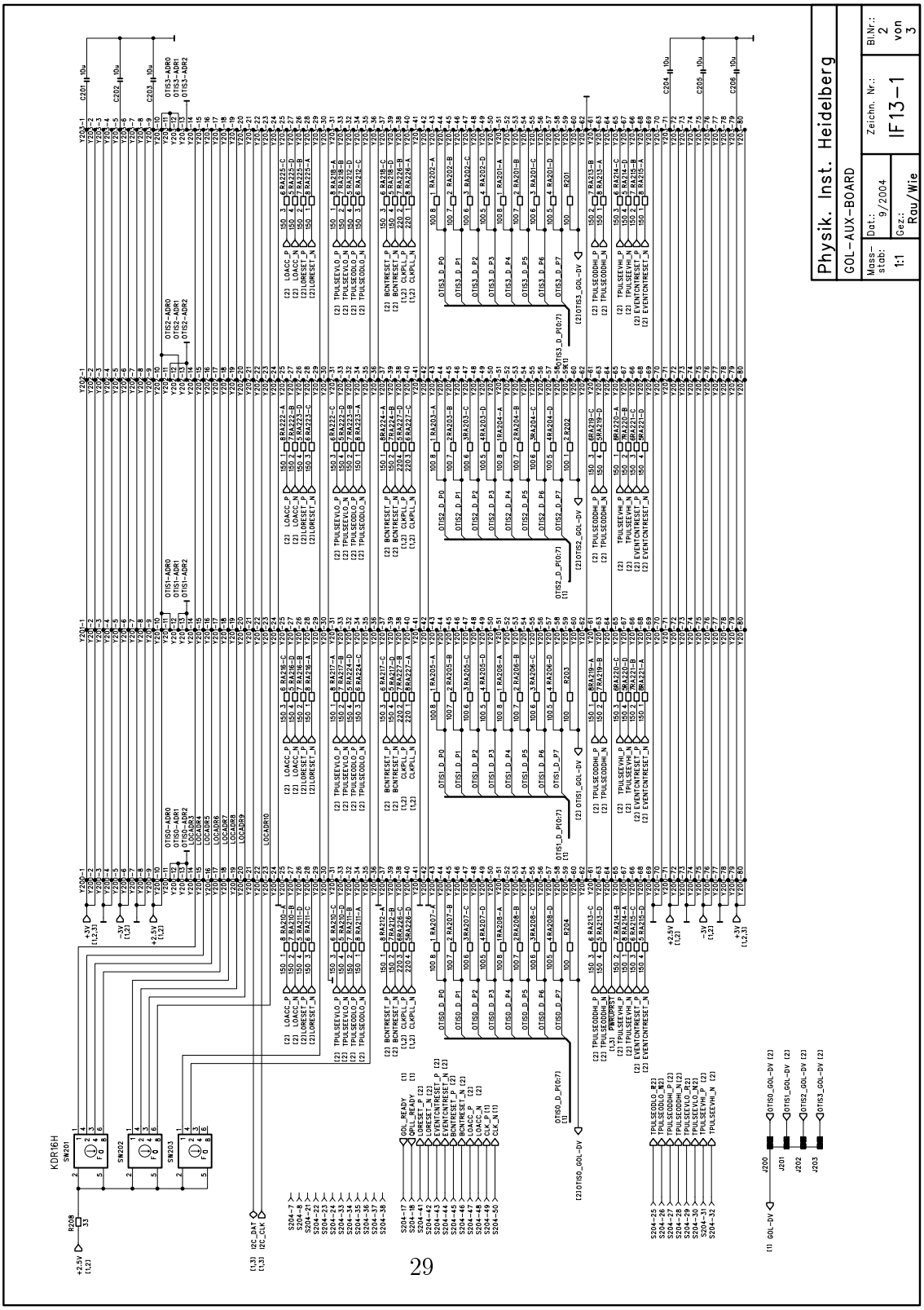
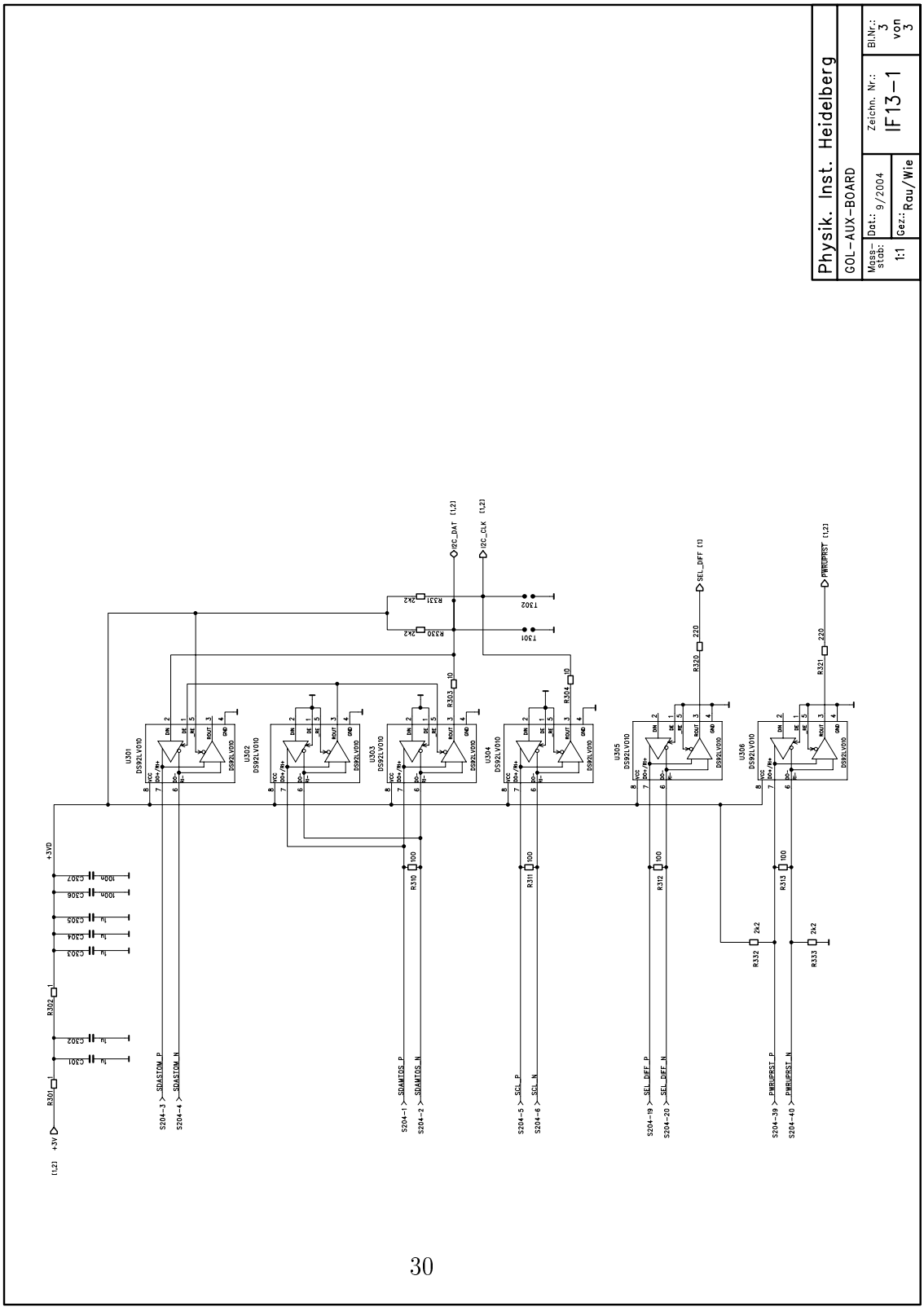


Figure 8: GOL-auxiliary board schematics (3/3)



B Layout

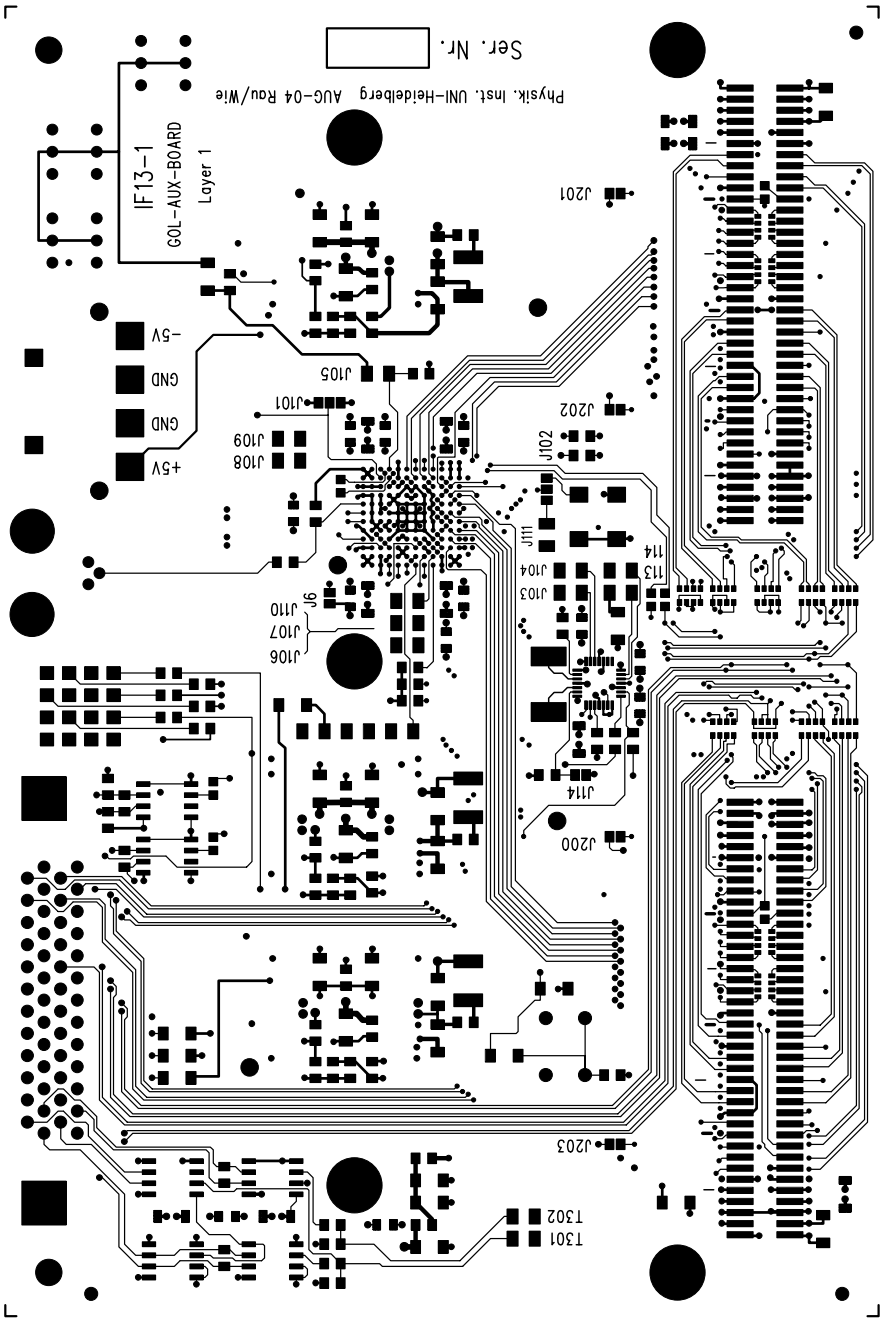


Figure 9: *Layout layer 1/6*

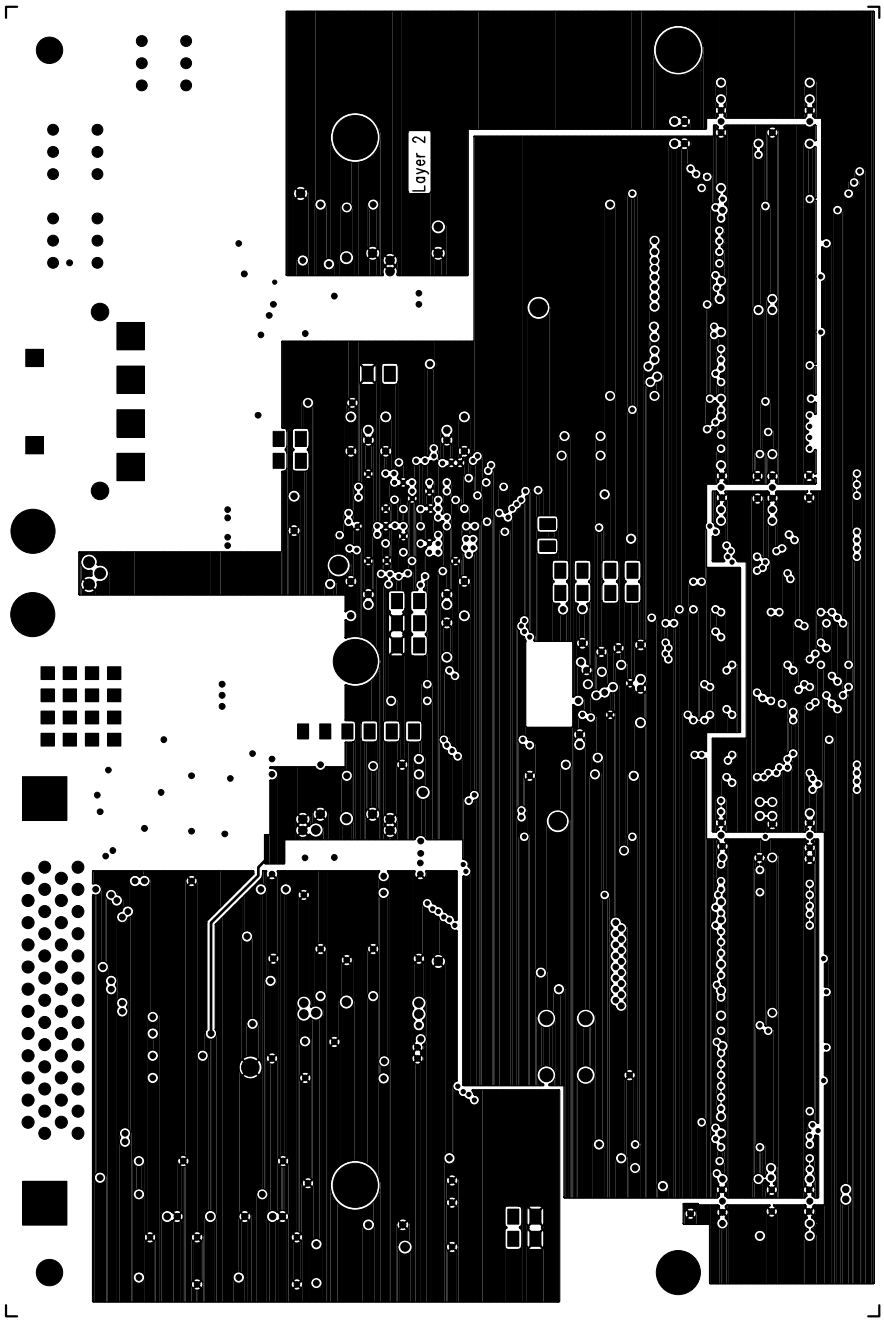


Figure 10: *Layout layer 2/6*

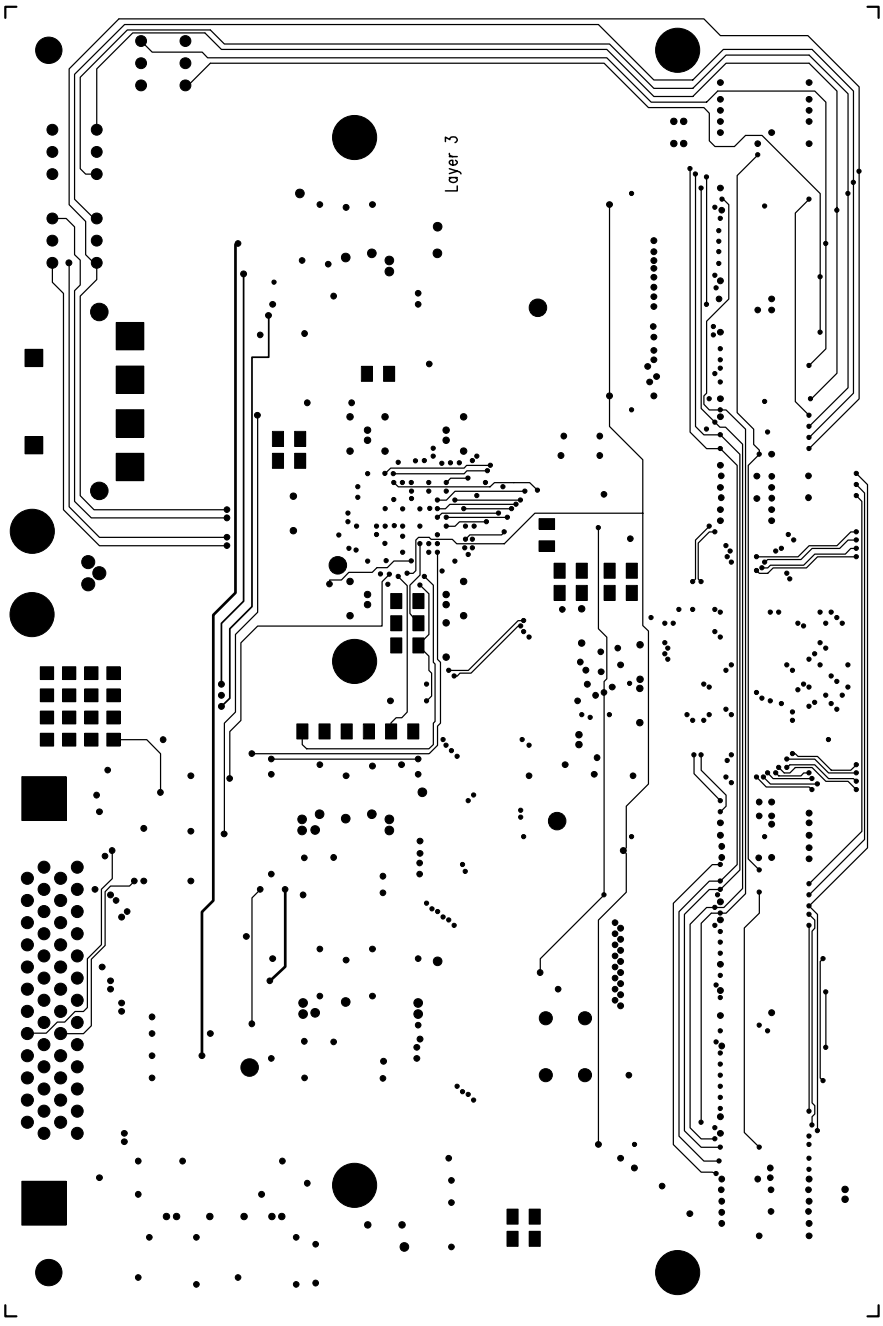


Figure 11: *Layout layer 3/6*

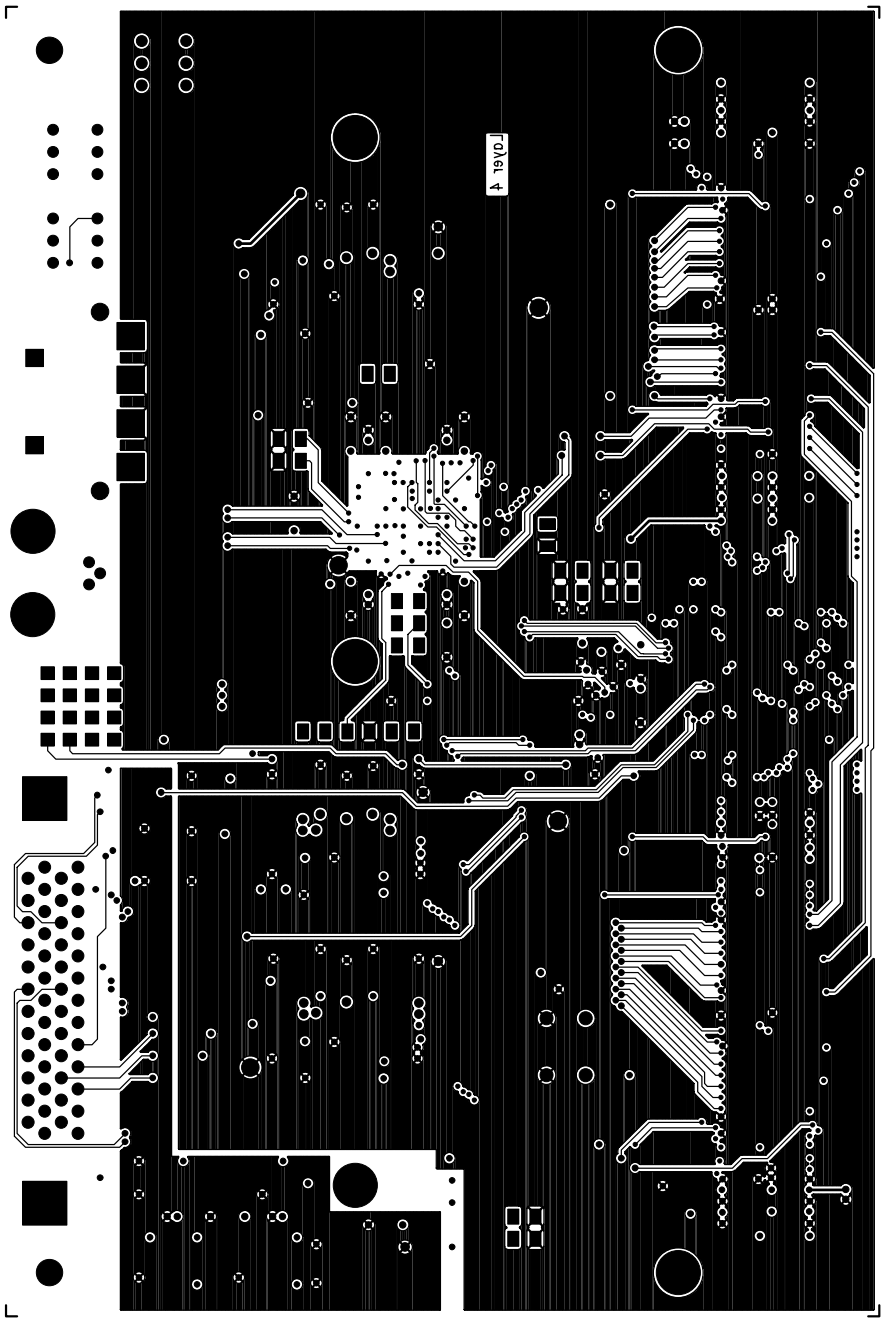


Figure 12: *Layout layer 4/6*

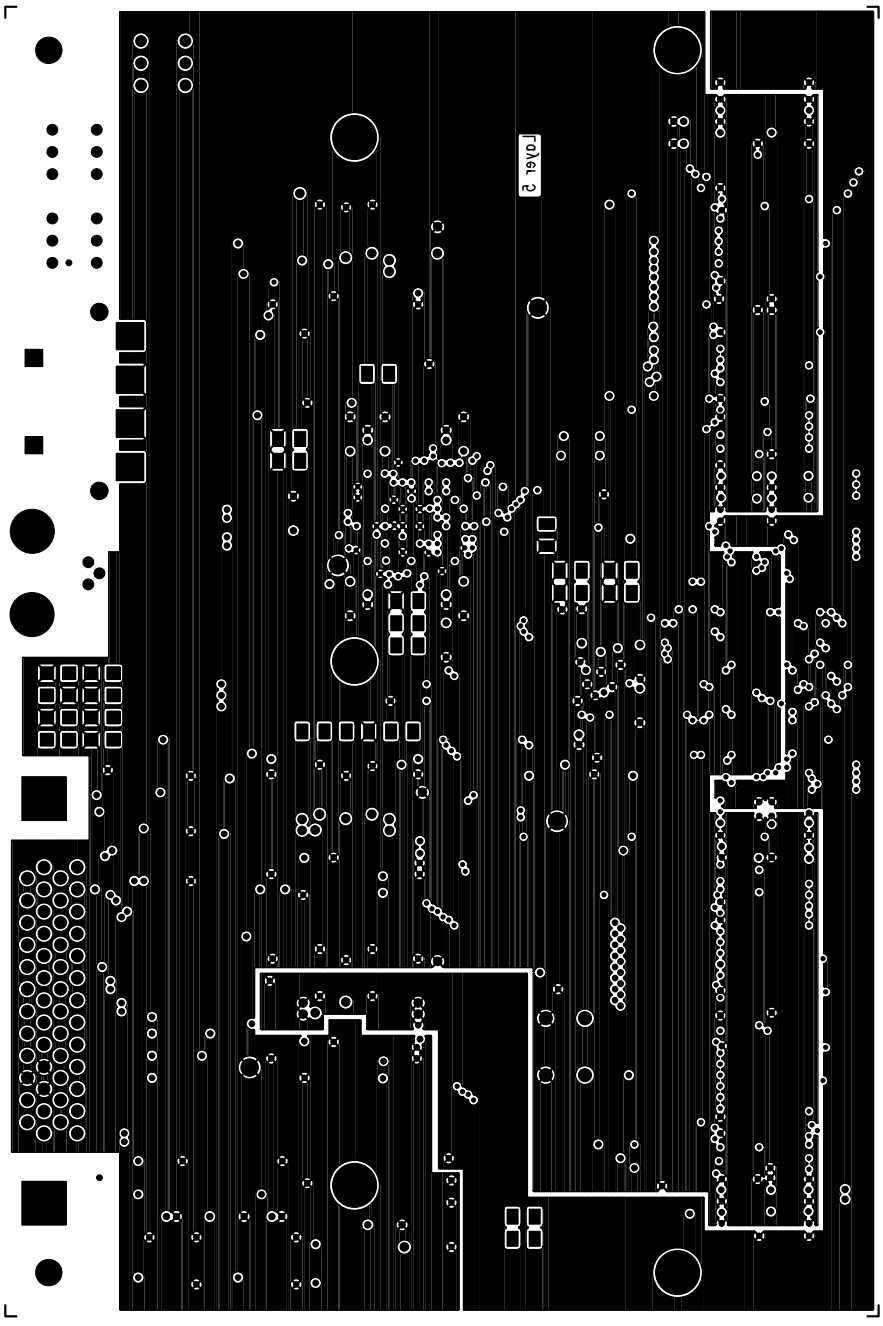


Figure 13: *Layout layer 5/6*

Figure 14: *Layout layer 6/6*

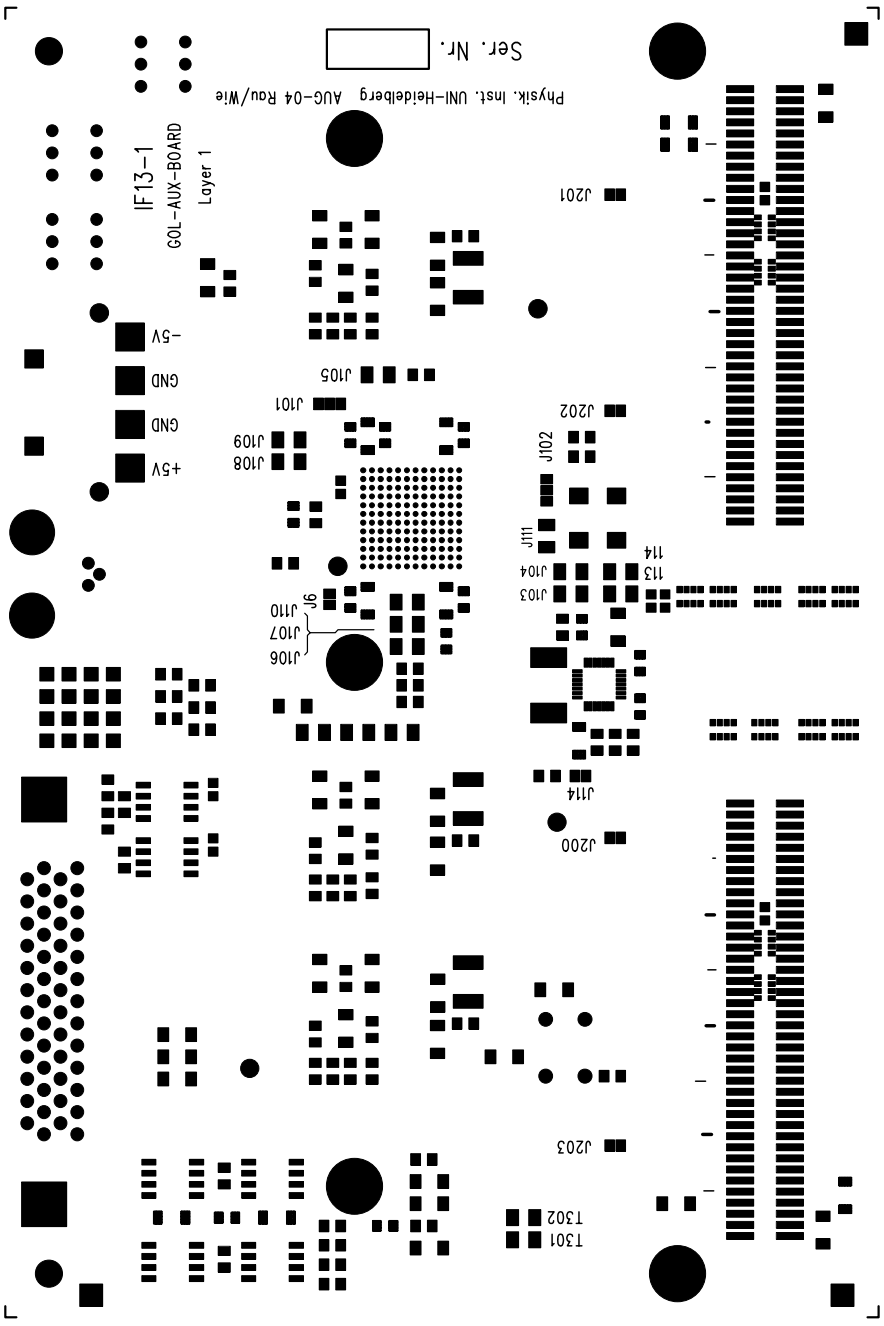


Figure 15: *Soldermask layer 1*

Figure 16: *Soldermask layer 6*

C Component placement specification

Do not use 100k resistors for R190-R192, because then the current limit is too low! J115 must be connected to GND.

If the I^2C interface is not used to control the GOL 1.0 output bias current, R136 must not be mounted, otherwise the output current is too low, see figure 17 for component placement on the top side. Figure 18 shows the component placement on the bottom side.

Figure 17: GOL-auxiliary board component placement specification top (1/2)
Do not use 100k resistors for R190-R192, because then the current limit is too low!

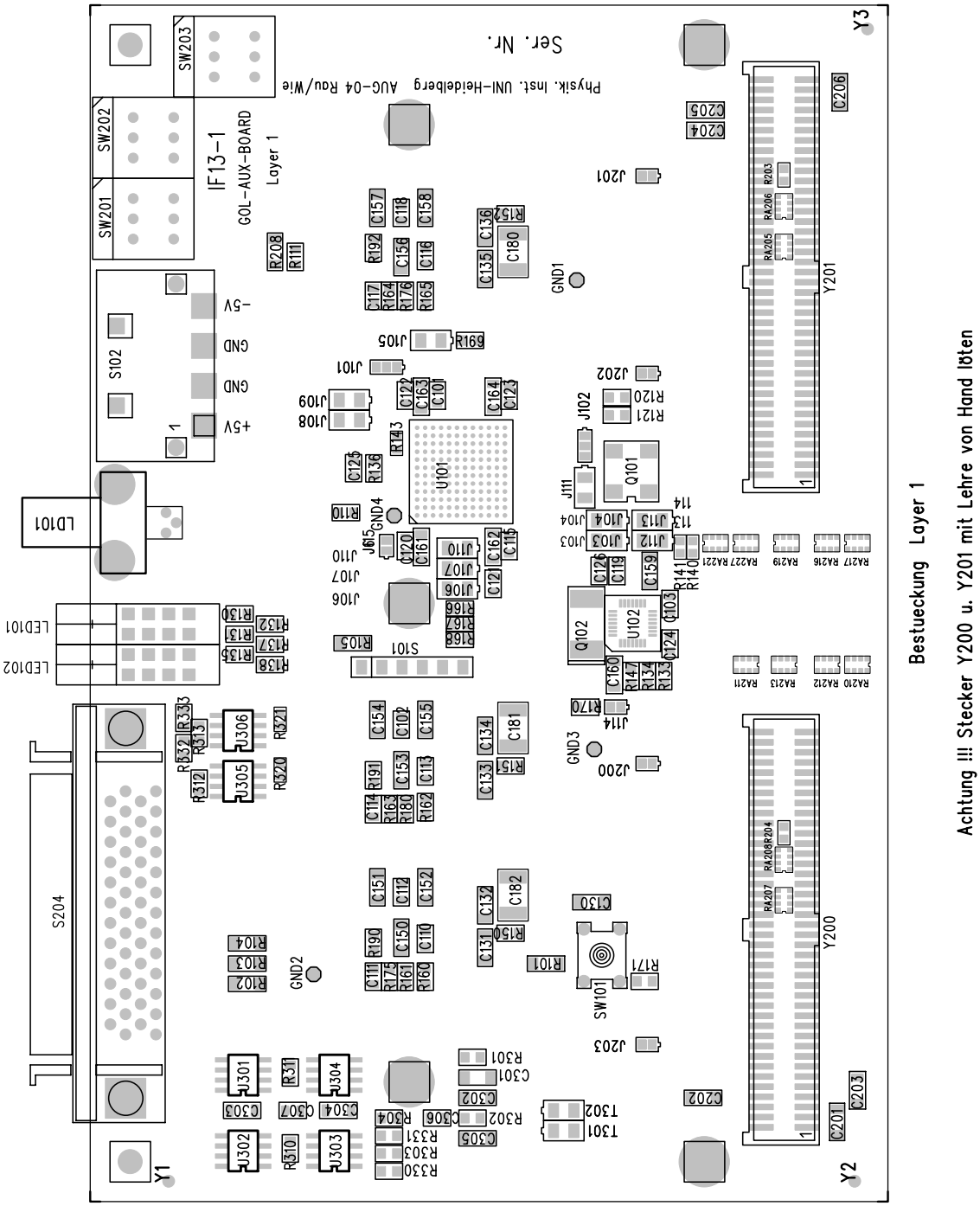


Figure 18: GOL-auxiliary board component placement specification bottom (2/2).

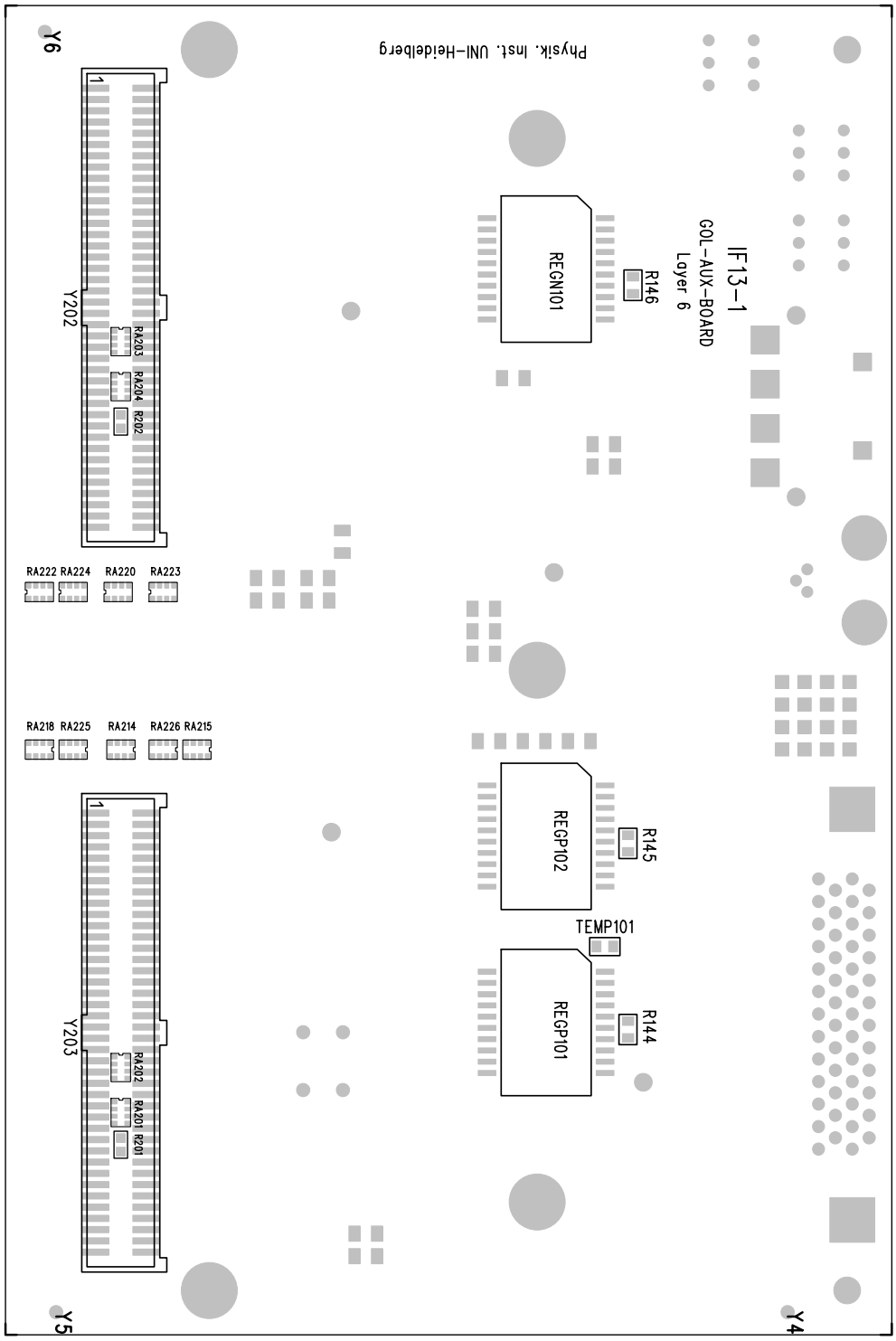
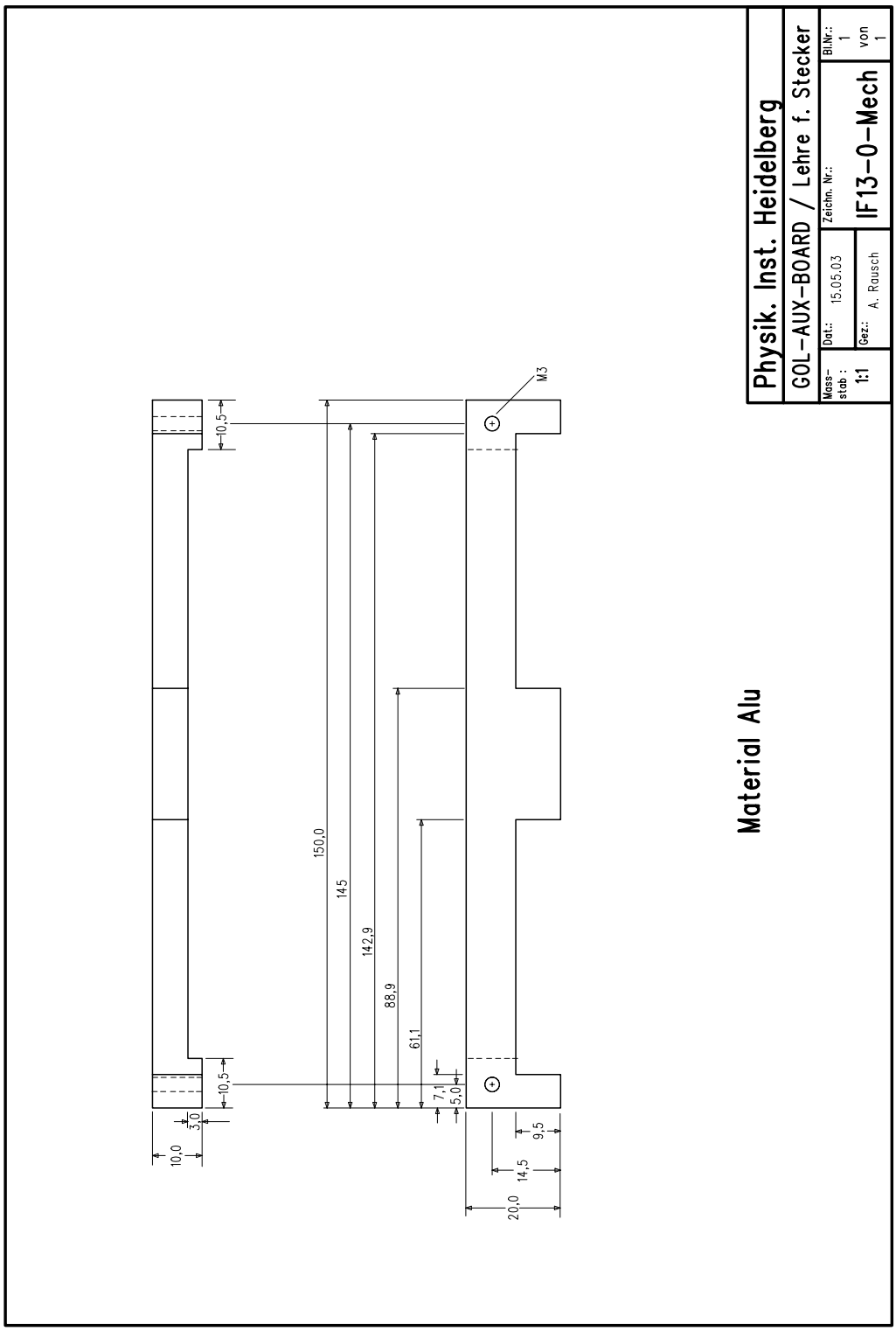


Figure 19: OTIS board connector soldering gauge



D Bill of materials

Table 13: Bill Of Materials

Qty:	Part-Nr.:	Part-Typ:	Val.:	Part-Description:
1	LD101	SMA-VCSEL		Laser VCSEL 850 nm
1	U101	GOL 1.0		GOL 1.0 serializer 1.6 Gbit/s
1	U102	QPLL2		Dejitter chip
1	Q102	Oscillator		Oscillator 160 MHz
6	U301-306	DS92LV010		LVDS transceiver
1	Q101	Q-SF8002CA		Frequency Oscillator 40 MHz
2	REGP101-102	LHC4913 DIP-20SMD		Positive power Regulator
1	REGN101	LHC7913 DIP-20SMD		Negative Power Regulator
2	LED101-102	LED-2X2	green	Signal Construct ZAZW 0422
1	TEMP101	R-0805Rau	NTC100k	Temperature sensor
4	Y200-203	ST-80-ZML		Samtec Connector ZML-140-54-S-D-530-SM
1	S204	BU-50-SCSI2		SCSI2 connector 50-pos
1	S102	ST-4-PC		Powerconnector 4-pos
1	SW101	SW-7906		Reset Button
3	SW201-203	SW-KDC16H		Hex Switch 4 pos.
1	S101	J-1x6		1 row jumper 6 pos
13	J103-113 T301-T302	J-1x2		1 row jumper 2 pos
6	J114-115 J200-203	J-1x2SMD		1 row solder jumper 2 pos
2	J101-J102	J-1x3SMD		1 row solder jumper 3 pos
3	C101-103	CK-0805SMD	3n3	SMD-Cap. l=2.0 mm w=1.25 mm
19	C110-126 C306-307	CK-0805SMD	100n	SMD-Cap. l=2.0 mm w=1.25 mm
12	C130-136 C301-305	CK-1206SMD	1u	SMD-Cap. l=3.2 mm w=1.6 mm
21	C150-C164 C201-206	CK-1206SMD	10u	SMD-Cap. l=3.2 mm w=1.6 mm

Table 13: Bill Of Materials

Qty:	Part-Nr.:	Part-Typ:	Val.:	Part-Description:
3	C180-182	CK-1812SMD	47u	SMD-Cap. l=4.5 mm w=3.2 mm
5	R143 R201-204	R-0603Rau	100	SMD-Resistor
4	R140-R141 R320-321	R-0603Rau	220	SMD-Resistor
5	150-152 R301-302	R-805Rau	1	SMD-Resistor
3	R111 R303-304	R-0805Rau	10	SMD-Resistor
3	R110 R120-121	R-0805Rau	22	SMD-Resistor
13	R130-138 R310-R313	R-0805Rau	100	SMD-Resistor
4	R144-147	R-0805Rau	510	SMD-Resistor
11	R160-170	R-0805Rau	1K	SMD-Resistor
7	R171 175-176 330-333	R-0805Rau	2k2	SMD-Resistor
1	R180	R-0805Rau	22k	SMD-Resistor
3	R190-192	R-0805Rau	100k	SMD-Resistor NOT USED
6	R101-105 R208	R-1206Rau	33	SMD-Resistor
8	RA201-208	R-0603x4	100	SMD-Resistor array
16	RA210-225	R-0603x4	150	SMD-Resistor array
2	RA226-227	R-0603x4	220	SMD-Resistor array

E Known bugs for version IF13-0

For the prototype boards version IF13-0 the footprint for the negative power regulators are wrongly the same as for the positive types, mounting of the negative type L7913 will result in severe SHORTS, a patch is shown in note [14]. Do not use 100k resistors for R190-R192, because then the current limit is too low, see section [14]

The negative power regulators from the Q5 silicon batch are oscillating, Q6 silicon is recommended.

The pull down resistor R185 (1K Ohm) must not be used, it would cause a bad reset condition for QPLL, GOL 1.0 and OTIS TDC.

If the I^2C interface is not used to control the GOL 1.0 output bias current, R136 must not be mounted, otherwise the output current is too low.

A start up problem has been reported for the GOL 1.0: The GOL 1.0 does not start properly if the clock is present at power on.

The clock distribution to the OTIS TDC doesn't work by just connecting all four TDCs in a starlike configuration to the clock signal.

The OTIS data signals need termination on the GOL-Aux Board.

The QPLL1 de-jitter chip locks only for a limited temperature range.

F Changes for the prototype IF13-1 in respect to IF13-0

In addition to the removal of the bugs mentioned above, a number of features will be added in the next Auxiliary Board Prototype:

- The negative power regulator pin-out has been adopted. In addition tantalum capacitors, or for longer lifetime, ceramic capacitors with a serial resistor have to be added to damp the oscillations.
- The select differential clock pin of the GOL (C11) must be connected to the distribution box in order to switch to a valid clock after power on, so to fix the bug.
- The distribution of all TFC signals, including ClkPLL, L0Acc, L0Res, TPulseEv, TPulseOd, BCntReset, EvCountReset, must be via a LVDS distribution scheme. The chosen scheme is source termination with 150 or 220 Ohm for each line.
- The OTIS TDC signals, which are now differential CMOS, are terminated with 100 Ohm on the GOL-Auxiliary Board.
- The QPLL1 de-jitter chip is replaced by the QPLL2 which has a bigger locking range. The recommended layout for the QPLL is now followed.
- The I^2C signal is now LVDS and distributed over the same connector as the TFC signals.
- A SCSI 50-pin connector replaces the former TFC, Monitor and I^2 connectors.

- In order to characterize the ASDBLR now 4 test-pulses are available odd-high, odd-low, even-high, even-low.
- An event counter reset signal has been added as the OTIS now sends event counter data.
- 13 instead of 7 address lines are going to each OTIS board, plus extra address selection switches have been added.
- Extra GOL-DV_p and GOL-DV_n lines going from each OTIS board to the Auxiliary board. The signal GOL Data Valid is now issued by the OTIS TDC for the periods of valid OTIS data (and comma). A jumper field selects which OTIS TDC enables the GOL data transmission.
- Keep offs around the regulator screws have been enlarged to allow bigger tooling.
- The monitoring signals temperature and OTIS_N_WritePointerWrap are no more available on the GOL Auxiliary IF13-1
- The VCSEL diode is now a ULM Photonics Ulm850-05-TN-USMB0P.

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